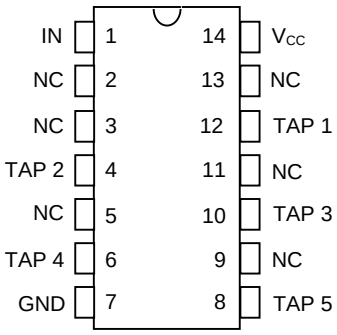
DS1005
5-Tap Silicon Delay Line

www.dalsemi.com

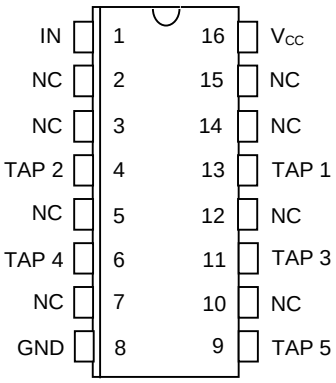
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

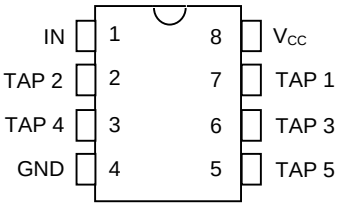
PIN ASSIGNMENT



DS1005 14-Pin DIP (300-mil)
See Mech. Drawings Section



DS1005S 16-Pin SOIC
(300-mil)
See Mech. Drawings Section



DS1005M 8-Pin DIP (300-mil)
See Mech. Drawings Section

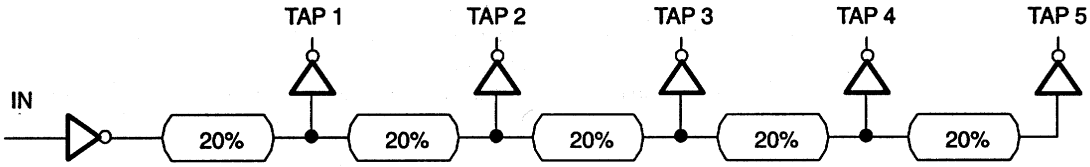
PIN DESCRIPTION

TAP 1-TAP 5	- TAP Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ±2 ns or ±3%, whichever is greater. This device is offered in a standard 14-pin DIP, making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371–4348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1005-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1005-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1005-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1005-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1005-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1005-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1005-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1005-250	50 ns	100 ns	150 ns	200 ns	250 ns

Custom delays available

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	u A	
Active Current	I_{CC}	V_{CC}=Max; Period=Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open.

3. V_{CC} = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns or ±3%, whichever is greater.

4. See Test Conditions.

5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional input-to-tap delay shift of ±1.5 ns or ±4%, whichever is greater.

6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.

7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature	25°C ± 3°C
Supply Voltage (V_{CC})	5.0V ± 0.1V
Input Pulse	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance	50 ohm maximum
Rise and Fall Time	3.0 ns maximum
Pulse Width	500 ns
Period	1 μs

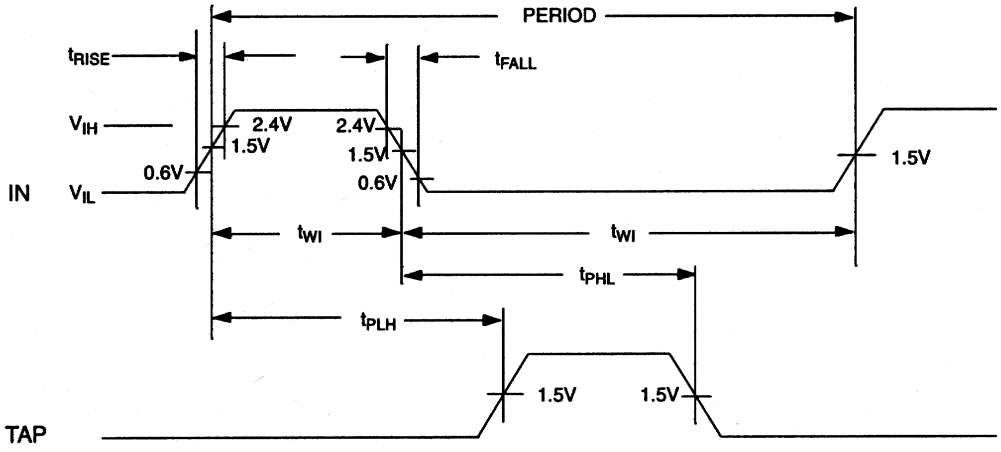
OUTPUT:

Each output is loaded with the equivalent of a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

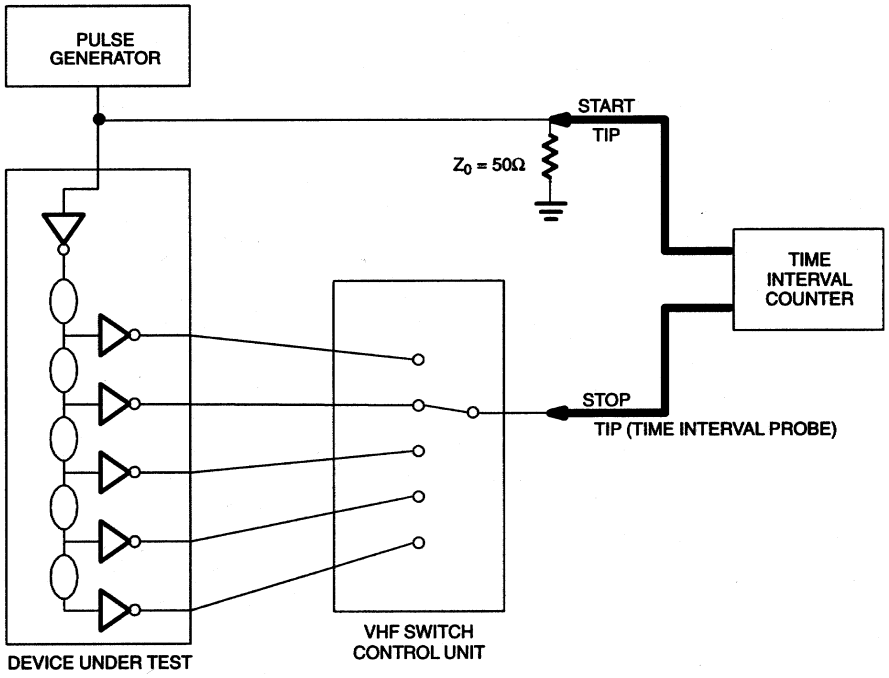
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



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ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
ОГРН: 1167746717709