

Digital Logic

Pocket Data Book

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Digital Logic
Pocket Data Book



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Little Logic

| Series | Supply Voltage V _{CC} (V) | Operating Free-air Temperature T _a (°C) |
|-----------------|------------------------------------|--|
| SN74AUP1G | 0.8~3.6 | -40~85 |
| SN74AUC1G/2G/3G | 0.8~2.7 | -40~85 |
| SN74LVC1G/2G/3G | 1.65~5.5 | -40~85 |
| SN74AHC1G | 2.0~5.5 | -40~85 |
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GATE/OCTAL/Widebus™/Widebus+

| Series | Supply Voltage V _{CC} (V) | Operating Free-air Temperature T _a (°C) |
|---------------------------------------|------------------------------------|--|
| SN74ABT | 4.5~5.5 | -40~85 |
| SN64BCT | 4.5~5.5 | -40~85 |
| SN74BCT SN74F SN74ALS SN74AS | 4.5~5.5 | 0~70 |
| SN74LS SN74S SN74xx(TTL) | 4.75~5.25 | 0~70 |
| SN74AC SN74AC11xxx SN74AHC | 2.0~5.5 | -40~85 |
| SN74HC | 2.0~6.0 | -40~85 |
| SN74LV | 2.0~5.5 | -40~85 |
| SN74LVC | 2.0~3.6 | -40~85 |
| SN74LVT | 2.7~3.6 | -40~85 |
| SN74ALVC | 1.65~3.6 | -40~85 |
| SN74ALVT | 2.3~3.6 | -40~85 |
| SN74AVC | 1.4~3.6 | -40~85 |
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| 576 | OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS | 453 |

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| Device | Function | |
| 577 | OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS | 454 |
| 580 | OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS | 455 |
| 590 | 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS | 456 |
| 592 | 8-BIT BINARY COUNTERS WITH INPUT REGISTERS | 458 |
| 593 | 8-BIT BINARY COUNTERS WITH INPUT REGISTERS | 460 |
| 594 | 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS | 462 |
| 595 | 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS | 464 |
| 596 | 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES | 466 |
| 597 | SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES | 468 |
| 598 | 8-BIT SHIFT REGISTERS WITH INPUT LATCHES | 470 |
| 620 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 472 |
| 621 | OCTAL BUS TRANSCIEVERS | 473 |
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| 624 | VOLTAGE-CONTROLLED OSCILLATORS | 475 |
| 628 | VOLTAGE-CONTROLLED OSCILLATORS | 476 |
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| 639 | OCTAL BUS TRANSCIEVERS | 479 |
| 640 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 480 |
| 641 | OCTAL BUS TRANSCIEVERS WITH OPEN-COLLECTOR OUTPUTS | 481 |
| 642 | OCTAL BUS TRANSCIEVERS WITH OPEN-COLLECTOR OUTPUTS | 482 |
| 645 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 483 |
| 646 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 484 |
| 647 | OCTAL BUS TRANSCIEVERS AND REGISTERS | 486 |
| 648 | OCTAL BUS TRANSCIEVERS AND REGISTERS | 488 |
| 651 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 490 |
| 652 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 492 |
| 653 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 494 |
| 654 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 496 |
| 657 | OCTAL BUS TRANSCIEVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS | 498 |
| 666 | 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS | 500 |
| 667 | 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS | 501 |
| 669 | SYNCHRONOUS 4-BIT UP/DOWN COUNTERS | 502 |
| 670 | 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS | 504 |
| 673 | 16-BIT SHIFT REGISTERS | 506 |
| 674 | 16-BIT SHFT REGISTERS | 508 |
| 679 | 12-BIT ADDRESS COMPARATOR | 510 |
| 682 | 8-BIT MAGNITUDE COMPARATORS | 512 |
| 684 | 8-BIT MAGNITUDE COMPARATORS | 514 |
| 686 | 8-BIT MAGNITUDE/IDENTITY COMPARATORS | 516 |
| 688 | 8-BIT IDENTITY COMPARATORS | 518 |
| 697 | SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS | 520 |

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| Device | Function | |
| 699 | SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS | 522 |
| 756 | OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS | 524 |
| 757 | OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS | 525 |
| 760 | OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS | 526 |
| 804 | HEX 2-INPUT NAND DRIVERS | 527 |
| 805 | HEX 2-INPUT NOR DRIVERS | 528 |
| 808 | HEX 2-INPUT AND DRIVERS | 528 |
| 821 | 10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS | 529 |
| 823 | 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 530 |
| 825 | 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 531 |
| 827 | 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 532 |
| 828 | 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 532 |
| 832 | HEX 2-INPUT OR DRIVERS | 533 |
| 833 | 8-BIT TO 9-BIT PARITY BUS TRANSCIEVERS | 534 |
| 841 | 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 536 |
| 843 | 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 537 |
| 853 | 8-BIT TO 9-BIT PARITY BUS TRANSCIEVERS | 538 |
| 857 | HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS | 540 |
| 861 | 10-BIT TRANSCIEVERS WITH 3-STATE OUTPUTS | 542 |
| 863 | 9-BIT BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 543 |
| 867 | SYNCHRONOUS 8-BIT UP/DOWN COUNTERS | 544 |
| 869 | SYNCHRONOUS 8-BIT UP/DOWN COUNTERS | 546 |
| 870 | DUAL 16-BY 4-BIT REGISTER FILES | 548 |
| 873 | DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS | 550 |
| 874 | DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS | 551 |
| 876 | DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS | 552 |
| 885 | 8-BIT MAGNITUDE COMPARATORS | 554 |
| 990 | 8-BIT D-TYPE TRANSPARENT READ-BACK LATCH | 556 |
| 992 | 9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS | 557 |
| 994 | 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH | 558 |
| 996 | 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES | 559 |
| 1000 | QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS | 560 |
| 1004 | HEX INVERTING DRIVERS | 560 |
| 1005 | HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS | 561 |
| 1008 | QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER | 561 |
| 1032 | QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS | 562 |
| 1034 | HEX DRIVERS | 562 |
| 1035 | HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS | 563 |
| 1240 | OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS | 563 |
| 1244 | OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS | 564 |
| 1245 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 564 |
| 1404 | OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR | 565 |
| 1640 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 566 |
| 1645 | OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 567 |
| 2240 | OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS | 568 |

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| Device | Function | |
| 2241 | OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS | 569 |
| 2244 | OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS | 570 |
| 2245 | OCTAL TRANSCIEVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS | 571 |
| 2373 | 25-W OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS | 572 |
| 2414 | MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR | 573 |
| 2541 | OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS | 574 |
| 2827 | 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 574 |
| 2828 | 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING | 575 |
| 2952 | OCTAL BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 576 |
| 2953 | OCTAL BUS TRANSCIEVER AND REGISTER WITH 3-STATE OUTPUTS | 578 |
| 4002 | DUAL 4-INPUT POSITIVE-NOR GATES | 579 |
| 4015 | DUAL 4-STAGE STATIC SHIFT REGISTER | 580 |
| 4016 | QUAD BILATERAL SWITCH | 581 |
| 4017 | DECADE COUNTERS/DIVIDER | 582 |
| 4020 | 14-STAGE BINARY COUNTERS | 583 |
| 4024 | 7-STAGE BINARY COUNTERS | 584 |
| 4040 | 12-STAGE BINARY COUNTERS | 585 |
| 4046 | PHASE-LOCKED-LOOP WITH VCO | 586 |
| 4049 | HEX INVERTING BUFFERS | 588 |
| 4050 | HEX NON-INVERTING BUFFERS | 588 |
| 4051 | 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTEPLEXERS | 589 |
| 4052 | DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTEPLEXERS | 590 |
| 4053 | TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTEPLEXERS | 591 |
| 4059 | CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER | 592 |
| 4060 | ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS | 593 |
| 4066 | QUADRUPLE BILATERAL SWITCHES | 594 |
| 4067 | 16-CHANNEL ANALOG MULTIPLEXER/DEMULTEPLEXER | 595 |
| 4075 | TRIPLE 3-INPUT OR GATES | 596 |
| 4094 | 8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE | 597 |
| 4316 | QUAD ANALOG SWITCH WITH LEVEL TRANSLATION | 598 |
| 4351 | ANALOG MULTIPLEXERS/DEMULTEPLEXERS WITH LATCH | 599 |
| 4352 | ANALOG MULTIPLEXERS/DEMULTEPLEXERS WITH LATCH | 600 |
| 4374 | OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS | 601 |
| 4511 | BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS | 602 |
| 4514 | 4-LINE TO 16-LINE DECODERS/DEMULTEPLEXERS WITH INPUT LATCHES | 604 |
| 4515 | 4-LINE TO 16-LINE DECODERS/DEMULTEPLEXERS WITH INPUT LATCHES | 605 |
| 4518 | DUAL SYNCHRONOUS COUNTERS | 606 |
| 4520 | DUAL SYNCHRONOUS COUNTERS | 607 |
| 4538 | DUAL RETRIGGERABLE PRECISION MONO STABLE MULTIVIBRATOR | 608 |
| 4543 | BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS | 610 |
| 4851 | 8-CHANNEL ANALOG MULTIPLEXER/DEMULTEPLEXER WITH INJECTION-CURRENT EFFECT CONTROL | 612 |

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| Device | Function | |
| 4852 | DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTEPLEXER WITH INJECTION-CURRENT EFFECT CONTROL | 612 |
| 5400 | 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS | 614 |
| 5401 | 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS | 614 |
| 5402 | 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS | 615 |
| 5403 | 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS | 615 |
| 7001 | QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS | 616 |
| 7002 | QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS | 616 |
| 7032 | QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS | 617 |
| 7046 | PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR | 618 |
| 7266 | QUAD 2-INPUT EXCLUSIVE-NOR GATES | 619 |
| 8003 | DUAL 2-INPUT POSITIVE-NAND GATES | 619 |
| 16240 | 16-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 620 |
| 16241 | 16-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 622 |
| 16244 | 16-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 624 |
| 16245 | 16-BIT BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 626 |
| 16260 | 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS | 628 |
| 16269 | 12-BIT TO 24-BIT REGISTERED BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 630 |
| 16270 | 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS | 632 |
| 16271 | 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS | 634 |
| 16282 | 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS | 636 |
| 16334 | 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 638 |
| 16344 | 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS | 640 |
| 16373 | 16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS | 642 |
| 16374 | 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS | 644 |
| 16409 | 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS | 646 |
| 16460 | 4-TO-1 MULTIPLEXED/DEMULTEPLEXED TRANSCIEVERS WITH 3-STATE OUTPUTS | 648 |
| 16470 | 16-BIT REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS | 650 |
| 16500 | 18-BIT UNIVERSAL BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 652 |
| 16501 | 18-BIT UNIVERSAL BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 654 |
| 16524 | 18-BIT REGISTERED BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 656 |
| 16525 | 18-BIT REGISTERED BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 658 |
| 16540 | 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 660 |
| 16541 | 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 661 |
| 16543 | 16-BIT REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS | 662 |
| 16600 | 18-BIT UNIVERSAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 664 |
| 16601 | 18-BIT UNIVERSAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 666 |
| 16620 | 16-BIT BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 668 |
| 16623 | 16-BIT BUS TRANSCIEVERS WITH 3-STATE OUTPUTS | 670 |
| 16640 | 16-BIT BUS TRANSCIEVER WITH 3-STATE OUTPUTS | 671 |
| 16646 | 16-BIT BUS TRANSCIEVERS AND REGISTERS WITH 3-STATE OUTPUTS | 672 |

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| Device | Function | |
| 16651 | 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS | 674 |
| 16652 | 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS | 676 |
| 16657 | 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS | 678 |
| 16721 | 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS | 680 |
| 16722 | 22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS | 681 |
| 16820 | 10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS | 682 |
| 16821 | 20-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 683 |
| 16823 | 18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS | 684 |
| 16825 | 18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 685 |
| 16827 | 20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 686 |
| 16831 | 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS | 688 |
| 16832 | 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS | 689 |
| 16833 | DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS | 690 |
| 16834 | 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 692 |
| 16835 | 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 693 |
| 16841 | 20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 694 |
| 16843 | 18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 695 |
| 16853 | DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS | 696 |
| 16861 | 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 698 |
| 16863 | 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 699 |
| 16901 | 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS | 700 |
| 16903 | 3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS | 702 |
| 16952 | 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS | 704 |
| 16973 | 8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS | 706 |
| 25244 | 25-W OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS | 708 |
| 25245 | 25-W OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 709 |
| 25642 | 25-W OCTAL BUS TRANSCEIVER | 710 |
| 29821 | 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 711 |
| 29825 | 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 712 |
| 29827 | 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 713 |
| 29828 | 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 714 |
| 29841 | 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 715 |
| 29843 | 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS | 716 |
| 29854 | 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER | 718 |
| 29863 | 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 720 |
| 29864 | 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 721 |
| 32240 | 32-BIT BUFFER/DRIVER | 722 |
| 32244 | 32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS | 724 |
| 32245 | 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 726 |
| 32316 | 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS | 728 |
| 32318 | 18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS | 730 |
| 32373 | 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS | 732 |

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| Device | Function | |
| 32374 | 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS | 734 |
| 32501 | 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 736 |
| 32543 | 36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS | 738 |
| 32973 | 16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH EIGHT INDEPENDENT BUFFERS | 740 |
| 40103 | 8-STAGE SYNCHRONOUS DOWN COUNTERS | 742 |
| 162240 | 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 744 |
| 162241 | 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 745 |
| 162244 | 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 746 |
| 162245 | 16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS | 747 |
| 162260 | 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS | 748 |
| 162268 | 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS | 750 |
| 162280 | 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS | 752 |
| 162282 | 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS | 754 |
| 162334 | 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 756 |
| 162344 | 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS | 758 |
| 162373 | 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS | 760 |
| 162374 | 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS | 761 |
| 162460 | 4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS | 762 |
| 162500 | 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 764 |
| 162501 | 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 766 |
| 162525 | 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 768 |
| 162541 | 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 770 |
| 162601 | 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS | 772 |
| 162721 | 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS | 774 |
| 162820 | 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS | 775 |
| 162823 | 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS | 776 |
| 162825 | 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 777 |
| 162827 | 20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS | 778 |
| 162830 | 1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS | 779 |
| 162831 | 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS | 780 |
| 162832 | 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS | 781 |
| 162834 | 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 782 |
| 162835 | 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 783 |
| 162836 | 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS | 784 |
| 162841 | 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS | 785 |
| 322244 | 32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS | 786 |
| 322374 | 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS | 787 |

FUNCTION

Translation

Single-Supply Voltage-Translator

| Description | Function | Device | CMOS Technology | | | | | |
|-------------------|---|--------|-----------------|-----|------|-----|-----------|--|
| | | | Low-Voltage | | | | Low-Power | |
| | | | LV | LVC | ALVC | AVC | AUP | |
| Configurable Gate | 2-input AND gate | 1G57 | | | | | | |
| | 2-input AND gate with both inputs inverted | | | | | | | |
| | 2-input NOR gate | | | | | | | |
| | 2-input NOR gate with both inputs inverted | | | | | | | |
| | 2-input NAND gate with inverted input | | | | | | ● | |
| | 2-input OR gate with inverted input | | | | | | | |
| | 2-input XNOR | 1G58 | | | | | | |
| | Inverter | | | | | | | |
| | Noninverted buffer | | | | | | | |
| | 2-input NAND gate | | | | | | | |
| | 2-input NAND gate with both inputs inverted | | | | | | | |
| | 2-input OR gate | | | | | | | |
| | 2-input OR gate with both inputs inverted | | | | | | | |
| | 2-input AND gate with inverted input | | | | | | ● | |
| | 2-input NOR gate with inverted input | | | | | | | |
| | 2-input XNOR | | 1G97 | | | | | |
| | Inverter | | | | | | | |
| | Noninverted buffer | | | | | | | |
| | 2-to-1 data selector | | | | | | | |
| | 2-input AND gate | | | | | | | |
| | 2-input AND gate with one inverted input | | | | | | | |
| | 2-input OR gate | | | | | | | |
| | 2-input OR gate with one inverted input | | | | | | ● | |
| | 2-input NAND gate with one inverted input | | | | | | | |
| | 2-input NOR gate with one inverted input | | | | | | | |
| | Inverter | 1G98 | | | | | | |
| | Noninverted buffer | | | | | | | |
| | 2-to-1 data selector | | | | | | | |
| | 2-input AND gate | | | | | | | |
| | 2-input AND gate with one inverted input | | | | | | | |
| | 2-input OR gate | | | | | | | |
| | 2-input OR gate with one inverted input | | | | | | ● | |
| | 2-input NAND gate with one inverted input | | | | | | | |
| | 2-input NOR gate with one inverted input | | | | | | | |
| | Inverter | | | | | | | |
| | Noninverted buffer | | | | | | | |

Dual-Supply Bus Transceiver

| Description | Device | Technology | | | | |
|------------------------|--------|------------------|------|------|------------------|----------------|
| | | Low-Voltage CMOS | | | | Low-Power CMOS |
| | | LV | LVC | ALVC | AVC | AUP |
| Single BusTransceiver | 1T45 | | ● | | ●/H● | |
| Dual BusTransceivers | 2T45 | | ● | | ●/H● | |
| 4-Bit BusTransceivers | 4T245 | | | | ●/H● | |
| | 8T245 | | ● | | ●/H● | |
| Octal BusTransceivers | 3245 | | C● | | | |
| | 4245 | | ●/C● | | | |
| | 16T245 | | ●/H● | | ●/H● | |
| 16-Bit BusTransceivers | 164245 | | | ● | A●/A●● B●/B●● | |
| 20-Bit BusTransceivers | 20T245 | | | | ●/H● | |
| 24-Bit BusTransceivers | 24T245 | | | | ●/H● | |
| 32-Bit BusTransceivers | 32T245 | | | | ●/H● | |
| | 324245 | | | | B● | |

Status ● : Product available in technology indicated * : New product planned in technology indicated

APPLICATION SPECIFIC (CompactFlash™, SD CARD, MultiMediaCards, iFC)

| Description | Device | Technology | | | | |
|---|--------|------------------|-----|------|-----|----------------|
| | | Low-Voltage CMOS | | | | Low-Power CMOS |
| | | LV | LVC | ALVC | AVC | AUP |
| MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD VOLTAGE-TRANSLATION TRANSCIEVER | 406 | | | | A● | |
| MMC, SD CARD, Memory Stick™ VOLTAGE-TRANSLATION TRANSCIEVER | 406L | | | | A● | |
| LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH DATA, 11-BIT ADDRESS, AND 13BIT CONTROL LINES | 4320 | ●A | | | | |

Status ● : Product available in technology indicated * : New product planned in technology indicated

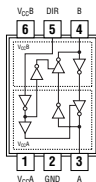
PIN ASSIGNMENTS

Translation

Pin Assignments

1T45

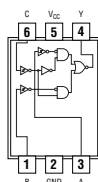
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 23

1T98

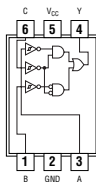
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



See page 30

1T57

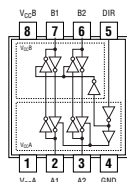
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



See page 27

2T45

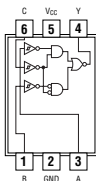
DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 31

1T58

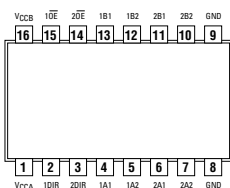
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



See page 28

4T245

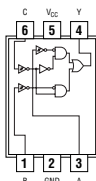
4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 35

1T97

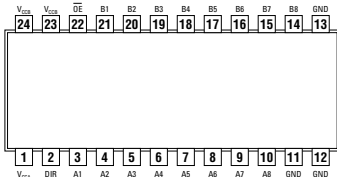
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION



See page 29

8T245

8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 37

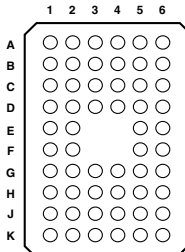
Pin Assignments

16T245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



QGL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

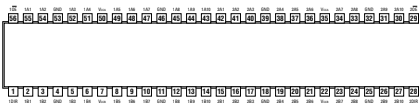
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------|-----|------|------|-----|------------------|
| A | 1DIR | NC | NC | NC | NC | $\overline{1OE}$ |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | VCCB | VCCA | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | VCCB | VCCA | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | $\overline{2OE}$ |

(1) NC - No internal connection

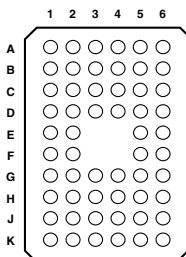
See page 41

20T245

20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



QGL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|------|------|------------------|------|-----|
| A | 1B1 | 1B2 | 1DIR | $\overline{1OE}$ | 1A2 | 1A1 |
| B | 1B3 | 1B4 | GND | GND | 1A4 | 1A3 |
| C | 1B5 | 1B6 | VCCB | VCCA | 1A6 | 1A5 |
| D | 1B7 | 1B8 | GND | GND | 1A8 | 1A7 |
| E | 1B9 | 1B10 | | | 1A10 | 1A9 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | VCCB | VCCA | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2B9 | 2B10 | 2DIR | $\overline{2OE}$ | 2A10 | 2A9 |

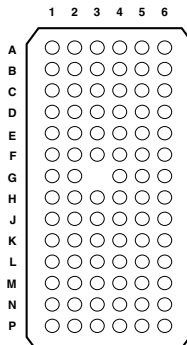
See page 45

Pin Assignments

24T245

24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

GRG OR ZRG PACKAGE
(TOP VIEW)



terminal assignments

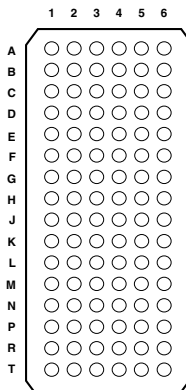
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------|------------------|------------------|------------------|------------------|------------------|
| A | $\overline{6OE}$ | $\overline{5OE}$ | $\overline{4OE}$ | $\overline{3OE}$ | $\overline{2OE}$ | $\overline{1OE}$ |
| B | 1B1 | 1B2 | V _{CCB} | V _{CCA} | 1A2 | 1A1 |
| C | 1B3 | 1B4 | GND | GND | 1A4 | 1A3 |
| D | 2B1 | 2B2 | V _{CCB} | V _{CCA} | 2A2 | 2A1 |
| E | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| F | 3B1 | 3B2 | GND | GND | 3A2 | 3A1 |
| G | 3B3 | 3B4 | | GND | 3A4 | 3A3 |
| H | 4B1 | 4B2 | V _{CCB} | V _{CCA} | 4A2 | 4A1 |
| J | 4B3 | 4B4 | GND | GND | 4A4 | 4A3 |
| K | 5B1 | 5B2 | GND | GND | 5A2 | 5A1 |
| L | 5B3 | 5B4 | V _{CCB} | V _{CCA} | 5A4 | 5A3 |
| M | 6B1 | 6B2 | GND | GND | 6A2 | 6A1 |
| N | 6B3 | 6B4 | V _{CCB} | V _{CCA} | 6A4 | 6A3 |
| P | 6DIR | 5DIR | 4DIR | 3DIR | 2DIR | 1DIR |

See page 47

32T245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS WITH 3-STATE DESELECTED OUTPUT

GRG OR ZRG PACKAGE
(TOP VIEW)



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|------------------|------------------|-----|-----|
| A | 1B2 | 1B1 | 1DIR | $\overline{1OE}$ | 1A1 | 1A2 |
| B | 1B4 | 1B3 | GND | GND | 1A3 | 1A4 |
| C | 1B6 | 1B5 | V _{CCB} | V _{CCA} | 1A5 | 1A6 |
| D | 1B8 | 1B7 | GND | GND | 1A7 | 1A8 |
| E | 2B2 | 2B1 | GND | GND | 2A1 | 2A2 |
| F | 2B4 | 2B3 | V _{CCB} | V _{CCA} | 2A3 | 2A4 |
| G | 2B6 | 2B5 | GND | GND | 2A5 | 2A6 |
| H | 2B7 | 2B8 | 2DIR | $\overline{2OE}$ | 2A8 | 2A7 |
| J | 3B2 | 3B1 | 3DIR | $\overline{3OE}$ | 3A1 | 3A2 |
| K | 3B4 | 3B3 | GND | GND | 3A3 | 3A4 |
| L | 3B6 | 3B5 | V _{CCB} | V _{CCA} | 3A5 | 3A6 |
| M | 3B8 | 3B7 | GND | GND | 3A7 | 3A8 |
| N | 4B2 | 4B1 | GND | GND | 4A1 | 4A2 |
| P | 4B4 | 4B3 | V _{CCB} | V _{CCA} | 4A3 | 4A4 |
| R | 4B6 | 4B5 | GND | GND | 4A5 | 4A6 |
| T | 4B7 | 4B8 | 4DIR | $\overline{4OE}$ | 4A8 | 4A7 |

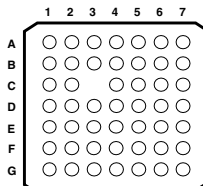
See page 50

Pin Assignments

406

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card
±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

GQC/ZQC PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS ⁽¹⁾

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------------------|------|-------|------------------|-------|------|-------------------|
| A | V _{CCA} | 2A | 4DIR | 2DIR | MODE1 | 10B1 | V _{CCB0} |
| B | 10A1 | 3A | 1A | 1DIR | MODE0 | 9B1 | 1B |
| C | 9A | 10A2 | | 3DIR | GND | 2B | 3B |
| D | 9DIR | 4A | 56DIR | GND | 4B | 11B | 12B |
| E | 78DIR | 6A | GND | $\overline{CS0}$ | GND | 10B2 | 9B2 |
| F | 7A | 8A | 12A | 13A | 7B | 5B | 14B |
| G | V _{CCA} | 5A | 11A | $\overline{CS1}$ | 8B | 6B | V _{CCB1} |

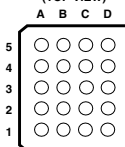
- (1) V_{CCA} powers all A-port I/Os and control inputs.
V_{CCB0} powers 1B, 2B, 3B, 4B, 9B1, and 10B1.
V_{CCB1} powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.

See page 53

406L

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

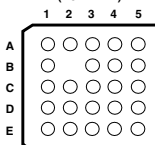
GXY OR ZXY PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS
(20-Ball GXY/ZXY Package)

| | A | B | C | D |
|---|------------------|---------|------------|------------------|
| 5 | V _{CCA} | CMD-dir | DAT0-dir | V _{CCB} |
| 4 | DAT3A | DAT2A | DAT2B | DAT3B |
| 3 | CLKA | GND | GND | CLKB |
| 2 | DAT1A | DAT0A | CMDB | DAT0B |
| 1 | CLK-f | CMDA | DAT123-dir | DAT1B |

GQS OR ZQS PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS
(24-Ball GQS/ZQS Package)

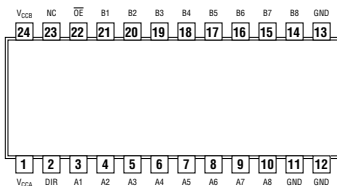
| | 1 | 2 | 3 | 4 | 5 |
|---|-------|---------|------------------|------------------|-------|
| A | DAT2A | CMD-dir | DAT0-dir | RSV | DAT2B |
| B | DAT3A | | V _{CCA} | V _{CCB} | DAT3B |
| C | CLKA | RSV | GND | GND | CLKB |
| D | DAT0A | CMDA | RSV | CMDB | DAT0B |
| E | DAT1A | CLK-f | DAT123-dir | RSV | DAT1B |

See page 58

Pin Assignments

3245

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

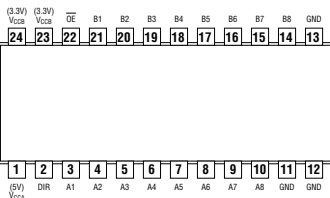


See page 61

4245

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS (SN74LVC4245A)

OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS (SN74LVCC4245A)

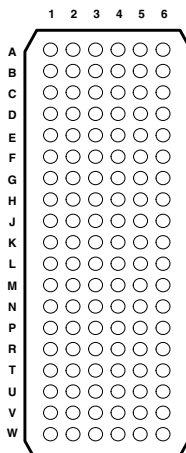


See page 62

4320

LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES

**GKF PACKAGE
(TOP VIEW)**



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|--------|--------|------------|-----------|--------|
| A | D12 | D04 | D03 | SD14 | SD12 | SD11 |
| B | D13 | D05 | D11 | SD13 | SD10 | SD09 |
| C | D14 | D06 | SD15 | SINPACK | SD08 | SD07 |
| D | D15 | D07 | VCC_CF | VCC_S | SD06 | SD05 |
| E | CE2 | CE1 | GND | GND | SD04 | SD03 |
| F | OE | A10 | VCC_CF | VCC_S | SD02 | SD01 |
| G | A09 | IORD | GND | GND | SD00 | SCET |
| H | A08 | IOWR | VCC_CF | VCC_S | EN_L | EN_H |
| J | A07 | WE | GND | GND | MASTER_EN | BUF_EN |
| K | A06 | READY | A05 | SCET | SOE | SIORD |
| L | A04 | RESET | GND | GND | SWE | SIOWR |
| M | A03 | WAIT | VCC_CF | VCC_S | SREADY | SRESET |
| N | A02 | INPACK | GND | GND | SWAIT | SREG |
| P | A01 | REG | VCC_CF | GND | SBVD2 | SBVD1 |
| R | A00 | BVD2 | VCC_CF | VCC_S | SA10 | SWP |
| T | D00 | BVD1 | VCC_SD | DIR (S/CF) | SA08 | SA09 |
| U | D01 | D08 | CD1 | DIR_OUT | SA06 | SA07 |
| V | D02 | D09 | CD2 | SA00 | SA04 | SA05 |
| W | WP | D10 | SCD | SA01 | SA02 | SA03 |

See page 63

164245

16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

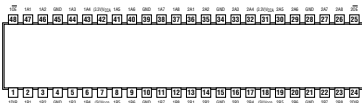
● SN74ALVC164245:

A port has V_{CCA} , which is set to operate at 2.5 V and 3.3 V
 B port has V_{CCB} , which is set to operate at 3.3 V and 5 V

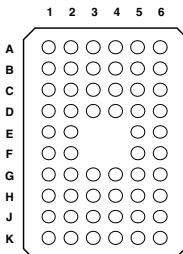
● SN74AVCB164245, SN74AVCBH164245:

The A-port is designed to track V_{CCA} .
 V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V

The B-port is designed to track V_{CCB} .
 V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V



**QGL OR ZQL PACKAGE
(TOP VIEW)**



TERMINAL ASSIGNMENTS ⁽¹⁾

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------|-----|-----------|-----------|-----|-----|
| A | 1DIR | NC | NC | NC | NC | 1OE |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V_{CCB} | V_{CCA} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V_{CCB} | V_{CCA} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | 2OE |

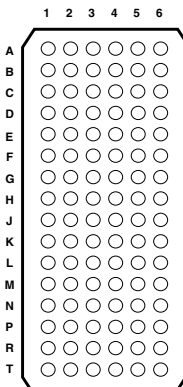
(1) NC - No internal connection

See page 67

324245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

**GKE PACKAGE
(TOP VIEW)**



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|-----------|-----------|-----|-----|
| A | 1B2 | 1B1 | 1DIR | 1OE | 1A1 | 1A2 |
| B | 1B4 | 1B3 | GND | GND | 1A3 | 1A4 |
| C | 1B6 | 1B5 | V_{CCB} | V_{CCA} | 1A5 | 1A6 |
| D | 1B8 | 1B7 | GND | GND | 1A7 | 1A8 |
| E | 2B2 | 2B1 | GND | GND | 2A1 | 2A2 |
| F | 2B4 | 2B3 | V_{CCB} | V_{CCA} | 2A3 | 2A4 |
| G | 2B6 | 2B5 | GND | GND | 2A5 | 2A6 |
| H | 2B7 | 2B8 | 2DIR | 2OE | 2A8 | 2A7 |
| J | 3B2 | 3B1 | 3DIR | 3OE | 3A1 | 3A2 |
| K | 3B4 | 3B3 | GND | GND | 3A3 | 3A4 |
| L | 3B6 | 3B5 | V_{CCB} | V_{CCA} | 3A5 | 3A6 |
| M | 3B8 | 3B7 | GND | GND | 3A7 | 3A8 |
| N | 4B2 | 4B1 | GND | GND | 4A1 | 4A2 |
| P | 4B4 | 4B3 | V_{CCB} | V_{CCA} | 4A3 | 4A4 |
| R | 4B6 | 4B5 | GND | GND | 4A5 | 4A6 |
| T | 4B7 | 4B8 | 4DIR | 4OE | 4A8 | 4A7 |

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**FUNCTION
AND
ELECTRICAL
CHARACTERISTICS**

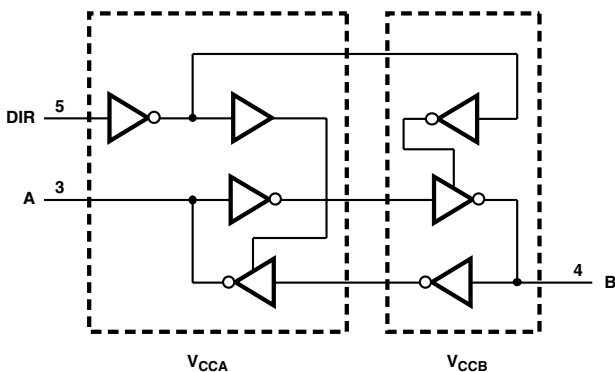
Translation

1T45

SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- This Single-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

Logic Diagram



FUNCTION TABLE ⁽¹⁾

| INPUT DIR | OPERATION |
|-----------|-----------------|
| L | B data to A bus |
| H | A data to B bus |

(1) Input circuits of the data I/Os always are active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | UNIT |
|------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.004 | 0.004 | 0.004 | 0.004 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

 $*I_{CCA} + I_{CCB}$
SWITCHING CHARACTERISTICS

| V _{CCA} = 1.5V | | | | | | | | | | | | |
|-------------------------|-------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | |
| t_{FHL} | A | B | MAX | 3.3 | 4.2 | 5.2 | 5.6 | 3.3 | 4.2 | 5.2 | 5.6 | |
| t_{FHL} | | | | 3.8 | 4.2 | 5.2 | 5.6 | 3.8 | 4.2 | 5.2 | 5.6 | |
| t_{FHL} | B | A | MAX | 4.8 | 4.9 | 5.3 | 5.5 | 4.8 | 4.9 | 5.3 | 5.5 | |
| t_{FHL} | | | | 4.8 | 4.9 | 5.3 | 5.5 | 4.8 | 4.9 | 5.3 | 5.5 | |
| t_{FHL} | DIR | A | MAX | 6.9 | 6.9 | 6.8 | 6.7 | 6.9 | 6.9 | 6.8 | 6.7 | |
| t_{FHL} | | | | 6.9 | 6.9 | 6.8 | 6.7 | 6.9 | 6.9 | 6.8 | 6.7 | |
| t_{FHL} | DIR | B | MAX | 4.5 | 4.7 | 7.1 | 8.1 | 4.5 | 4.7 | 7.1 | 8.1 | |
| t_{FHL} | | | | 4.5 | 4.7 | 7.1 | 8.1 | 4.5 | 4.7 | 7.1 | 8.1 | |
| t_{FHL}^* | DIR | A | MAX | 9.3 | 9.6 | 12.4 | 13.6 | 9.3 | 9.6 | 12.4 | 13.6 | |
| t_{FHL}^* | | | | 9.3 | 9.6 | 12.4 | 13.6 | 9.3 | 9.6 | 12.4 | 13.6 | |
| t_{FHL}^* | DIR | B | MAX | 10.7 | 11.1 | 12 | 12.3 | 10.7 | 11.1 | 12 | 12.3 | |
| t_{FHL}^* | | | | 10.7 | 11.1 | 12 | 12.3 | 10.7 | 11.1 | 12 | 12.3 | |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 1.8V | | | | | | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | |
| t_{FHL} | A | B | MAX | 7.2 | 8.3 | 10.3 | 17.7 | 3.4 | 3.9 | 5 | 5.3 | |
| t_{FHL} | | | | 7 | 7.1 | 8.5 | 14.3 | 3.4 | 3.9 | 5 | 5.3 | |
| t_{FHL} | B | A | MAX | 15.1 | 15.5 | 16 | 17.7 | 4.4 | 4.6 | 5 | 5.2 | |
| t_{FHL} | | | | 12.2 | 12.6 | 12.9 | 14.3 | 4.4 | 4.6 | 5 | 5.2 | |
| t_{FHL} | DIR | A | MAX | 17.1 | 18.4 | 18.5 | 19.4 | 6 | 5.9 | 5.9 | 5.9 | |
| t_{FHL} | | | | 10.9 | 10.7 | 10.5 | 10.5 | 6 | 5.9 | 5.9 | 5.9 | |
| t_{FHL} | DIR | B | MAX | 8.2 | 10.3 | 11.5 | 21.9 | 5.3 | 4.4 | 6.8 | 7.7 | |
| t_{FHL} | | | | 6.4 | 8.4 | 9.2 | 16 | 5.3 | 4.4 | 6.8 | 7.7 | |
| t_{FHL}^* | DIR | A | MAX | 12.8 | 23.9 | 25.2 | 33.7 | 8.7 | 9 | 11.8 | 12.9 | |
| t_{FHL}^* | | | | 13.3 | 22.9 | 24.4 | 36.2 | 8.7 | 9 | 11.8 | 12.9 | |
| t_{FHL}^* | DIR | B | MAX | 10.9 | 19 | 20.8 | 28.2 | 9.4 | 9.8 | 10.9 | 11.2 | |
| t_{FHL}^* | | | | 12.7 | 25.5 | 27 | 33.7 | 9.4 | 9.8 | 10.9 | 11.2 | |

| V _{CCA} = 1.8V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{FHL} | A | B | MAX | 3.4 | 3.9 | 5 | 5.3 |
| t_{FHL} | | | | 3.4 | 3.9 | 5 | 5.3 |
| t_{FHL} | B | A | MAX | 4.4 | 4.6 | 5 | 5.2 |
| t_{FHL} | | | | 4.4 | 4.6 | 5 | 5.2 |
| t_{FHL} | DIR | A | MAX | 6 | 5.9 | 5.9 | 5.9 |
| t_{FHL} | | | | 6 | 5.9 | 5.9 | 5.9 |
| t_{FHL} | DIR | B | MAX | 5.3 | 4.4 | 6.8 | 7.7 |
| t_{FHL} | | | | 5.3 | 4.4 | 6.8 | 7.7 |
| t_{FHL}^* | DIR | A | MAX | 8.7 | 9 | 11.8 | 12.9 |
| t_{FHL}^* | | | | 8.7 | 9 | 11.8 | 12.9 |
| t_{FHL}^* | DIR | B | MAX | 9.4 | 9.8 | 10.9 | 11.2 |
| t_{FHL}^* | | | | 9.4 | 9.8 | 10.9 | 11.2 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V |
| t _{PLH} | A | B | MAX | 5.1 | 6.4 | 8.5 | 16 | 3 | 3.4 | 4.6 | 4.9 |
| t _{PHL} | | | | 4.6 | 5.4 | 7.5 | 12.9 | 3 | 3.4 | 4.6 | 4.9 |
| t _{PLH} | B | A | MAX | 7.5 | 8 | 8.5 | 10.3 | 3.3 | 3.4 | 3.8 | 4.2 |
| t _{PHL} | | | | 6.2 | 7 | 7.5 | 8.5 | 3.3 | 3.4 | 3.8 | 4.2 |
| t _{PLZ} | DIR | A | MAX | 8.1 | 8.1 | 8.1 | 8.1 | 3.8 | 3.8 | 3.8 | 3.8 |
| t _{PHZ} | | | | 5.8 | 5.9 | 5.9 | 5.9 | 3.8 | 3.8 | 3.8 | 3.8 |
| t _{PLZ} | DIR | B | MAX | 7.1 | 10.2 | 11.4 | 23.7 | 4 | 4.1 | 6.5 | 7.6 |
| t _{PHZ} | | | | 5.3 | 8.4 | 9.6 | 18.9 | 4 | 4.1 | 6.5 | 7.6 |
| t _{PLH} * | DIR | A | MAX | 12.8 | 16.4 | 18.1 | 29.2 | 7.3 | 7.5 | 10.3 | 11.8 |
| t _{PHL} * | | | | 13.3 | 17.2 | 18.9 | 32.2 | 7.3 | 7.5 | 10.3 | 11.8 |
| t _{PLZ} * | DIR | B | MAX | 10.9 | 12.3 | 14.4 | 21.9 | 6.6 | 7 | 8.1 | 8.6 |
| t _{PHZ} * | | | | 12.7 | 13.5 | 15.6 | 21 | 6.6 | 7 | 8.1 | 8.6 |

| V _{CCA} = 2.5V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 3 | 3.4 | 4.6 | 4.9 |
| t _{PHL} | | | | 3 | 3.4 | 4.6 | 4.9 |
| t _{PLH} | B | A | MAX | 3.3 | 3.4 | 3.8 | 4.2 |
| t _{PHL} | | | | 3.3 | 3.4 | 3.8 | 4.2 |
| t _{PLZ} | DIR | A | MAX | 3.8 | 3.8 | 3.8 | 3.8 |
| t _{PHZ} | | | | 3.8 | 3.8 | 3.8 | 3.8 |
| t _{PLZ} | DIR | B | MAX | 4 | 4.1 | 6.5 | 7.6 |
| t _{PHZ} | | | | 4 | 4.1 | 6.5 | 7.6 |
| t _{PLH} * | DIR | A | MAX | 7.3 | 7.5 | 10.3 | 11.8 |
| t _{PHL} * | | | | 7.3 | 7.5 | 10.3 | 11.8 |
| t _{PLZ} * | DIR | B | MAX | 6.6 | 7 | 8.1 | 8.6 |
| t _{PHZ} * | | | | 6.6 | 7 | 8.1 | 8.6 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V |
| t _{PLH} | A | B | MAX | 4.4 | 5.8 | 8 | 15.5 | 2.8 | 3.3 | 4.4 | 4.7 |
| t _{PHL} | | | | 4 | 5 | 7 | 12.6 | 2.8 | 3.3 | 4.4 | 4.7 |
| t _{PLH} | B | A | MAX | 5.4 | 5.8 | 6.4 | 8.3 | 2.8 | 3 | 3.4 | 3.8 |
| t _{PHL} | | | | 4.5 | 5 | 5.4 | 7.1 | 2.8 | 3 | 3.4 | 3.8 |
| t _{PLZ} | DIR | A | MAX | 7.3 | 7.3 | 7.3 | 7.3 | 4.3 | 4.3 | 4.3 | 4.3 |
| t _{PHZ} | | | | 5.7 | 5.7 | 5.6 | 5.6 | 4.3 | 4.3 | 4.3 | 4.3 |
| t _{PLZ} | DIR | B | MAX | 6.8 | 8.8 | 10.1 | 20.5 | 4.9 | 4 | 6.5 | 7.4 |
| t _{PHZ} | | | | 4.9 | 7.1 | 7.8 | 14.5 | 4.9 | 4 | 6.5 | 7.4 |
| t _{PLH} * | DIR | A | MAX | 10.3 | 12.9 | 14.2 | 22.8 | 6.7 | 7 | 9.9 | 11.2 |
| t _{PHL} * | | | | 11.3 | 13.8 | 15.5 | 27.6 | 6.7 | 7 | 9.9 | 11.2 |
| t _{PLZ} * | DIR | B | MAX | 10.1 | 11.5 | 13.6 | 21.1 | 6.8 | 7.2 | 8.5 | 8.9 |
| t _{PHZ} * | | | | 11.3 | 12.3 | 14.3 | 19.9 | 6.8 | 7.2 | 8.5 | 8.9 |

| V _{CCA} = 3.3V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.8 | 3.3 | 4.4 | 4.7 |
| t _{PHL} | | | | 2.8 | 3.3 | 4.4 | 4.7 |
| t _{PLH} | B | A | MAX | 2.8 | 3 | 3.4 | 3.8 |
| t _{PHL} | | | | 2.8 | 3 | 3.4 | 3.8 |
| t _{PLZ} | DIR | A | MAX | 4.3 | 4.3 | 4.3 | 4.3 |
| t _{PHZ} | | | | 4.3 | 4.3 | 4.3 | 4.3 |
| t _{PLZ} | DIR | B | MAX | 4.9 | 4 | 6.5 | 7.4 |
| t _{PHZ} | | | | 4.9 | 4 | 6.5 | 7.4 |
| t _{PLH} * | DIR | A | MAX | 6.7 | 7 | 9.9 | 11.2 |
| t _{PHL} * | | | | 6.7 | 7 | 9.9 | 11.2 |
| t _{PLZ} * | DIR | B | MAX | 6.8 | 7.2 | 8.5 | 8.9 |
| t _{PHZ} * | | | | 6.8 | 7.2 | 8.5 | 8.9 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 5.0V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-------------|-------------|-------------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
| t _{FRH} | A | B | MAX | 3.9 | 5.4 | 7.5 | 15.1 |
| t _{FRL} | | | | 3.5 | 4.5 | 6.2 | 12.2 |
| t _{FRH} | B | A | MAX | 3.9 | 4.4 | 5.1 | 7.2 |
| t _{FRL} | | | | 3.5 | 4 | 4.6 | 7 |
| t _{FRZ} | DIR | A | MAX | 5.4 | 5.5 | 5.4 | 5.4 |
| t _{FRZ} | | | | 3.7 | 3.7 | 3.8 | 3.8 |
| t _{FRZ} | DIR | B | MAX | 6.5 | 8.5 | 9.8 | 20.2 |
| t _{FRZ} | | | | 4.5 | 7 | 7.4 | 14.8 |
| t _{FRZ} * | DIR | A | MAX | 8.4 | 11.4 | 12.5 | 22 |
| t _{FRZ} * | | | | 10 | 12.5 | 14.4 | 27.2 |
| t _{FRZ} * | DIR | B | MAX | 7.6 | 9.1 | 11.3 | 18.9 |
| t _{FRZ} * | | | | 8.6 | 10 | 11.6 | 17.6 |

UNIT : ns

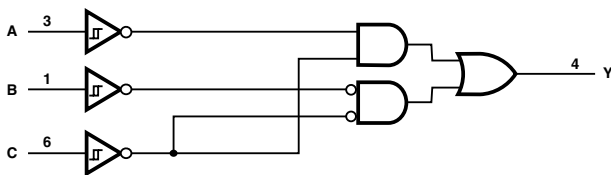
*The enable time is a calculated value, derived using the formula shown in the enable times section.

1T57

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|--------|---|---|-------------|
| C | B | A | |
| L | L | L | H |
| L | L | H | L |
| L | H | L | L |
| L | H | H | L |
| H | L | L | L |
| H | L | H | L |
| H | H | L | H |
| H | H | H | H |

FUNCTION SELECTION TABLE

| LOGIC FUNCTION |
|--|
| 2-input AND gate |
| 2-input NOR gate with both inputs inverted |
| 2-input NAND gate with inverted input |
| 2-input OR gate with inverted input |
| 2-input AND gate with both inputs inverted |
| 2-input NOR gate |
| 2-input XNOR gate |
| Inverter |
| Noninverted buffer |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AUP 3.3V | AUP 2.5V | UNIT |
|-----------|------------|-------------|-------------|------|
| I_{CC} | MAX | 0.0009 | 0.0009 | mA |
| I_{BH} | MAX | -4 | -3.1 | mA |
| I_{BL} | MAX | 4 | 3.1 | mA |

SWITCHING CHARACTERISTICS

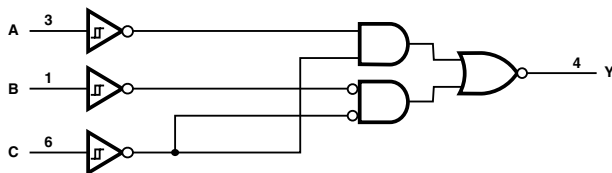
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUP 3.3V | AUP 2.5V |
|-----------|--------------|------------|------------|-------------|-------------|
| t_{PLH} | $V_i = 1.8V$ | A, B, or C | Y | MAX | 8.5 |
| | | | | | 7.9 |
| t_{PHL} | $V_i = 1.8V$ | A, B, or C | Y | MAX | 8.5 |
| | | | | | 7.9 |
| t_{PLH} | $V_i = 2.5V$ | A, B, or C | Y | MAX | 6.1 |
| | | | | | 7.1 |
| t_{PHL} | $V_i = 2.5V$ | A, B, or C | Y | MAX | 6.1 |
| | | | | | 7.1 |

UNIT : ns

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|--------|---|---|-------------|
| C | B | A | |
| L | L | L | L |
| L | L | H | H |
| L | H | L | L |
| L | H | H | H |
| H | L | L | H |
| H | L | H | H |
| H | H | L | L |
| H | H | H | L |

FUNCTION SELECTION TABLE

| LOGIC FUNCTION |
|---|
| 2-input NAND gate |
| 2-input OR gate with both inputs inverted |
| 2-input AND gate with inverted input |
| 2-input NOR gate with inverted input |
| 2-input NAND gate with both inputs inverted |
| 2-input OR gate |
| 2-input XOR gate |
| Inverter |
| Noninverted buffer |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AUP 3.3V | AUP 2.5V | UNIT |
|-----------|------------|-------------|-------------|------|
| I_{CC} | MAX | 0.0009 | 0.0009 | mA |
| I_{DS} | MAX | -4 | -3.1 | mA |
| I_{OL} | MAX | 4 | 3.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUP 3.3V | AUP 2.5V |
|-----------|--------------|------------|------------|-------------|-------------|
| | | | | 8.5 | 7.9 |
| t_{RHS} | $V_i = 1.8V$ | A, B, or C | Y | MAX | 8.5 |
| t_{FHL} | | | | | 7.9 |
| t_{RHS} | $V_i = 2.5V$ | A, B, or C | Y | MAX | 6.1 |
| t_{FHL} | | | | | 7.1 |
| | | | | | 6.1 |
| | | | | | 7.1 |

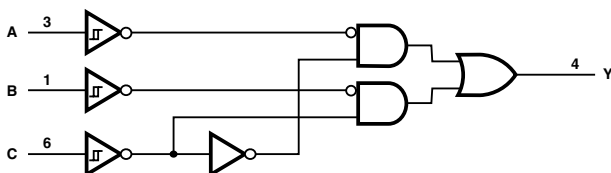
UNIT : ns

1T97

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| C | B | A | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

FUNCTION SELECTION TABLE

| LOGIC FUNCTION |
|---|
| 2-to-1 data selector |
| 2-input AND gate |
| 2-input OR gate with one inverted input |
| 2-input NAND gate with one inverted input |
| 2-input AND gate with one inverted input |
| 2-input NOR gate with one inverted input |
| 2-input OR gate |
| Inverter |
| Noninverted buffer |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AUP 3.3V | AUP 2.5V | UNIT |
|-----------|------------|-------------|-------------|------|
| I_{CC} | MAX | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -4 | -3.1 | mA |
| I_{OL} | MAX | 4 | 3.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUP 3.3V | AUP 2.5V |
|-----------|---------------------------|--------|------------|-------------|-------------|
| t_{PLH} | $V_i = 1.8V$, A, B, or C | Y | MAX | 8.5 | 7.9 |
| t_{PHL} | | | | 8.5 | 7.9 |
| t_{PLH} | $V_i = 2.5V$, A, B, or C | Y | MAX | 6.1 | 7.1 |
| t_{PHL} | | | | 6.1 | 7.1 |
| t_{PLH} | $V_i = 3.3V$, A, B, or C | Y | MAX | 5.7 | 6.5 |
| t_{PHL} | | | | 5.7 | 6.5 |

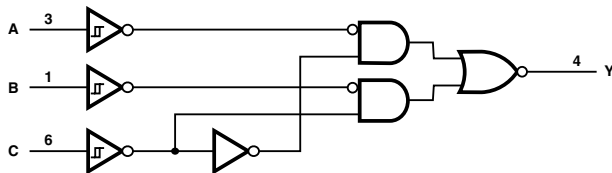
UNIT : ns

1T98

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|--------|---|---|-------------|
| C | B | A | |
| L | L | L | H |
| L | L | H | H |
| L | H | L | L |
| L | H | H | L |
| H | L | L | H |
| H | L | H | L |
| H | H | L | H |
| H | H | H | L |

FUNCTION SELECTION TABLE

| LOGIC FUNCTION |
|---|
| 2-to-1 data selector |
| 2-input AND gate |
| 2-input OR gate with one inverted input |
| 2-input NAND gate with one inverted input |
| 2-input AND gate with one inverted input |
| 2-input NOR gate with one inverted input |
| 2-input OR gate |
| Inverter |
| Noninverted buffer |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AUP 3.3V | AUP 2.5V | UNIT |
|-----------|------------|-------------|-------------|------|
| I_{CC} | MAX | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -4 | -3.1 | mA |
| I_{OL} | MAX | 4 | 3.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUP 3.3V | AUP 2.5V |
|-----------|--------------|------------|------------|-------------|-------------|
| t_{rHL} | $V_i = 1.8V$ | A, B, or C | Y | MAX | 8.5 |
| | | | | | 7.9 |
| t_{rHL} | $V_i = 2.5V$ | A, B, or C | Y | MAX | 6.1 |
| | | | | | 7.1 |
| t_{rHL} | $V_i = 3.3V$ | A, B, or C | Y | MAX | 5.7 |
| | | | | | 6.5 |

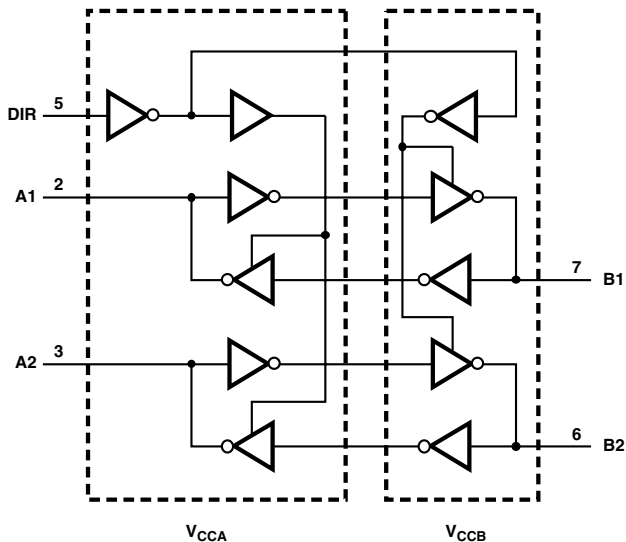
UNIT : ns

2T45

DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- This Dual-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

Logic Diagram



FUNCTION TABLE⁽¹⁾
(each transceiver)

| INPUT | OPERATION |
|-------|-----------------|
| DIR | |
| L | B data to A bus |
| H | A data to B bus |

(1) Input circuits of the data I/Os always are active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | UNIT |
|------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.004 | 0.004 | 0.004 | 0.004 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

* I_{CCA} + I_{CCB}

SWITCHING CHARACTERISTICS

| $V_{CCA} = 1.5V$ | | | | | | | | | | | | | |
|------------------|-------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | | |
| t_{PLH} | A | B | MAX | 3.5 | 3.7 | 4.6 | 5.4 | 3.5 | 3.7 | 4.6 | 5.4 | | |
| t_{PHL} | | | | 3.5 | 3.7 | 4.6 | 5.4 | 3.5 | 3.7 | 4.6 | 5.4 | | |
| t_{PLH} | B | A | MAX | 4.7 | 4.9 | 5.2 | 5.4 | 4.7 | 4.9 | 5.2 | 5.4 | | |
| t_{PHL} | | | | 4.7 | 4.9 | 5.2 | 5.4 | 4.7 | 4.9 | 5.2 | 5.4 | | |
| t_{FHLZ} | DIR | A | MAX | 7.6 | 7.7 | 7.8 | 8.5 | 4.6 | 5.5 | 7.1 | 8.5 | | |
| t_{FLZ} | | | | 7.6 | 7.7 | 7.8 | 8.5 | 4.6 | 5.5 | 7.1 | 8.5 | | |
| t_{FHLZ} | DIR | B | MAX | 7.1 | 6.9 | 6.9 | 7 | 7.1 | 6.9 | 6.9 | 7 | | |
| t_{FLZ} | | | | 7.1 | 6.9 | 6.9 | 7 | 7.1 | 6.9 | 6.9 | 7 | | |
| t_{R2H}^* | DIR | A | MAX | 11.8 | 11.8 | 12.1 | 12.4 | 11.8 | 11.8 | 12.1 | 12.4 | | |
| t_{R2L}^* | | | | 11.8 | 11.8 | 12.1 | 12.4 | 11.8 | 11.8 | 12.1 | 12.4 | | |
| t_{R2H}^* | DIR | B | MAX | 7.8 | 9.1 | 11.6 | 13.9 | 7.8 | 9.1 | 11.6 | 13.9 | | |
| t_{R2L}^* | | | | 7.8 | 9.1 | 11.6 | 13.9 | 7.8 | 9.1 | 11.6 | 13.9 | | |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| $V_{CCA} = 1.8V$ | | | | | | | | | | | | | |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|--|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | | |
| t_{PLH} | A | B | MAX | 7.2 | 8.3 | 10.3 | 17.7 | 3.1 | 3.4 | 4.3 | 5.2 | | |
| t_{PHL} | | | | 7 | 7.1 | 8.5 | 14.3 | 3.1 | 3.4 | 4.3 | 5.2 | | |
| t_{PLH} | B | A | MAX | 15.1 | 15.5 | 16 | 17.7 | 3.8 | 4 | 4.4 | 4.7 | | |
| t_{PHL} | | | | 12.2 | 12.6 | 12.9 | 14.3 | 3.8 | 4 | 4.4 | 4.7 | | |
| t_{FHLZ} | DIR | A | MAX | 29.3 | 30.5 | 30.5 | 30.9 | 5.2 | 5.3 | 6.9 | 8.1 | | |
| t_{FLZ} | | | | 19.4 | 19.5 | 19.6 | 19.7 | 5.2 | 5.3 | 6.9 | 8.1 | | |
| t_{FHLZ} | DIR | B | MAX | 8.6 | 11.3 | 14.9 | 27.9 | 5.9 | 5.7 | 5.9 | 5.8 | | |
| t_{FLZ} | | | | 7.1 | 9.7 | 12.6 | 19.5 | 5.9 | 5.7 | 5.9 | 5.8 | | |
| t_{R2H}^* | DIR | A | MAX | 22.2 | 25.2 | 28.6 | 37.2 | 9.7 | 9.7 | 10.3 | 10.4 | | |
| t_{R2L}^* | | | | 20.8 | 23.9 | 27.8 | 42.2 | 9.7 | 9.7 | 10.3 | 10.4 | | |
| t_{R2H}^* | DIR | B | MAX | 26.6 | 27.8 | 29.9 | 37.4 | 8.3 | 8.6 | 11.2 | 13.3 | | |
| t_{R2L}^* | | | | 36.3 | 37.6 | 39 | 45.2 | 8.3 | 8.6 | 11.2 | 13.3 | | |

| $V_{CCA} = 1.8V$ | | | | | | | |
|------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 3.1 | 3.4 | 4.3 | 5.2 |
| t_{PHL} | | | | 3.1 | 3.4 | 4.3 | 5.2 |
| t_{PLH} | B | A | MAX | 3.8 | 4 | 4.4 | 4.7 |
| t_{PHL} | | | | 3.8 | 4 | 4.4 | 4.7 |
| t_{FHLZ} | DIR | A | MAX | 4.5 | 5.3 | 6.9 | 8.1 |
| t_{FLZ} | | | | 4.5 | 5.3 | 6.9 | 8.1 |
| t_{FHLZ} | DIR | B | MAX | 5.9 | 5.7 | 5.9 | 5.8 |
| t_{FLZ} | | | | 5.9 | 5.7 | 5.9 | 5.8 |
| t_{R2H}^* | DIR | A | MAX | 9.7 | 9.7 | 10.3 | 10.4 |
| t_{R2L}^* | | | | 9.7 | 9.7 | 10.3 | 10.4 |
| t_{R2H}^* | DIR | B | MAX | 7.4 | 8.6 | 11.2 | 13.3 |
| t_{R2L}^* | | | | 7.4 | 8.6 | 11.2 | 13.3 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V |
| t _{PLH} | A | B | MAX | 5.1 | 6.4 | 8.5 | 16 | 2.6 | 3 | 4 | 4.9 |
| t _{PHL} | | | | 4.6 | 5.4 | 7.5 | 12.9 | 2.6 | 3 | 4 | 4.9 |
| t _{PLH} | B | A | MAX | 7.5 | 8 | 8.5 | 10.3 | 2.8 | 3 | 3.4 | 3.8 |
| t _{PHL} | | | | 6.2 | 7 | 7.5 | 8.5 | 2.8 | 3 | 3.4 | 3.8 |
| t _{PLZ} | DIR | A | MAX | 16.5 | 16.8 | 16.8 | 17.1 | 4.3 | 5 | 6.4 | 7.9 |
| t _{PHZ} | | | | 12.3 | 12.3 | 12.5 | 12.6 | 4.3 | 5 | 6.4 | 7.9 |
| t _{PLZ} | DIR | B | MAX | 7.6 | 10.5 | 13.9 | 27.9 | 4.1 | 4.2 | 4.3 | 4.3 |
| t _{PHZ} | | | | 6.2 | 8.9 | 11.2 | 18.9 | 4.1 | 4.2 | 4.3 | 4.3 |
| t _{PLZ*} | DIR | A | MAX | 13.7 | 16.9 | 19.7 | 29.2 | 6.9 | 7.2 | 7.7 | 7.9 |
| t _{PHZ*} | | | | 13.8 | 17.5 | 21.4 | 36.4 | 6.9 | 7.2 | 7.7 | 7.9 |
| t _{PLZ*} | DIR | B | MAX | 17.4 | 18.7 | 21 | 28.6 | 6.8 | 7.9 | 10.4 | 12.8 |
| t _{PHZ*} | | | | 21.1 | 22.2 | 24.3 | 30 | 6.8 | 7.9 | 10.4 | 12.8 |

| V _{CCA} = 2.5V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.6 | 3 | 4 | 4.9 |
| t _{PHL} | | | | 2.6 | 3 | 4 | 4.9 |
| t _{PLH} | B | A | MAX | 2.8 | 3 | 3.4 | 3.8 |
| t _{PHL} | | | | 2.8 | 3 | 3.4 | 3.8 |
| t _{PLZ} | DIR | A | MAX | 4.3 | 5 | 6.4 | 7.9 |
| t _{PHZ} | | | | 4.3 | 5 | 6.4 | 7.9 |
| t _{PLZ} | DIR | B | MAX | 4.1 | 4.2 | 4.3 | 4.3 |
| t _{PHZ} | | | | 4.1 | 4.2 | 4.3 | 4.3 |
| t _{PLZ*} | DIR | A | MAX | 6.9 | 7.2 | 7.7 | 7.9 |
| t _{PHZ*} | | | | 6.9 | 7.2 | 7.7 | 7.9 |
| t _{PLZ*} | DIR | B | MAX | 6.8 | 7.9 | 10.4 | 12.8 |
| t _{PHZ*} | | | | 6.8 | 7.9 | 10.4 | 12.8 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V |
| t _{PLH} | A | B | MAX | 4.4 | 5.8 | 8 | 15.5 | 2.4 | 2.8 | 3.8 | 4.7 |
| t _{PHL} | | | | 4 | 5 | 7 | 12.6 | 2.4 | 2.8 | 3.8 | 4.7 |
| t _{PLH} | B | A | MAX | 5.4 | 5.8 | 6.4 | 8.3 | 2.4 | 2.6 | 3.1 | 3.6 |
| t _{PHL} | | | | 4.5 | 5 | 5.4 | 7.1 | 2.4 | 2.6 | 3.1 | 3.6 |
| t _{PLZ} | DIR | A | MAX | 10.4 | 10.8 | 10.8 | 10.9 | 4 | 4.7 | 6.5 | 8 |
| t _{PHZ} | | | | 7.8 | 8.1 | 8.4 | 8.4 | 4 | 4.7 | 6.5 | 8 |
| t _{PLZ} | DIR | B | MAX | 7.4 | 10.4 | 13.7 | 27.3 | 4.2 | 4.6 | 5.6 | 6.6 |
| t _{PHZ} | | | | 5.6 | 8.3 | 11.3 | 17.7 | 4.2 | 4.6 | 5.6 | 6.6 |
| t _{PLZ*} | DIR | A | MAX | 11 | 14.1 | 17.7 | 26 | 6.6 | 6.2 | 6.6 | 6.9 |
| t _{PHZ*} | | | | 11.9 | 15.4 | 19.1 | 34.4 | 6.6 | 6.2 | 6.6 | 6.9 |
| t _{PLZ*} | DIR | B | MAX | 12.2 | 13.9 | 16.4 | 23.9 | 6.3 | 7.4 | 10.3 | 12.7 |
| t _{PHZ*} | | | | 14.4 | 15.8 | 17.8 | 23.5 | 6.3 | 7.4 | 10.3 | 12.7 |

| V _{CCA} = 3.3V | | | | | | | |
|-------------------------|-------|--------|------------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.4 | 2.8 | 3.8 | 4.7 |
| t _{PHL} | | | | 2.4 | 2.8 | 3.8 | 4.7 |
| t _{PLH} | B | A | MAX | 2.4 | 2.6 | 3.1 | 3.6 |
| t _{PHL} | | | | 2.4 | 2.6 | 3.1 | 3.6 |
| t _{PLZ} | DIR | A | MAX | 4 | 4.7 | 6.5 | 8 |
| t _{PHZ} | | | | 4 | 4.7 | 6.5 | 8 |
| t _{PLZ} | DIR | B | MAX | 3.5 | 4.6 | 5.6 | 6.6 |
| t _{PHZ} | | | | 3.5 | 4.6 | 5.6 | 6.6 |
| t _{PLZ*} | DIR | A | MAX | 5.9 | 6.2 | 6.6 | 6.9 |
| t _{PHZ*} | | | | 5.9 | 6.2 | 6.6 | 6.9 |
| t _{PLZ*} | DIR | B | MAX | 6.3 | 7.4 | 10.3 | 12.7 |
| t _{PHZ*} | | | | 6.3 | 7.4 | 10.3 | 12.7 |

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

| V _{CCA} = 5.0V | | | | | | | |
|-------------------------|-------|--------|------------|--------|----------|----------|----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
| t _{FRH} | A | B | MAX | 3.9 | 5.4 | 7.5 | 15.1 |
| t _{FRL} | | | | 3.5 | 4.5 | 6.2 | 12.2 |
| t _{FRH} | B | A | MAX | 3.9 | 4.4 | 5.1 | 7.2 |
| t _{FRL} | | | | 3.5 | 4 | 4.6 | 7 |
| t _{FRZ} | DIR | A | MAX | 5.4 | 5.5 | 5.4 | 5.4 |
| t _{FRZ} | | | | 3.7 | 3.7 | 3.8 | 3.8 |
| t _{FRZ} | DIR | B | MAX | 6.5 | 8.5 | 9.8 | 20.2 |
| t _{FRZ} | | | | 4.5 | 7 | 7.4 | 14.8 |
| t _{FRZ} * | DIR | A | MAX | 8.4 | 11.4 | 12.5 | 22 |
| t _{FRZ} * | | | | 10 | 12.5 | 14.4 | 27.2 |
| t _{FRZ} * | DIR | B | MAX | 7.6 | 9.1 | 11.3 | 18.9 |
| t _{FRZ} * | | | | 8.6 | 10 | 11.6 | 17.6 |

UNIT : ns

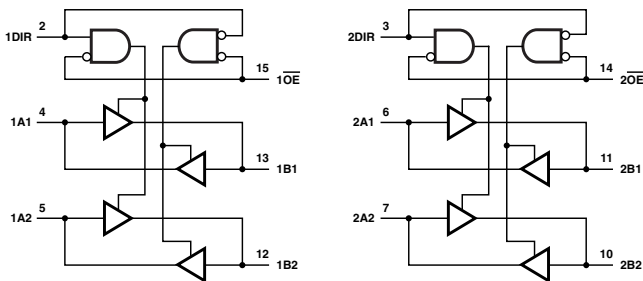
*The enable time is a calculated value, derived using the formula shown in the enable times section.

4T245

4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- This 4-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 4-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | All output Hi-Z |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | UNIT |
|------------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.016 | 0.016 | 0.016 | 0.016 | 0.016 | 0.016 | 0.016 | 0.016 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

* $I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | $V_{CCA} = 1.5V$ | | | | | | | |
|-----------|-----------------|--------|------------|------------------|----------|----------|----------|-----------|-----------|-----------|-----------|
| | | | | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 4.2 | 4.2 | 5.2 | 6.3 | 4.2 | 4.2 | 5.2 | 6.3 |
| t_{PHL} | | | | 4.2 | 4.2 | 5.2 | 6.3 | 4.2 | 4.2 | 5.2 | 6.3 |
| t_{PLH} | B | A | MAX | 5.6 | 5.7 | 6 | 6.3 | 5.6 | 5.7 | 6 | 6.3 |
| t_{PHL} | | | | 5.6 | 5.7 | 6 | 6.3 | 5.6 | 5.7 | 6 | 6.3 |
| t_{r2H} | \overline{OE} | A | MAX | 9.4 | 9.4 | 9.5 | 9.6 | 9.4 | 9.4 | 9.5 | 9.6 |
| t_{r2L} | | | | 9.4 | 9.4 | 9.5 | 9.6 | 9.4 | 9.4 | 9.5 | 9.6 |
| t_{r2H} | \overline{OE} | B | MAX | 5.6 | 5.8 | 7.7 | 9.6 | 5.6 | 5.8 | 7.7 | 9.6 |
| t_{r2L} | | | | 5.6 | 5.8 | 7.7 | 9.6 | 5.6 | 5.8 | 7.7 | 9.6 |
| t_{r2H} | \overline{OE} | A | MAX | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 |
| t_{r2L} | | | | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 | 10.2 |
| t_{r2H} | \overline{OE} | B | MAX | 7.6 | 7.4 | 9.1 | 10.3 | 7.6 | 7.4 | 9.1 | 10.3 |
| t_{r2L} | | | | 7.6 | 7.4 | 9.1 | 10.3 | 7.6 | 7.4 | 9.1 | 10.3 |

UNIT: ns

| V _{CCA} = 1.8V | | | | | | | | | | | |
|-------------------------|-------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 3.9 | 3.9 | 4.9 | 6 | 3.9 | 3.9 | 4.9 | 6 |
| t _{PHL} | | | | 3.9 | 3.9 | 4.9 | 6 | 3.9 | 3.9 | 4.9 | 6 |
| t _{PLH} | B | A | MAX | 4.5 | 4.6 | 4.9 | 5.3 | 4.5 | 4.6 | 4.9 | 5.3 |
| t _{PHL} | | | | 4.5 | 4.6 | 4.9 | 5.3 | 4.5 | 4.6 | 4.9 | 5.3 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 7.2 | 7.3 | 7.3 | 7.4 | 7.2 | 7.3 | 7.3 | 7.4 |
| t _{PLZL} | | | | 7.2 | 7.3 | 7.3 | 7.4 | 7.2 | 7.3 | 7.3 | 7.4 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 4.6 | 5.3 | 7.4 | 9.2 | 4.6 | 5.3 | 7.4 | 9.2 |
| t _{PLZL} | | | | 4.6 | 5.3 | 7.4 | 9.2 | 4.6 | 5.3 | 7.4 | 9.2 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 8.7 | 8.7 | 8.7 | 8.6 | 8.7 | 8.7 | 8.7 | 8.6 |
| t _{PLZL} | | | | 8.7 | 8.7 | 8.7 | 8.6 | 8.7 | 8.7 | 8.7 | 8.6 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 6.9 | 6.9 | 8.7 | 9.9 | 6.9 | 6.9 | 8.7 | 9.9 |
| t _{PLZL} | | | | 6.9 | 6.9 | 8.7 | 9.9 | 6.9 | 6.9 | 8.7 | 9.9 |

UNIT : ns

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 3.6 | 3.5 | 4.6 | 5.7 | 3.6 | 3.5 | 4.6 | 5.7 |
| t _{PHL} | | | | 3.6 | 3.5 | 4.6 | 5.7 | 3.6 | 3.5 | 4.6 | 5.7 |
| t _{PLH} | B | A | MAX | 3.3 | 3.4 | 3.9 | 4.2 | 3.3 | 3.4 | 3.9 | 4.2 |
| t _{PHL} | | | | 3.3 | 3.4 | 3.9 | 4.2 | 3.3 | 3.4 | 3.9 | 4.2 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 4.8 | 4.8 | 5.2 | 6.5 | 4.8 | 4.8 | 5.2 | 6.5 |
| t _{PLZL} | | | | 4.8 | 4.8 | 5.2 | 6.5 | 4.8 | 4.8 | 5.2 | 6.5 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 4 | 4.8 | 7 | 8.8 | 4 | 4.8 | 7 | 8.8 |
| t _{PLZL} | | | | 4 | 4.8 | 7 | 8.8 | 4 | 4.8 | 7 | 8.8 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 6.6 | 6.2 | 8.4 | 8.4 | 6.6 | 6.2 | 8.4 | 8.4 |
| t _{PLZL} | | | | 6.6 | 6.2 | 8.4 | 8.4 | 6.6 | 6.2 | 8.4 | 8.4 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 5.2 | 6.2 | 8.2 | 9.4 | 5.2 | 6.2 | 8.2 | 9.4 |
| t _{PLZL} | | | | 5.2 | 6.2 | 8.2 | 9.4 | 5.2 | 6.2 | 8.2 | 8.8 |

UNIT : ns

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.9 | 3.3 | 4.5 | 5.6 | 2.9 | 3.3 | 4.5 | 5.6 |
| t _{PHL} | | | | 2.9 | 3.3 | 4.5 | 5.6 | 2.9 | 3.3 | 4.5 | 5.6 |
| t _{PLH} | B | A | MAX | 2.8 | 3 | 3.4 | 4.2 | 2.8 | 3 | 3.4 | 4.2 |
| t _{PHL} | | | | 2.8 | 3 | 3.4 | 4.2 | 2.8 | 3 | 3.4 | 4.2 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 3.8 | 3.8 | 5.2 | 8.7 | 3.8 | 3.8 | 5.2 | 8.7 |
| t _{PLZL} | | | | 3.8 | 3.8 | 5.2 | 8.7 | 3.8 | 3.8 | 5.2 | 8.7 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 3.8 | 4.7 | 6.8 | 8.7 | 3.8 | 4.7 | 6.8 | 8.7 |
| t _{PLZL} | | | | 3.8 | 4.7 | 6.8 | 8.7 | 3.8 | 4.7 | 6.8 | 8.7 |
| t _{PLZH} | 0 \bar{E} | A | MAX | 6.6 | 5.6 | 8.3 | 9.3 | 6.6 | 5.6 | 8.3 | 9.3 |
| t _{PLZL} | | | | 6.6 | 5.6 | 8.3 | 9.3 | 6.6 | 5.6 | 8.3 | 9.3 |
| t _{PLZH} | 0 \bar{E} | B | MAX | 6.2 | 6.4 | 8.1 | 9.3 | 6.2 | 6.4 | 8.1 | 9.3 |
| t _{PLZL} | | | | 6.2 | 6.4 | 8.1 | 9.3 | 6.2 | 6.4 | 8.1 | 9.3 |

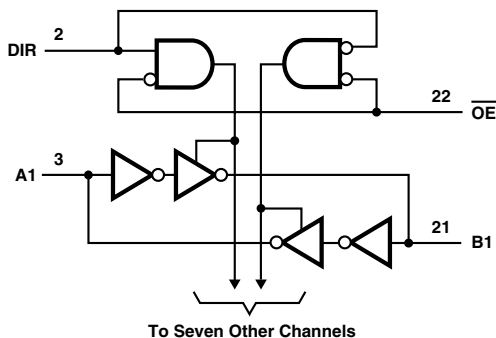
UNIT : ns

8T245

8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State
- This 8-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE⁽¹⁾
(each 8-bit section)

| CONTROL INPUTS | | OUTPUTS CIRCUITS | | OPERATION |
|-----------------|-----|------------------|---------|-----------------|
| \overline{OE} | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

(1) Input circuits of the data I/Os are always active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V | UNIT |
|------------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.025 | 0.025 | 0.025 | 0.025 | 0.03 | 0.03 | 0.03 | 0.03 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 32 | 24 | 8 | 4 | mA |

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | UNIT |
|------------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.025 | 0.025 | 0.025 | 0.025 | 0.025 | 0.025 | 0.025 | 0.025 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

 $*I_{CCDA} + I_{CCB}$
SWITCHING CHARACTERISTICS

| $V_{CCA} = 1.5V$ | | | | | | | | | | | | |
|------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | |
| t_{PLH} | A | B | MAX | 6.8 | 4.9 | 4.6 | 5.4 | 6.8 | 4.9 | 4.6 | 5.4 | |
| t_{PHL} | | | | 6.8 | 4.9 | 4.6 | 5.4 | 6.8 | 4.9 | 4.6 | 5.4 | |
| t_{PLH} | B | A | MAX | 4.5 | 4.7 | 5.1 | 5.4 | 4.5 | 4.7 | 5.1 | 5.4 | |
| t_{PHL} | | | | 4.5 | 4.7 | 5.1 | 5.4 | 4.5 | 4.7 | 5.1 | 5.4 | |
| t_{PZH} | \overline{OE} | A | MAX | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | |
| t_{PZL} | | | | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | |
| t_{PZH} | \overline{OE} | B | MAX | 5.2 | 5.6 | 7.1 | 7.6 | 5.2 | 5.6 | 7.1 | 7.6 | |
| t_{PZL} | | | | 5.2 | 5.6 | 7.1 | 7.6 | 5.2 | 5.6 | 7.1 | 7.6 | |
| t_{PHZ} | \overline{OE} | A | MAX | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | |
| t_{PLZ} | | | | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | |
| t_{PHZ} | \overline{OE} | B | MAX | 7.8 | 7.2 | 7.6 | 8.4 | 7.8 | 7.2 | 7.6 | 8.4 | |
| t_{PLZ} | | | | 7.8 | 7.2 | 7.6 | 8.4 | 7.8 | 7.2 | 7.6 | 8.4 | |

UNIT : ns

| $V_{CCA} = 1.8V$ | | | | | | | | | | | | |
|------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V | |
| t_{PLH} | A | B | MAX | 7.1 | 7.4 | 9.2 | 21.9 | 7.1 | 7.4 | 9.2 | 21.9 | |
| t_{PHL} | | | | 7.1 | 7.4 | 9.2 | 21.9 | 7.1 | 7.4 | 9.2 | 21.9 | |
| t_{PLH} | B | A | MAX | 23.4 | 23.4 | 23.6 | 23.8 | 23.4 | 23.4 | 23.6 | 23.8 | |
| t_{PHL} | | | | 23.4 | 23.4 | 23.6 | 23.8 | 23.4 | 23.4 | 23.6 | 23.8 | |
| t_{PZH} | \overline{OE} | A | MAX | 23.7 | 23.7 | 23.8 | 24 | 23.7 | 23.7 | 23.8 | 24 | |
| t_{PZL} | | | | 23.7 | 23.7 | 23.8 | 24 | 23.7 | 23.7 | 23.8 | 24 | |
| t_{PZH} | \overline{OE} | B | MAX | 10.8 | 12.6 | 16 | 32 | 10.8 | 12.6 | 16 | 32 | |
| t_{PZL} | | | | 10.8 | 12.6 | 16 | 32 | 10.8 | 12.6 | 16 | 32 | |
| t_{PHZ} | \overline{OE} | A | MAX | 29.2 | 29.3 | 29.4 | 29.6 | 29.2 | 29.3 | 29.4 | 29.6 | |
| t_{PLZ} | | | | 29.2 | 29.3 | 29.4 | 29.6 | 29.2 | 29.3 | 29.4 | 29.6 | |
| t_{PHZ} | \overline{OE} | B | MAX | 10.3 | 12 | 13.1 | 32.2 | 10.3 | 12 | 13.1 | 32.2 | |
| t_{PLZ} | | | | 10.3 | 12 | 13.1 | 32.2 | 10.3 | 12 | 13.1 | 32.2 | |

| $V_{CCA} = 1.8V$ | | | | | | | | | | | | |
|------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | |
| t_{PLH} | A | B | MAX | 3.9 | 4 | 4.4 | 5.1 | 3.9 | 4 | 4.4 | 5.1 | |
| t_{PHL} | | | | 3.9 | 4 | 4.4 | 5.1 | 3.9 | 4 | 4.4 | 5.1 | |
| t_{PLH} | B | A | MAX | 3.7 | 3.9 | 4.4 | 4.6 | 3.7 | 3.9 | 4.4 | 4.6 | |
| t_{PHL} | | | | 3.7 | 3.9 | 4.4 | 4.6 | 3.7 | 3.9 | 4.4 | 4.6 | |
| t_{PZH} | \overline{OE} | A | MAX | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | |
| t_{PZL} | | | | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | |
| t_{PZH} | \overline{OE} | B | MAX | 4.5 | 5.1 | 6.7 | 8.2 | 4.5 | 5.1 | 6.7 | 8.2 | |
| t_{PZL} | | | | 4.5 | 5.1 | 6.7 | 8.2 | 4.5 | 5.1 | 6.7 | 8.2 | |
| t_{PHZ} | \overline{OE} | A | MAX | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | |
| t_{PLZ} | | | | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | |
| t_{PHZ} | \overline{OE} | B | MAX | 5.8 | 6 | 6.9 | 7.8 | 5.8 | 6 | 6.9 | 7.8 | |
| t_{PLZ} | | | | 5.8 | 6 | 6.9 | 7.8 | 5.8 | 6 | 6.9 | 7.8 | |

UNIT : ns

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PLH} | A | B | MAX | 4.8 | 6.2 | 9 | 21.4 | 4.8 | 6.2 | 9 | 21.4 |
| t _{PHL} | | | | 4.8 | 6.2 | 9 | 21.4 | 4.8 | 6.2 | 9 | 21.4 |
| t _{PLH} | B | A | MAX | 8.8 | 8.9 | 9.1 | 9.3 | 8.8 | 8.9 | 9.1 | 9.3 |
| t _{PHL} | | | | 8.8 | 8.9 | 9.1 | 9.3 | 8.8 | 8.9 | 9.1 | 9.3 |
| t _{20H} | \overline{OE} | A | MAX | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 |
| t _{21L} | | | | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 |
| t _{20H} | \overline{OE} | B | MAX | 6.9 | 9.4 | 12.9 | 28.2 | 6.9 | 9.4 | 12.9 | 28.2 |
| t _{21L} | | | | 6.9 | 9.4 | 12.9 | 28.2 | 6.9 | 9.4 | 12.9 | 28.2 |
| t _{PHZ} | \overline{OE} | A | MAX | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| t _{PLZ} | | | | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| t _{PHZ} | \overline{OE} | B | MAX | 6.9 | 9.3 | 11 | 29.6 | 6.9 | 9.3 | 11 | 29.6 |
| t _{PLZ} | | | | 6.9 | 9.3 | 11 | 29.6 | 6.9 | 9.3 | 11 | 29.6 |

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.8 | 3.1 | 3.9 | 4.7 | 2.8 | 3.1 | 3.9 | 4.7 |
| t _{PHL} | | | | 2.8 | 3.1 | 3.9 | 4.7 | 2.8 | 3.1 | 3.9 | 4.7 |
| t _{PLH} | B | A | MAX | 2.9 | 3.1 | 4 | 4.9 | 2.9 | 3.1 | 4 | 4.9 |
| t _{PHL} | | | | 2.9 | 3.1 | 4 | 4.9 | 2.9 | 3.1 | 4 | 4.9 |
| t _{20H} | \overline{OE} | A | MAX | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 |
| t _{21L} | | | | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 |
| t _{20H} | \overline{OE} | B | MAX | 4 | 4.6 | 6.4 | 7.9 | 4 | 4.6 | 6.4 | 7.9 |
| t _{21L} | | | | 4 | 4.6 | 6.4 | 7.9 | 4 | 4.6 | 6.4 | 7.9 |
| t _{PHZ} | \overline{OE} | A | MAX | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 |
| t _{PLZ} | | | | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 | 5.1 |
| t _{PHZ} | \overline{OE} | B | MAX | 3.9 | 5.1 | 6.3 | 7.1 | 3.9 | 5.1 | 6.3 | 7.1 |
| t _{PLZ} | | | | 3.9 | 5.1 | 6.3 | 7.1 | 3.9 | 5.1 | 6.3 | 7.1 |

UNIT : ns

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PLH} | A | B | MAX | 4.4 | 6.3 | 8.8 | 21.2 | 4.4 | 6.2 | 8.8 | 21.2 |
| t _{PHL} | | | | 4.4 | 6.3 | 8.8 | 21.2 | 4.4 | 6.2 | 8.8 | 21.2 |
| t _{PLH} | B | A | MAX | 6 | 6.1 | 6.2 | 7.2 | 6 | 6.1 | 6.2 | 7.2 |
| t _{PHL} | | | | 6 | 6.1 | 6.2 | 7.2 | 6 | 6.1 | 6.2 | 7.2 |
| t _{20H} | \overline{OE} | A | MAX | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 |
| t _{21L} | | | | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 |
| t _{20H} | \overline{OE} | B | MAX | 6.4 | 8.5 | 12.4 | 27.7 | 6.4 | 8.5 | 12.4 | 27.7 |
| t _{21L} | | | | 6.4 | 8.5 | 12.4 | 27.7 | 6.4 | 8.5 | 12.4 | 27.7 |
| t _{PHZ} | \overline{OE} | A | MAX | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| t _{PLZ} | | | | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| t _{PHZ} | \overline{OE} | B | MAX | 6.3 | 8.6 | 10.3 | 29 | 6.3 | 8.6 | 10.3 | 29 |
| t _{PLZ} | | | | 6.3 | 8.6 | 10.3 | 29 | 6.3 | 8.6 | 10.3 | 29 |

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.5 | 2.9 | 3.7 | 4.5 | 2.5 | 2.9 | 3.7 | 4.5 |
| t _{PHL} | | | | 2.5 | 2.9 | 3.7 | 4.5 | 2.5 | 2.9 | 3.7 | 4.5 |
| t _{PLH} | B | A | MAX | 2.5 | 2.8 | 3.9 | 6.8 | 2.5 | 2.8 | 3.9 | 6.8 |
| t _{PHL} | | | | 2.5 | 2.8 | 3.9 | 6.8 | 2.5 | 2.8 | 3.9 | 6.8 |
| t _{20H} | \overline{OE} | A | MAX | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| t _{21L} | | | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| t _{20H} | \overline{OE} | B | MAX | 3.9 | 4.5 | 6.2 | 7.8 | 3.9 | 4.5 | 6.2 | 7.8 |
| t _{21L} | | | | 3.9 | 4.5 | 6.2 | 7.8 | 3.9 | 4.5 | 6.2 | 7.8 |
| t _{PHZ} | \overline{OE} | A | MAX | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| t _{PLZ} | | | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| t _{PHZ} | \overline{OE} | B | MAX | 4.2 | 4.8 | 6 | 6.9 | 4.2 | 4.8 | 6 | 6.9 |
| t _{PLZ} | | | | 4.2 | 4.8 | 6 | 6.9 | 4.2 | 4.8 | 6 | 6.9 |

UNIT : ns

| V _{CCA} = 5.0V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PHL} | A | B | MAX | 4.2 | 6 | 8.8 | 21.4 | 4.2 | 6 | 8.8 | 21.4 |
| t _{PHL} | | | | 4.2 | 6 | 8.8 | 21.4 | 4.2 | 6 | 8.8 | 21.4 |
| t _{PLH} | B | A | MAX | 4.3 | 4.5 | 4.8 | 7 | 4.3 | 4.5 | 4.8 | 7 |
| t _{PLH} | | | | 4.3 | 4.5 | 4.8 | 7 | 4.3 | 4.5 | 4.8 | 7 |
| t _{PHL} | \overline{OE} | A | MAX | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 |
| t _{PHL} | | | | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 | 6.4 |
| t _{PHL} | \overline{OE} | B | MAX | 6 | 8.1 | 11.4 | 27.6 | 6 | 8.1 | 11.4 | 27.6 |
| t _{PHL} | | | | 6 | 8.1 | 11.4 | 27.6 | 6 | 8.1 | 11.4 | 27.6 |
| t _{PLH} | \overline{OE} | A | MAX | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PLH} | | | | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PLH} | \overline{OE} | B | MAX | 5.7 | 8 | 9.7 | 28.7 | 5.7 | 8 | 9.7 | 28.7 |
| t _{PLH} | | | | 5.7 | 8 | 9.7 | 28.7 | 5.7 | 8 | 9.7 | 28.7 |

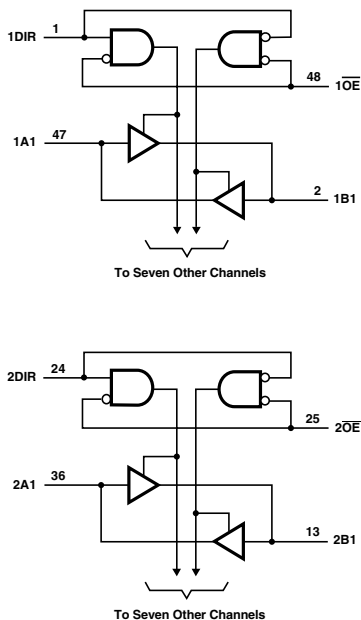
UNIT : ns

16T245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 16-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V | UNIT |
|------------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 32 | 24 | 8 | 4 | mA |

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.8V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.8V | UNIT |
|------------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.045 | 0.045 | 0.045 | 0.045 | 0.045 | 0.045 | 0.045 | 0.045 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

 $*I_{CCA} + I_{CCB}$
SWITCHING CHARACTERISTICS

| V _{CCA} = 1.5V | | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | |
| t_{PLH} | A | B | MAX | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 | |
| t_{PHL} | | | | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 | |
| t_{PLH} | B | A | MAX | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 | |
| t_{PHL} | | | | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 | |
| t_{PZH} | \overline{OE} | A | MAX | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | |
| t_{PZL} | | | | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | | |
| t_{PZH} | \overline{OE} | B | MAX | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 | |
| t_{PZL} | | | | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 | |
| t_{PHZ} | \overline{OE} | A | MAX | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | |
| t_{PLZ} | | | | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | | |
| t_{PHZ} | \overline{OE} | B | MAX | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 | |
| t_{PLZ} | | | | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 | |

UNIT : ns

| V _{CCA} = 1.8V | | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V | |
| t_{PLH} | A | B | MAX | 7.1 | 7.4 | 9.2 | 21.9 | 7.1 | 7.4 | 9.2 | 21.9 | |
| t_{PHL} | | | | 7.1 | 7.4 | 9.2 | 21.9 | 7.1 | 7.4 | 9.2 | 21.9 | |
| t_{PLH} | B | A | MAX | 23.4 | 23.4 | 23.6 | 23.8 | 23.4 | 23.4 | 23.8 | 23.8 | |
| t_{PHL} | | | | 23.4 | 23.4 | 23.6 | 23.8 | 23.4 | 23.4 | 23.8 | 23.8 | |
| t_{PZH} | \overline{OE} | A | MAX | 23.7 | 23.7 | 23.8 | 24 | 23.7 | 23.7 | 23.8 | 24 | |
| t_{PZL} | | | | 23.7 | 23.7 | 23.8 | 24 | 23.7 | 23.7 | 23.8 | 24 | |
| t_{PZH} | \overline{OE} | B | MAX | 10.8 | 12.6 | 16 | 32 | 10.8 | 12.6 | 18 | 32 | |
| t_{PZL} | | | | 10.8 | 12.6 | 16 | 32 | 10.8 | 12.6 | 18 | 32 | |
| t_{PHZ} | \overline{OE} | A | MAX | 29.2 | 29.3 | 29.4 | 29.6 | 29.2 | 29.3 | 29.4 | 29.6 | |
| t_{PLZ} | | | | 29.2 | 29.3 | 29.4 | 29.6 | 29.2 | 29.3 | 29.4 | 29.6 | |
| t_{PHZ} | \overline{OE} | B | MAX | 10.3 | 12 | 13.1 | 32.2 | 10.3 | 12 | 13.1 | 32.2 | |
| t_{PLZ} | | | | 10.3 | 12 | 13.1 | 32.2 | 10.3 | 12 | 13.1 | 32.2 | |

| V _{CCA} = 1.8V | | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V | |
| t_{PLH} | A | B | MAX | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 | |
| t_{PHL} | | | | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 | |
| t_{PLH} | B | A | MAX | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 | |
| t_{PHL} | | | | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 | |
| t_{PZH} | \overline{OE} | A | MAX | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | |
| t_{PZL} | | | | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | | |
| t_{PZH} | \overline{OE} | B | MAX | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 | |
| t_{PZL} | | | | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 | |
| t_{PHZ} | \overline{OE} | A | MAX | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | |
| t_{PLZ} | | | | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | | |
| t_{PHZ} | \overline{OE} | B | MAX | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 | |
| t_{PLZ} | | | | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 | |

UNIT : ns

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PLH} | A | B | MAX | 4.8 | 6.2 | 9 | 21.4 | 4.8 | 6.2 | 9 | 21.4 |
| t _{PHL} | | | | 4.8 | 6.2 | 9 | 21.4 | 4.8 | 6.2 | 9 | 21.4 |
| t _{PLH} | B | A | MAX | 8.8 | 8.9 | 9.1 | 9.3 | 8.8 | 8.9 | 9.1 | 9.3 |
| t _{PHL} | | | | 8.8 | 8.9 | 9.1 | 9.3 | 8.8 | 8.9 | 9.1 | 9.3 |
| t _{PLH} | \overline{OE} | A | MAX | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 |
| t _{PHL} | | | | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 | 10.9 |
| t _{PLH} | \overline{OE} | B | MAX | 6.9 | 9.4 | 12.9 | 28.2 | 6.9 | 9.4 | 12.9 | 28.2 |
| t _{PHL} | | | | 6.9 | 9.4 | 12.9 | 28.2 | 6.9 | 9.4 | 12.9 | 28.2 |
| t _{PLH} | \overline{OE} | A | MAX | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| t _{PHL} | | | | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| t _{PLH} | \overline{OE} | B | MAX | 6.9 | 9.3 | 11 | 29.6 | 6.9 | 9.3 | 11 | 29.6 |
| t _{PHL} | | | | 6.9 | 9.3 | 11 | 29.6 | 6.9 | 9.3 | 11 | 29.6 |

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t _{PHL} | | | | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t _{PLH} | B | A | MAX | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t _{PHL} | | | | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t _{PLH} | \overline{OE} | A | MAX | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t _{PHL} | | | | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t _{PLH} | \overline{OE} | B | MAX | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t _{PHL} | | | | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t _{PLH} | \overline{OE} | A | MAX | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t _{PHL} | | | | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t _{PLH} | \overline{OE} | B | MAX | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |
| t _{PHL} | | | | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |

UNIT : ns

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|--------|----------|----------|----------|---------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PLH} | A | B | MAX | 4.4 | 6.1 | 8.8 | 21.2 | 4.4 | 6.2 | 8.8 | 21.2 |
| t _{PHL} | | | | 4.4 | 6.1 | 8.8 | 21.2 | 4.4 | 6.2 | 8.8 | 21.2 |
| t _{PLH} | B | A | MAX | 6 | 6.1 | 6.2 | 7.2 | 6 | 6.1 | 6.2 | 7.2 |
| t _{PHL} | | | | 6 | 6.1 | 6.2 | 7.2 | 6 | 6.1 | 6.2 | 7.2 |
| t _{PLH} | \overline{OE} | A | MAX | 7.8 | 7.8 | 7.8 | 7.8 | 8.1 | 8.1 | 8.1 | 7.8 |
| t _{PHL} | | | | 7.8 | 7.8 | 7.8 | 7.8 | 8.1 | 8.1 | 8.1 | 7.8 |
| t _{PLH} | \overline{OE} | B | MAX | 8.4 | 8.5 | 12.4 | 27.7 | 6.4 | 8.5 | 12.4 | 27.7 |
| t _{PHL} | | | | 8.4 | 8.5 | 12.4 | 27.7 | 6.4 | 8.5 | 12.4 | 27.7 |
| t _{PLH} | \overline{OE} | A | MAX | 8.2 | 6.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| t _{PHL} | | | | 8.2 | 6.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| t _{PLH} | \overline{OE} | B | MAX | 6.3 | 8.6 | 10.3 | 29 | 6.3 | 8.8 | 10.3 | 29 |
| t _{PHL} | | | | 6.3 | 8.6 | 10.3 | 29 | 6.3 | 8.8 | 10.3 | 29 |

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PHL} | | | | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PLH} | B | A | MAX | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PHL} | | | | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PLH} | \overline{OE} | A | MAX | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PHL} | | | | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PLH} | \overline{OE} | B | MAX | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PHL} | | | | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PLH} | \overline{OE} | A | MAX | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PHL} | | | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PLH} | \overline{OE} | B | MAX | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |
| t _{PHL} | | | | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |

UNIT : ns

| V _{CCA} = 5.0V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|-----------|-------------|-------------|-------------|------------|--------------|--------------|--------------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | LVCH 5V | LVCH 3.3V | LVCH 2.5V | LVCH 1.8V |
| t _{PLH} | A | B | MAX | 4.2 | 6 | 8.8 | 21.4 | 4.2 | 6 | 8.8 | 21.4 |
| t _{PHL} | | | | 4.2 | 6 | 8.8 | 21.4 | 4.2 | 6 | 8.8 | 21.4 |
| t _{PLH} | B | A | MAX | 4.3 | 4.5 | 4.8 | 6.8 | 4.3 | 4.5 | 4.8 | 7 |
| t _{PHL} | | | | 4.3 | 4.5 | 4.8 | 6.8 | 4.3 | 4.5 | 4.8 | 7 |
| t _{PLZ} | \overline{OE} | A | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PHZ} | | | | 5.5 | 5.5 | 5.5 | 5.5 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PLZ} | \overline{OE} | B | MAX | 6 | 8.1 | 11.4 | 27.6 | 6 | 8.1 | 11.4 | 27.6 |
| t _{PHZ} | | | | 6 | 8.1 | 11.4 | 27.6 | 6 | 8.1 | 11.4 | 27.6 |
| t _{PLZ} | \overline{OE} | A | MAX | 6.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PHZ} | | | | 6.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 | 5.4 |
| t _{PLZ} | \overline{OE} | B | MAX | 5.7 | 8 | 9.7 | 28.7 | 5.7 | 8 | 9.7 | 28.7 |
| t _{PHZ} | | | | 5.7 | 8 | 9.7 | 28.7 | 5.7 | 8 | 9.7 | 28.7 |

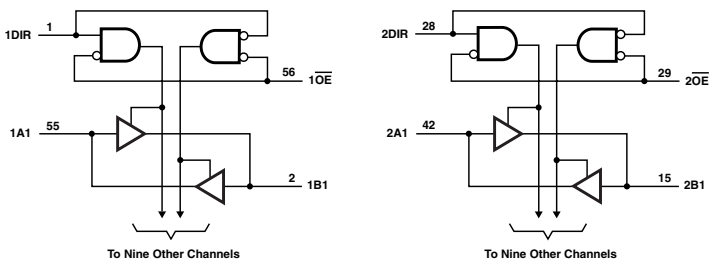
UNIT : ns

20T245

20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 20-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.8V | AVC 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.8V | UNIT |
|------------|------------|----------|----------|----------|----------|----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.065 | 0.065 | 0.065 | 0.065 | 0.065 | 0.065 | 0.065 | 0.065 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

* $I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | $V_{CCA} = 1.5V$ | | | | | | | |
|-----------|-------|--------|------------|------------------|----------|----------|----------|-----------|-----------|-----------|-----------|
| | | | | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 3.9 | 4.3 | 5.4 | 6.4 | 3.9 | 4.3 | 5.4 | 6.4 |
| | | | | 3.9 | 4.3 | 5.4 | 6.4 | 3.9 | 4.3 | 5.4 | 6.4 |
| t_{PHL} | B | A | MAX | 5.7 | 5.8 | 6.1 | 6.4 | 5.7 | 5.8 | 6.1 | 6.4 |
| | | | | 5.7 | 5.8 | 6.1 | 6.4 | 5.7 | 5.8 | 6.1 | 6.4 |
| t_{RZH} | OE | A | MAX | 10.2 | 10.2 | 10.3 | 10.3 | 10.2 | 10.2 | 10.3 | 10.3 |
| | | | | 10.2 | 10.2 | 10.3 | 10.3 | 10.2 | 10.2 | 10.3 | 10.3 |
| t_{RZL} | OE | B | MAX | 5.3 | 6.1 | 8.4 | 10.3 | 5.3 | 6.1 | 8.4 | 10.3 |
| | | | | 5.3 | 6.1 | 8.4 | 10.3 | 5.3 | 6.1 | 8.4 | 10.3 |
| t_{PHZ} | OE | A | MAX | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| | | | | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| t_{PLZ} | OE | B | MAX | 5.9 | 6.4 | 7.8 | 9 | 5.9 | 6.4 | 7.8 | 9 |
| | | | | 5.9 | 6.4 | 7.8 | 9 | 5.9 | 6.4 | 7.8 | 9 |

UNIT : ns

| V _{CCA} = 1.8V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 3.5 | 3.9 | 5 | 6.1 | 3.5 | 3.9 | 5 | 6.1 |
| t _{PHL} | | | | 3.5 | 3.9 | 5 | 6.1 | 3.5 | 3.9 | 5 | 6.1 |
| t _{PLH} | B | A | MAX | 4.6 | 4.7 | 5 | 5.4 | 4.6 | 4.7 | 5 | 5.4 |
| t _{PHL} | | | | 4.6 | 4.7 | 5 | 5.4 | 4.6 | 4.7 | 5 | 5.4 |
| t _{PLZH} | \overline{OE} | A | MAX | 7.9 | 7.9 | 7.9 | 8.1 | 7.9 | 7.9 | 7.9 | 8.1 |
| t _{PLZL} | | | | 7.9 | 7.9 | 7.9 | 8.1 | 7.9 | 7.9 | 7.9 | 8.1 |
| t _{PLZH} | \overline{OE} | B | MAX | 4.8 | 5.7 | 7.9 | 10 | 4.8 | 5.7 | 7.9 | 10 |
| t _{PLZL} | | | | 4.8 | 5.7 | 7.9 | 10 | 4.8 | 5.7 | 7.9 | 10 |
| t _{PLHZ} | \overline{OE} | A | MAX | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 |
| t _{PLZZ} | | | | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 | 7.4 |
| t _{PLHZ} | \overline{OE} | B | MAX | 5.1 | 5.8 | 7.4 | 8.7 | 5.1 | 5.8 | 7.4 | 8.7 |
| t _{PLZZ} | | | | 5.1 | 5.8 | 7.4 | 8.7 | 5.1 | 5.8 | 7.4 | 8.7 |

UNIT : ns

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 3 | 3.5 | 4.7 | 5.8 | 3 | 3.5 | 4.7 | 5.8 |
| t _{PHL} | | | | 3 | 3.5 | 4.7 | 5.8 | 3 | 3.5 | 4.7 | 5.8 |
| t _{PLH} | B | A | MAX | 3.4 | 3.5 | 3.9 | 4.3 | 3.4 | 3.5 | 3.9 | 4.3 |
| t _{PHL} | | | | 3.4 | 3.5 | 3.9 | 4.3 | 3.4 | 3.5 | 3.9 | 4.3 |
| t _{PLZH} | \overline{OE} | A | MAX | 5.2 | 5.2 | 5.3 | 5.4 | 5.2 | 5.2 | 5.3 | 5.4 |
| t _{PLZL} | | | | 5.2 | 5.2 | 5.3 | 5.4 | 5.2 | 5.2 | 5.3 | 5.4 |
| t _{PLZH} | \overline{OE} | B | MAX | 4.3 | 5.3 | 7.6 | 9.6 | 4.3 | 5.3 | 7.6 | 9.6 |
| t _{PLZL} | | | | 4.3 | 5.3 | 7.6 | 9.6 | 4.3 | 5.3 | 7.6 | 9.6 |
| t _{PLHZ} | \overline{OE} | A | MAX | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 |
| t _{PLZZ} | | | | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 |
| t _{PLHZ} | \overline{OE} | B | MAX | 5 | 5.3 | 6.9 | 8.2 | 5 | 5.3 | 6.9 | 8.2 |
| t _{PLZZ} | | | | 5 | 5.3 | 6.9 | 8.2 | 5 | 5.3 | 6.9 | 8.2 |

UNIT : ns

| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.9 | 3.4 | 4.6 | 5.7 | 2.9 | 3.4 | 4.6 | 5.7 |
| t _{PHL} | | | | 2.9 | 3.4 | 4.6 | 5.7 | 2.9 | 3.4 | 4.6 | 5.7 |
| t _{PLH} | B | A | MAX | 2.9 | 3 | 3.5 | 3.9 | 2.9 | 3 | 3.5 | 3.9 |
| t _{PHL} | | | | 2.9 | 3 | 3.5 | 3.9 | 2.9 | 3 | 3.5 | 3.9 |
| t _{PLZH} | \overline{OE} | A | MAX | 4.1 | 4.2 | 4.3 | 4.4 | 4.1 | 4.2 | 4.3 | 4.4 |
| t _{PLZL} | | | | 4.1 | 4.2 | 4.3 | 4.4 | 4.1 | 4.2 | 4.3 | 4.4 |
| t _{PLZH} | \overline{OE} | B | MAX | 4.1 | 5.1 | 7.5 | 9.6 | 4.1 | 5.1 | 7.5 | 9.6 |
| t _{PLZL} | | | | 4.1 | 5.1 | 7.5 | 9.6 | 4.1 | 5.1 | 7.5 | 9.6 |
| t _{PLHZ} | \overline{OE} | A | MAX | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PLZZ} | | | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PLHZ} | \overline{OE} | B | MAX | 5 | 5.1 | 6.7 | 8.1 | 5 | 5.1 | 6.7 | 8.1 |
| t _{PLZZ} | | | | 5 | 5.1 | 6.7 | 8.1 | 5 | 5.1 | 6.7 | 8.1 |

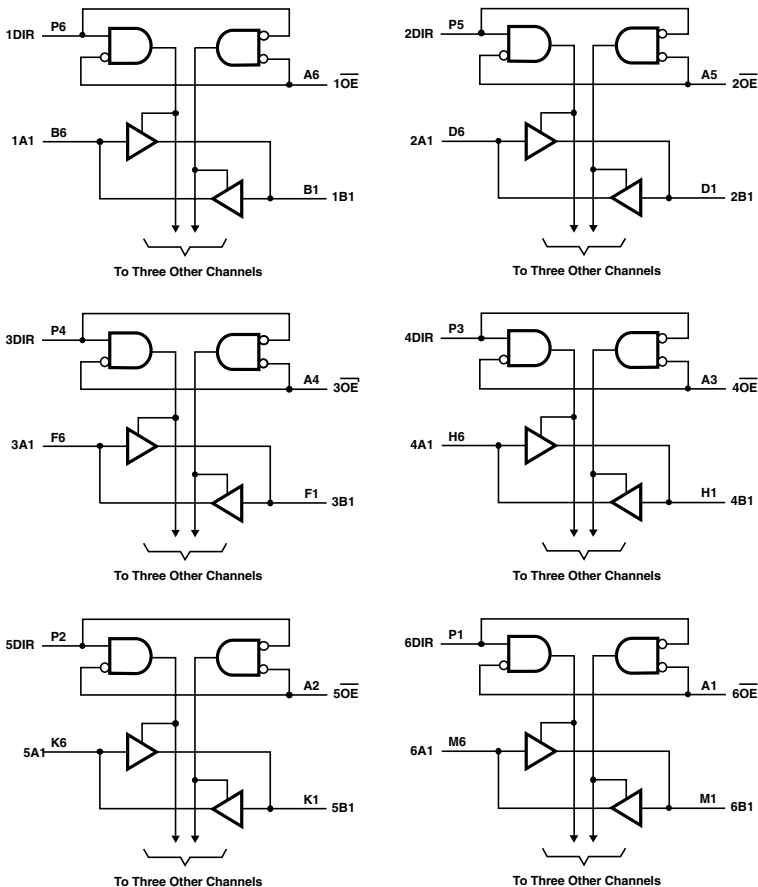
UNIT : ns

24T245

24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 4-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.8V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.8V | UNIT |
|-------------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC2}^* | MAX | 0.075 | 0.075 | 0.075 | 0.075 | 0.075 | 0.075 | 0.075 | 0.075 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

* $I_{CCA} + I_{CC2}$

SWITCHING CHARACTERISTICS

| $V_{CCA} = 1.5V$ | | | | | | | | | | | |
|------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{F1H} | A | B | MAX | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 |
| t_{F1L} | | | | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 |
| t_{F2H} | B | A | MAX | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 |
| t_{F2L} | | | | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 |
| t_{F2H} | \overline{OE} | A | MAX | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 |
| t_{F2L} | | | | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 |
| t_{F2H} | \overline{OE} | B | MAX | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 |
| t_{F2L} | | | | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 |
| t_{F1Z} | \overline{OE} | A | MAX | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 |
| t_{F1Z} | | | | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 |
| t_{F1Z} | \overline{OE} | B | MAX | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 |
| t_{F1Z} | | | | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 |

UNIT : ns

| $V_{CCA} = 1.8V$ | | | | | | | | | | | |
|------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{F1H} | A | B | MAX | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 |
| t_{F1L} | | | | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 |
| t_{F2H} | B | A | MAX | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 |
| t_{F2L} | | | | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 |
| t_{F2H} | \overline{OE} | A | MAX | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 |
| t_{F2L} | | | | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | |
| t_{F2H} | \overline{OE} | B | MAX | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 |
| t_{F2L} | | | | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 |
| t_{F1Z} | \overline{OE} | A | MAX | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 |
| t_{F1Z} | | | | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | |
| t_{F1Z} | \overline{OE} | B | MAX | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 |
| t_{F1Z} | | | | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 |

UNIT : ns

| V _{CCA} = 2.5V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t _{PHL} | | | | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t _{PLH} | B | A | MAX | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t _{PHL} | | | | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t _{PLH} | \overline{OE} | A | MAX | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t _{PHL} | | | | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t _{PLH} | \overline{OE} | B | MAX | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t _{PHL} | | | | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t _{PLH} | \overline{OE} | A | MAX | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t _{PHL} | | | | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t _{PLH} | \overline{OE} | B | MAX | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |
| t _{PHL} | | | | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |

UNIT : ns

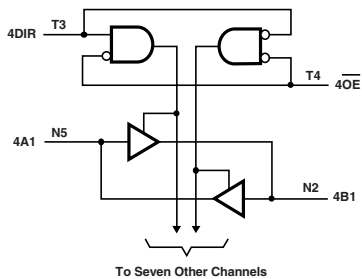
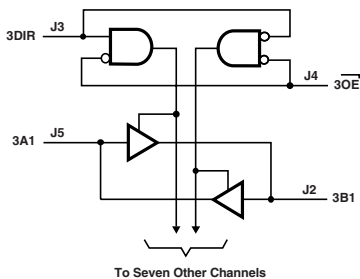
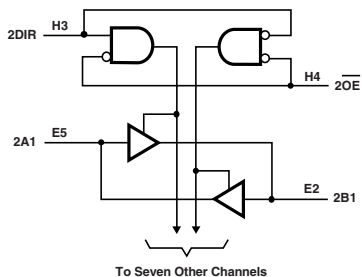
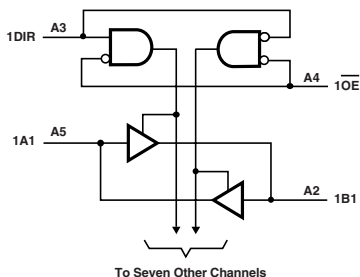
| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PHL} | | | | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PLH} | B | A | MAX | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PHL} | | | | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PLH} | \overline{OE} | A | MAX | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PHL} | | | | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PLH} | \overline{OE} | B | MAX | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PHL} | | | | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PLH} | \overline{OE} | A | MAX | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PHL} | | | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PLH} | \overline{OE} | B | MAX | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |
| t _{PHL} | | | | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |

UNIT : ns

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.8V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.8V | UNIT |
|------------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|------|
| I_{CC}^* | MAX | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 | mA |
| I_{OH} | MAX | -12 | -9 | -8 | -6 | -12 | -9 | -8 | -6 | mA |
| I_{OL} | MAX | 12 | 9 | 8 | 6 | 12 | 9 | 8 | 6 | mA |

 $*I_{CC} + I_{CCA}$
SWITCHING CHARACTERISTICS

| V _{CC} = 1.5V | | | | | | | | | | | |
|------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 |
| t_{PHL} | | | | 3.7 | 4.1 | 5.2 | 6.2 | 3.7 | 4.1 | 5.2 | 6.2 |
| t_{PLH} | B | A | MAX | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 |
| t_{PHL} | | | | 5.5 | 5.6 | 5.9 | 6.2 | 5.5 | 5.6 | 5.9 | 6.2 |
| t_{r2H} | \overline{OE} | A | MAX | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 |
| t_{r2L} | | | | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 | 10.1 |
| t_{r2H} | \overline{OE} | B | MAX | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 |
| t_{r2L} | | | | 5.2 | 5.9 | 8.1 | 10.1 | 5.2 | 5.9 | 8.1 | 10.1 |
| t_{f2H} | \overline{OE} | A | MAX | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 |
| t_{f2L} | | | | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 |
| t_{f2H} | \overline{OE} | B | MAX | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 |
| t_{f2L} | | | | 6.3 | 6.5 | 7.5 | 8.7 | 6.3 | 6.5 | 7.5 | 8.7 |

UNIT : ns

| V _{CC} = 1.8V | | | | | | | | | | | |
|------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 |
| t_{PHL} | | | | 3.3 | 3.7 | 4.8 | 5.9 | 3.3 | 3.7 | 4.8 | 5.9 |
| t_{PLH} | B | A | MAX | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 |
| t_{PHL} | | | | 4.4 | 4.5 | 4.8 | 5.2 | 4.4 | 4.5 | 4.8 | 5.2 |
| t_{r2H} | \overline{OE} | A | MAX | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 |
| t_{r2L} | | | | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 |
| t_{r2H} | \overline{OE} | B | MAX | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 |
| t_{r2L} | | | | 4.5 | 5.3 | 7.4 | 9.2 | 4.5 | 5.3 | 7.4 | 9.2 |
| t_{f2H} | \overline{OE} | A | MAX | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 |
| t_{f2L} | | | | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 | 7.7 |
| t_{f2H} | \overline{OE} | B | MAX | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 |
| t_{f2L} | | | | 5.7 | 5.9 | 7.1 | 8.4 | 5.7 | 5.9 | 7.1 | 8.4 |

UNIT : ns

| V _{CC} = 2.5V | | | | | | | | | | | |
|------------------------|-----------------|--------|------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t_{PLH} | A | B | MAX | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t_{PHL} | | | | 2.8 | 3.3 | 4.5 | 5.6 | 2.8 | 3.3 | 4.5 | 5.6 |
| t_{PLH} | B | A | MAX | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t_{PHL} | | | | 3.2 | 3.3 | 3.7 | 4.1 | 3.2 | 3.3 | 3.7 | 4.1 |
| t_{r2H} | \overline{OE} | A | MAX | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t_{r2L} | | | | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 | 5.3 |
| t_{r2H} | \overline{OE} | B | MAX | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t_{r2L} | | | | 4.5 | 5.1 | 7.3 | 9.4 | 4.5 | 5.1 | 7.3 | 9.4 |
| t_{f2H} | \overline{OE} | A | MAX | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t_{f2L} | | | | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 |
| t_{f2H} | \overline{OE} | B | MAX | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |
| t_{f2L} | | | | 5.2 | 6.1 | 6.6 | 7.9 | 5.2 | 6.1 | 6.6 | 7.9 |

UNIT : ns

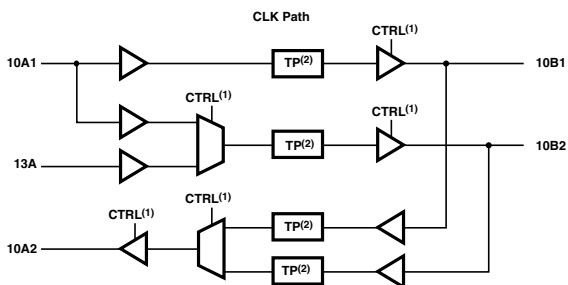
| V _{CCA} = 3.3V | | | | | | | | | | | |
|-------------------------|-----------------|--------|------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3.3V | AVC 2.5V | AVC 1.8V | AVC 1.5V | AVCH 3.3V | AVCH 2.5V | AVCH 1.8V | AVCH 1.5V |
| t _{PLH} | A | B | MAX | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PHL} | | | | 2.7 | 3.2 | 4.4 | 5.5 | 2.7 | 3.2 | 4.4 | 5.5 |
| t _{PLH} | B | A | MAX | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PHL} | | | | 2.7 | 2.8 | 3.3 | 3.7 | 2.7 | 2.8 | 3.3 | 3.7 |
| t _{PLZ} | \overline{OE} | A | MAX | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PHZ} | | | | 4 | 4.1 | 4.2 | 4.3 | 4 | 4.1 | 4.2 | 4.3 |
| t _{PLZ} | \overline{OE} | B | MAX | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PHZ} | | | | 4 | 4.9 | 7.2 | 9.3 | 4 | 4.9 | 7.2 | 9.3 |
| t _{PLZ} | \overline{OE} | A | MAX | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PHZ} | | | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t _{PLZ} | \overline{OE} | B | MAX | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |
| t _{PHZ} | | | | 5 | 5.2 | 6.5 | 7.7 | 5 | 5.2 | 6.5 | 7.7 |

UNIT : ns

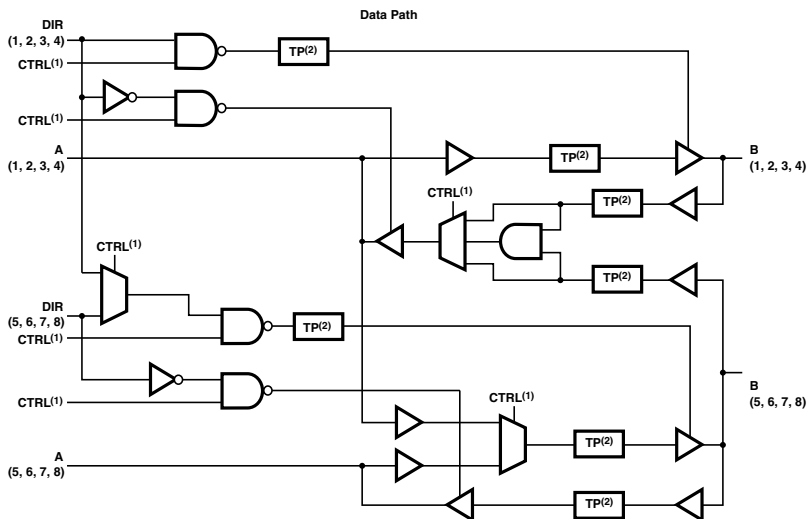
MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ± 15 -kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

- Transceiver for Memory Card Interface
[MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Compliant Products, SmartMedia Card, and xD-Picture Card™]
- For Low-Power Operation, A ports Are Placed in High-Impedance State When Card-Side Supply Voltage Is Switched Off

Logic Diagram



- (1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point



- (1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point

ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 0V$ | AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 3.3V$ | AVCA $V_{CCA} = 2.5V$ $V_{CCB} = 2.5V$ | AVCA $V_{CCA} = 1.8V$ $V_{CCB} = 0V$ | AVCA $V_{CCA} = 1.8V$ $V_{CCB} = 1.8V$ | AVCA $V_{CCA} = 1.5V$ $V_{CCB} = 1.5V$ | UNIT |
|-----------|------------|--|--|--|--|--|--|------|
| I_{CCA} | MAX | 0.01 | 0.01 | 0.0055 | 0.005 | 0.005 | 0.0045 | mA |
| I_{CCB} | MAX | 0.01 | 0.001 | 0.0075 | 0.0005 | 0.007 | 0.0065 | mA |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AVCA 3.3V | AVCA 2.5V | AVCA 1.8V | AVCA 1.5V | UNIT |
|-----------|---------------|--------------|--------------|--------------|--------------|------|
| I_{OH} | A port MAX | -8 | -4 | -2 | -1 | mA |
| I_{OL} | | 8 | 4 | 2 | 1 | mA |
| I_{OH} | B port MAX | -16 | -8 | -4 | -2 | mA |
| I_{OL} | | 16 | 8 | 4 | 2 | mA |

* $I_{B_SD} = 0$

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | $V_{CCA} = 1.5V$ | | |
|-----------|----------------------|---------------------|------------------|---------------------------|---------------------------|---------------------------|
| | | | | AVCA V_{CCA} 3.3V | AVCA V_{CCA} 2.5V | AVCA V_{CCA} 1.8V |
| t_{pd} | A | B | MAX | 4.4 | 4.9 | 7.7 |
| t_{pd} | B | A | MAX | 5 | 5 | 6.3 |
| t_{pd} | CLK, or SCLK.h | CLK, or SCLK.0 | MAX | 4.9 | 5 | 7.7 |
| t_{pd} | CLK, or SCLK.h | CLK, or SCLK-f.h | MAX | 9.7 | 12 | 19 |
| t_{pd} | CMD.h | CMD.0 | MAX | 3.6 | 4.1 | 7.1 |
| t_{pd} | CMD.h | CMD.1 | MAX | 4.2 | 4.6 | 7 |
| t_{pd} | CMD.0 | CMD.h | MAX | 4.7 | 4.9 | 6.2 |
| t_{pd} | CS0 | B | MAX | 3.9 | 4.2 | 6 |
| t_{pd} | R/B | R/B.h | MAX | 4.8 | 4.8 | 5.7 |
| t_{pd} | WE | WE.h | MAX | 4.2 | 4.3 | 7.4 |
| t_{pd} | WP | WP.h | MAX | 4.3 | 4.5 | 6.6 |
| t_{cs} | DAT1.0 or DATA1.0 | IRQ | MAX | 3.3 | 3.3 | 4.8 |
| t_{cs} | DAT1.0 or DATA1.1 | IRQ | MAX | 3.3 | 3.4 | 4.9 |
| t_{cs} | DIR | B | MAX | 4.6 | 4.5 | 6.7 |
| t_{cs} | DIR | A | MAX | 9.5 | 9.6 | 10.3 |
| t_{cs} | R/B | R/B.h open drain | MAX | 5.4 | 5.4 | 5.9 |
| t_{cs} | DAT1.0 or DATA1.0 | IRQ | MAX | 5.5 | 4.9 | 6.7 |
| t_{cs} | DAT1.0 or DATA1.1 | IRQ | MAX | 5.4 | 4.7 | 6.5 |
| t_{cs} | DIR | B | MAX | 6.3 | 6.4 | 6.9 |
| t_{cs} | DIR | A | MAX | 5.2 | 5.3 | 5.3 |
| t_{cs} | R/B | R/B.h open drain | MAX | 4.1 | 17.4 | 16.9 |

UNIT : ns

| V _{CCA} = 1.8V | | | | | | |
|-------------------------|-------------------|-------------------|------------|----------------------------|----------------------------|----------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V | AVCA V _{CCA} 2.5V | AVCA V _{CCA} 1.8V |
| t _{pd} | A | B | MAX | 3.7 | 4.6 | 7.5 |
| t _{pd} | B | A | MAX | 4 | 4.2 | 4.6 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK.0 | MAX | 4.2 | 4.8 | 8 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK-.f.h | MAX | 8.3 | 9.4 | 17.9 |
| t _{pd} | CMD.h | CMD.0 | MAX | 3.3 | 3.7 | 7.4 |
| t _{pd} | CMD.h | CMD.1 | MAX | 3.5 | 4.4 | 6.2 |
| t _{pd} | CMD.0 | CMD.h | MAX | 3.8 | 4 | 4.5 |
| t _{pd} | CS0 | B | MAX | 3.8 | 4 | 6.6 |
| t _{pd} | R/B | R/B.h | MAX | 3.8 | 4 | 4.4 |
| t _{pd} | WE | WE.h | MAX | 3.7 | 3.9 | 7.3 |
| t _{pd} | WP | WP.h | MAX | 3.8 | 4 | 5.6 |
| t _{en} | DAT1.0 or DATA1.0 | IRQ | MAX | 3.3 | 3.3 | 5 |
| t _{en} | DAT1.0 or DATA1.1 | IRQ | MAX | 3.1 | 3.1 | 4.6 |
| t _{en} | DIR | B | MAX | 3.6 | 3.8 | 6.4 |
| t _{en} | DIR | A | MAX | 6.9 | 6.9 | 7.7 |
| t _{en} | R/B | R/B.h open drain | MAX | 4.1 | 4.1 | 4.4 |
| t _{dis} | DAT1.0 or DATA1.0 | IRQ | MAX | 5.5 | 4.8 | 6.5 |
| t _{dis} | DAT1.0 or DATA1.1 | IRQ | MAX | 5.3 | 4.8 | 6.6 |
| t _{dis} | DIR | B | MAX | 5.7 | 5.4 | 6.3 |
| t _{dis} | DIR | A | MAX | 5.2 | 5.3 | 5.2 |
| t _{dis} | R/B | R/B.h open drain | MAX | 3.8 | 19.5 | 15.9 |

UNIT : ns

| V _{CCA} = 2.5V | | | | | |
|-------------------------|-------------------|-------------------|------------|----------------------------|----------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V | AVCA V _{CCA} 2.5V |
| t _{pd} | A | B | MAX | 3.1 | 4 |
| t _{pd} | B | A | MAX | 3.6 | 3.7 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK.0 | MAX | 3.5 | 3.9 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK-.f.h | MAX | 7 | 8.3 |
| t _{pd} | CMD.h | CMD.0 | MAX | 2.7 | 3.2 |
| t _{pd} | CMD.h | CMD.1 | MAX | 2.8 | 3.6 |
| t _{pd} | CMD.0 | CMD.h | MAX | 3 | 3 |
| t _{pd} | CS0 | B | MAX | 3.3 | 4.2 |
| t _{pd} | R/B | R/B.h | MAX | 2.9 | 3.1 |
| t _{pd} | WE | WE.h | MAX | 3 | 3.6 |
| t _{pd} | WP | WP.h | MAX | 2.9 | 3.5 |
| t _{en} | DAT1.0 or DATA1.0 | IRQ | MAX | 3.2 | 3.3 |
| t _{en} | DAT1.0 or DATA1.1 | IRQ | MAX | 3.2 | 3.6 |
| t _{en} | DIR | B | MAX | 3.6 | 4.7 |
| t _{en} | DIR | A | MAX | 5.1 | 5.3 |
| t _{en} | R/B | R/B.h open drain | MAX | 3 | 3.2 |
| t _{dis} | DAT1.0 or DATA1.0 | IRQ | MAX | 5.4 | 7.2 |
| t _{dis} | DAT1.0 or DATA1.1 | IRQ | MAX | 5.4 | 7 |
| t _{dis} | DIR | B | MAX | 5.1 | 4.5 |
| t _{dis} | DIR | A | MAX | 3.7 | 3.7 |
| t _{dis} | R/B | R/B.h open drain | MAX | 3.9 | 3.2 |

UNIT : ns

| V _{CCA} = 3.3V | | | | |
|-------------------------|-------------------|-------------------|------------|----------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V |
| t _{pd} | A | B | MAX | 2.9 |
| t _{pd} | B | A | MAX | 3.8 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK.0 | MAX | 3.3 |
| t _{pd} | CLK, or SCLK.h | CLK, or SCLK-.f.h | MAX | 6.1 |
| t _{pd} | CMD.h | CMD.0 | MAX | 2.7 |
| t _{pd} | CMD.h | CMD.1 | MAX | 2.7 |
| t _{pd} | CMD.0 | CMD.h | MAX | 2.6 |
| t _{pd} | CS0 | B | MAX | 3.7 |
| t _{pd} | R/B | R/B.h | MAX | 2.5 |
| t _{pd} | WE | WE.h | MAX | 3 |
| t _{pd} | WP | WP.h | MAX | 2.8 |
| t _{en} | DAT1.0 or DATA1.0 | IRQ | MAX | 3.2 |
| t _{en} | DAT1.0 or DATA1.1 | IRQ | MAX | 3.2 |
| t _{en} | DIR | B | MAX | 3.7 |
| t _{en} | DIR | A | MAX | 4.7 |
| t _{en} | R/B | R/B.h open drain | MAX | 4.9 |
| t _{dis} | DAT1.0 or DATA1.0 | IRQ | MAX | 5.3 |
| t _{dis} | DAT1.0 or DATA1.1 | IRQ | MAX | 5.2 |
| t _{dis} | DIR | B | MAX | 5 |
| t _{dis} | DIR | A | MAX | 4.7 |
| t _{dis} | R/B | R/B.h open drain | MAX | 6 |

UNIT : ns

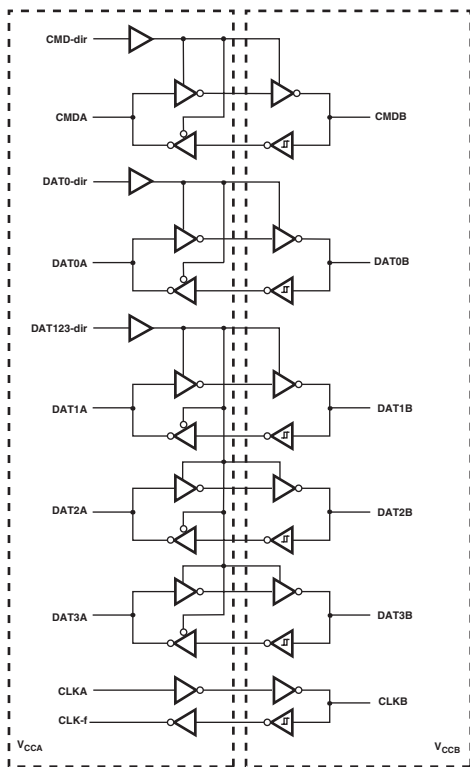
MAXIMUM FREQUENCY AND OUTPUT SKEW

| PARAMETER | | V _{CC} = 3.3V | | | | | | | UNIT |
|--------------------|-------|------------------------|-------------|------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|------|
| | | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CC} 3.3V | AVCA V _{CC} 2.5V | AVCA V _{CC} 1.8V | AVCA V _{CC} 1.5V | |
| f _{max} | Clock | A | B | MIN | 52 | 52 | 52 | 52 | MHz |
| | | B | A | | 52 | 52 | 52 | 52 | MHz |
| | Data | A | B | MIN | 26 | 26 | 26 | 26 | MHz |
| | | B | A | | 26 | 26 | 26 | 26 | MHz |
| t _{setup} | | A | B | MAX | 0.7 | 0.7 | 0.8 | 1.5 | ns |

UNIT : ns

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ± 15 -kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

- Transceiver for Memory Card Interface
[MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Compliant Products]
- For Low-Power Operation, A and B ports Are Placed in High-Impedance State When Either Supply Voltage Is Switched Off

Logic Diagram

FUNCTION TABLES

| CONTROL INPUT CMD-dir | OUTPUT CIRCUITS | | OPERATION |
|--------------------------|-----------------|---------|--------------|
| | CMDA | CMDB | |
| High | Hi-Z | Enabled | CMDA to CMDB |
| Low | Enabled | Hi-Z | CMDB to CMDA |

| CONTROL INPUT DAT0-dir | OUTPUT CIRCUITS | | FUNCTION |
|---------------------------|-----------------|---------|----------------|
| | DAT0A | DAT0B | |
| High | Hi-Z | Enabled | DAT0A to DAT0B |
| Low | Enabled | Hi-Z | DAT0B to DAT0A |

ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 0V$ | AVCA $V_{CCA} = 0V$ $V_{CCB} = 3.3V$ | AVCA $V_{CCA} = 1.2$ to $3.3V$ $V_{CCB} = 1.2$ to $3.3V$ | UNIT |
|---------------------|------------|--|--|--|------|
| I_{CCA} | MAX | 0.01 | -0.001 | 10 | mA |
| I_{CCB} | MAX | -0.001 | 0.01 | 10 | mA |
| $I_{CCA} + I_{CCB}$ | MAX | - | - | 15 | mA |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AVCA 3.3V | AVCA 2.5V | AVCA 1.8V | AVCA 1.5V | UNIT | |
|-----------|------------|--------------|--------------|--------------|--------------|------|----|
| I_{OH} | A port | MAX | -8 | -4 | -2 | -1 | mA |
| I_{OL} | | | 8 | 4 | 2 | 1 | mA |
| I_{OH} | B port | MAX | -16 | -8 | -4 | -2 | mA |
| I_{OL} | | | 16 | 8 | 4 | 2 | mA |

* $I_{O,SD} = 0$

SWITCHING CHARACTERISTICS

| $V_{CCA} = 1.5V$ | | | | | | | |
|------------------|--------------|-------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA $V_{CCA} = 3.3V$ | AVCA $V_{CCA} = 2.5V$ | AVCA $V_{CCA} = 1.8V$ | AVCA $V_{CCA} = 1.5V$ |
| t_{pd} | A | B | MAX | 3.8 | 3.9 | 4.8 | 5.6 |
| t_{pd} | B | A | MAX | 5.2 | 5.2 | 5.6 | 6 |
| t_{pd} | CLKA | CLKB | MAX | 3.8 | 3.9 | 4.8 | 5.6 |
| t_{pd} | | CLK-f | MAX | 9 | 9.1 | 10.4 | 116 |
| t_{pd} | CMDA | CMDB | MAX | 3.8 | 3.9 | 4.8 | 5.6 |
| t_{pd} | CMDB | CMDA | MAX | 5.2 | 5.2 | 5.6 | 6 |
| t_{en} | DIR | B | MAX | 5.9 | 6.1 | 6.9 | 7.7 |
| t_{en} | | A | MAX | 7.7 | 8.2 | 7.4 | 7 |
| t_{es} | DIR | B | MAX | 11.4 | 8.7 | 10.4 | 8.9 |
| t_{es} | | A | MAX | 6.6 | 6.5 | 6.8 | 7 |

UNIT : ns

| $V_{CCA} = 1.8V$ | | | | | | | |
|------------------|--------------|-------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA $V_{CCA} = 3.3V$ | AVCA $V_{CCA} = 2.5V$ | AVCA $V_{CCA} = 1.8V$ | AVCA $V_{CCA} = 1.5V$ |
| t_{pd} | A | B | MAX | 3.1 | 3.5 | 4.4 | 5.2 |
| t_{pd} | B | A | MAX | 4.3 | 4.3 | 4.8 | 5.2 |
| t_{pd} | CLKA | CLKB | MAX | 3.1 | 3.5 | 4.4 | 5.2 |
| t_{pd} | | CLK-f | MAX | 7.4 | 7.8 | 9.1 | 10.4 |
| t_{pd} | CMDA | CMDB | MAX | 3.1 | 3.5 | 4.4 | 5.2 |
| t_{pd} | CMDB | CMDA | MAX | 4.3 | 4.3 | 4.8 | 5.2 |
| t_{en} | DIR | B | MAX | 4.8 | 5.1 | 6 | 6.8 |
| t_{en} | | A | MAX | 5.3 | 5.1 | 5.2 | 4.7 |
| t_{es} | DIR | B | MAX | 8.2 | 8.2 | 9.5 | 8.4 |
| t_{es} | | A | MAX | 7.6 | 7.5 | 7.9 | 7.7 |

UNIT : ns

| $V_{CCA} = 2.5V$ | | | | | | | |
|------------------|--------------|-------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA $V_{CCA} = 3.3V$ | AVCA $V_{CCA} = 2.5V$ | AVCA $V_{CCA} = 1.8V$ | AVCA $V_{CCA} = 1.5V$ |
| t_{pd} | A | B | MAX | 2.5 | 2.9 | 3.8 | 4.7 |
| t_{pd} | B | A | MAX | 3.2 | 3.3 | 3.9 | 4.4 |
| t_{pd} | CLKA | CLKB | MAX | 2.5 | 2.9 | 3.8 | 4.7 |
| t_{pd} | | CLK-f | MAX | 5.7 | 6.2 | 7.7 | 9.1 |
| t_{pd} | CMDA | CMDB | MAX | 2.5 | 2.9 | 3.8 | 4.7 |
| t_{pd} | CMDB | CMDA | MAX | 3.2 | 3.3 | 3.9 | 4.4 |
| t_{en} | DIR | B | MAX | 3.6 | 3.9 | 4.8 | 5.7 |
| t_{en} | | A | MAX | 4.7 | 4.4 | 4.3 | 3.5 |
| t_{es} | DIR | B | MAX | 7.5 | 7.2 | 8.4 | 7.6 |
| t_{es} | | A | MAX | 5.8 | 5.5 | 5.4 | 5.6 |

UNIT : ns

| V _{CCA} = 3.3V | | | | | | | |
|-------------------------|--------------|-------------|------------|----------------------------|----------------------------|----------------------------|----------------------------|
| PARAMETER | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V | AVCA V _{CCA} 2.5V | AVCA V _{CCA} 1.8V | AVCA V _{CCA} 1.5V |
| t _{sd} | A | B | MAX | 2.3 | 2.7 | 3.6 | 4.5 |
| t _{sd} | B | A | MAX | 2.7 | 3 | 3.7 | 4.3 |
| t _{sd} | CLKA | CLKB | MAX | 2.3 | 2.7 | 3.6 | 4.5 |
| | | CLK-f | MAX | 5 | 5.7 | 7.3 | 8.8 |
| t _{sd} | CMDA | CMDB | MAX | 2.3 | 2.7 | 3.6 | 4.5 |
| t _{sd} | CMDB | CMDA | MAX | 2.7 | 3 | 3.7 | 4.3 |
| t _{en} | DIR | B | MAX | 3 | 3.4 | 4.3 | 5.1 |
| t _{en} | | A | MAX | 5.4 | 5.4 | 5.4 | 3.1 |
| t _{en} | DIR | B | MAX | 7.3 | 7 | 8.3 | 7.4 |
| t _{en} | | A | MAX | 8 | 7.9 | 7.9 | 8.1 |

UNIT : ns

MAXIMUM FREQUENCY

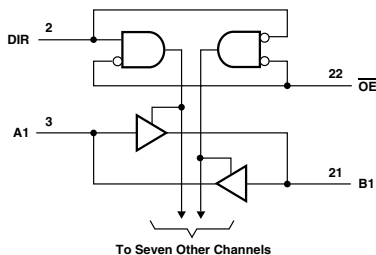
| PARAMETER | | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V | AVCA V _{CCA} 2.5V | AVCA V _{CCA} 1.8V | AVCA V _{CCA} 1.5V | UNIT |
|------------------|-------|--------------|-------------|------------|----------------------------|----------------------------|----------------------------|----------------------------|------|
| f _{max} | Clock | CLKA | CLKB | MIN | 95 | 95 | 95 | 95 | MHz |
| | | | CLK-f | MIN | 95 | 95 | 95 | 95 | MHz |
| | Data | A | B | MIN | 95 | 95 | 95 | 95 | MHz |
| | | B | A | MIN | 95 | 95 | 95 | 95 | MHz |

OUTPUT SKEW

| PARAMETER | V _{CCA} | INPUT (FROM) | OUTPUT (TO) | MAX or MIN | AVCA V _{CCA} 3.3V | AVCA V _{CCA} 2.5V | AVCA V _{CCA} 1.8V | AVCA V _{CCA} 1.5V | UNIT |
|-------------------|------------------|--------------|-------------|------------|----------------------------|----------------------------|----------------------------|----------------------------|------|
| t _{skid} | 3.3V | DIR | B | MIN | 0.4 | 0.3 | 0.4 | 0.3 | ns |
| | 2.5V | DIR | B | MIN | 0.3 | 0.2 | 0.3 | 0.3 | ns |
| | 1.8V | DIR | B | MIN | 0.3 | 0.3 | 0.3 | 0.3 | ns |
| | 1.5V | DIR | B | MIN | 0.4 | 0.3 | 0.3 | 0.3 | ns |

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

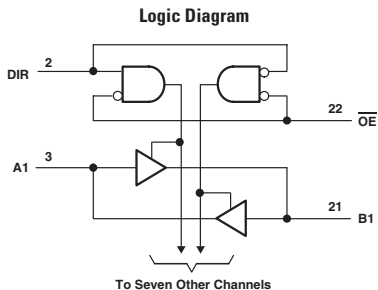
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | V _{CCA} (V) | V _{CCB} (V) | LVCC | UNIT |
|------------------|--------|------------|----------------------|----------------------|------|------|
| I _{CCA} | B to A | MAX | 3.6 | 3.6 | 0.05 | mA |
| | | | | 5.5 | 0.05 | |
| I _{CCB} | A to B | MAX | 3.6 | 3.6 | 0.05 | mA |
| | | | | 5.5 | 0.08 | |
| I _{OHA} | MAX | MAX | 2.3 | 3.0 | -8 | mA |
| | | | 2.7 | | -12 | |
| | | | 3.3 | | -24 | |
| I _{OHB} | MAX | MAX | 2.3 | 3.3 | -8 | mA |
| | | | 2.7 | | -12 | |
| | | | 3.3 | | -24 | |
| I _{OLA} | MAX | MAX | 2.3 | 3.0 | 8 | mA |
| | | | 2.7 | | 12 | |
| | | | 3.3 | | 24 | |
| I _{OLB} | MAX | MAX | 2.3 | 3.3 | 8 | mA |
| | | | 2.7 | | 12 | |
| | | | 3.3 | | 24 | |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCC | LVCC | LVCC | LVCC | LVCC |
|------------------|-------|--------|------------|--|--|--|--|--|
| | | | | V _{CCA} = 2.3V V _{CCB} = 3.0V | V _{CCA} = 2.7V V _{CCB} = 5.5V | V _{CCA} = 3.6V V _{CCB} = 5.5V | V _{CCA} = 2.7V V _{CCB} = 3.0V | V _{CCA} = 3.6V V _{CCB} = 3.0V |
| t _{PLH} | A | B | MAX | 9.4 | 6.0 | 6.0 | 7.1 | 7.1 |
| t _{PHL} | | | | 9.1 | 5.3 | 5.3 | 7.2 | 7.2 |
| t _{PLH} | B | A | MAX | 11.2 | 5.8 | 5.8 | 6.4 | 6.4 |
| t _{PHL} | | | | 9.9 | 7.0 | 7.0 | 7.6 | 7.6 |
| t _{PZL} | OE | A | MAX | 14.5 | 9.2 | 9.2 | 9.7 | 9.7 |
| t _{PZH} | | | | 12.9 | 9.5 | 9.5 | 9.5 | 9.5 |
| t _{PZL} | OE | B | MAX | 13 | 8.1 | 8.1 | 9.2 | 9.2 |
| t _{PZH} | | | | 12.8 | 8.4 | 8.4 | 9.9 | 9.9 |
| t _{PLZ} | OE | A | MAX | 7.1 | 7.0 | 7.0 | 6.6 | 6.6 |
| t _{PHZ} | | | | 6.9 | 7.8 | 7.8 | 6.9 | 6.9 |
| t _{PLZ} | OE | B | MAX | 8.8 | 7.3 | 7.3 | 7.5 | 7.5 |
| t _{PHZ} | | | | 8.9 | 7.0 | 7.0 | 7.9 | 7.9 |

UNIT: ns

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS (SN74LVC4245A)
OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS (SN74LVCC4245A)
**FUNCTION TABLE**

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LVC | LVCC | UNIT |
|------------------|--|------------|------|------|------|
| I _{CCA} | V _{CCA} =5.5V V _{CCB} =5.5V | MAX | 0.08 | 0.08 | mA |
| | V _{CCA} =5.5V V _{CCB} =3.6V | MAX | 0.08 | 0.08 | mA |
| I _{CCB} | V _{CCA} =5.5V V _{CCB} =5.5V | MAX | 0.05 | 0.08 | mA |
| | V _{CCA} =5.5V V _{CCB} =3.6V | MAX | 0.05 | 0.05 | mA |
| I _{OH} | V _{CCB} =3.3V | MAX | -24 | -24 | mA |
| I _{OL} | | | 24 | 24 | |
| I _{OH} | V _{CCB} =2.7V | MAX | -12 | -24 | mA |
| I _{OL} | | | 12 | 24 | |
| I _{OH} | V _{CCA} =4.5V | MAX | -24 | -24 | mA |
| I _{OL} | | | 24 | 24 | |

SWITCHING CHARACTERISTICS

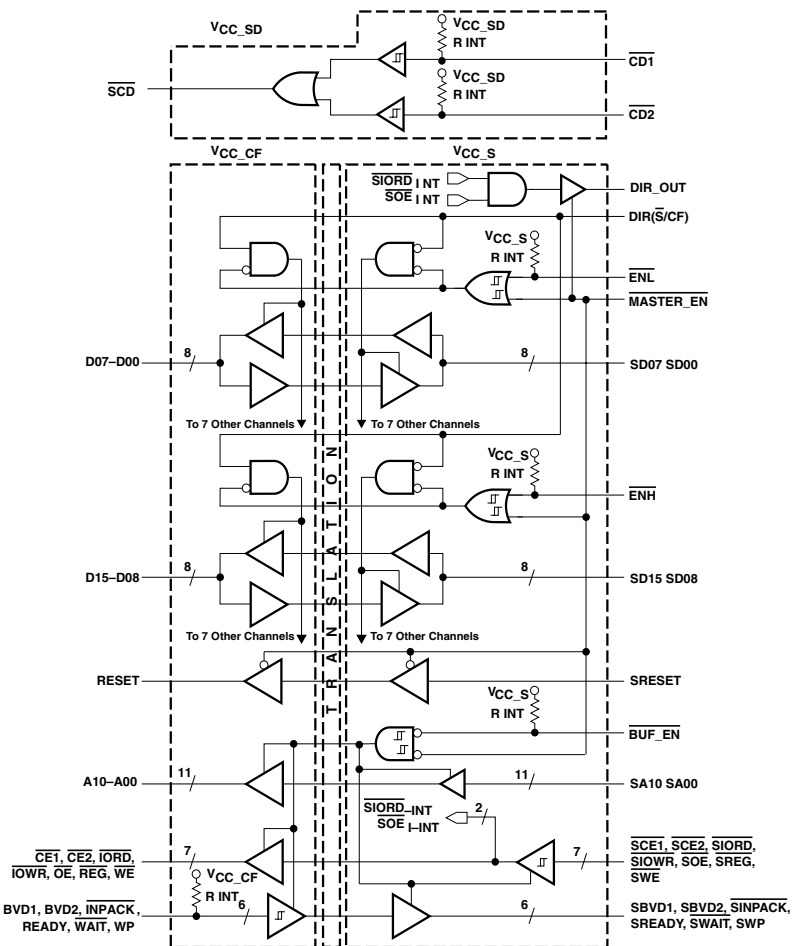
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC | | LVCC | | |
|------------------|-----------------|--------|------------|--|--|--|--|--|
| | | | | V _{CCA} =5.5V V _{CCB} =2.7V | V _{CCA} =5.5V V _{CCB} =3.6V | V _{CCA} =5.5V V _{CCB} =5.5V | V _{CCA} =5.5V V _{CCB} =2.7V | V _{CCA} =5.5V V _{CCB} =3.6V |
| t _{PLH} | A | B | MAX | 6.3 | 6.3 | 7.1 | 7.0 | 7.0 |
| t _{PHL} | | | | 6.7 | 6.7 | 6.0 | 7.0 | 7.0 |
| t _{PLH} | B | A | MAX | 6.1 | 6.1 | 6.8 | 6.2 | 6.2 |
| t _{PHL} | | | | 5.0 | 5.0 | 6.1 | 5.3 | 5.3 |
| t _{PZL} | \overline{OE} | A | MAX | 9.0 | 9.0 | 9.0 | 9.0 | 9.0 |
| t _{PZH} | | | | 8.1 | 8.1 | 8.3 | 8.0 | 8.0 |
| t _{PZL} | \overline{OE} | B | MAX | 8.8 | 8.8 | 8.2 | 10.0 | 10.0 |
| t _{PZH} | | | | 9.8 | 9.8 | 8.1 | 10.2 | 10.2 |
| t _{PLZ} | \overline{OE} | A | MAX | 7.0 | 7.0 | 4.7 | 5.2 | 5.2 |
| t _{PHZ} | | | | 5.8 | 5.8 | 4.9 | 5.2 | 5.2 |
| t _{PLZ} | \overline{OE} | B | MAX | 7.7 | 7.7 | 5.4 | 5.4 | 5.4 |
| t _{PHZ} | | | | 7.8 | 7.8 | 6.3 | 7.4 | 7.4 |

UNIT: ns

LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES

- Designed to Optimize Power Savings in Portable Applications
- Matched Pinout with CompactFlash™ (CF) Connector Pin Configurations to Optimize PCB Layout
- Input-Disable Feature Allows Floating Input Conditions

Logic Diagram



NOTE: R INT \geq 100 k Ω

FUNCTION TABLES

Lower 8-Bit Data Bus Transceivers (D07-D00, SD07-SD00)

| INPUTS | | | OPERATION |
|-----------|-----|----------------------|--|
| MASTER_EN | ENL | DIR (\bar{S}/CF) | |
| L | L | H | SD data to D bus |
| L | L | L | D data to SD bus |
| L | H | X | Isolation. D07-D00 and SD07-SD00 inputs can float. |
| H | X | X | Isolation, low power mode |

X = H or L

Upper 8-Bit Data Bus Transceivers (D15-D08, SD15-SD08)

| INPUTS | | | OPERATION |
|-----------|-----|----------------------|--|
| MASTER_EN | ENH | DIR (\bar{S}/CF) | |
| L | L | H | SD data to D bus |
| L | L | L | D data to SD bus |
| L | H | X | Isolation. D15-D08 and SD15-SD08 inputs can float. |
| H | X | X | Isolation, low power mode |

X = H or L

Address Bus Buffers

| INPUTS | | | OUTPUT A |
|-----------|--------|----|-------------------------|
| MASTER_EN | BUF_EN | SA | |
| L | L | H | H |
| L | L | L | L |
| L | H | X | Z. SA inputs can float. |
| H | X | X | Z, low power mode |

X = H or L

Command Line Buffers

(BVD1, BVD2, INPACK, OE, IORD, IOWR,
READY, REG, CE1, CE2, WAIT, WE, WP,)

| INPUTS | | | OUTPUT |
|-----------|--------|-------|--|
| MASTER_EN | BUF_EN | INPUT | |
| L | L | H | H |
| L | L | L | L |
| L | H | X | Z. Command line buffer inputs can float. |
| H | X | X | Z, low power mode |

X = H or L

Reset

| INPUTS | | OUTPUT RESET |
|-----------|--------|-------------------|
| MASTER_EN | SRESET | |
| L | H | H |
| L | L | L |
| H | X | Z, low power mode |

X = H or L

DIR_OUT

| INPUTS | | | | OUTPUT DIR_OUT |
|--------|-----------|-----|-------|-------------------|
| BUF_EN | MASTER_EN | SOE | SIORD | |
| L | L | L | L | L |
| L | L | L | H | L |
| L | L | H | L | L |
| L | L | H | H | H |
| H | L | X | X | L |
| X | H | X | X | Z, low power mode |

X = H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LV 5V | LV 3.3V | LV 2.5V | LV 1.8V | UNIT |
|---------------------------------|--|--------------------|----------|------------|------------|------------|-------|
| I _{CC,SD} | CD1 and CD2 = V _{CC,SD} | MAX | 0.001 | - | - | - | mA |
| | CD1 or CD2 = GND, CD1 or CD2 = V _{CC,SD} | MAX | 0.01 | - | - | - | mA |
| I _{CC,S} * | Inputs SD12-SD00, SA10-SA00, SCE1, SCE2, SIORD SIOWR, SOE, SREG, SWE | MAX | - | 0.003 | 0.003 | 0.003 | mA |
| | Control inputs (ENL, ENH, BUF_EN) | V _{CC,S} | MAX | - | 0.003 | 0.003 | 0.003 |
| GND, Other = V _{CC,S} | | MAX | - | 0.036 | 0.036 | 0.036 | mA |
| I _{CC,CF} | Input (D15- D00) | MAX | - | 0.003 | 0.003 | 0.003 | mA |
| | Input (BVD1, BVD2, INPACK, READY, WAIT, WP) | V _{CC,CF} | MAX | - | 0.003 | 0.003 | 0.003 |
| GND, Other = V _{CC,CF} | | MAX | - | 0.06 | 0.06 | 0.06 | mA |
| I _{OH} | Card detect | MAX | -12 | -8 | -4 | -2 | mA |
| I _{OL} | | | 12 | 8 | 4 | 2 | mA |
| I _{OH} | System port | MAX | - | 12 | 6 | 2 | mA |
| I _{OL} | | | - | 12 | 6 | 2 | mA |
| I _{OH} | CF port | MAX | 16 | 12 | - | - | mA |
| I _{OL} | | | 16 | 12 | - | - | mA |

*I_{0,SD} = 0

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC,SD} | LV 5V | LV 3.3V | LV 2.5V | LV 1.8V |
|------------------|------------|--------|------------|--------------------|----------|------------|------------|------------|
| t _{PLH} | CD1 or CD2 | SCD | MAX | 5.5 | 5.5 | 6.8 | 9.1 | 15.5 |
| t _{PHL} | | | | 5.5 | 5.5 | 6.8 | 9.1 | 15.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC,CF} | LV V _{CC,S} 3.3V | LV V _{CC,S} 2.5V | LV V _{CC,S} 1.8V |
|------------------|-----------|----------|------------|--------------------|---------------------------------|---------------------------------|---------------------------------|
| t _{PLH} | CF input | S output | MAX | 3.3V | 8.8 | 10 | 12.9 |
| t _{PHL} | | | | | 8.8 | 10 | 12.9 |
| t _{PLH} | CF input | S output | MAX | 5V | 7 | 8.6 | 13.9 |
| t _{PHL} | | | | | 7 | 8.6 | 13.9 |
| t _{PZH} | MASTER_EN | S output | MAX | 3.3V | 18.3 | 22.6 | 35.5 |
| t _{PZL} | | | | | 18.3 | 22.6 | 35.5 |
| t _{PZH} | MASTER_EN | S output | MAX | 5V | 18.2 | 22.6 | 35.6 |
| t _{PZL} | | | | | 18.2 | 22.6 | 35.6 |
| t _{PHZ} | MASTER_EN | S output | MAX | 3.3V | 13.2 | 14.5 | 25.1 |
| t _{PLZ} | | | | | 13.2 | 14.5 | 25.1 |
| t _{PHZ} | MASTER_EN | S output | MAX | 5V | 18.2 | 14.5 | 23.3 |
| t _{PLZ} | | | | | 18.2 | 14.5 | 23.3 |
| t _{PZH} | BUF_EN | S output | MAX | 3.3V | 18.3 | 22.6 | 35.5 |
| t _{PZL} | | | | | 18.3 | 22.6 | 35.5 |
| t _{PZH} | BUF_EN | S output | MAX | 5V | 18.2 | 22.6 | 35.6 |
| t _{PZL} | | | | | 18.2 | 22.6 | 35.6 |
| t _{PHZ} | BUF_EN | S output | MAX | 3.3V | 12.3 | 14.5 | 24.2 |
| t _{PLZ} | | | | | 12.3 | 14.5 | 24.2 |
| t _{PHZ} | BUF_EN | S output | MAX | 5V | 12.4 | 14.2 | 22.8 |
| t _{PLZ} | | | | | 12.4 | 14.2 | 22.8 |
| t _{PLH} | D | SD | MAX | 3.3V | 8.8 | 10 | 13.7 |
| t _{PHL} | | | | | 8.8 | 10 | 13.7 |
| t _{PLH} | D | SD | MAX | 5V | 7 | 12.4 | 13.9 |
| t _{PHL} | | | | | 7 | 12.4 | 13.9 |
| t _{PLH} | SD | D | MAX | 3.3V | 7.6 | 8.2 | 11.1 |
| t _{PHL} | | | | | 7.6 | 8.2 | 11.1 |
| t _{PLH} | SD | D | MAX | 5V | 6 | 7 | 9.6 |
| t _{PHL} | | | | | 6 | 7 | 9.6 |

UNIT : ns

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC_CF} | LV V _{CC_S} 3.3V | LV V _{CC_S} 2.5V | LV V _{CC_S} 1.8V |
|------------------|------------|--------|------------|--------------------|---------------------------------|---------------------------------|---------------------------------|
| t _{PZH} | MASTER_EN | D | MAX | 3.3V | 21.4 | 23 | 27.9 |
| t _{PZL} | | | | | 21.4 | 23 | 27.9 |
| t _{PHZ} | MASTER_EN | D | MAX | 5V | 20.3 | 21.8 | 31 |
| t _{PZL} | | | | | 20.3 | 21.8 | 31 |
| t _{PZH} | MASTER_EN | SD | MAX | 3.3V | 18.3 | 22.6 | 36.3 |
| t _{PZL} | | | | | 18.3 | 22.6 | 36.3 |
| t _{PHZ} | MASTER_EN | SD | MAX | 5V | 18.2 | 22.6 | 36.2 |
| t _{PZL} | | | | | 18.2 | 22.6 | 36.2 |
| t _{PHZ} | MASTER_EN | D | MAX | 3.3V | 15 | 16.4 | 20.2 |
| t _{PLZ} | | | | | 15 | 16.4 | 20.2 |
| t _{PHZ} | MASTER_EN | D | MAX | 5V | 12.5 | 13.8 | 17.8 |
| t _{PLZ} | | | | | 12.5 | 13.8 | 17.8 |
| t _{PHZ} | MASTER_EN | SD | MAX | 3.3V | 12 | 14.5 | 24.2 |
| t _{PLZ} | | | | | 12 | 14.5 | 24.2 |
| t _{PHZ} | MASTER_EN | SD | MAX | 5V | 18.2 | 14.2 | 22.8 |
| t _{PLZ} | | | | | 18.2 | 14.2 | 22.8 |
| t _{PZH} | ENL or ENH | D | MAX | 3.3V | 21.4 | 22.8 | 27.2 |
| t _{PZL} | | | | | 21.4 | 22.8 | 27.2 |
| t _{PZH} | ENL or ENH | D | MAX | 5V | 20.3 | 21.6 | 27.8 |
| t _{PZL} | | | | | 20.3 | 21.6 | 27.8 |
| t _{PZH} | ENL or ENH | SD | MAX | 3.3V | 18.3 | 22.6 | 35.5 |
| t _{PZL} | | | | | 18.3 | 22.6 | 35.5 |
| t _{PZH} | ENL or ENH | SD | MAX | 5V | 18.2 | 22.6 | 35.6 |
| t _{PZL} | | | | | 18.2 | 22.6 | 35.6 |
| t _{PHZ} | ENL or ENH | D | MAX | 3.3V | 15 | 16.4 | 20.2 |
| t _{PLZ} | | | | | 15 | 16.4 | 20.2 |
| t _{PHZ} | ENL or ENH | D | MAX | 5V | 12 | 13.1 | 16.6 |
| t _{PLZ} | | | | | 12 | 13.1 | 16.6 |
| t _{PHZ} | ENL or ENH | SD | MAX | 3.3V | 12 | 14.5 | 24.2 |
| t _{PLZ} | | | | | 12 | 14.5 | 24.2 |
| t _{PHZ} | ENL or ENH | SD | MAX | 5V | 18.2 | 14.2 | 22.8 |
| t _{PLZ} | | | | | 18.2 | 14.2 | 22.8 |

UNIT : ns

164245

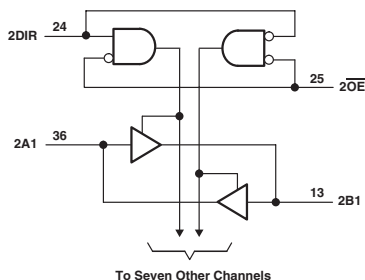
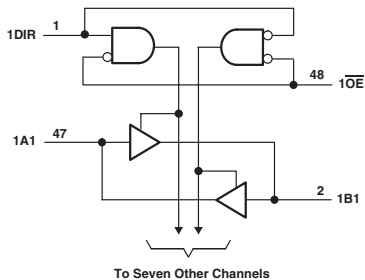
16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:
A port has V_{CCA} , which is set to operate at 2.5 V and 3.3 V
B port has V_{CCB} , which is set to operate at 3.3 V and 5 V
- SN74AVCB164245, SN74AVCBH164245:
The A-port is designed to track V_{CCA} , V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V
The B-port is designed to track V_{CCB} , V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V

FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC | AVCA | AVCAH | AVCB | AVCBH | UNIT | |
|-----------|----------------------------------|----------|----------|-------|-------|-------|-------|----|
| I_{CC} | $V_{CCA}=3.6V$ $V_{CCB}=5.5V$ | MAX | 0.04 | - | - | - | mA | |
| | $V_{CCA}=2.3V$ $V_{CCB}=3.3V$ | MAX | 0.02 | - | - | - | mA | |
| | $V_{CCA}=3.6V$ $V_{CCB}=3.6V$ | MAX | - | 0.04 | 0.04 | 0.04 | 0.04 | mA |
| | $V_{CCA}=3.6V$ $V_{CCB}=0V$ | MAX | - | -0.04 | -0.04 | -0.04 | -0.04 | mA |
| | $V_{CCA}=0V$ $V_{CCB}=3.6V$ | MAX | - | 0.04 | 0.04 | 0.04 | 0.04 | mA |
| | $V_{CCA}=2.7V$ $V_{CCB}=2.7V$ | MAX | - | 0.03 | 0.03 | 0.03 | 0.03 | mA |
| | $V_{CCA}=1.6V$ $V_{CCB}=1.6V$ | MAX | - | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | $V_{CCB}=3.3V$ | MAX | -24 | -12 | -12 | -12 | -12 | mA |
| | | I_{OL} | 24 | 12 | 12 | 12 | 12 | |
| I_{OH} | $V_{CCA}=3.0V$ | MAX | -24 | -12 | -12 | -12 | -12 | mA |
| | | | I_{OL} | 24 | 12 | 12 | 12 | |
| I_{OH} | $V_{CCA}=2.3V$ | MAX | -18 | -8 | -8 | -8 | -8 | mA |
| | | | I_{OL} | 18 | 8 | 8 | 8 | |
| I_{OH} | $V_{CCA}=1.4V$ | MAX | - | -2 | -2 | -2 | -2 | mA |
| | | | I_{OL} | - | 2 | 2 | 2 | |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC | | |
|-----------|-----------------|--------|------------|-----------|-----------|-----------|
| | | | | VCCB=3.3V | VCCB=5.5V | VCCB=5.5V |
| | | | | VCCA=2.3V | VCCA=2.7V | VCCA=3.3V |
| EP LH | A | B | MAX | 7.6 | 5.9 | 5.8 |
| EP HL | | | | 7.6 | 5.9 | 5.8 |
| EP LH | B | A | MAX | 7.6 | 6.7 | 5.8 |
| EP HL | | | | 7.6 | 6.7 | 5.8 |
| EP ZL | \overline{OE} | B | MAX | 11.5 | 9.3 | 8.9 |
| EP ZH | | | | 11.5 | 9.3 | 8.9 |
| EP ZL | \overline{OE} | A | MAX | 12.3 | 10.2 | 9.1 |
| EP ZH | | | | 12.3 | 10.2 | 9.1 |
| EP LZ | \overline{OE} | B | MAX | 10.5 | 9.2 | 9.5 |
| EP HZ | | | | 10.5 | 9.2 | 9.5 |
| EP LZ | \overline{OE} | A | MAX | 9.3 | 9.0 | 8.6 |
| EP HZ | | | | 9.3 | 9.0 | 8.6 |

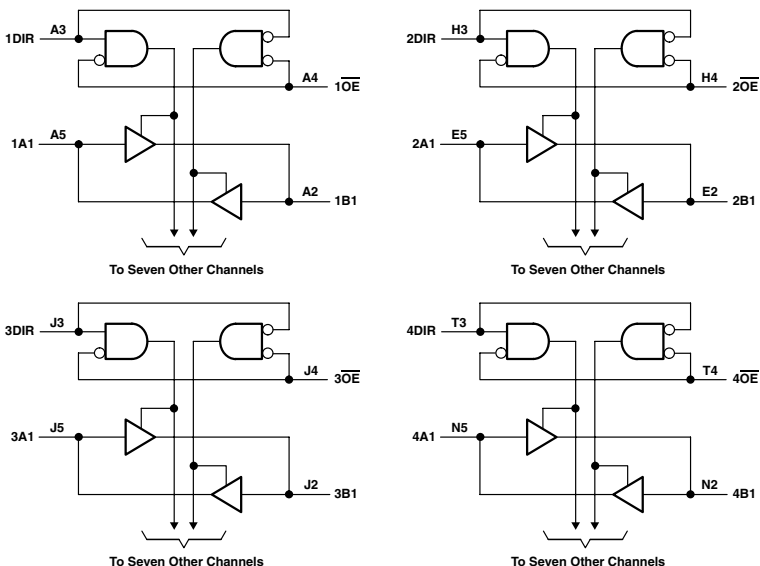
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCA/AVCAH | | | | | |
|-----------|-----------------|--------|------------|------------|-----------|-----------|-----------|-----------|-----------|
| | | | | VCCA=1.4V | VCCA=1.4V | VCCA=2.3V | VCCA=2.3V | VCCA=3.6V | VCCA=3.6V |
| | | | | VCCB=2.3V | VCCB=3.6V | VCCB=1.4V | VCCB=3.6V | VCCB=1.4V | VCCB=2.3V |
| EP LH | A | B | MAX | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| EP HL | | | | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| EP LH | B | A | MAX | 7.6 | 7.3 | 4.6 | 3.7 | 4.5 | 3.3 |
| EP HL | | | | 7.6 | 7.3 | 4.6 | 3.7 | 4.5 | 3.3 |
| EP ZL | \overline{OE} | B | MAX | 10.8 | 10.7 | 4.1 | 5.3 | 2.6 | 4.1 |
| EP ZH | | | | 10.8 | 10.7 | 4.1 | 5.3 | 2.6 | 4.1 |
| EP ZL | \overline{OE} | A | MAX | 6.3 | 5.6 | 7.4 | 4.5 | 7.0 | 5.0 |
| EP ZH | | | | 6.3 | 5.6 | 7.4 | 4.5 | 7.0 | 5.0 |
| EP LZ | \overline{OE} | B | MAX | 6.5 | 6.4 | 4.5 | 3.7 | 5.4 | 3.6 |
| EP HZ | | | | 6.5 | 6.4 | 4.5 | 3.7 | 5.4 | 3.6 |
| EP LZ | \overline{OE} | A | MAX | 5.3 | 6.1 | 5.7 | 4.0 | 5.4 | 3.3 |
| EP HZ | | | | 5.3 | 6.1 | 5.7 | 4.0 | 5.4 | 3.3 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCB/AVCBH | | | | | |
|-----------|-----------------|--------|------------|------------|-----------|-----------|-----------|-----------|-----------|
| | | | | VCCA=1.4V | VCCA=1.4V | VCCA=2.3V | VCCA=2.3V | VCCA=3.6V | VCCA=3.6V |
| | | | | VCCB=2.3V | VCCB=3.6V | VCCB=1.4V | VCCB=3.6V | VCCB=1.4V | VCCB=2.3V |
| EP LH | A | B | MAX | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| EP HL | | | | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| EP LH | B | A | MAX | 7.6 | 7.3 | 4.6 | 3.7 | 4.5 | 3.3 |
| EP HL | | | | 7.6 | 7.3 | 4.6 | 3.7 | 4.5 | 3.3 |
| EP ZL | \overline{OE} | B | MAX | 10.0 | 9.8 | 5.7 | 5.1 | 4.9 | 4.3 |
| EP ZH | | | | 10.0 | 9.8 | 5.7 | 5.1 | 4.9 | 4.3 |
| EP ZL | \overline{OE} | A | MAX | 5.2 | 4.2 | 8.5 | 4.2 | 8.3 | 5.2 |
| EP ZH | | | | 5.2 | 4.2 | 8.5 | 4.2 | 8.3 | 5.2 |
| EP LZ | \overline{OE} | B | MAX | 5.1 | 4.8 | 5.8 | 3.3 | 6.9 | 3.8 |
| EP HZ | | | | 5.1 | 4.8 | 5.8 | 3.3 | 6.9 | 3.8 |
| EP LZ | \overline{OE} | A | MAX | 3.6 | 3.0 | 7.0 | 3.0 | 7.0 | 3.5 |
| EP HZ | | | | 3.6 | 3.0 | 7.0 | 3.0 | 7.0 | 3.5 |

UNIT: ns

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | AVCB | UNIT |
|-----------------|--|------------|-------|------|
| I _{CC} | V _{CCA} =3.6V V _{CCB} =3.6V | MAX | 0.08 | mA |
| | V _{CCA} =3.6V V _{CCB} =0V | MAX | -0.08 | mA |
| | V _{CCA} =0V V _{CCB} =3.6V | MAX | 0.08 | mA |
| | V _{CCA} =2.7V V _{CCB} =2.7V | MAX | 0.04 | mA |
| | V _{CCA} =1.6V V _{CCB} =1.6V | MAX | 0.04 | mA |
| I _{OH} | V _{CCB} =3.3V | MAX | -12 | mA |
| I _{OL} | | | 12 | |
| I _{OH} | V _{CCA} =3.0V | MAX | -12 | mA |
| I _{OL} | | | 12 | |
| I _{OH} | V _{CCA} =2.3V | MAX | -8 | mA |
| I _{OL} | | | 8 | |
| I _{OH} | V _{CCA} =1.4V | MAX | -2 | mA |
| I _{OL} | | | 2 | |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVCB | | | | | |
|------------------|-----------------|--------|------------|--|--|--|--|--|--|
| | | | | V _{CCA} =1.4V V _{CCB} =2.3V | V _{CCA} =1.4V V _{CCB} =3.6V | V _{CCA} =2.3V V _{CCB} =1.4V | V _{CCA} =2.3V V _{CCB} =3.6V | V _{CCA} =3.6V V _{CCB} =1.4V | V _{CCA} =3.6V V _{CCB} =2.3V |
| t _{PLH} | A | B | MAX | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| t _{PHL} | | | | 5.5 | 5.8 | 6.0 | 3.4 | 5.9 | 3.7 |
| t _{PLH} | B | A | MAX | 5.9 | 5.9 | 5.4 | 3.7 | 5.8 | 3.3 |
| t _{PHL} | | | | 5.9 | 5.9 | 5.4 | 3.7 | 5.8 | 3.3 |
| t _{PZL} | \overline{OE} | B | MAX | 7.6 | 7.5 | 6.1 | 4.2 | 5.1 | 5.2 |
| t _{PZH} | | | | 7.6 | 7.5 | 6.1 | 4.2 | 5.1 | 5.2 |
| t _{PZL} | \overline{OE} | A | MAX | 10.0 | 9.8 | 5.7 | 5.1 | 4.9 | 4.3 |
| t _{PZH} | | | | 10.0 | 9.8 | 5.7 | 5.1 | 4.9 | 4.3 |
| t _{PLZ} | \overline{OE} | B | MAX | 5.8 | 5.7 | 6.0 | 3.0 | 5.5 | 3.5 |
| t _{PHZ} | | | | 5.8 | 5.7 | 6.0 | 3.0 | 5.5 | 3.5 |
| t _{PLZ} | \overline{OE} | A | MAX | 5.1 | 4.8 | 5.8 | 3.3 | 6.9 | 3.8 |
| t _{PHZ} | | | | 5.1 | 4.8 | 5.8 | 3.3 | 6.9 | 3.8 |

UNIT: ns

FUNCTION

1G / 2G / 3G

LITTLE LOGIC GATE (AND/NAND/OR/NOR/EX-OR)

| Description | No. of Input | Circuit | Input | Output | Device | Technology | | | | |
|-----------------|--------------|---------|-------|--------|--------|---------------|------|------------------|-----|----------------|
| | | | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | | | AHC | AHCT | LVC | AUC | AUP |
| POSITIVE AND | 2 | 1 | | | 1G08 | ● | ● | ● | ● | ● |
| | | 2 | | | 2G08 | | | ● | ● | |
| | | 3 | 1 | | 1G11 | | | ● | * | |
| POSITIVE NAND | 2 | 1 | | OD | 1G00 | ● | ● | ● | ● | ● |
| | | | SCH | 1G38 | | | ● | | | |
| | | | | 1G132 | | | ● | | | |
| | 2 | | | OD | 2G00 | | | ● | | |
| | | SCH | 2G38 | | | ● | | | | |
| | | | 2G132 | | | | | | | |
| 3 | 1 | | | 1G10 | | | ● | * | | |
| POSITIVE OR | 2 | 1 | | | 1G32 | ● | ● | ● | ● | ● |
| | 3 | 1 | | | 2G32 | | | ● | ● | |
| | | | | | 1G332 | | | ● | | |
| POSITIVE NOR | 2 | 1 | | | 1G02 | ● | ● | ● | ● | ● |
| | | 2 | | | 2G02 | | | ● | ● | |
| | 3 | 1 | | | 1G27 | | | ● | | |
| EXCLUSIVE OR | 2 | 1 | | | 1G86 | ● | ● | ● | ● | |
| | | 2 | | | 2G86 | | | ● | ● | |
| | 3 | 1 | | | 1G386 | | | ● | | |
| POSITIVE AND-OR | 3 | 1 | | | 1G0832 | | | ● | | |
| POSITIVE OR-AND | 3 | 1 | | | 1G3208 | | | ● | | |

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC GATE (INVERTER / NON-INVERTER)

| Description | No. of Input | Circuit | Input | Output | Device | Technology | | | | |
|---------------|--------------|---------|---------|--------|--------|---------------|------|------------------|-----|----------------|
| | | | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | | | AHC | AHCT | LVC | AUC | AUP |
| INVERTING | 1 | 1 | | BUF | 1G04 | ● | ● | ● | ● | ● |
| | | | UBF | 1GU04 | ● | | ● | ● | | |
| | | | UBF/BUF | 1GX04 | | | ● | | | |
| | | | OC | 1G06 | | | ● | ● | ● | |
| | | | SCH | 1G14 | ● | ● | ● | ● | ● | |
| | | | | 1G14 | | | ● | ● | ● | |
| | 2 | | | BUF | 2G04 | | | ● | ● | |
| | | UBF | 2GU04 | | | ● | ● | ● | ● | |
| | | OC | 2G06 | | | ● | ● | ● | ● | |
| | | SCH | 2G14 | | | ● | | * | | |
| | | | 2G14 | | | ● | | | | |
| | | | 2G14 | | | ● | | | | |
| 3 | | | BUF | 3G04 | | | ● | ● | | |
| | UBF | 3GU04 | | | ● | ● | ● | ● | | |
| | OC | 3G06 | | | ● | ● | ● | ● | | |
| | SCH | 3G14 | | | ● | | | | | |
| NON-INVERTING | 1 | 1 | | OC | 1G07 | | | ● | ● | ● |
| | | | SCH | 1G17 | | | ● | ● | ● | |
| | | | BUF | 1G34 | | | ● | | | |
| | | | OC | 2G07 | | | ● | ● | ● | |
| | | | SCH | 2G17 | | | ● | | | |
| | 2 | | | BUF | 2G34 | | | ● | ● | |
| | | OC | 2G07 | | | ● | ● | ● | ● | |
| | | SCH | 2G17 | | | ● | | | | |
| | | BUF | 2G34 | | | ● | | ● | | |
| | | OC | 3G07 | | | ● | ● | ● | ● | |
| 3 | 1 | 1 | SCH | 3G17 | | | ● | ● | ● | |
| | | | | 3G17 | | | ● | ● | ● | |
| | | | BUF | 3G34 | | | ● | | | |

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC BUFFER/DRIVER

| Description | Circuit | Output | Device | Technology | | | | |
|---------------|---------|--------|--------|---------------|------|------------------|-----|----------------|
| | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | AHC | AHCT | LVC | AUC | AUP |
| NON-INVERTING | 1 | 3S | 1G125 | ● | ● | ● | ● | ● |
| | | 3S | 1G126 | ● | ● | ● | ● | ● |
| | | 3S | 2G125 | | | ● | ● | |
| | 2 | 3S | 2G126 | | | ● | ● | |
| | | 3S | 2G241 | | | ● | ● | |
| | | 3S | 2G240 | | | ● | ● | ● |
| INVERTING | 1 | 3S | 1G240 | | | ● | ● | ● |
| | 2 | 3S | 2G240 | | | ● | ● | ● |

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC LATCH

| Type | Circuit | PRE-CLR | Output | Q · \bar{Q} | Device | Technology | | | | |
|------|---------|---------|--------|---------------|--------|---------------|------|------------------|-----|----------------|
| | | | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | | | AHC | AHCT | LVC | AUC | AUP |
| D | 4 | | 3S | Q | 373 | | | ● | | |

Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch

R-B: Read-Back Latch D: D-Type Transparent Latch

LITTLE LOGIC D-TYPE FLIP-FLOP

| Trigger | Circuit | Edge | PRE-CLR | Output | Q · \bar{Q} | Device | Technology | | | | |
|---------|---------|------|---------|--------|---------------|--------|---------------|------|------------------|-----|----------------|
| | | | | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | | | | AHC | AHCT | LVC | AUC | AUP |
| POS | 1 | S | B | 2S | B | 1G74 | | | ● | ● | |
| | | S | | 2S | Q | 1G79 | | | ● | ● | |
| | | S | | 2S | \bar{Q} | 1G80 | | | ● | ● | |
| | | | C | 2S | Q | 1G175 | | | ● | | |
| | | | | 3S | Q | 1G374 | | | ● | | |
| | | S | B | 2S | B | 2G74 | | | ● | | |
| | | D | | 2S | Q | 2G79 | | | ● | ● | |
| | | D | | 2S | \bar{Q} | 2G80 | | | ● | ● | |
| | | | | | | | | | ● | ● | |

Explanatory notes [Trigger] POS: POSITIVE EDGE, NEG: NEGATIVE EDGE

[PRE-CLR] B: Preset and Clear, C: Clear only

[Edge] S: Single Edge Triggered, D: Dual Edge Triggered

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q · \bar{Q}] B: Q · \bar{Q} -Output Q: Q-Output \bar{Q} : \bar{Q} -Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC DATA SELECTOR/MULTIPLEXER

| No. of Input/Output | Output | Circuit | Device | Technology | | | | |
|---------------------|--------|---------|--------|---------------|------|------------------|-----|----------------|
| | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | AHC | AHCT | LVC | AUC | AUP |
| 1/2 | 3S | 1 | 1G18 | | | ● | | |
| 2/1 | 2S | 1 | 2G157 | | | ● | | |

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC MONOSTABLE MULTIVIBRATOR

| Circuit | CLR | Retrigger | Device | Technology | | | | |
|---------|-----|-----------|--------|---------------|------|------------------|-----|----------------|
| | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | AHC | AHCT | LVC | AUC | AUP |
| 1 | C | 1 | 1G123 | | | ● | | |

Explanatory notes [CLR] C: With Clear

[Retrigger] R: With Retrigger

LITTLE LOGIC DECODER/DEMULTIPLEXER

| No. of Input/Output | Output | Circuit | Type | Technology | | | | |
|---------------------|--------|---------|-------|---------------|------|------------------|-----|----------------|
| | | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | | AHC | AHCT | LVC | AUC | AUP |
| 1/1 | 2S | 1 | 1G19 | | | ● | ● | |
| 2/3 | 2S | 1 | 1G29 | | | ● | | |
| 2/4 | 2S | 1 | 1G139 | | | ● | | |

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC ANALOG SWITCH

| Description | Type | Technology | | | | |
|---------------------------------------|--------|---------------|------|------------------|-----|----------------|
| | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | AHC | AHCT | LVC | AUC | AUP |
| DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER | 1G3157 | | | ● | | |
| DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER | 2G53 | | | ● | ● | |
| SINGLE BILATERAL ANALOG SWITCH | 1G66 | | | ● | ● | |
| DUAL BILATERAL ANALOG SWITCH | 2G66 | | | ● | ● | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC MULTIFUNCTION GATE

| Description | Input | Type | Technology | | | | |
|--|-------|------|---------------|------|------------------|-----|----------------|
| | | | Advanced CMOS | | Low-Voltage CMOS | | Low-Power CMOS |
| | | | AHC | AHCT | LVC | AUC | AUP |
| CONFIGURABLE MULTI-FUNCTION GATE AND gate/ AND with both inputs inverted NAND with inverted input OR with inverted input NOR gate / NOR with both inputs inverted XNOR | 3 | 1G57 | | | ● | | ● |
| CONFIGURABLE MULTI-FUNCTION GATE AND with inverted input NAND gate, NAND with both inputs inverted OR gate / OR with both inputs inverted NOR with inverted input XOR gate | 3 | 1G58 | | | ● | | ● |
| CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector AND gate OR gate with one inverted input NAND gate with one inverted input AND gate with one inverted input NOR gate with one inverted input OR gate Inverter Noninverted buffer | 3 | 1G97 | | | ● | | ● |
| CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector with inverted output NAND gate NOR gate with one inverted input AND gate with one inverted input NAND gate with one inverted input OR gate with one inverted input NOR gate Noninverted buffer Inverter | 3 | 1G98 | | | ● | | ● |
| ULTRA-CONFIGURABLE MULTI-FUNCTION GATE PRIMARY FUNCTION 3-state buffer 3-state inverter 3-state 2-in-1 data selector MUX 3-state 2-in-1 data selector MUX, inverted out 3-state 2-input AND 3-state 2-input AND, one input inverted 3-state 2-input AND, both inputs inverted 3-state 2-input NAND 3-state 2-input NAND, one input inverted 3-state 2-input NAND, both inputs inverted 3-state 2-input XOR 3-state 2-input XNOR COMPLEMENTARY FUNCTION 3-state 2-input NOR 3-state 2-input NOR, one input inverted 3-state 2-input NOR, both inputs inverted 3-state 2-input OR 3-state 2-input OR, one input inverted 3-state 2-input OR, both inputs inverted 3-state 2-input XOR, one input inverted | 4 | 1G99 | | | ● | | ● |

Status ●: Product available in technology indicated *: New product planned in technology indicated

PIN ASSIGNMENTS

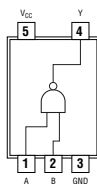
1G / 2G / 3G

Pin Assignments

1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

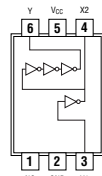
$$Y = \overline{A \cdot B}$$



See page 91

1GX04

CRYSTAL OSCILLATOR DRIVER



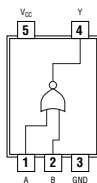
NC-No internal connection

See page 93

1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

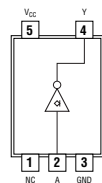
$$Y = \overline{A + B}$$



See page 91

1G06

SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT



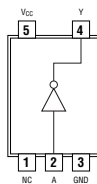
NC-No internal connection

See page 94

1G04

SINGLE INVERTER GATE

$$Y = \overline{A}$$

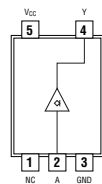


NC-No internal connection

See page 92

1G07

SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT



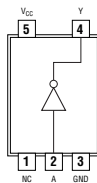
NC-No internal connection

See page 94

1GU04

SINGLE INVERTER

$$Y = \overline{A}$$



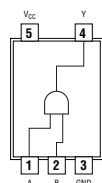
NC-No internal connection

See page 92

1G08

SINGLE 2-INPUT POSITIVE-AND GATE

$$Y = A \cdot B$$



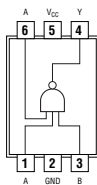
See page 95

Pin Assignments

1G10

SINGLE 3-INPUT POSITIVE-NAND GATE

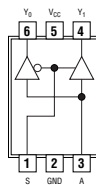
$$Y = \overline{A \cdot B \cdot C}$$



See page 95

1G18

1-OF-2 NONINVERTING DEMULTIPLEXER
WITH 3-STATE DESELECTED OUTPUT

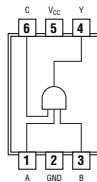


See page 97

1G11

SINGLE 3-INPUT POSITIVE-AND GATE

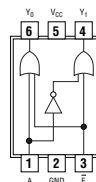
$$Y = A \cdot B \cdot C$$



See page 96

1G19

1-OF-2 DECODER/DEMULTIPLEXER

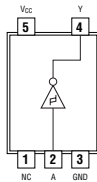


See page 98

1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

$$Y = \overline{A}$$



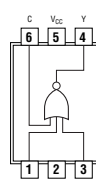
NC-No internal connection

See page 96

1G27

3-INPUT POSITIVE-NOR GATE

$$Y = \overline{A + B + C}$$

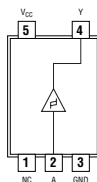


See page 98

1G17

SINGLE SCHMITT-TRIGGER BUFFER

$$Y = A$$

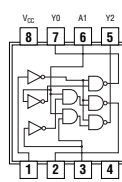


NC-No internal connection

See page 97

1G29

2-OF-3 DECODER/DEMULTIPLEXER



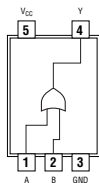
See page 99

Pin Assignments

1G32

SINGLE 2-INPUT POSITIVE-OR GATE

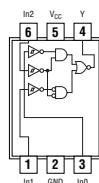
$$Y = A + B$$



See page 100

1G58

CONFIGURABLE MULTIFUNCTION GATE

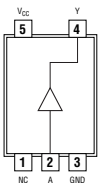


See page 102

1G34

SINGLE BUFFER GATE

$$Y = A$$

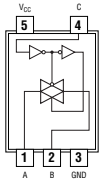


See page 100

NC-No internal connection

1G66

SINGLE BILATERAL ANALOG SWITCH

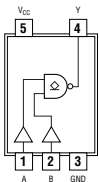


See page 102

1G38

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

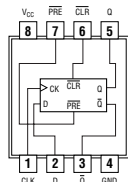
$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A + B}$$



See page 101

1G74

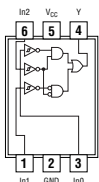
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



See page 103

1G57

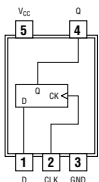
CONFIGURABLE MULTIFUNCTION GATE



See page 101

1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

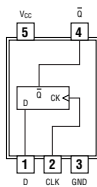


See page 104

Pin Assignments

1G80

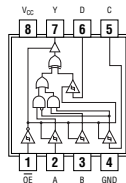
SINGLE POSITIVE-EDGE-TRIGGERED
D-TYPE FLIP-FLOP



See page 105

1G99

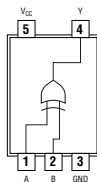
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR
WITH SCHMITT-TRIGGER INPUTS



See page 108

1G86

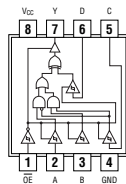
SINGLE 2-INPUT EXCLUSIVE-OR GATE
 $Y = A \oplus B$



See page 106

1G123

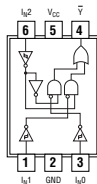
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR
WITH SCHMITT-TRIGGER INPUTS



See page 109

1G97

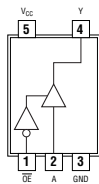
CONFIGURABLE MULTIPLE-FUNCTION GATE



See page 106

1G125

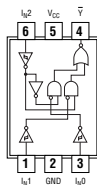
SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT
 $Y = A$



See page 110

1G98

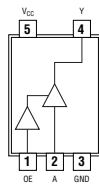
CONFIGURABLE MULTIPLE-FUNCTION GATE



See page 107

1G126

SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT
 $Y = A$



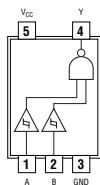
See page 110

Pin Assignments

1G132

SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A + B}$$

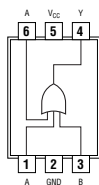


See page 111

1G332

SINGLE 3-INPUT POSITIVE-OR GATE

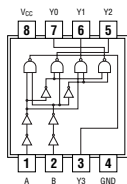
$$Y = A + B + C$$



See page 114

1G139

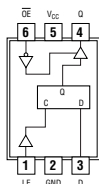
2-TO-4 LINE DECODER



See page 112

1G373

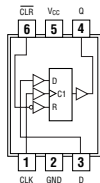
SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT



See page 115

1G175

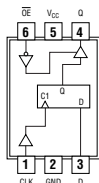
SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR



See page 113

1G374

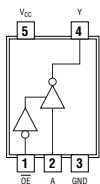
SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT



See page 116

1G240

SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

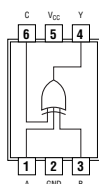


See page 114

1G386

SINGLE 3-INPUT EXCLUSIVE-XOR GATE

$$Y = A \oplus B \oplus C$$



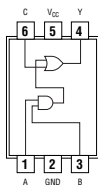
See page 117

Pin Assignments

1G0832

SINGLE 3-INPUT POSITIVE AND-OR GATE

$$Y = (A \cdot B) + C$$

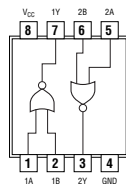


See page 117

2G02

DUAL 2-INPUT POSITIVE-NOR GATE

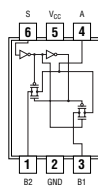
$$Y = \overline{A + B}$$



See page 120

1G3157

SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

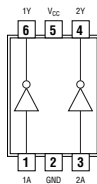


See page 118

2G04

DUAL INVERTER GATE

$$Y = \overline{A}$$

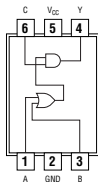


See page 121

1G3208

SINGLE 3-INPUT POSITIVE OR-AND GATE

$$Y = (A + B) \cdot C$$

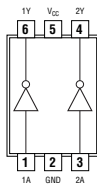


See page 119

2GU04

DUAL INVERTER GATE

$$Y = \overline{A}$$

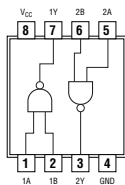


See page 121

2G00

DUAL 2-INPUT POSITIVE-NAND GATE

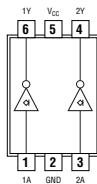
$$Y = A \cdot B$$



See page 120

2G06

DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

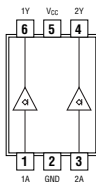


See page 122

Pin Assignments

2G07

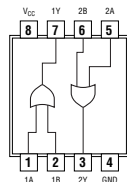
DUAL BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 122

2G32

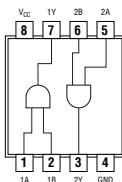
DUAL 2-INPUT POSITIVE-OR GATE
 $Y = A + B$



See page 124

2G08

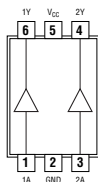
DUAL 2-INPUT POSITIVE-AND GATE
 $Y = A \cdot B$



See page 123

2G34

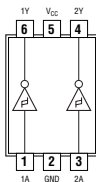
DUAL INVERTER GATE
 $Y = \bar{A}$



See page 125

2G14

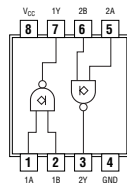
DUAL INVERTER GATE
 $Y = \bar{A}$



See page 123

2G38

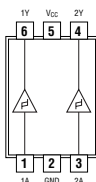
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT
 $Y = \overline{A \cdot B}$ or $Y = \bar{A} + \bar{B}$



See page 125

2G17

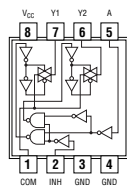
DUAL SCHMITT-TRIGGER BUFFER
 $Y = A$



See page 124

2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR
2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

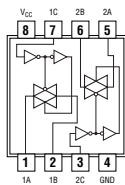


See page 126

Pin Assignments

2G66

DUAL BILATERAL ANALOG SWITCH

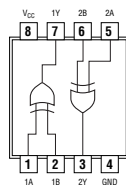


See page 126

2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

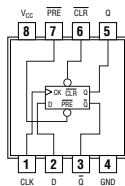
$$Y = A \oplus B$$



See page 130

2G74

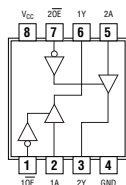
SINGLE POSITIVE-EDGE-TRIGGERED
D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



See page 127

2G125

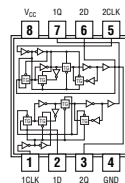
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 130

2G79

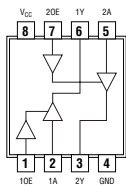
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



See page 128

2G126

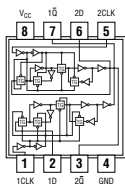
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 131

2G80

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

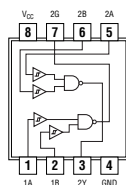


See page 129

2G132

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

$$Y = A \cdot B \text{ or } Y = \overline{A + B}$$

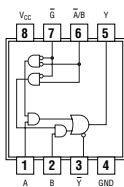


See page 131

Pin Assignments

2G157

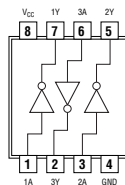
SINGLE 2-LINE TO 1-LINE DATA
SELECTOR/MULTIPLEXER



See page 132

3GU04

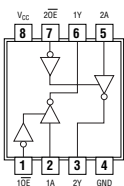
TRIPLE INVERTER GATE
 $Y = \bar{A}$



See page 134

2G240

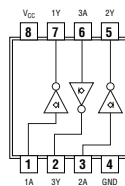
DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 133

3G06

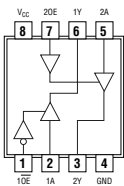
TRIPLE INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 135

2G241

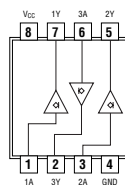
DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



See page 133

3G07

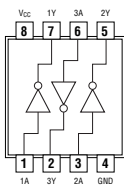
TRIPLE BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 135

3G04

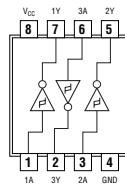
TRIPLE INVERTER GATE
 $Y = A$



See page 134

3G14

TRIPLE SCHMITT-TRIGGER INVERTER
 $Y = A$



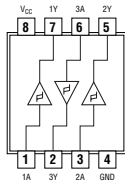
See page 136

Pin Assignments

3G17

TRIPLE SCHMITT-TRIGGER BUFFER

$Y = A$

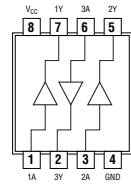


See page 136

3G34

TRIPLE BUFFER GATE

$Y = A$



See page 137

**FUNCTION
AND
ELECTRICAL
CHARACTERISTICS**

1G / 2G / 3G

1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|--------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 8.5 | 9 | 4 | 4.7 | 5.5 | 9 | 2 | 2.2 | 5.2 | 6.8 | 9.8 | 18.8 |
| t _{PHL} | | | | 8.5 | 9 | 4 | 4.7 | 5.5 | 9 | 2 | 2.2 | 5.2 | 6.8 | 9.8 | 18.8 |

UNIT:ns

1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

$$\bullet Y = \overline{A + B}$$

Logic Diagram (positive logic)



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|--------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 8.5 | 9 | 4 | 4.5 | 5.5 | 8 | 2.1 | 2.4 | 5 | 6.5 | 9.5 | 17.9 |
| t _{PHL} | | | | 8.5 | 9 | 4 | 4.5 | 5.5 | 8 | 2.1 | 2.4 | 5 | 6.5 | 9.5 | 17.9 |

UNIT:ns

1G04

SINGLE INVERTER GATE

$$\bullet Y = \bar{A}$$

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------|-------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 8.5 | 8.5 | 3.7 | 4.2 | 5.2 | 7.5 | 1.9 | 2.2 | 4.5 | 5.6 | 7.9 | 15 |
| t_{PHL} | | | | 8.5 | 8.5 | 3.7 | 4.2 | 5.2 | 7.5 | 1.9 | 2.2 | 4.5 | 5.6 | 7.9 | 15 |

UNIT:ns

1GU04

SINGLE INVERTER GATE

$$\bullet Y = \bar{A}$$

● Unbuffered Output

● Supply Voltage Range : 2V to 5.5V

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -8 | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 8 | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

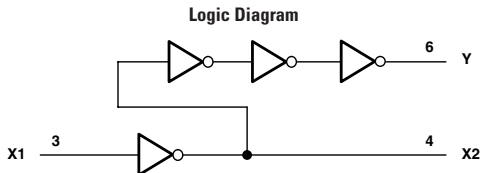
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 8 | 3 | 3.7 | 4 | 5 | 2.1 | 2.4 |
| t_{PHL} | | | | 8 | 3 | 3.7 | 4 | 5 | 2.1 | 2.4 |

UNIT:ns

1GX04

CRYSTAL OSCILLATOR DRIVER

- One Unbuffered Inverter (1GU04)
- One Buffered Inverter (1G04)
- Suitable for Commonly Used Clock Frequencies
- Optimized for Use in Crystal Oscillator Applications



FUNCTION TABLE

| OUTPUT X1 | INPUTS | |
|--------------|--------|---|
| | X2 | Y |
| H | L | H |
| L | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------------|------------|-----------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t _{PLH} | X1 | X2 | MAX | 3 | 3.7 | 4 | 7 |
| | | | | 3 | 3.7 | 4 | 7 |
| t _{PHL} | X1 | Y* | MAX | 5 | 7.8 | 7.4 | 18 |
| | | | | 5 | 7.8 | 7.4 | 18 |

UNIT : ns

*X2 : no external load

1G06

SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| V _O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | 3.6 | 3.6 | 3.6 | 3.6 | V |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 3 | 4 | 4 | 6.5 | 1.8 | 2.5 | 4.9 | 4.5 | 6.7 | 14.1 |
| t _{PHL} | | | | 3 | 4 | 4 | 6.5 | 1.8 | 2.5 | 4.9 | 4.5 | 6.7 | 14.1 |

UNIT:ns

1G07

SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | 3.6 | 3.6 | 3.6 | 3.6 | V |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 3.5 | 4.2 | 5.5 | 8.3 | 1.8 | 2.5 | 4.5 | 4.8 | 7.1 | 16.2 |
| t _{PHL} | | | | 3.5 | 4.2 | 5.5 | 8.3 | 1.8 | 2.5 | 4.5 | 4.8 | 7.1 | 16.2 |

UNIT:ns

1G08

SINGLE 2-INPUT POSITIVE-AND GATE

$$\bullet Y = A \cdot B$$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|--|--------|
| A | B | | Y |
| H | H | | H |
| L | X | | L |
| X | L | | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | | |
|------------------|--------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|---|------|
| t _{PLH} | A or B | Y | MAX | | | 9 | 9 | 4 | 4.5 | 5.5 | 8 | 2 | 2.4 | 4.7 | 6.1 | 9 | 17.2 |
| t _{PHL} | | | | | | 9 | 9 | 4 | 4.5 | 5.5 | 8 | 2 | 2.4 | 4.7 | 6.1 | 9 | 17.2 |

UNIT:ns

1G10

SINGLE 3-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{A \cdot B \cdot C}$$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-----------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A, B or C | Y | MAX | 3.6 | 5.0 | 6.5 | 18.0 | TBD | TBD |
| t _{PHL} | | | | 3.6 | 5.0 | 6.5 | 18.0 | TBD | TBD |

UNIT:ns

1G11

SINGLE 3-INPUT POSITIVE-AND GATE

$$Y = A \cdot B \cdot C$$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-----------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A, B or C | Y | MAX | 3.5 | 4.9 | 6.2 | 17.2 | TBD | TBD |
| t _{PHL} | | | | 3.5 | 4.9 | 6.2 | 17.2 | TBD | TBD |

UNIT:ns

1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

$$Y = \bar{A}$$

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 12 | 9 | 5 | 5.5 | 6.5 | 11 | 2.5 | 2.5 | 5.6 | 6.8 | 9.5 | 16.7 |
| t _{PHL} | | | | 12 | 9 | 5 | 5.5 | 6.5 | 11 | 2.5 | 2.5 | 5.6 | 6.8 | 9.5 | 16.7 |

UNIT:ns

1G17

SINGLE SCHMITT-TRIGGER BUFFER

● Y = A

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 5 | 5.5 | 6.5 | 11 | 2.5 | 2.4 | 5.7 | 6.8 | 9 | 15.6 |
| t _{PHL} | | | | 5 | 5.5 | 6.5 | 11 | 2.5 | 2.4 | 5.7 | 6.8 | 9 | 15.6 |

UNIT:ns

Logic Diagram

5pin Package



4pin Package



1G18

1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE DESELECTED OUTPUT

FUNCTION TABLE

| INPUTS | | OUTPUTS | |
|--------|---|----------------|----------------|
| S | A | Y ₀ | Y ₁ |
| L | L | L | Z |
| L | H | H | Z |
| H | L | Z | L |
| H | H | Z | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

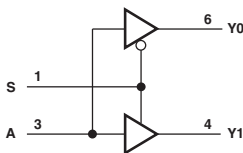
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|-------|--------|------------|--------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 3.2 | 4.2 | 5 | 9.3 |
| t _{PHL} | | | | 3.2 | 4.2 | 5 | 9.3 |
| t _{PZL} | S | Y | MAX | 3.4 | 4.6 | 5.6 | 10.2 |
| t _{PZH} | | | | 3.4 | 4.6 | 5.6 | 10.2 |
| t _{PLZ} | S | Y | MAX | 3.3 | 4.9 | 5.3 | 12.7 |
| t _{PHZ} | | | | 3.3 | 4.9 | 5.3 | 12.7 |

UNIT:ns

Logic Diagram



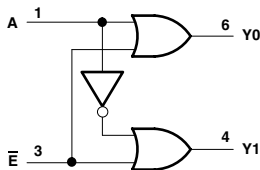
1G19

1-OF-2 DECODER/DEMULTIPLEXER

FUNCTION TABLE

| INPUTS | | OUTPUTS | |
|-----------|---|----------------|----------------|
| \bar{E} | A | Y ₀ | Y ₁ |
| L | L | L | H |
| L | H | H | L |
| H | X | H | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT | AUC 2.5V | AUC 1.8V |
|-----------------|------------|--------|----------|----------|----------|------|----------|----------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA | 0.01 | 0.01 |
| I _{DH} | MAX | -32 | -24 | -8 | -4 | mA | -9 | -8 |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA | 9 | 8 |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|----------------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A or \bar{E} | Y | MAX | 3.9 | 5.2 | 6.5 | 16.1 | 2.0 | 2.8 |
| t _{PHL} | | | | 3.9 | 5.2 | 6.5 | 16.1 | 2.0 | 2.8 |

UNIT:ns

1G27

SINGLE 3-INPUT POSITIVE-NOR GATE

● $Y = \overline{A + B + C}$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

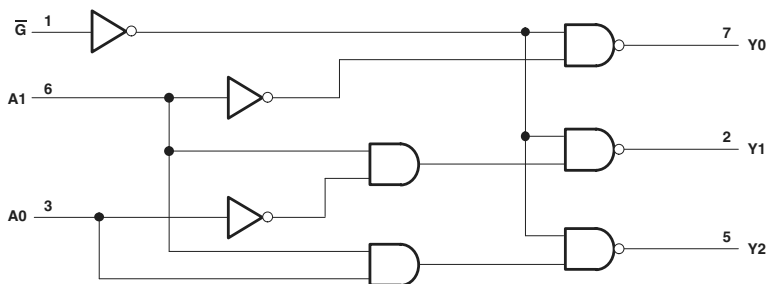
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{DH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|-----------|--------|------------|--------|----------|----------|----------|
| t _{PLH} | A, B or C | Y | MAX | 3.6 | 5.4 | 7.1 | 20.5 |
| t _{PHL} | | | | 3.6 | 5.4 | 7.1 | 20.5 |

UNIT:ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUTS | | |
|-----------|----|----|---------|----|----|
| \bar{G} | A1 | A0 | Y0 | Y1 | Y2 |
| L | L | X | L | H | H |
| L | H | L | H | L | H |
| L | H | H | H | H | L |
| H | X | X | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|----------------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A or \bar{G} | Y | MAX | 5.1 | 6.1 | 7.5 | 15.8 |
| t_{PHL} | | | | 5.1 | 6.1 | 7.5 | 15.8 |

UNIT : ns

1G32

SINGLE 2-INPUT POSITIVE-OR GATE

● $Y = A + B$

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| H | L | L |
| L | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUC 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------|--------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 8.5 | 9 | 4 | 4.5 | 5.5 | 8 | 2.1 | 2.4 | 5 | 6.6 | 9.6 | 18.4 |
| t_{PHL} | | | | 8.5 | 9 | 4 | 4.5 | 5.5 | 8 | 2.1 | 2.4 | 5 | 6.6 | 9.6 | 18.4 |

UNIT: ns

1G34

SINGLE BUFFER GATE

● $Y = A$

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.001 | 0.001 | 0.001 | 0.001 | 0.009 | 0.009 | 0.009 | 0.009 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 3.2 | 4.1 | 4.4 | 8.6 | 4.8 | 5.8 | 8.3 | 15.4 |
| t_{PHL} | | | | 3.2 | 4.1 | 4.4 | 8.6 | 4.8 | 5.8 | 8.3 | 15.4 |

UNIT : ns

1G38

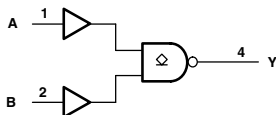
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

● $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | UNIT |
|-----------------|------------|-----------------------|-------------------------|-------------------------|-------------------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V _O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V |
|------------------|--------|--------|------------|-----------------------|-------------------------|-------------------------|-------------------------|
| t _{PLH} | A or B | Y | MAX | 3.9 | 4.5 | 6 | 10 |
| t _{PHL} | | | | 3.9 | 4.5 | 6 | 10 |

UNIT: ns

1G57

CONFIGURABLE MULTIPLE-FUNCTION GATE

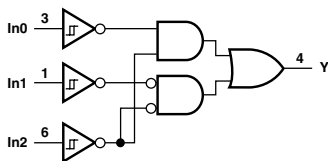
FUNCTION SELECTION TABLE

| |
|---------------------------------------|
| 2-input AND |
| 2-input AND with both inputs inverted |
| 2-input NAND with inverted input |
| 2-input OR with inverted input |
| 2-input NOR |
| 2-input NOR with both inputs inverted |
| 2-input XNOR |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|-----|--------|
| In2 | In1 | In0 | Y |
| L | L | L | H |
| L | L | H | L |
| L | H | L | H |
| L | H | H | L |
| H | L | L | L |
| H | L | H | L |
| H | H | L | H |
| H | H | H | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | A _{UP} 3.3V | A _{UP} 2.5V | A _{UP} 1.8V | A _{UP} 1.1V | UNIT |
|-----------------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | A _{UP} 3.3V | A _{UP} 2.5V | A _{UP} 1.8V | A _{UP} 1.1V |
|------------------|--------|--------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| t _{PLH} | Any In | Y | MAX | 5.1 | 6.3 | 8.3 | 14.4 | 6.1 | 7.3 | 10 | 18.1 |
| t _{PHL} | | | | 5.1 | 6.3 | 8.3 | 14.4 | 6.1 | 7.3 | 10 | 18.1 |

UNIT: ns

1G58

CONFIGURABLE MULTIPLE-FUNCTION GATE

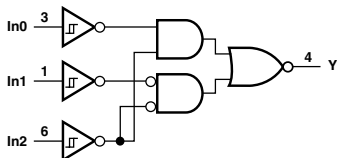
FUNCTION SELECTION TABLE

| |
|--|
| 2-input AND with inverted input |
| 2-input NAND |
| 2-input NAND with both inputs inverted |
| 2-input OR |
| 2-input OR with both inputs inverted |
| 2-input NOR with inverted input |
| 2-input XOR |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|-----|--------|
| In2 | In1 | In0 | Y |
| L | L | L | L |
| L | L | H | H |
| L | H | L | L |
| L | H | H | H |
| H | L | L | H |
| H | L | H | H |
| H | H | L | L |
| H | H | H | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|--------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | Any In | Y | MAX | 5.1 | 6.3 | 8.3 | 14.4 | 6.3 | 7.6 | 10.2 | 19 |
| t _{PHL} | | | | 5.1 | 6.3 | 8.3 | 14.4 | 6.3 | 7.6 | 10.2 | 19 |

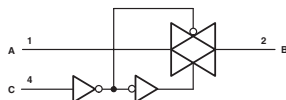
UNIT:ns

1G66

SINGLE BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | OFF |
| H | ON |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

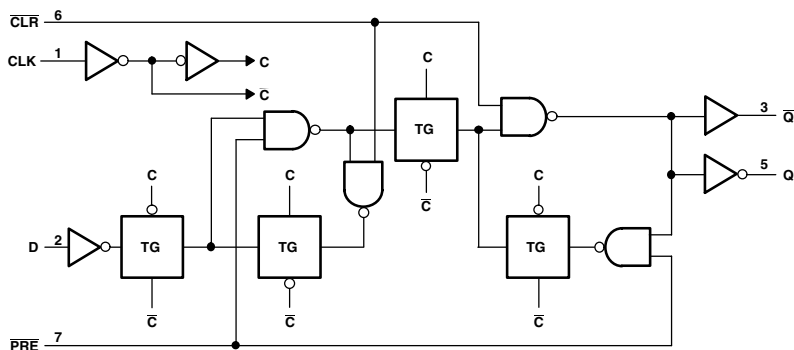
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|--------------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| R _{ON} | MAX | 10 | 15 | 20 | 30 | 15 | 20 | Ω |
| R _{ON(P)} | MAX | 15 | 20 | 30 | 120 | 20 | 80 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A or B | B or A | MAX | 0.6 | 0.8 | 1.2 | 2 | 0.3 | 0.3 |
| t _{PHL} | | | | 0.6 | 0.8 | 1.2 | 2 | 0.3 | 0.3 |
| t _{PZH} | C | B or A | MAX | 4.2 | 5 | 6.5 | 12 | 1.4 | 2.3 |
| t _{PZL} | | | | 4.2 | 5 | 6.5 | 12 | 1.4 | 2.3 |
| t _{PHZ} | C | B or A | MAX | 5 | 6.5 | 6.9 | 10 | 1.5 | 2.9 |
| t _{PLZ} | | | | 5 | 6.5 | 6.9 | 10 | 1.5 | 2.9 |

UNIT : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-----|-----|---|---------|-------------|
| PRE | CLR | CLK | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| X | L | X | X | L | H |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q_0 | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

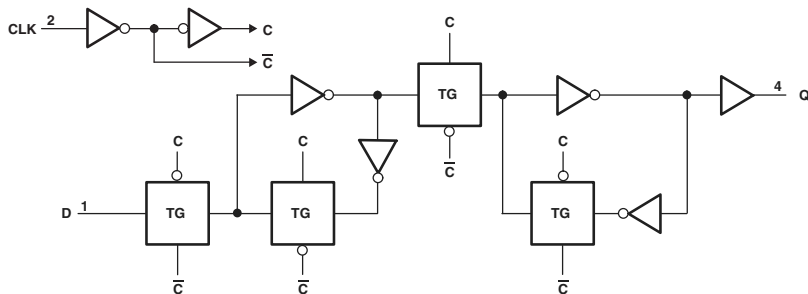
| PARAMETER | MAX or MIN | TEMPERATURE RANGE | | | | | | UNIT |
|-----------|------------|-------------------|----------|----------|----------|----------|----------|------|
| | | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | |
| I_{CC} | MAX | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TEMPERATURE RANGE | | | | | | |
|-----------|--------------------------------------|--------------------------------------|------------|-------------------|----------|----------|----------|----------|----------|-----|
| | | | | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | |
| t_{max} | | | MIN | 275 | 250 | 160 | 130 | 60 | 50 | |
| t_w | Pulse duration | CLK | MIN | 1 | 1 | 2 | 2 | 2 | 2 | |
| | | \overline{PRE} or \overline{CLR} | low | MIN | 1 | 1 | 2 | 2 | 2 | |
| t_{su} | Setup time, before CLK ↑ | Data | high | MIN | 0.4 | 0.5 | 0.5 | 0.5 | 1 | 1.3 |
| | | | low | MIN | 0.4 | 0.5 | 1 | 1 | 1 | 1.2 |
| | | \overline{PRE} or \overline{CLR} | inactive | MIN | 0.4 | 0.7 | 0.5 | 0.5 | 0.5 | 0.5 |
| t_h | Hold time, data after CLK ↑ | | MIN | 0.3 | 0.3 | 0 | 0 | 0 | 0 | |
| t_{PLH} | CLK | Q | MAX | 1.8 | 2.4 | 5.3 | 7 | 10.4 | 21.8 | |
| t_{PHL} | | | | 1.8 | 2.4 | 5.3 | 7 | 10.4 | 21.8 | |
| t_{PLH} | CLK | \bar{Q} | MAX | 1.8 | 2.4 | 5.2 | 6.7 | 9.9 | 20.3 | |
| t_{PHL} | | | | 1.8 | 2.4 | 5.2 | 6.7 | 9.9 | 20.3 | |
| t_{PLH} | \overline{PRE} or \overline{CLR} | Q or \bar{Q} | MAX | 2.1 | 2.8 | 5.8 | 7.4 | 10.8 | 21.4 | |
| t_{PHL} | | | | 2.1 | 2.8 | 5.8 | 7.4 | 10.8 | 21.4 | |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|----------------|
| CLK | D | Q |
| ↑ | H | H |
| ↑ | L | L |
| L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

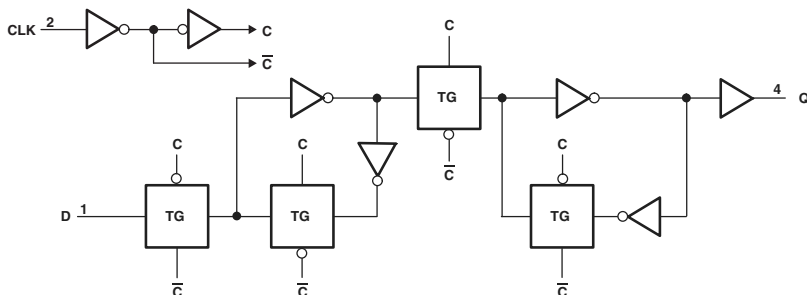
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------------------------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| f _{max} | | | MIN | 160 | 160 | 160 | 160 | 275 | 250 | 260 | 250 | 240 | 160 |
| t _w | CLK high or low | | MIN | 2.5 | 2.5 | 2.5 | 2.5 | 1.7 | 1.7 | 1.9 | 1.7 | 1.6 | 2.2 |
| t _{su} | Before CLK ↑, Data high | | MIN | 1.2 | 1.3 | 1.4 | 2.2 | 0.7 | 0.5 | 0.6 | 0.7 | 0.9 | 1.4 |
| | | | | 1.2 | 1.3 | 1.4 | 2.6 | 0.7 | 0.5 | 1 | 1 | 1.1 | 1.8 |
| t _h | Data after CLK ↑ | | MIN | 0.5 | 1.0 | 0.4 | 0.3 | 0.1 | 0 | 0 | 0 | 0 | 0 |
| t _{PHL} | CLK | Q | MAX | 4.5 | 5 | 7 | 9.9 | 1.8 | 2.4 | 4.5 | 5.7 | 8 | 14.4 |
| t _{PHL} | | | | 4.5 | 5 | 7 | 9.9 | 1.8 | 2.4 | 4.5 | 5.7 | 8 | 14.4 |

UNIT f_{max}: MHz other: ns

1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|----------------|
| CLK | D | Q |
| ↑ | H | L |
| ↑ | L | H |
| L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------------------------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| f _{max} | | | MIN | 160 | 160 | 160 | 160 | 275 | 250 | 260 | 250 | 240 | 170 |
| t _w | CLK high or low | | MIN | 2.5 | 2.5 | 2.5 | 2.5 | 1.7 | 1.7 | 1.9 | 1.7 | 1.6 | 2.5 |
| t _{su} | Before CLK ↑, Data high | | MIN | 1.1 | 1.3 | 1.5 | 2.3 | 0.5 | 0.6 | 0.4 | 0.6 | 0.8 | 1.2 |
| | | | | 1.1 | 1.3 | 1.5 | 2.5 | 0.5 | 0.6 | 0.7 | 0.8 | 1.1 | 2 |
| t _h | Data after CLK ↑ | | MIN | 0.4 | 0.9 | 0.2 | 0 | 0.1 | 0.1 | 0 | 0 | 0 | 0 |
| τ _{PLH} | CLK | Q̄ | MAX | 4.5 | 5.2 | 7 | 9.9 | 1.8 | 2.4 | 4.9 | 6.3 | 7.3 | 17.7 |
| τ _{PHL} | | | | 4.5 | 5.2 | 7 | 9.9 | 1.8 | 2.4 | 4.9 | 6.3 | 7.3 | 17.7 |

UNIT f_{max}: MHz other: ns

1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

$$Y = A \oplus B$$

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

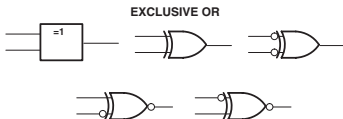
| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|------|------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------------|--------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|
| T _{PH} | A or B | Y | MAX | 10 | 9 | 4 | 5 | 5.5 | 9.9 | 2 | 2.6 |
| | | | | 10 | 9 | 4 | 5 | 5.5 | 9.9 | 2 | 2.6 |

UNIT:ns

Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

1G97

CONFIGURABLE MULTIPLE-FUNCTION GATE

FUNCTION SELECTION TABLE

| |
|---|
| 2-to-1 data selector |
| 2-input AND gate |
| 2-input OR gate with one inverted input |
| 2-input NAND gate with one inverted input |
| 2-input AND gate with one inverted input |
| 2-input NOR gate with one inverted input |
| 2-input OR gate |
| Inverter |
| Noninverted buffer |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|-----|--------|
| In2 | In1 | In0 | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

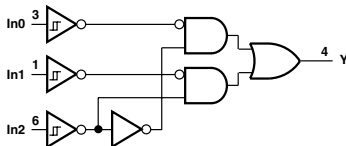
| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------------|--------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|
| T _{PH} | Any In | Y | MAX | 5.1 | 6.3 | 8.3 | 14.4 | 6.4 | 7.8 | 10.5 | 19.2 |
| | | | | 5.1 | 6.3 | 8.3 | 14.4 | 6.4 | 7.8 | 10.5 | 19.2 |

UNIT:ns

Logic Diagram



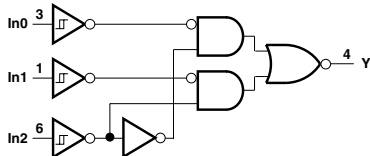
1G98

CONFIGURABLE MULTIPLE-FUNCTION GATE

FUNCTION SELECTION TABLE

| |
|---|
| 2-to-1 data selector with inverted output |
| 2-input NAND gate |
| 2-input NOR gate with one inverted input |
| 2-input AND gate with one inverted input |
| 2-input NAND gate with one inverted input |
| 2-input OR gate with one inverted input |
| 2-input NOR gate |
| Noninverted buffer |
| Inverter |

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|-----|--------|
| In2 | In1 | In0 | Y |
| L | L | L | H |
| L | L | H | H |
| L | H | L | L |
| L | H | H | L |
| H | L | L | H |
| H | L | H | L |
| H | H | L | H |
| H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

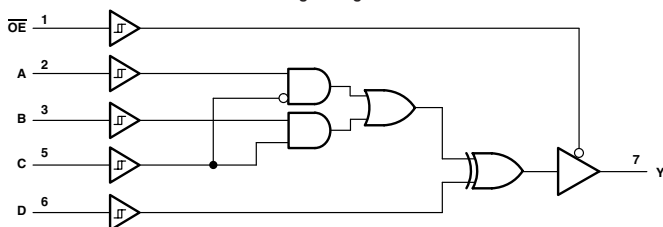
| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|--------|--------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------|-------------|-------------|-------------|
| t _{PLH} | Any In | Y | MAX | 5.1 | 6.3 | 8.3 | 14.4 | 6 | 7.3 | 10.2 | 19 |
| t _{PHL} | | | | 5.1 | 6.3 | 8.3 | 14.4 | 6 | 7.3 | 10.2 | 19 |

UNIT:ns

SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

- Offers Nine Different Logic Functions in a Single Package

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|--------|--------|--------|--------|--------|--------|
| OE | D | C | B | A | Y |
| L | L | L | L | L | L |
| L | L | L | L | H | H |
| L | L | L | H | L | L |
| L | L | L | H | H | H |
| L | L | H | L | L | L |
| L | L | H | L | H | L |
| L | L | H | H | L | H |
| L | L | H | H | H | H |
| L | H | L | L | L | H |
| L | H | L | L | H | L |
| L | H | L | H | L | H |
| L | H | L | H | H | L |
| L | H | H | L | L | H |
| L | H | H | L | H | H |
| L | H | H | H | L | L |
| L | H | H | H | H | H |
| H | H or L | H or L | H or L | H or L | Z |

PRIMARY FUNCTION

| |
|--|
| 3-state buffer |
| 3-state inverter |
| 3-state 2-in-1 data selector MUX |
| 3-state 2-in-1 data selector MUX, inverted out |
| 3-state 2-input AND |
| 3-state 2-input AND, one input inverted |
| 3-state 2-input AND, both inputs inverted |
| 3-state 2-input NAND |
| 3-state 2-input NAND, one input inverted |
| 3-state 2-input NAND, both inputs inverted |
| 3-state 2-input XOR |
| 3-state 2-input XNOR |

COMPLEMENTARY FUNCTION

| |
|---|
| 3-state 2-input NOR, both inputs inverted |
| 3-state 2-input NOR, one input inverted |
| 3-state 2-input NOR |
| 3-state 2-input OR, both inputs inverted |
| 3-state 2-input OR, one input inverted |
| 3-state 2-input OR |
| 3-state 2-input XOR, one input inverted |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{DH} | MAX | -32 | -24 | -8 | -4 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

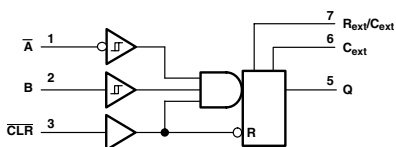
| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _{CC} 5V | V _{CC} 3.3V | V _{CC} 2.5V | V _{CC} 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|-----------------------|-------------------------|-------------------------|-------------------------|-------------|-------------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 5.5 | 8.4 | 11.7 | 30.8 | 8.4 | 10.5 | 14.5 | 29.8 |
| | | | | 5.5 | 8.4 | 11.7 | 30.8 | 8.4 | 10.5 | 14.5 | 29.8 |
| t _{PHL} | B | Y | MAX | 5.4 | 8.2 | 11.3 | 28.9 | 8.4 | 10.5 | 14.5 | 29.8 |
| | | | | 5.4 | 8.2 | 11.3 | 28.9 | 8.4 | 10.5 | 14.5 | 29.8 |
| t _{PLH} | C | Y | MAX | 5.7 | 8.6 | 12.3 | 29.8 | 8.4 | 10.5 | 14.5 | 29.8 |
| | | | | 5.7 | 8.6 | 12.3 | 29.8 | 8.4 | 10.5 | 14.5 | 29.8 |
| t _{PHL} | D | Y | MAX | 5.2 | 7.6 | 10.7 | 25.7 | 8.4 | 10.5 | 14.5 | 29.8 |
| | | | | 5.2 | 7.6 | 10.7 | 25.7 | 8.4 | 10.5 | 14.5 | 29.8 |
| t _{PZH} | OE | Y | MAX | 4.7 | 7 | 11.3 | 25.2 | 8.2 | 9.9 | 14.8 | 29.3 |
| | | | | 4.7 | 7 | 11.3 | 25.2 | 8.2 | 9.9 | 14.8 | 29.3 |
| t _{PHZ} | OE | Y | MAX | 4.5 | 5.6 | 5.8 | 15 | 5.8 | 5.5 | 7.9 | 10 |
| | | | | 4.5 | 5.6 | 5.8 | 15 | 5.8 | 5.5 | 7.9 | 10 |

UNIT: ns

SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

- Schmitt-Triggered Circuitry on \bar{A} and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Outputs Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs

Logic Diagram

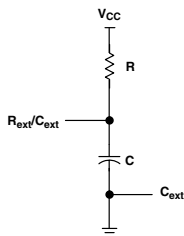


FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----------|---|------------------|
| CLR | \bar{A} | B | Q |
| L | X | X | L |
| X | H | X | L ⁽¹⁾ |
| X | X | L | L ⁽¹⁾ |
| H | L | ↑ | ⌋⌋ |
| H | ↓ | H | ⌋⌋ |
| ↑ | L | H | ⌋⌋ |

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

REQUIRED TIMING CIRCUIT



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------------|--------------|------------|--------|----------|----------|----------|------|
| I _{CC} | Quiescent | MAX | 0.01 | - | - | - | mA |
| I _{CC} | Active State | MAX | 0.975 | 0.65 | 0.28 | 0.22 | mA |
| I _{QH} | | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | | MAX | 32 | 24 | 8 | 4 | mA |

TIMING REQUIREMENTS

| PARAMETER | | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|------------------------|------------|--------|----------|----------|----------|
| t _{wIN} | CLR | MAX | 2.5 | 3 | 4 | 8 |
| | \bar{A} or B trigger | MAX | 2.5 | 3 | 4 | 8 |

UNIT : ns

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|----------------|--------|------------|--------|----------|----------|----------|
| t _{PLH} | \bar{A} or B | Q | MAX | 8.2 | 12.5 | 18.5 | 57 |
| t _{PHL} | | | | 8.2 | 12.5 | 18.5 | 57 |
| t _{PLH} | CLR | Q | MAX | 6 | 8.6 | 12.5 | 36.5 |
| t _{PHL} | | | | 6 | 8.6 | 12.5 | 36.5 |
| t _{PLH} | CLR trigger | Q | MAX | 7.5 | 11.5 | 17 | 59 |
| t _{PHL} | | | | 7.5 | 11.5 | 17 | 59 |

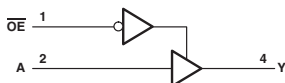
UNIT : ns

1G125

Logic Diagram

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

$$\bullet Y = A$$



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------|-----------------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 8.5 | 8.5 | 4 | 4.5 | 5.5 | 9 | 1.7 | 2.5 | 5.2 | 6.4 | 9.1 | 16.6 |
| t_{PHL} | | | | 8.5 | 8.5 | 4 | 4.5 | 5.5 | 9 | 1.7 | 2.5 | 5.2 | 6.4 | 9.1 | 16.6 |
| t_{PZH} | \overline{OE} | Y | MAX | 8 | 8 | 5 | 5.3 | 6.6 | 10.1 | 1.9 | 2.6 | 6.4 | 7.8 | 11 | 20.2 |
| t_{PZL} | | | | 8 | 8 | 5 | 5.3 | 6.6 | 10.1 | 1.9 | 2.6 | 6.4 | 7.8 | 11 | 20.2 |
| t_{PHZ} | \overline{OE} | Y | MAX | 10 | 10 | 4.2 | 5 | 5 | 9.2 | 1.7 | 3.1 | 5.6 | 5.4 | 7.5 | 14 |
| t_{PLZ} | | | | 10 | 10 | 4.2 | 5 | 5 | 9.2 | 1.7 | 3.1 | 5.6 | 5.4 | 7.5 | 14 |

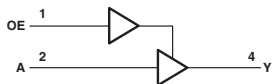
UNIT:ns

1G126

Logic Diagram

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

$$\bullet Y = A$$



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------|------------|------|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I_{OH} | MAX | -8 | -8 | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I_{OL} | MAX | 8 | 8 | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|-----------|-----------------|--------|------------|-----|------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 8.5 | 8.5 | 4 | 4.5 | 5.5 | 8 | 1.7 | 2.5 | 5.2 | 6.4 | 9.1 | 16.6 |
| t_{PHL} | | | | 8.5 | 8.5 | 4 | 4.5 | 5.5 | 8 | 1.7 | 2.5 | 5.2 | 6.4 | 9.1 | 16.6 |
| t_{PZH} | \overline{OE} | Y | MAX | 8 | 8 | 5 | 5.3 | 6.6 | 9.4 | 1.9 | 2.5 | 6.4 | 7.8 | 11 | 20.2 |
| t_{PZL} | | | | 8 | 8 | 5 | 5.3 | 6.6 | 9.4 | 1.9 | 2.5 | 6.4 | 7.8 | 11 | 20.2 |
| t_{PHZ} | \overline{OE} | Y | MAX | 10 | 10 | 4.2 | 5.5 | 5.5 | 9.8 | 2.1 | 3.1 | 5.6 | 5.4 | 7.5 | 14 |
| t_{PLZ} | | | | 10 | 10 | 4.2 | 5.5 | 5.5 | 9.8 | 2.1 | 3.1 | 5.6 | 5.4 | 7.5 | 14 |

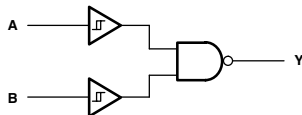
UNIT:ns

1G132

SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

● $Y = \overline{A \cdot B}$ or $Y = \overline{\overline{A} + \overline{B}}$

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

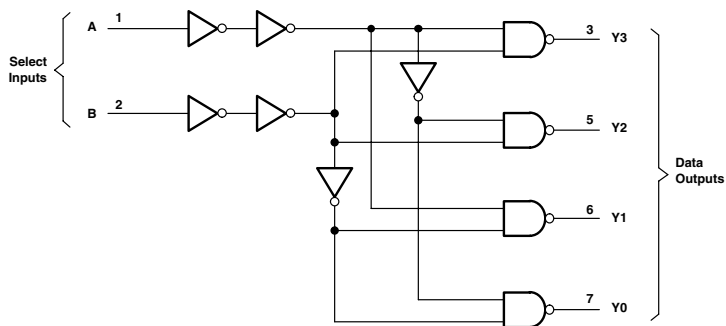
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|--------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A or B | Y | MAX | 5 | 6 | 7.5 | 16 |
| t_{PHL} | | | | 5 | 6 | 7.5 | 16 |

UNIT : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|--------|---|---------|----|----|----|
| B | A | Y0 | Y1 | Y2 | Y3 |
| L | L | L | H | H | H |
| L | H | H | L | H | H |
| H | L | H | H | L | H |
| H | H | H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

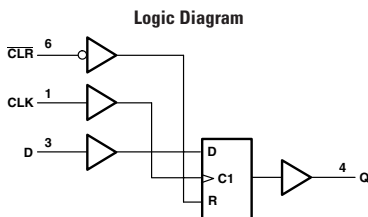
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|--------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A or B | Y | MAX | 4.2 | 5.9 | 8.2 | 16.7 |
| t_{PHL} | | | | 4.2 | 5.9 | 8.2 | 16.7 |

UNIT : ns

1G175

SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR

- Complementary Outputs (Q , \bar{Q})
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|--------|---|--------|
| CLR | CLK | D | Q |
| H | ↑ | L | L |
| H | ↑ | H | H |
| H | H or L | X | Q_0 |
| L | X | X | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

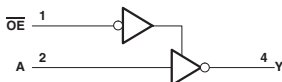
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------------------------------|--------------|-------------|------------|--------|----------|----------|----------|
| f_{max} | | | MIN | 175 | 150 | 125 | 100 |
| t_w Pulse duration | CLR | Low | MIN | 2.5 | 2.8 | 3 | 5.6 |
| | CLK | High or low | MIN | 2.5 | 2.8 | 3 | 3.5 |
| t_{su} Setup time, before CLK ↑ | Data | | MIN | 1.5 | 2 | 2.5 | 3 |
| | CLR inactive | | MIN | 0.5 | 0.5 | 0 | 0 |
| t_h Hold time, data after CLK ↑ | | | MIN | 0.5 | 0.5 | 0 | 0 |
| t_{PLH} | CLK | Q | MAX | 4 | 5.7 | 7.1 | 13.4 |
| t_{PHL} | | | | 4 | 5.7 | 7.1 | 13.4 |
| t_{PLH} | CLR | Q | MAX | 4.1 | 5.8 | 7 | 12.9 |
| t_{PHL} | | | | 4.1 | 5.8 | 7 | 12.9 |

UNIT f_{max} : MHz other: ns

1G240

SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.0009 | 0.0009 | 0.0009 | 0.0009 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | -4 | -3.1 | -1.9 | -1.1 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | 4 | 3.1 | 1.9 | 1.1 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | AUP 3.3V | AUP 2.5V | AUP 1.8V | AUP 1.1V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 4 | 4.5 | 5.5 | 8.6 | 1.7 | 2.5 | 5.2 | 6.3 | 9.1 | 17.3 |
| t _{PHL} | | | | 4 | 4.5 | 5.5 | 8.6 | 1.7 | 2.5 | 5.2 | 6.3 | 9.1 | 17.3 |
| t _{PZH} | OE | Y | MAX | 5.2 | 5.4 | 6.5 | 10.0 | 1.9 | 2.6 | 6.3 | 7.7 | 10.9 | 20.9 |
| t _{PZL} | | | | 5.2 | 5.4 | 6.5 | 10.0 | 1.9 | 2.6 | 6.3 | 7.7 | 10.9 | 20.9 |
| t _{PHZ} | OE | Y | MAX | 4.1 | 5.2 | 4.9 | 9.4 | 1.7 | 3.1 | 9.1 | 7.3 | 10.1 | 12.9 |
| t _{PLZ} | | | | 4.1 | 5.2 | 4.9 | 9.4 | 1.7 | 3.1 | 9.1 | 7.3 | 10.1 | 12.9 |

UNIT:ns

1G332

SINGLE 3-INPUT POSITIVE-OR GATE

Logic Diagram



● $Y = A + B + C$

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | X | X | H |
| X | H | X | H |
| X | X | H | H |
| L | L | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|-----------|--------|------------|--------|----------|----------|----------|
| t _{PLH} | A, B or C | Y | MAX | 3.5 | 4.8 | 6.2 | 17.2 |
| t _{PHL} | | | | 3.5 | 4.8 | 6.2 | 17.2 |

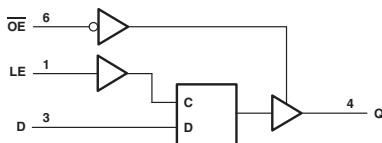
UNIT:ns

1G373

SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | L | L |
| L | H | H | H |
| L | L | X | Q _O |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|------------------------------|--------|------------|--------|----------|----------|----------|
| t _w | Pulse duration, LE high | | MIN | 3 | 3 | 3 | 3 |
| t _{su} | Setup time, data before LE ↓ | | MIN | 1.5 | 1.5 | 2 | 2.4 |
| t _h | Hold time, data after LE ↓ | | MIN | 1.5 | 1.5 | 1.5 | 2.5 |
| t _{PLH} | D | Q | MAX | 4 | 5.4 | 7.3 | 16 |
| t _{PHL} | | | | 4 | 5.4 | 7.3 | 16 |
| t _{PLH} | LE | Q | MAX | 4 | 5.5 | 7.4 | 16.3 |
| t _{PHL} | | | | 4 | 5.5 | 7.4 | 16.3 |
| t _{PZH} | OE | Q | MAX | 3.7 | 5.1 | 6.3 | 13 |
| t _{PZL} | | | | 3.7 | 5.1 | 6.3 | 13 |
| t _{PHZ} | OE | Q | MAX | 4.6 | 6.5 | 5.9 | 17.4 |
| t _{PLZ} | | | | 4.6 | 6.5 | 5.9 | 17.4 |

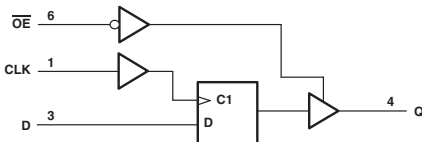
UNIT : ns

1G374

SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | L | L |
| L | ↑ | H | H |
| L | H or L | X | Q |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|---------------------------------|--------|------------|--------|----------|----------|----------|
| f_{max} | | | MIN | 175 | 150 | 125 | 100 |
| t_w | Pulse duration, CLK high or low | | MIN | 2.5 | 2.8 | 3 | 3.3 |
| t_{su} | Setup time, data before CLK ↑ | | MIN | 1.5 | 2 | 2.5 | 3.5 |
| t_h | Hold time, data after CLK ↑ | | MIN | 1.5 | 1.5 | 1.6 | 3.4 |
| t_{PLH} | CLK | Q | MAX | 4 | 6 | 8.2 | 18.3 |
| t_{PHL} | | | | 4 | 6 | 8.2 | 18.3 |
| t_{PZH} | \overline{OE} | Q | MAX | 3.5 | 5 | 6.3 | 13 |
| t_{PZL} | | | | 3.5 | 5 | 6.3 | 13 |
| t_{PHZ} | \overline{OE} | Q | MAX | 3.1 | 4.5 | 5.3 | 14 |
| t_{PLZ} | | | | 3.1 | 4.5 | 5.3 | 14 |

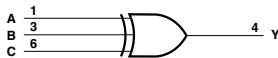
UNIT f_{max} : MHz other: ns

1G386

Logic Diagram

SINGLE 3-INPUT EXCLUSIVE-XOR GATE

● $Y = A \oplus B \oplus C$



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| L | L | L | L |
| L | L | H | H |
| L | H | L | H |
| L | H | H | L |
| H | L | L | H |
| H | L | H | L |
| H | H | L | L |
| H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _L C 5V | V _L C 3.3V | V _L C 2.5V | V _L C 1.8V | UNIT |
|-----------------|------------|------------------------|--------------------------|--------------------------|--------------------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _L C 5V | V _L C 3.3V | V _L C 2.5V | V _L C 1.8V |
|------------------|-----------|--------|------------|------------------------|--------------------------|--------------------------|--------------------------|
| t _{PLH} | A, B or C | Y | MAX | 4 | 5 | 5.5 | 12 |
| t _{PHL} | | | | 4 | 5 | 5.5 | 12 |

UNIT: ns

1G0832

SINGLE 3-INPUT POSITIVE AND-OR GATE

- $Y = (A \cdot B) + C$
- Can Be Used in Three Combinations
AND-OR Gate
AND Gate
OR Gate

Logic Diagram



FUNCTION SELECTION TABLE

| |
|-----------------------|
| 2-Input AND Gate |
| 2-Input OR Gate |
| $Y = (A \cdot B) + C$ |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| X | X | H | H |
| H | H | X | H |
| X | L | L | L |
| L | X | L | L |

X = Valid H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | V _L C 5V | V _L C 3.3V | V _L C 2.5V | V _L C 1.8V | UNIT |
|-----------------|------------|------------------------|--------------------------|--------------------------|--------------------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | V _L C 5V | V _L C 3.3V | V _L C 2.5V | V _L C 1.8V |
|------------------|------------|--------|------------|------------------------|--------------------------|--------------------------|--------------------------|
| t _{PLH} | A, B, or C | Y | MAX | 4 | 5.9 | 7.6 | 17.5 |
| t _{PHL} | | | | 4 | 5.9 | 7.6 | 17.5 |

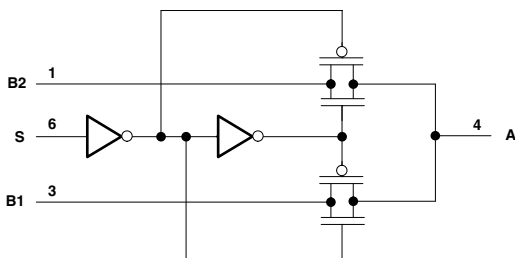
UNIT: ns

1G3157

SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

| CONTROL INPUT S | ON CHANNEL |
|-----------------|------------|
| L | B1 |
| H | B2 |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |

ELECTRICAL CHARACTERISTICS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT | | | | |
|-----------|------------|--------|----------|----------|----------|------|----|----|----|----|
| I_O | | 30 | -30 | 24 | -24 | 8 | -8 | 4 | -4 | mA |
| R_{ON} | MAX | 7 | 15 | 9 | 20 | 12 | 30 | 20 | 50 | W |

UNIT:ns

SWITCHING CHARACTERISTICS

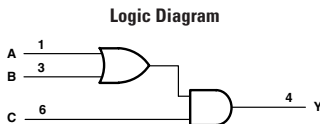
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|---------|---------|------------|--------|----------|----------|----------|
| t_{PLH} | A or Bn | Bn or A | MAX | 0.3 | 0.8 | 1.2 | 2 |
| t_{PHL} | | | | 0.3 | 0.8 | 1.2 | 2 |
| t_{PZH} | S | Bn | MAX | 5.7 | 7.6 | 14 | 24 |
| t_{PZL} | | | | 5.7 | 7.6 | 14 | 24 |
| t_{PHZ} | S | Bn | MAX | 3.8 | 5.3 | 7.5 | 13 |
| t_{PLZ} | | | | 3.8 | 5.3 | 7.5 | 13 |

UNIT:ns

1G3208

SINGLE 3-INPUT POSITIVE OR-AND GATE

- $Y = (A + B) \cdot C$
- Can Be Used in Three Combinations
OR-AND Gate
OR Gate
AND Gate



FUNCTION SELECTION TABLE

| |
|-----------------------|
| 2-Input AND Gate |
| 2-Input OR Gate |
| $Y = (A + B) \cdot C$ |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | X | H | H |
| X | H | H | H |
| X | X | L | L |
| L | L | H | L |

X = Valid H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|------------|--------|------------|--------|----------|----------|----------|
| t_{PLH} | A, B, or C | Y | MAX | 4 | 5.9 | 7.6 | 17.5 |
| t_{PHL} | | | | 4 | 5.9 | 7.6 | 17.5 |

UNIT : ns

2G00

DUAL 2-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{A \cdot B}$$

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

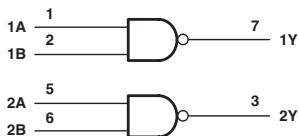
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 3.3 | 4.3 | 4.8 | 8.6 | 1.7 | 2.1 |
| t_{PHL} | | | | 3.3 | 4.3 | 4.8 | 8.6 | 1.7 | 2.1 |

UNIT:ns

Logic Diagram



2G02

DUAL 2-INPUT POSITIVE-NOR GATE

$$\bullet Y = \overline{A + B}$$

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

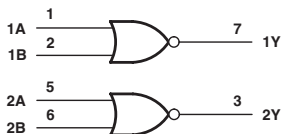
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 4.4 | 4.9 | 5.4 | 8.9 | 1.9 | 2.4 |
| t_{PHL} | | | | 4.4 | 4.9 | 5.4 | 8.9 | 1.9 | 2.4 |

UNIT:ns

Logic Diagram

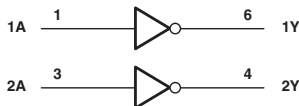


2G04

DUAL INVERTER GATE

$$\bullet Y = \bar{A}$$

Logic Diagram



FUNCTION TABLE

(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3.2 | 4.1 | 4.4 | 8 | 1.5 | 2 |
| t_{PHL} | | | | 3.2 | 4.1 | 4.4 | 8 | 1.5 | 2 |

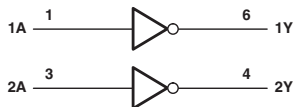
UNIT:ns

2GU04

DUAL INVERTER GATE

$$\bullet Y = \bar{A}$$

Logic Diagram



FUNCTION TABLE

(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

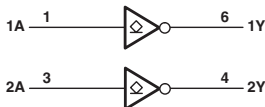
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3 | 3.7 | 4 | 5.5 | 2 | 2.7 |
| t_{PHL} | | | | 3 | 3.7 | 4 | 5.5 | 2 | 2.7 |

UNIT:ns

2G06

DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V_O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | V |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

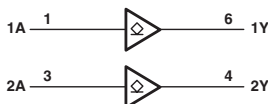
| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 2.9 | 3.4 | 3.9 | 7.2 | 1.2 | 2.5 |
| t_{PHL} | | | | 2.9 | 3.4 | 3.9 | 7.2 | 1.8 | 2.3 |

UNIT:ns

2G07

DUAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer/deiver)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V_O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | V |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 2.9 | 3.7 | 4.4 | 8.6 | 1.2 | 2.5 |
| t_{PHL} | | | | 2.9 | 3.7 | 4.4 | 8.6 | 1.8 | 2.3 |

UNIT:ns

2G08

DUAL 2-INPUT POSITIVE-AND GATE

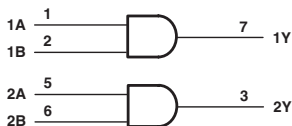
● $Y = A \cdot B$

FUNCTION TABLE

(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 3.8 | 4.7 | 5.1 | 9 | 1.6 | 2.1 |
| t_{PHL} | | | | 3.8 | 4.7 | 5.1 | 9 | 1.6 | 2.1 |

UNIT:ns

2G14

DUAL SCHMITT-TRIGGER INVERTER

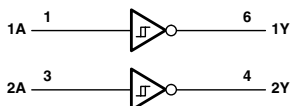
● $Y = \overline{A}$

FUNCTION TABLE

(each inverter)

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | L |
| L | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 4.3 | 5.4 | 5.7 | 9.5 | TBD | TBD |
| t_{PHL} | | | | 4.3 | 5.4 | 5.7 | 9.5 | TBD | TBD |

UNIT:ns

2G17

DUAL SCHMITT-TRIGGER BUFFER

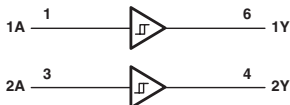
● $Y = A$

FUNCTION TABLE

(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 4.3 | 5.4 | 5.7 | 9.3 |
| t_{PHL} | | | | 4.3 | 5.4 | 5.7 | 9.3 |

UNIT:ns

2G32

DUAL 2-INPUT POSITIVE-OR GATE

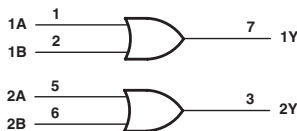
● $Y = A + B$

FUNCTION TABLE

(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|--------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A or B | Y | MAX | 3.2 | 3.8 | 4.4 | 8 | 1.7 | 2.1 |
| t_{PHL} | | | | 3.2 | 3.8 | 4.4 | 8 | 1.7 | 2.1 |

UNIT:ns

2G34

DUAL BUFFER GATE

● $Y = A$

FUNCTION TABLE

(each gate)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

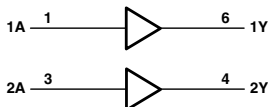
| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3.2 | 4.1 | 4.4 | 8.6 | 1.8 | 2.4 |
| t_{PHL} | | | | 3.2 | 4.1 | 4.4 | 8.6 | 1.8 | 2.4 |

UNIT: ns

Logic Diagram



2G38

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

● $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

FUNCTION TABLE

(each gate)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

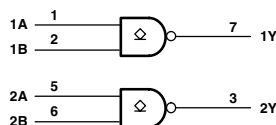
| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V_{O1} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|--------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A or B | Y | MAX | 3.9 | 4.5 | 6 | 10 |
| t_{PHL} | | | | 3.9 | 4.5 | 6 | 10 |

UNIT: ns

Logic Diagram

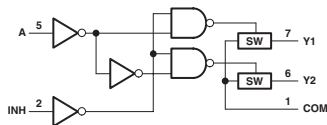


2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

| CONTROL INPUTS | | ON CHANNEL |
|----------------|---|------------|
| INH | A | |
| L | L | Y1 |
| L | H | Y2 |
| H | X | None |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|--------------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.001 | 0.001 | 0.001 | 0.001 | 0.01 | 0.01 | mA |
| R _{ON} | MAX | 13 | 17 | 20 | 30 | 15 | 20 | mΩ |
| R _{ON(P)} | MAX | 15 | 20 | 30 | 120 | 20 | 80 | mΩ |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|----------|----------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | COM or Y | Y or COM | MAX | 0.6 | 0.8 | 1.2 | 2 | 0.2 | 0.4 |
| | | | | 0.6 | 0.8 | 1.2 | 2 | 0.2 | 0.4 |
| t _{PZH} | INH | COM or Y | MAX | 4.5 | 5.4 | 6.1 | 9 | 2.2 | 3.1 |
| | | | | 4.5 | 5.4 | 6.1 | 9 | 2.2 | 3.1 |
| t _{PZL} | INH | COM or Y | MAX | 8 | 8.1 | 8.3 | 10.9 | 2.2 | 3.4 |
| | | | | 8 | 8.1 | 8.3 | 10.9 | 2.2 | 3.4 |
| t _{PHZ} | A | COM or Y | MAX | 5.4 | 5.8 | 7.2 | 10.3 | 2.2 | 3.0 |
| | | | | 5.4 | 5.8 | 7.2 | 10.3 | 2.2 | 3.0 |
| t _{PHZ} | A | COM or Y | MAX | 5 | 7.2 | 7.9 | 9.4 | 2.3 | 3.0 |
| | | | | 5 | 7.2 | 7.9 | 9.4 | 2.3 | 3.0 |
| t _{PLZ} | A | COM or Y | MAX | 5 | 7.2 | 7.9 | 9.4 | 2.3 | 3.0 |
| | | | | 5 | 7.2 | 7.9 | 9.4 | 2.3 | 3.0 |

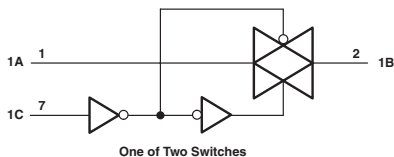
UNIT:ns

2G66

DUAL BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity
- Rail-to-Rail Input/Output

Logic Diagram, each switch



One of Two Switches

FUNCTION TABLE

(each section)

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | OFF |
| H | ON |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|--------------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| R _{ON} | MAX | 10 | 15 | 20 | 30 | 15 | 20 | mΩ |
| R _{ON(P)} | MAX | 15 | 20 | 30 | 120 | 20 | 80 | mΩ |

SWITCHING CHARACTERISTICS

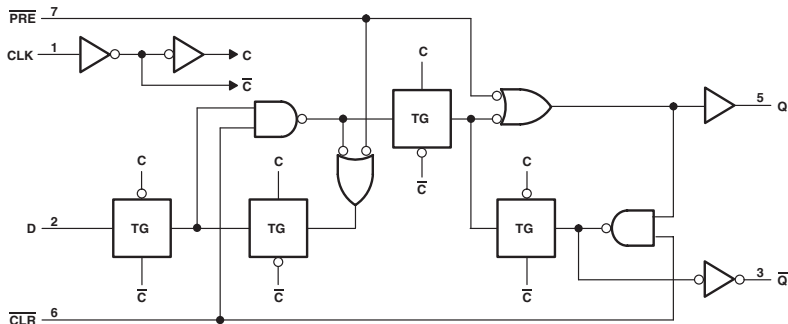
| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A or B | B or A | MAX | 0.6 | 0.8 | 1.2 | 2 | 0.7 | 0.7 |
| | | | | 0.6 | 0.8 | 1.2 | 2 | 0.7 | 0.7 |
| t _{PZH} | C | A or B | MAX | 3.9 | 4.4 | 5.6 | 10 | 2.3 | 2.7 |
| | | | | 3.9 | 4.4 | 5.6 | 10 | 2.3 | 2.7 |
| t _{PHZ} | C | A or B | MAX | 6.3 | 7.2 | 6.9 | 10.5 | 2 | 3.4 |
| | | | | 6.3 | 7.2 | 6.9 | 10.5 | 2 | 3.4 |
| t _{PLZ} | C | A or B | MAX | 6.3 | 7.2 | 6.9 | 10.5 | 2 | 3.4 |
| | | | | 6.3 | 7.2 | 6.9 | 10.5 | 2 | 3.4 |

UNIT:ns

2G74

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-----|-----|---|----------------|----------------|
| PRE | CLR | CLK | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H [†] | H [†] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | \bar{Q}_0 |

[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -16 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 16 | 8 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

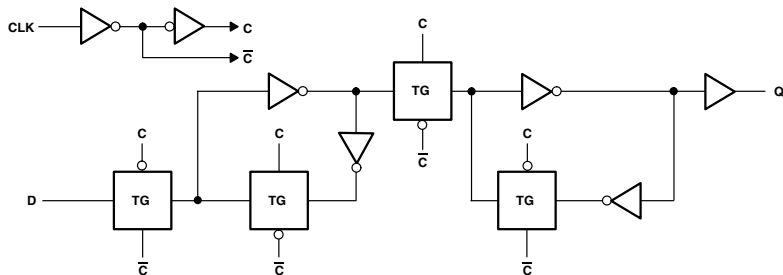
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|----------------------------|----------------|------------|--------|----------|----------|----------|
| f _{max} | | | MIN | 200 | 175 | 175 | 80 |
| t _w | CLK | | MIN | 2 | 2.7 | 2.7 | 6.2 |
| | PRE or CLR low | | | 2 | 2.7 | 2.7 | 6.2 |
| t _{su} | Data | | MIN | 1.1 | 1.3 | 1.7 | 2.9 |
| | PRE or CLR inactive | | | 1 | 1.2 | 1.4 | 1.9 |
| t _h | | | MIN | 0.5 | 1.2 | 0.3 | 0 |
| t _{PLH} | CLK | Q | MAX | 4.1 | 5.9 | 7.1 | 13.4 |
| t _{PHL} | | | | 4.1 | 5.9 | 7.1 | 13.4 |
| t _{PLH} | CLK | \bar{Q} | MAX | 4.4 | 6.2 | 7.7 | 14.4 |
| t _{PHL} | | | | 4.4 | 6.2 | 7.7 | 14.4 |
| t _{PLH} | \bar{PRE} or \bar{CLR} | Q or \bar{Q} | MAX | 4.1 | 5.9 | 7 | 12.9 |
| t _{PHL} | | | | 4.1 | 5.9 | 7 | 12.9 |

UNIT:ns

2G79

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|----------------|
| CLK | D | Q |
| ↑ | H | H |
| ↑ | L | L |
| L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.005 | 0.005 | 0.005 | 0.005 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

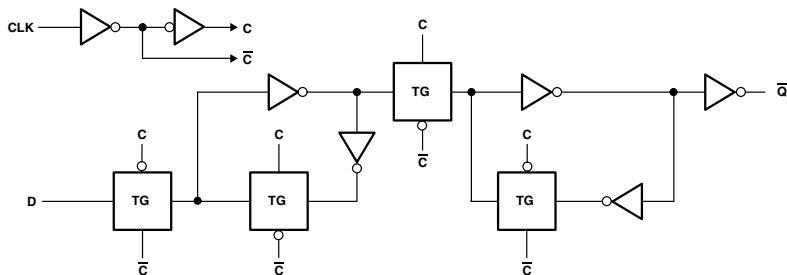
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-------------------------|--------|------------|--------|----------|----------|----------|----------|----------|
| f _{max} | | | MIN | 160 | 160 | 160 | 160 | 275 | 250 |
| t _w | CLK high or low | | MIN | 2.5 | 2.5 | 2.5 | 2.5 | 1 | 1 |
| t _{su} | Before CLK ↑, Data high | | MIN | 0.9 | 1.1 | 1.4 | 2.2 | 0.5 | 0.6 |
| | Before CLK ↓, Data low | | | 0.9 | 1.1 | 1.4 | 2.2 | 0.5 | 0.6 |
| t _h | Data after CLK ↑ | | MIN | 0.5 | 0.7 | 0.8 | 1.4 | 0.1 | 0.1 |
| I _{PLH} | CLK | Q | MAX | 4.5 | 5.2 | 7.0 | 9.9 | 1.8 | 2.4 |
| | | | | 4.5 | 5.2 | 7.0 | 9.9 | 1.8 | 2.4 |

UNIT f_{max}: MHz other: ns

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram


FUNCTION TABLE
 (each flip-flop)

| INPUTS | | OUTPUT |
|--------|---|----------------|
| CLK | D | Q |
| ↑ | H | L |
| ↑ | L | H |
| L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|-----------|-------------|-------------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.005 | 0.005 | 0.005 | 0.005 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-------------------------|--------|------------|-----------|-------------|-------------|-------------|-------------|-------------|
| f _{max} | | | MIN | 160 | 160 | 160 | 160 | 275 | 250 |
| t _w | CLK high or low | | MIN | 2.5 | 2.5 | 2.5 | 2.5 | 1 | 1 |
| t _{su} | Before CLK ↑, Data high | | MIN | 0.9 | 1.1 | 1.4 | 2.2 | 0.5 | 0.6 |
| | Before CLK ↑, Data low | | | 0.9 | 1.1 | 1.4 | 2.2 | 0.5 | 0.6 |
| t _h | Data after CLK ↑ | | MIN | 0.6 | 0.8 | 1.0 | 1.6 | 0.5 | 0.1 |
| t _{PLH} | CLK | Q | MAX | 4.5 | 5.2 | 7.0 | 13.9 | 1.8 | 2.4 |
| t _{PHL} | | | | 4.5 | 5.2 | 7.0 | 13.9 | 1.8 | 2.4 |

UNIT f_{max}: MHz other: ns

2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

$$\bullet Y = A \oplus B$$

FUNCTION TABLE

(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

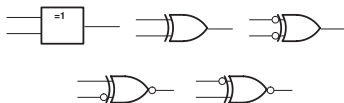
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|--------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 3.6 | 4.7 | 5.7 | 9.9 | 2.0 | 2.6 |
| t_{PHL} | | | | 3.6 | 4.7 | 5.7 | 9.9 | 2.0 | 2.6 |

UNIT:ns

Logic Diagram

EXCLUSIVE OR



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

2G125

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

FUNCTION TABLE

(each buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

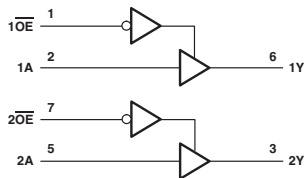
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------|------------|--------|----------|----------|----------|----------|----------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|-----------|-----------------|--------|------------|--------|----------|----------|----------|----------|----------|
| t_{PLH} | A | Y | MAX | 3.7 | 4.3 | 4.8 | 9.1 | 1.8 | 2.6 |
| t_{PHL} | | | | 3.7 | 4.3 | 4.8 | 9.1 | 1.8 | 2.6 |
| t_{PZH} | \overline{OE} | Y | MAX | 3.8 | 4.7 | 5.6 | 9.9 | 2.2 | 2.9 |
| t_{PZL} | | | | 3.8 | 4.7 | 5.6 | 9.9 | 2.2 | 2.9 |
| t_{PHZ} | \overline{OE} | Y | MAX | 3.4 | 4.6 | 5.8 | 11.6 | 2 | 3.6 |
| t_{PLZ} | | | | 3.4 | 4.6 | 5.8 | 11.6 | 2 | 3.6 |

UNIT:ns

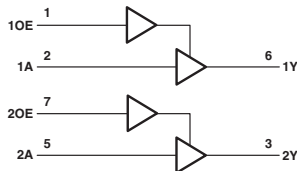
Logic Diagram



2G126

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 3.2 | 4 | 4.9 | 9.8 | 1.8 | 2.3 |
| | | | | 3.2 | 4 | 4.9 | 9.8 | 1.8 | 2.3 |
| t _{PZH} | OE | Y | MAX | 3.1 | 4.1 | 5 | 10 | 2.2 | 2.4 |
| | | | | 3.1 | 4.1 | 5 | 10 | 2.2 | 2.4 |
| t _{PHZ} | OE | Y | MAX | 3.3 | 4.4 | 5.7 | 12.6 | 1.8 | 3.3 |
| | | | | 3.3 | 4.4 | 5.7 | 12.6 | 1.8 | 3.3 |

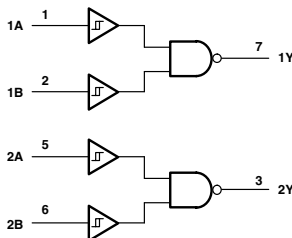
UNIT: ns

2G132

DUAL 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUT

$$\bullet Y = \overline{A \cdot B} \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

Logic Diagram



FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

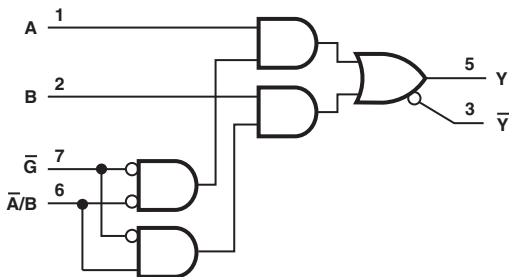
| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|--------|--------|------------|--------|----------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 5 | 6 | 7.5 | 16 |
| | | | | 5 | 6 | 7.5 | 16 |

UNIT: ns

2G157

SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-----|---|---|---------|---|
| G | A/B | A | B | Y | Y |
| H | X | X | X | L | L |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------------|------------|-----------|-------------|-------------|-------------|------|
| I _{cc} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{oh} | MAX | -32 | -24 | -8 | -4 | mA |
| I _{ol} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|------------------|--------|--------|------------|-----------|-------------|-------------|-------------|
| t _{PLH} | A or B | Y or Y | MAX | 4 | 6 | 8 | 14 |
| t _{PHL} | | | | 4 | 6 | 8 | 14 |
| t _{PLH} | A/B | Y or Y | MAX | 4 | 6 | 9 | 16 |
| t _{PHL} | | | | 4 | 6 | 9 | 16 |
| t _{PLH} | G | Y or Y | MAX | 4 | 6 | 8 | 14 |
| t _{PHL} | | | | 4 | 6 | 8 | 14 |

UNIT:ns

2G240

DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | H |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

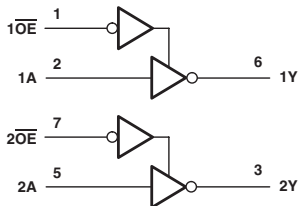
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 4 | 4.6 | 5.5 | 11.3 | 1.7 | 2.5 |
| | | | | 4 | 4.6 | 5.5 | 11.3 | 1.7 | 2.5 |
| t _{PHL} | A | Y | MAX | 5 | 5.4 | 6.6 | 11.7 | 2.1 | 3.1 |
| | | | | 5 | 5.4 | 6.6 | 11.7 | 2.1 | 3.1 |
| t _{PLZ} | OE | Y | MAX | 4.2 | 5.5 | 5.7 | 12.8 | 1.9 | 3.7 |
| | | | | 4.2 | 5.5 | 5.7 | 12.8 | 1.9 | 3.7 |
| t _{PHZ} | OE | Y | MAX | 4.2 | 5.5 | 5.7 | 12.8 | 1.9 | 3.7 |
| | | | | 4.2 | 5.5 | 5.7 | 12.8 | 1.9 | 3.7 |

UNIT:ns

Logic Diagram



2G241

DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

FUNCTION TABLE

| INPUTS | | OUTPUT | INPUTS | | OUTPUT |
|--------|----|--------|--------|----|--------|
| 1OE | 1A | 1Y | 2OE | 2A | 2Y |
| L | H | H | H | H | H |
| L | L | L | H | L | L |
| H | X | Z | L | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

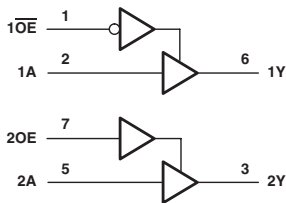
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V | UNIT |
|-----------------|------------|--------|----------|----------|----------|----------|----------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -4 | -9 | -8 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | 9 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | AUC 2.5V | AUC 1.8V |
|------------------|-------|--------|------------|--------|----------|----------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 3.7 | 4.3 | 4.8 | 8.8 | 1.8 | 2.5 |
| | | | | 3.7 | 4.3 | 4.8 | 8.8 | 1.8 | 2.5 |
| t _{PHL} | A | Y | MAX | 3.8 | 4.7 | 5.6 | 9.9 | 2 | 2.8 |
| | | | | 3.8 | 4.7 | 5.6 | 9.9 | 2 | 2.8 |
| t _{PLZ} | OE | Y | MAX | 3.4 | 4.4 | 5.8 | 11.6 | 2.1 | 3.6 |
| | | | | 3.4 | 4.4 | 5.8 | 11.6 | 2.1 | 3.6 |
| t _{PHZ} | OE | Y | MAX | 3.3 | 4.1 | 4.7 | 8.8 | 2 | 2.8 |
| | | | | 3.3 | 4.1 | 4.7 | 8.8 | 2 | 2.8 |
| t _{PLZ} | OE | Y | MAX | 3.3 | 4.2 | 5.2 | 12.5 | 2.1 | 8.6 |
| | | | | 3.3 | 4.2 | 5.2 | 12.5 | 2.1 | 8.6 |
| t _{PHZ} | OE | Y | MAX | 3.3 | 4.2 | 5.2 | 12.5 | 2.1 | 8.6 |
| | | | | 3.3 | 4.2 | 5.2 | 12.5 | 2.1 | 8.6 |

UNIT:ns

Logic Diagram



3G04

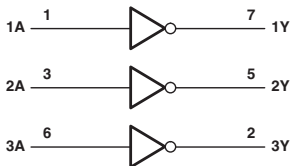
TRIPLE INVERTER GATE

$$\bullet Y = \bar{A}$$

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3.2 | 4.1 | 4.4 | 7.9 |
| t_{PHL} | | | | 3.2 | 4.1 | 4.4 | 7.9 |

UNIT: ns

3GU04

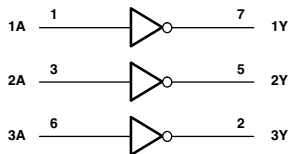
TRIPLE INVERTER GATE

$$\bullet Y = \bar{A}$$

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3.2 | 3.9 | 4 | 9.2 |
| t_{PHL} | | | | 3.2 | 3.9 | 4 | 9.2 |

UNIT: ns

3G06

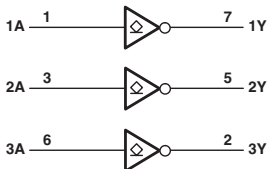
TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

FUNCTION TABLE

(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------------|------------|-----------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V _O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 2.9 | 3.4 | 3.9 | 7.2 |
| t _{PHL} | | | | 2.9 | 3.4 | 3.9 | 7.2 |

UNIT:ns

3G07

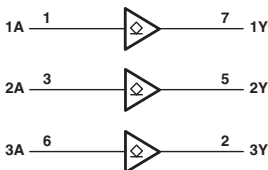
TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

FUNCTION TABLE

(each buffer/driver)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------------|------------|-----------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| V _O | MAX | 5.5 | 5.5 | 5.5 | 5.5 | mA |
| I _{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|------------------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 2.9 | 3.7 | 4.3 | 7.8 |
| t _{PHL} | | | | 2.9 | 3.7 | 4.3 | 7.8 |

UNIT:ns

3G14

TRIPLE SCHMITT-TRIGGER INVERTER

$$\bullet Y = \bar{A}$$

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

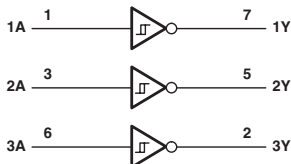
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 4.3 | 5.4 | 5.7 | 9.2 |
| t_{PHL} | | | | 4.3 | 5.4 | 5.7 | 9.2 |

UNIT:ns

Logic Diagram



3G17

TRIPLE SCHMITT-TRIGGER BUFFER

$$\bullet Y = A$$

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

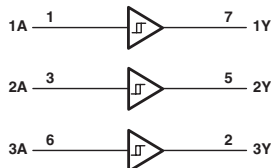
| PARAMETER | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | VLC 5V | VLC 3.3V | VLC 2.5V | VLC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 4.1 | 5.4 | 6.2 | 9.2 |
| t_{PHL} | | | | 4.1 | 5.4 | 6.2 | 9.2 |

UNIT:ns

Logic Diagram



3G34

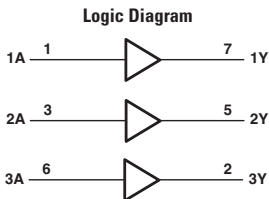
TRIPLE BUFFER GATE

● $Y = A$

FUNCTION TABLE

(each gate)

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | H |
| L | L |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V | UNIT |
|-----------|------------|-----------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -8 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 5V | LVC 3.3V | LVC 2.5V | LVC 1.8V |
|-----------|-------|--------|------------|-----------|-------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 3.2 | 4.1 | 4.4 | 7.9 |
| t_{PHL} | | | | 3.2 | 4.1 | 4.4 | 7.9 |

UNIT:ns

FUNCTION

Standard

BUFFER / DRIVER (NON-INVERTING)

| Description | No. of Output | Output | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|---------------|---------------|--------|--------|------------|----|---|-----|------|---|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-------|-----|------|-----|-----|
| | | | | Bipolar | | | | CMOS | | | | BiCMOS | | | | Advanced CMOS | | | | | | | | | |
| | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LV-AT | LVC | ALVC | AVC | AUC |
| NON-INVERTING | 4 | 3S | 125 | X | ●A | | | | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | 3S | 126 | X | ●A | | | | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | 3S | 365 | X | ●A | | | | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | 3S | 267 | X | ●A | | | | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 8 | 3S | 341 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | 3S | 244 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | 3S | 455 | | | | | | | | X/- | | | | | | | | | | | | | | |
| | | 3S | 465 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 467 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 541 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | 3S | 656 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 747 | | | | | | | | | | | | | | | | | | | | | | |
| | | OC | 757 | | | | | | | | | | | | | | | | | | | | | | |
| | | OC | 750 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 1241 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 1244 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 2241 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 2244 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 2541 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 25241 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 25244 | | | | | | | | | | | | | | | | | | | | | | |
| | | OC | 25757 | | | | | | | | | | | | | | | | | | | | | | |
| | | OC | 25760 | | | | | | | | | | | | | | | | | | | | | | |
| | | 10 | 3S | 827 | | | | | | | | | | | | | | | | | | | | | |
| | R3S | | 2827 | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | | 29827 | | | | | | | | | | | | | | | | | | | | | | |
| | 11 | R3S | 5400 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 5402 | | | | | | | | | | | | | | | | | | | | | | |
| | 12 | R3S | 16903 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 16241 | | | | | | | | | | | | | | | | | | | | | | |
| | 16 | 3S | 16244 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 16541 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 162241 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 162244 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 162541 | | | | | | | | | | | | | | | | | | | | | | |
| | 18 | 3S | 16825 | | | | | | | | | | | | | | | | | | | | | | |
| | | R3S | 162825 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 16835 | | | | | | | | | | | | | | | | | | | | | | |
| | 20 | 3S | 16827 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 162827 | | | | | | | | | | | | | | | | | | | | | | |
| 32 | 3S | 32244 | | | | | | | | | | | | | | | | | | | | | | | |
| | R3S | 32244 | | | | | | | | | | | | | | | | | | | | | | | |

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER / DRIVER (INVERTING, INVERTING AND NON-INVERTING, ADDRESS DRIVERS)

| Description | No. of Output | Output | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|-----------------|-----------------------------|--------|--------|------------|----|---|-----|------|---|--------|-------|-----|-----|---------------|------|-----|-----|-----|------|-----|-------|-----|------|-----|-----|
| | | | | Bipolar | | | | CMOS | | BICMOS | | | | Advanced CMOS | | | | | | | | | | | |
| | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LV-AT | LVC | ALVC | AVC | AUC |
| INVERTING | 6 | 3S | 366 | X | X | | | | | X/● | | | | | | | | | | | | | | | |
| | | 3S | 368 | X | A | ● | A | | | ●/● | -/● | | | | | | | | | | | | | | |
| | | 3S | 436 | | | X | | | | | | | | | | | | | | | | | | | |
| | | 3S | 437 | X | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 231 | | | | X | X | | | | | | | | | | | | | | | | | |
| | | 3S | 240 | | ● | ● | ● | ● | A | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 456 | | | | | | | | X/- | | | | | | | | | | | | | | | |
| | 3S | 466 | | X | | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 468 | | X | | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 540 | | ● | | ● | 1 | | X | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● |
| | 3S | 655 | | | | | | | | | | | | X/- | X/- | | | | | | | | | | |
| | 3S | 746 | | | | X | | | | | | | | | | | | | | | | | | | |
| | OC | 756 | | | X | | ● | | | ●/● | | | | | | | | | | | | | | | |
| | OC | 763 | | | | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 1240 | | | | X | | | | | ●/● | ●/● | | | | | | | | | | | | | |
| | R3S | 2240 | | | | X | | | | | | | | | | | | | | | | | | | |
| | R3S | 2540 | | | | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 25240 | | | | | | | | | X/- | | | | | | | | | | | | | | |
| | OC | 25756 | | | | | | | | | X/- | | | | | | | | | | | | | | |
| | 3S | 828 | | | | | | | | | | | | X/- | X/- | | | | | | | ●/● | | | |
| | R3S | 2828 | | | | | | | | | X/- | | | | | | | | | | | | | | |
| | 3S | 29828 | | | | X | | | | | X/B/- | | | | | | | | | | | | | | |
| | 11 | R3S | 5401 | | | | | | | | | ● | | | | | | | | | | | | | |
| | 12 | R3S | 5403 | | | | | | | | | ● | | | | | | | | | | | | | |
| | 16 | 3S | 16240 | | | | | | | | ●/● | ●/● | ●/● | ●/● | X | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● |
| | | 3S | 16540 | | | | | | | | ●/● | ●/● | ●/● | ●/● | | | X | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | ●/● | |
| | | R3S | 162240 | | | | | | | | | ●/● | | | | | | | | | | | | - | |
| | | R3S | 162540 | | | | | | | | | | | | | | | | | | | | | X | |
| | | 3S | 16828 | | | | | | | | | | | | | | X | | | | | | | X | |
| | 32 | 3S | 32240 | | | | | | | | | | | | | | | | | | | | Z●/● | | |
| | INVERTING AND NON-INVERTING | 8 | 3S | 230 | | | | X | X | | | | | | | | | | | | | | | | |
| | | | OC | 762 | | | | | X | | | | | | | | | | | | | | | | |
| ADDRESS DRIVERS | 1-2 | 3S | 16830 | | | | | | | | | | | | | | | | | | | | H* | | |
| | | R3S | 162830 | | | | | | | | | | | | | | | | | | | | H● | | |
| | 1-4 | 3S | 16344 | | | | | | | | | | | | | | | | | | | | | H● | |
| | | 3S | 16831 | | | | | | | | | | | | | | | | | | | | | H● | |
| | | 3S | 16832 | | | | | | | | | | | | | | | | | | | | | H● | |
| | | R3S | 162344 | | | | | | | | | | | | | | | | | | | | | H● | |
| | | R3S | 162831 | | | | | | | | | | | | | | | | | | | | | ● | |
| | | R3S | 162832 | | | | | | | | | | | | | | | | | | | | | H● | |

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated * : New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (NON-INVERTING)

| Description | No. of Output | Output | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|---------------|---------------|--------|--------|------------|-----------|---|-----|------|-----|-----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-------|-----|------|-----|-----|
| | | | | Bipolar | | | | CMOS | | | | BICMOS | | | | Advanced CMOS | | | | | | | | | |
| | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LV-AT | LVC | ALVC | AVC | AUC |
| 4 | 3S | 226 | | | X | | | | | | | | | | | | | | | | | | | | |
| | 3S | 440 | X | | | | | | | | | | | | | | | | | | | | | | |
| | OC | 441 | X | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 442 | ● | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 443 | X | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 444 | X | | | | | | | | | | | | | | | | | | | | | | |
| | OC | 448 | X | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 449 | X | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 243 | ● | ●A | X | X | - | ● | - | ● | | | | | | | | | | | | | | | |
| | 3S | 1243 | | | | | | | | | | | | | | | | | | | | | | | |
| NON-INVERTING | 8 | 3S | 245 | ● | ●A ●A1 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 470 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 472 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 474 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 543 | | | | | ● | | | | | | | | | | | | | | | | | | |
| | OC | 615 | | | X | | | | | | | | | | | | | | | | | | | | |
| | OC | 621 | X | ●A ●A1 | X | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 623 | ● | ●A ●A1 | X | X | ●/- | ●/- | ●/- | ● | | | | | | | | | | | | | | | |
| | 3SOC | 639 | ● | ●A ●A1 | X | | | | | | | | | | | | | | | | | | | | |
| | OC | 641 | ● | ●A ●A1 | ● | | | | | | | | | | | | | | | | | | | | |
| | 3S | 645 | ● | ●A ●A1 | ● | | ●/- | ●/- | | | | | | | | | | | | | | | | | |
| | 3S | 646 | ● | ●A ●A1 | ● | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | OC | 647 | X | X | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 652 | ● | ●A ●A1 | ● | | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3SOC | 654 | X | ● | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 657 | | | | | ● | | | | | | | | | | | | | | | | | | |
| | 3S | 659 | | | | | | X/- | X/- | X/- | | | | | | | | | | | | | | | |
| | 3S | 665 | | | | | | X/- | X/- | | | | | | | | | | | | | | | | |
| | 3S | 852 | | | | | X | | | | | | | | | | | | | | | | | | |
| | 3S | 856 | | | | | X | | | | | | | | | | | | | | | | | | |
| | 3S | 877 | | | | | X | | | | | | | | | | | | | | | | | | |
| | 3S | 999 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1245 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1645 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 2245 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 2623 | | | | | X | | | | | | | | | | | | | | | | | | |
| | 3S | 2645 | | | | | X | | | | | | | | | | | | | | | | | | |
| | 3S | 2952 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25245 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25543 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25521 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25623 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25641 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25646 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25647 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25652 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3S | 25654 | | | | | | | | | | | | | | | | | | | | | | | |
| | 8+1P | 3SOC | 833 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3SOC | 853 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3SOC | 29833 | | | | X | | | | | | | | | | | | | | | | | | |
| | 3SOC | 29853 | | | | X | | | | | | | | | | | | | | | | | | | |
| | 9 | 3S | 863 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 29863 | | | | ● | | | | | | | | | | | | | | | | | | |
| | 9 x 4 | 3S | 16409 | | | | | | | | | | | | | | | | | | | | | | |
| | | 3S | 861 | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 3S | 29861 | | | | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 29861 | | | | | | | | | | | | | | | | | | | | | | | |

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

J/K FLIP-FLOP

| Trigger | Circuit | PRE • CLR | Output | Q • Q̄ | Device | Technology | | | | | | | | | | | | | | | | | | | |
|---------|---------|-----------------|--------|--------------|--------|------------|----|---|-----|----|---|------|-----|-----|-----|--------|------|----|-----|---------------|------|----|-------|-----|------|
| | | | | | | Bipolar | | | | | | CMOS | | | | BICMOS | | | | Advanced CMOS | | | | | |
| | | | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LV-AT | LVC | ALVC |
| POS | 1 | B | 2S | B | 72 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 70 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 73 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | B | 2S | B | 109 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 2 | B | 2S | B | 110 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 111 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | Q | 376 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | Q | 376 | X | | | | | | | | | | | | | | | | | | | |
| NEG | 2 | B | 2S | B | 76 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 78 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 107 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | B | 2S | B | 112 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 4 | B | 2S | B | 113 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| | | B | 2S | Q | 376 | X | | | | | | | | | | | | | | | | | | | |
| | | B | 2S | B | 114 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| | | B | 2S | Q | 276 | X | | | | | | | | | | | | | | | | | | | |

D-TYPE FLIP-FLOP

| Trigger | Circuit | PRE • CLR | Output | Q • Q̄ | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|---------|---------|-----------------|--------|--------------|--------|------------|----|---|-----|----|---|------|-----|-----|-----|--------|------|----|-----|---------------|------|----|-------|-----|------|-----|-----|
| | | | | | | Bipolar | | | | | | CMOS | | | | BICMOS | | | | Advanced CMOS | | | | | | | |
| | | | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LV-AT | LVC | ALVC | AVC | AUC |
| POS | 2 | B | 2S | B | 74 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | |
| | | C | 2S | B | 171 | X | | | | | | | | | | | | | | | | | | | | | |
| | 4 | C | 2S | B | 175 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | C | 2S | B | 379 | X | | | | | | | | | | | | | | | | | | | | | |
| | 6 | C | 2S | Q | 174 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | | 2S | Q | 378 | X | | | | | | | | | | | | | | | | | | | | | |
| | | C | 2S | Q | 273 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 374 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | C | 2S | Q | 377 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 478 | X | | | | | | | | | | | | | | | | | | | | | |
| | | 8 | C | 3S | Q̄ | 534 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | | 3S | Q̄ | 564 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | C | 3S | Q | 574 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | | | 3S | Q | 575 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | | C | 3S | Q | 576 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | | | 3S | Q̄ | 577 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | C | | 3S | Q | 825 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 826 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | 9 | | C | 3S | Q | 874 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | | 3S | Q̄ | 876 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | C | 3S | Q | 878 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | | | 3S | Q̄ | 879 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | | C | 3S | Q | 4374 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 29825 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | C | 3S | Q | 29826 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 823 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | C | 3S | Q̄ | 824 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 29823 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | C | 3S | Q̄ | 29824 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | | | 3S | Q | 821 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | |
| | C | 3S | Q | 822 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q | 16821 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | C | 3S | Q | 29821 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q̄ | 29822 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | 10X2 | C | 3S | Q | 16820 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | | 3S | Q | 162820 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | 16 | C | 3S | Q | 16374 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | | 3S | Q̄ | 16534 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | C | 3S | Q | 162374 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q | 16823 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | C | 3S | Q | 162823 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q | 16721 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | C | 3S | Q | 16821 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q | 162721 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | C | 3S | Q | 162821 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | 3S | Q | 16722 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | 32 | C | 3S | Q | 32374 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| | | | 3S | Q | 322374 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |

Explanatory notes [Trigger] POS: Positive edge NEG: Negative Edge

[PRE - CLR] B: Preset and Clear C: Clear Only

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q-Q̄] B: Q-Output Q: Q-Output Q̄: Q̄-Output

Status ●: Product available in technology indicated * : New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

REGISTER (ETC)

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | |
|------------------------------------|--------|------------|----|---|-----|----|------|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|
| | | Bipolar | | | | | CMOS | | | BICMOS | | | | Advanced CMOS | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC |
| REGISTER FILES 8W x 2B | 172 | X | | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 4W x 4B | 170 | X | X | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 4W x 4B | 670 | | ● | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 16W x 5B | 670 | | | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 16W x 5B | 858 | | | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 16W x 6B | 871 | | | | | | | | | | | | | | | | | | | | | |
| REGISTER FILES 32W x 4B | 859 | | | | | | | | | | | | | | | | | | | | | |
| MUX WITH STRAGE | 298 | X | ● | | | | | | | | | | | | | | | | | | | |
| MUX WITH STRAGE | 398 | X | | | | | | | | | | | | | | | | | | | | |
| 4BIT BUS-BUFFER REGISTER | 173 | X | ●A | | | | | | | | | | | | | | | | | | | |
| 8BIT STORAGE REGISTER | 396 | X | | | | | | | | | | | | | | | | | | | | |
| 8BIT DIAGNOSTICS/PIPELINE REGISTER | 816 | | | | | | | | | | | | | | | | | | | | | |
| | 819 | | | | | | | | | | | | | | | | | | | | | |
| | 29816 | | | | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MONOSTABLE MULTIVIBRATOR

| Circuit | CLR | Retrigger | Device | Technology | | | | | | | | | | | | | | | | | | |
|---------|-----|-----------|--------|------------|----|---|-----|----|------|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|
| | | | | Bipolar | | | | | CMOS | | | BICMOS | | | | Advanced CMOS | | | | | | |
| | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC |
| 1 | | | 121 | ● | | | | | | | | | | | | | | | | | | |
| | C | R | 122 | X | ● | | | | | | | | | | | | | | | | | |
| | C | R | 422 | X | | | | | | | | | | | | | | | | | | |
| 2 | C | R | 123 | ● | ● | | | | | | | | | | | | | | | | | |
| | C | | 221 | ● | ● | | | | | | | | | | | | | | | | | |
| | C | R | 423 | | ● | | | | | | | | | | | | | | | | | |
| | C | R | 4538 | | | | | | | | | | | | | | | | | | | |

Explanatory notes [CLR] C: With Clear

[Retrigger] R: With Retrigger

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

RATE MULTIPLIER/FREQUENCY DIVIDERS

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|--|--------|------------|----|---|-----|----|------|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|--|
| | | Bipolar | | | | | CMOS | | | BiCMOS | | | | Advanced CMOS | | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC | |
| FREQUENCY DIVIDERS | 56 | X | | | | | | | | | | | | | | | | | | | | | |
| FREQUENCY DIVIDERS | 57 | X | | | | | | | | | | | | | | | | | | | | | |
| 6BIT BINARY RATE MULTIPLIER | 97 | ● | | | | | | | | | | | | | | | | | | | | | |
| DECADE RATE MULTIPLIER | 167 | X | | | | | | | | | | | | | | | | | | | | | |
| PROGRAMABLE FREQUENCY DIVIDER/DIGITAL TIMERS | 292 | ● | | | | | | | | | | | | | | | | | | | | | |
| | 294 | ● | | | | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DATA SELECTOR/MULTIPLEXER

| No. of Input/output | Output | Circuit | ETC | Device | Technology | | | | | | | | | | | | | | | | | | | |
|---------------------|--------|---------|-----|--------|------------|----|---|-----|----|------|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|
| | | | | | Bipolar | | | | | CMOS | | | BiCMOS | | | | Advanced CMOS | | | | | | | |
| | | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC |
| 16/1 | 2S | 1 | | 150 | ● | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 250 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 850 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 851 | | | | | | | | | | | | | | | | | | | | |
| | 2S | 1 | | 4067 | | | | | | | | | | | | | | | | | | | | |
| 8/1 | 2S | 1 | | 151 | X | A | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 2S | 1 | | 152 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 251 | X | ● | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 1 | | 354 | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 356 | X | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 4051 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 4351 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 4851 | | | | | | | | | | | | | | | | | | | | |
| | OC | 1 | | 355 | X | | | | | | | | | | | | | | | | | | | |
| OC | 1 | | 357 | X | | | | | | | | | | | | | | | | | | | | |
| 4/1 | 2S | 2 | | 352 | X | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| | 3S | 2 | | 153 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 2 | | 253 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 2 | | 353 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| | 3S | 2 | | 4052 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 2 | | 4352 | | | | | | | | | | | | | | | | | | | | |
| 2/1 | 3S | 4 | | 16460 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 4 | | 162460 | | | | | | | | | | | | | | | | | | | | |
| | 2S | 1 | | 157 | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 2S | 1 | | 158 | ● | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 2S | 4 | S | 399 | ● | | | | | | | | | | | | | | | | | | | |
| | 3S | 1 | | 257 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 1 | | 258 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 4 | | 4053 | ● | X | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | 3S | 6 | U | 857 | | | | | | | | | | | | | | | | | | | | |
| | 3S | 8 | S | 604 | X | | | | | | | | | | | | | | | | | | | |
| OC | 8 | S | 605 | X | | | | | | | | | | | | | | | | | | | | |
| 3S | 8 | S | 606 | X | | | | | | | | | | | | | | | | | | | | |
| OC | 8 | S | 607 | X | | | | | | | | | | | | | | | | | | | | |
| 16 | 3S | 16 | AD | 16254 | | | | | | | | | | | | | | | | | | | | |

Explanatory notes [Output] 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output [ETC] S: Storage Register

Status ●: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

Display Decoder / Driver

| Function | V _{OH} (V) | Device | Technology | | | | | | | | | | | | | | | | | | | |
|----------|---------------------|--------|------------|----|-----|----|------|----|-----|--------|-----|-----|---------------|----|-----|-----|------|----|-----|------|-----|-----|
| | | | Bipolar | | | | CMOS | | | BiCMOS | | | Advanced CMOS | | | | | | | | | |
| | | | TTL | LS | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC |
| D | 30 | 45 | ● | | | | | | | | | | | | | | | | | | | |
| D | 60 | 141 | × | | | | | | | | | | | | | | | | | | | |
| D | 15 | 145 | ● | ● | | | | | | | | | | | | | | | | | | |
| D | 7 | 445 | × | | | | | | | | | | | | | | | | | | | |
| 7 | 30 | 46 | × | | | | | | | | | | | | | | | | | | | |
| 7 | 15 | 47 | ● | ● | | | | | | | | | | | | | | | | | | |
| 7 | 5.5 | 48 | × | × | | | | | | | | | | | | | | | | | | |
| 7 | 5.5 | 49 | × | | | | | | | | | | | | | | | | | | | |
| 7 | 30 | 246 | × | | | | | | | | | | | | | | | | | | | |
| 7 | 15 | 247 | × | ● | | | | | | | | | | | | | | | | | | |
| 7 | 7 | 347 | | | | | | | | | | | | | | | | | | | | |
| 7 | 7 | 447 | | | | | | | | | | | | | | | | | | | | |
| 7 | 5.5 | 248 | × | | | | | | | | | | | | | | | | | | | |
| 7 | 5.5 | 249 | × | | | | | | | | | | | | | | | | | | | |
| B | 7 | 142 | × | | | | | | | | | | | | | | | | | | | |
| B | 7 | 143 | × | | | | | | | | | | | | | | | | | | | |
| B | 7 | 144 | × | | | | | | | | | | | | | | | | | | | |

Explanatory notes [Function] D: BCD TO DECIMAL, 7: BCD TO 7-SEGMENT, B: COUNTER/LATCH/DECODER/DRIVER [VOH] Off-Stage Output Voltage (V)

Status ●: Product available in technology indicated * : New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

COMPARATOR

| No. of Bit | Input | P=Q | P̄=Q̄ | P>Q | P<Q | Output | Device | Technology | | | | | | | | | | | | | | | |
|------------|-------|-----|-------|-----|-----|--------|--------|------------|----|-----|----|------|----|-----|--------|-----|-----|---------------|----|-------|-------|------|----|
| | | | | | | | | Bipolar | | | | CMOS | | | BiCMOS | | | Advanced CMOS | | | | | |
| | | | | | | | | TTL | LS | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV |
| 4 | S | Y | N | Y | Y | 2S | 85 | × | ● | ● | × | | | | ×/A/● | -/● | | | | | | | |
| 6 | S | N | Y | N | N | 2S | 29806 | | | × | | | | | | | | | | | | | |
| 8 | 20 | Y | N | N | N | OC | 518 | | | ● | × | | | | | | | | | | | | |
| 8 | 20 | N | Y | N | N | 2S | 520 | | | ● | × | | | | | | | | | ×/A/- | ×/A/- | | |
| 8 | 20 | N | Y | N | N | OC | 522 | | | ● | × | | | | | | | | | | | | |
| 8 | 20 | N | Y | Y | N | 2S | 682 | | ● | | | | | | | | | | | | | | |
| 8 | 20 | N | Y | Y | N | OC | 683 | | × | | | | | | | | | | | | | | |
| 8 | S | Y | N | N | N | OC | 519 | | | × | × | | | | | | | | | | | | |
| 8 | S | N | Y | N | N | 2S | 521 | | | ● | × | | | | | | | | | ×/A/- | ×/A/- | | |
| 8 | S | N | Y | Y | N | 2S | 684 | | ● | | | | | | | | | | | | | | |
| 8 | S | N | Y | Y | N | OC | 685 | | × | | | | | | | | | | | | | | |
| 8 | S | N | Y | Y | N | 2S | 686 | | × | | | | | | | | | | | | | | |
| 8 | S | N | Y | Y | N | OC | 687 | | × | | | | | | | | | | | | | | |
| 8 | S | N | Y | N | N | 2S | 688 | | ● | × | | | | | | | | | | | | | |
| 8 | S | N | Y | N | N | OC | 689 | | × | × | | | | | | | | | | | | | |
| 8 | S | Y | N | Y | Y | 2S | 860 | | | | | | | | | | | | | ×/A/- | ×/A/- | | |
| 8 | S | N | N | Y | Y | 2S | 865 | | | | | | | | | | | | | ×/A/- | ×/A/- | | |
| 8 | LP | N | N | Y | Y | 2S | 866 | | | | | | | | | | | | | ×/A/- | ×/A/- | | |
| 8 | LPQ | Y | N | Y | Y | OC | 866 | | | | | | | | | | | | | | | | |
| 9 | - | N | Y | N | N | 2S | 29809 | | | × | | | | | | | | | | | | | |

Explanatory notes [Input] S: Standard 20: 20-kW Pullup Resistors LP: P-Port Latch LPQ: L,P-port Latch

[P=Q, P̄=Q̄, P>Q, P<Q] Y: Yes N: No

[Output] 2S: Totem Pole Output, OC: Open-Collector Output

Status ●: Product available in technology indicated * : New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCxx

BCT: SN74BCTxx / SN64BCTxx

ADDRESS COMPARATOR / FUSE-PROGRAMMABLE IDENTITY COMPARATOR

| Description | No. of Bit | ETC | Device | Technology | | | | | | | | | | | | | | | | | | | |
|-------------|------------|-----|--------|------------|----|---|-----|------|----|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|
| | | | | Bipolar | | | | CMOS | | | | BiCMOS | | | | Advanced CMOS | | | | | | | |
| | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC |
| A | 16-4 | OE | 677 | | | | ×A | | ×/ | | | | | ×/ | ×/ | | | | | | | | |
| A | 16-4 | L | 678 | | | | × | | ×/ | | | | | ×/ | ×/ | | | | | | | | |
| A | 12-4 | OE | 679 | | | | ● | | ×/ | | | | | | | | | | | | | | |
| A | 12-4 | L | 680 | | | | × | | ×/ | | | | | | | | | | | | | | |
| F | 16 | | 526 | | | | × | | | | | | | | | | | | | | | | |
| F | 12 | | 528 | | | | × | | | | | | | | | | | | | | | | |
| F | 8 | | 527 | | | | × | | | | | | | | | | | | | | | | |

Explanatory notes [Function] A: Address Comparator F: Fuse-Programmable Identity Comparators
[ETC] OE: Output-With Enable L: Output-With Latch

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PARITY GENERATOR / CHECKER

| No. of Bit | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|------------|--------|------------|----|---|-----|------|---|----|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|--|
| | | Bipolar | | | | CMOS | | | | BiCMOS | | | | Advanced CMOS | | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC | |
| 8 | 180 | × | | | | | | ×/ | | | | | | | | | | | | | | | |
| 9 | 250 | | ● | ● | ● | ● | ● | ● | ×/ | ● | | | ×/ | ● | | | | | | | | | |
| 9 | 286 | | | | | ● | × | | | | | | ×/ | ● | | | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

VOLTAGE CONTROLLED OSCILLATOR (VCO)

| Curcuit | Fmax (MHz) | COMPL Z OUT | ENABLE | RANGE INPUT | Rest | PLL | Device | Technology | | | | | | | | | | | | | | | |
|---------|------------|-------------|--------|-------------|------|-----|--------|------------|----|---|-----|------|---|----|-----|--------|-----|-----|------|---------------|-----|-----|------|
| | | | | | | | | Bipolar | | | | CMOS | | | | BiCMOS | | | | Advanced CMOS | | | |
| | | | | | | | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT |
| 1 | 20 | Y | Y | Y | | | 624 | ● | | | | | | | | | | | | | | | |
| | 20 | Y | Y | Y | Y | | 628 | ● | | | | | | | | | | | | | | | |
| | 24 | | | | Y | Y | 7046 | | | | | | | | ● | ● | | | | | | | |
| 2 | 20 | | | | | | 627 | × | | | | | | | | | | | | | | | |
| | 20 | | Y | Y | | | 629 | ● | | | | | | | | | | | | | | | |
| | 20 | Y | | | | | 625 | × | | | | | | | | | | | | | | | |
| | 60 | Y | Y | Y | | | 626 | × | | | | | | | | | | | | | | | |
| | 24 | | | | Y | Y | 4046 | | | | | | | | ● | ● | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ACCUMULATORS / ARITHMETIC LOGIC UNIT (ALU) / LOOK-AHEAD CARRY GENERATOR

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------------|--------|------------|----|---|-----|-----|---|------|-----|-----|--------|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|--|
| | | Bipolar | | | | | | CMOS | | | BICMOS | | | Advanced CMOS | | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC | |
| 4BIT PARALLEL BINARY ACCUMULATORS | 281 | | | X | | | | | | | | | | | | | | | | | | | |
| 4BIT PARALLEL BINARY ACCUMULATORS | 681 | X | | | | | | | | | | | | | | | | | | | | | |
| 4BIT ALU/FUNCTION GENERATORS | 181 | X | ● | X | | ●A | | | | | | | X/H- | X/H- | | | | | | | | | |
| 4BIT ALU/FUNCTION GENERATORS | 381 | X | X | | | X | | | | | | | | | | | | | | | | | |
| 4BIT ALU/FUNCTION GENERATORS | 881 | X | | | | X/A | | | | | | | X/H- | X/H- | | | | | | | | | |
| 4BIT ALU WITH RIFLE CARRY | 362 | X | | | | X | | | | | | | | | | | | | | | | | |
| LOOK AHEAD CARRY GENERATORS | 254 | | | | | X | | | | | | | | | | | | | | | | | |
| LOOK AHEAD CARRY GENERATORS | 182 | X | | X | | X | | | | | | | | | | | | | | | | | |
| LOOK AHEAD CARRY GENERATORS | 282 | | | | | X | | | | | | | | | | | | | | | | | |
| LOOK AHEAD CARRY GENERATORS | 882 | | | | | X/A | | | | | | | X/H- | X/H- | | | | | | | | | |
| QUAD SERIAL ADDER/SUBTRACTOR | 385 | X | | | | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *; New product planned in technology indicated
 X: Discontinued ■: Not recommended for new designs
 HC: SN74HCxx / CD74HCxx
 HCT: SN74HCTxx / CD74HCTxx
 BCT: SN74BCTxx / SN64BCTxx
 AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADDER

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|--------|------------|----|---|-----|----|----|------|-----|-----|--------|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|--|
| | | Bipolar | | | | | | CMOS | | | BICMOS | | | Advanced CMOS | | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC | |
| 4BIT BINARY FULL ADDER | 83 | X | X | | | | | | | | | | | | | | | | | | | | |
| 4BIT BINARY FULL ADDER | 283 | X | ● | ● | | ● | -● | -● | | | | | -/● | -/● | | | | | | | | | |
| DUAL CARRY SAVE FULL ADDER | 183 | X | | | | | | | | | | | | | | | | | | | | | |
| GATED FULL ADDER | 89 | X | | | | | | | | | | | | | | | | | | | | | |
| 2BIT BINARY FULL ADDER | 82 | X | | | | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *; New product planned in technology indicated
 X: Discontinued ■: Not recommended for new designs
 HC: SN74HCxx / CD74HCxx
 HCT: SN74HCTxx / CD74HCTxx
 BCT: SN74BCTxx / SN64BCTxx
 AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MULTIPLIER

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | | |
|---------------------------------|--------|------------|----|---|-----|----|---|------|-----|-----|--------|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|--|
| | | Bipolar | | | | | | CMOS | | | BICMOS | | | Advanced CMOS | | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC | |
| 2-4 PARALLEL BINARY MULTIPLIERS | 261 | X | X | | | | | | | | | | | | | | | | | | | | |
| 4-4 PARALLEL BINARY MULTIPLIERS | 264 | X | | | | | | | | | | | | | | | | | | | | | |
| 4-4 PARALLEL BINARY MULTIPLIERS | 285 | X | | | | | | | | | | | | | | | | | | | | | |
| 2'S COMPLEMENT MULTIPLIERS | 384 | X | | | | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *; New product planned in technology indicated
 X: Discontinued ■: Not recommended for new designs
 HC: SN74HCxx / CD74HCxx
 HCT: SN74HCTxx / CD74HCTxx
 BCT: SN74BCTxx / SN64BCTxx
 AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MEMORY

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | |
|----------------------------|--------|------------|----|---|-----|----|---|------|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|
| | | Bipolar | | | | | | CMOS | | BiCMOS | | | | Advanced CMOS | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC |
| MEMORY REFRESH CONTROLLERS | 600 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY REFRESH CONTROLLERS | 601 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY REFRESH CONTROLLERS | 603 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY CYCLE CONTROLLER | 608 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY MAPPERS | 612 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY MAPPERS | 613 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY MAPPERS WITH LATCH | 610 | × | | | | | | | | | | | | | | | | | | | | |
| MEMORY MAPPERS WITH LATCH | 611 | × | | | | | | | | | | | | | | | | | | | | |
| MULTI-MODE LATCH | 412 | | × | | | | | | | | | | | | | | | | | | | |
| 3-8 MEMORY DECIDER | 2414 | | | | | | | | | ● | | | | | | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CLOCK GENERATOR CIRCUIT

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|--------|------------|----|---|-----|----|---|------|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|
| | | Bipolar | | | | | | CMOS | | BiCMOS | | | | Advanced CMOS | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC |
| QUAD COMPLEMENTARY-OUTPUT LOGIC | 265 | × | | | | | | | | | | | | | | | | | | | | |
| DUAL PULSE SYNCHRONIZERS/DRIVERS | 120 | × | | | | | | | | | | | | | | | | | | | | |
| CRYSTAL-CONTROLLED OSCILLATORS | 320 | × | | | | | | | | | | | | | | | | | | | | |
| CRYSTAL-CONTROLLED OSCILLATORS | 321 | × | | | | | | | | | | | | | | | | | | | | |
| DIGITAL PHASE-LOCK LOOP | 297 | ● | | | | | | ● | ● | | | | | | ● | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SWITCH, SHIFTER, ERROR DETECTION CORRECTION CIRCUIT, HARD DISK DRIVER

| Description | Device | Technology | | | | | | | | | | | | | | | | | | | | |
|---|--------|------------|----|---|-----|----|---|------|-----|--------|-----|-----|------|---------------|-----|-----|------|----|-----|------|-----|-----|
| | | Bipolar | | | | | | CMOS | | BiCMOS | | | | Advanced CMOS | | | | | | | | |
| | | TTL | LS | S | ALS | AS | F | HC | HCT | BCT | ABT | LVT | ALVT | AC | ACT | AHC | AHCT | LV | LVC | ALVC | AVC | AUC |
| QUAD BILATERAL SWITCHES | 4016 | | | | | | | | | | | | | | | | | | | | | |
| QUAD BILATERAL SWITCHES | 4066 | | | | | | | ● | ● | ● | ● | | | | | | | | | | | |
| ANALOG SWITCHES WITH LEVEL TRANSLATION | 4316 | | | | | | | ● | ● | | | | | | | | | | | | | |
| 4BIT SHIFTERS | 350 | | × | | | | | | | | | | | | | | | | | | | |
| 8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT | 636 | × | | | | | | | | | | | | | | | | | | | | |
| | 637 | × | | | | | | | | | | | | | | | | | | | | |
| | 616 | | | | × | | | | | | | | | | | | | | | | | |
| | 617 | | | | | | | | | | | | | | | | | | | | | |
| 16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT | 630 | × | | | | | | | | | | | | | | | | | | | | |
| | 631 | × | | | | | | | | | | | | | | | | | | | | |
| | 632 | | | × | × | | | | | | | | | | | | | | | | | |
| | 633 | | | × | | | | | | | | | | | | | | | | | | |
| | 634 | | | × | × | | | | | | | | | | | | | | | | | |
| | 635 | | | × | | | | | | | | | | | | | | | | | | |
| HARD DISK DRIVER | 1250 | | | × | | | | | | | | | | | | | | | | | | |

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PIN ASSIGNMENTS

Standard

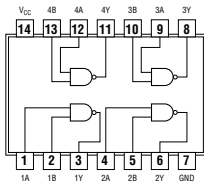
Pin Assignments

00

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \overline{A \cdot B}$$



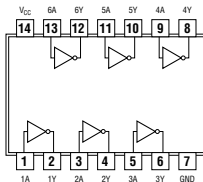
See page 231

04

HEX INVERTERS

positive logic:

$$Y = \overline{A}$$



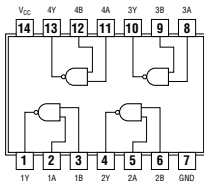
See page 235

01

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$$Y = \overline{A \cdot B}$$



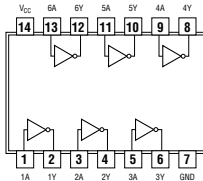
See page 232

U04

HEX INVERTERS

positive logic:

$$Y = \overline{A}$$



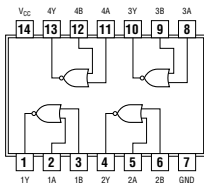
See page 236

02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:

$$Y = \overline{A + B}$$



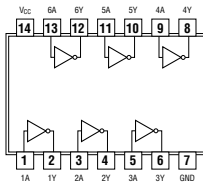
See page 233

05

HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

positive logic:

$$Y = \overline{A}$$



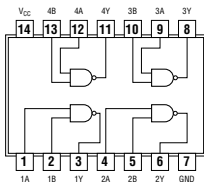
See page 236

03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$$Y = \overline{A \cdot B}$$



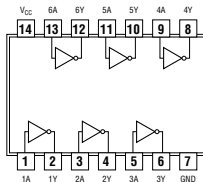
See page 234

06

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

positive logic:

$$Y = \overline{A}$$



See page 237

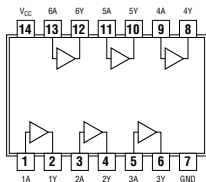
Pin Assignments

07

HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

positive logic:

$$Y = \bar{A}$$



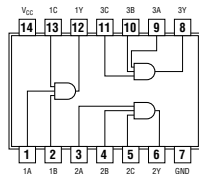
See page 237

11

TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \cdot B \cdot C$$



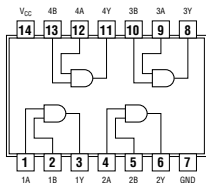
See page 241

08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \cdot B$$



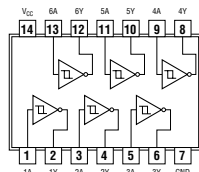
See page 238

14

HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$$Y = \bar{A}$$



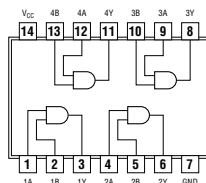
See page 242

09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$$Y = A \cdot B$$



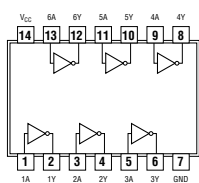
See page 239

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$$Y = \bar{A}$$



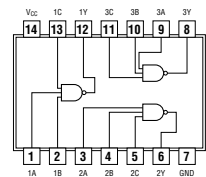
See page 243

10

TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \overline{A \cdot B \cdot C}$$



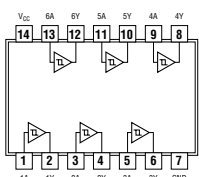
See page 240

17

HEX SCHMITT-TRIGGER BUFFER

positive logic:

$$Y = A$$



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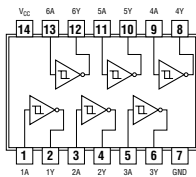
Pin Assignments

19

HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$$Y = \bar{A}$$



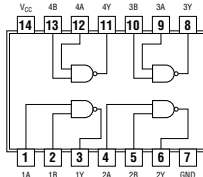
See page 244

26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$$Y = \bar{A}B$$



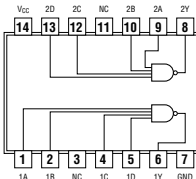
See page 247

20

DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \bar{A}B \cdot \bar{C}D$$



See page 245

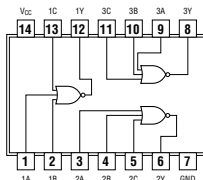
NC-No internal connection

27

TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$$Y = \bar{A} + \bar{B} + \bar{C}$$



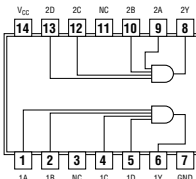
See page 247

21

DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \cdot B \cdot C \cdot D$$



See page 246

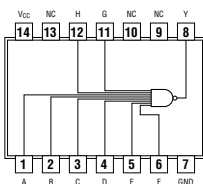
NC-No internal connection

30

8-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} \cdot \bar{G} \cdot \bar{H}$$



See page 248

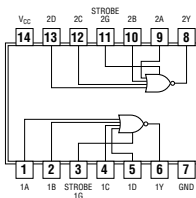
NC-No internal connection

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

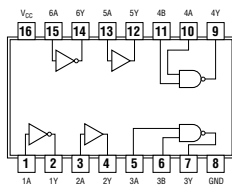
$$Y = G(\bar{A} + \bar{B} + \bar{C} + \bar{D})$$



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31

DELAY ELEMENTS



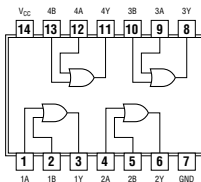
See page 248

Pin Assignments

32

QUADRUPLE 2-INPUT POSITIVE-OR GATES

positive logic:
 $Y = A + B$

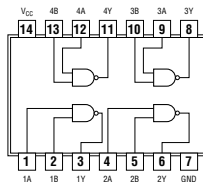


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37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

positive logic:
 $Y = \overline{A \cdot B}$

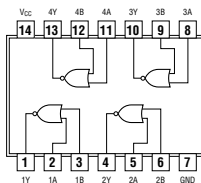


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33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = \overline{A + B}$

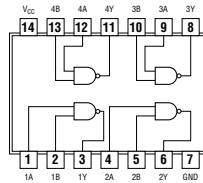


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38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

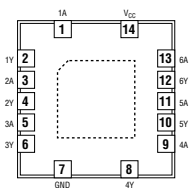
positive logic:
 $Y = \overline{A \cdot B}$



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34

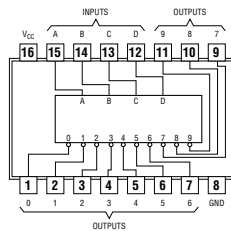
HEX BUFFER GATE



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42

4-LINE-TO-10-LINE DECODERS (1 of 10)

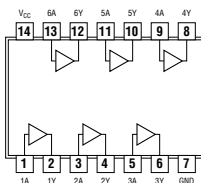


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35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

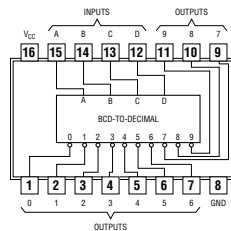
positive logic:
 $Y = A$



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45

BCD-TO-DECIMAL DECODERS/DRIVERS

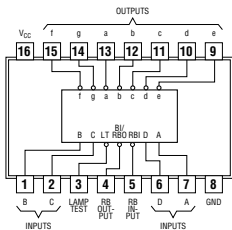


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Pin Assignments

47

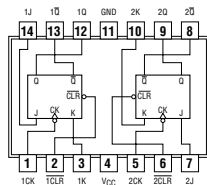
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



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73

DUAL J-K FLIP-FLOPS WITH CLEAR

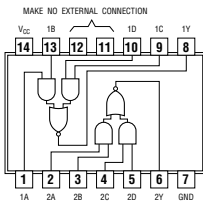


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51

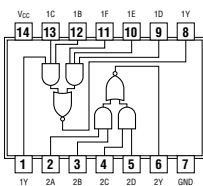
AND-OR-INVERT GATES
'51, 'S51 DUAL 2-WIDE 2-INPUT

positive logic:
 $Y = AB + CD$



AND-OR-INVERT GATES
'LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT

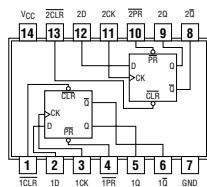
positive logic:
 $1Y = (1A 1B 1C) + (1D 1E 1F)$
 $2Y = (2A 2B) + (2C 2D)$



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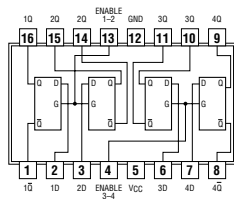
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



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75

4-BIT BISTABLE LATCHES

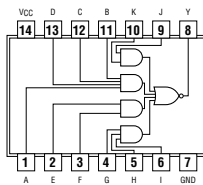


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64

4-2-3-2 INPUT AND-OR INVERT GATES

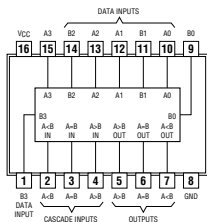
positive logic:
 $Y = ABCD + EF + GHI + JK$



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85

4-BIT MAGNITUDE COMPARATORS



See page 267

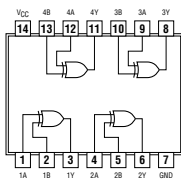
Pin Assignments

86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:

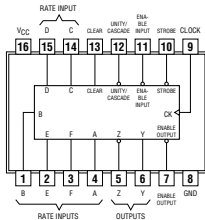
$$Y = A \oplus B \text{ or } Y = \overline{AB} + \overline{A\overline{B}}$$



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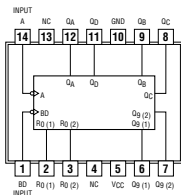
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS



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90

DECADE COUNTER

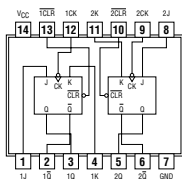


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NC-No internal connection

107

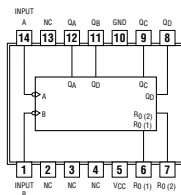
DUAL J-K FLIP-FLOPS WITH CLEAR



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92

DIVIDE-BY-TWELVE DECODE COUNTERS

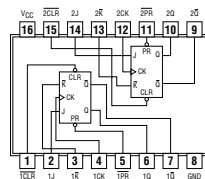


See page 270

NC-No internal connection

109

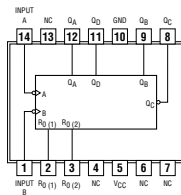
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



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4-BIT BINARY COUNTERS

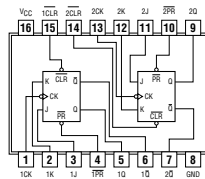


See page 271

NC-No internal connection

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

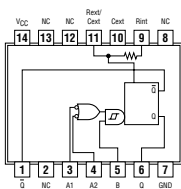


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Pin Assignments

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MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



NC-No internal connection

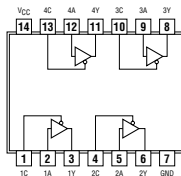
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QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

positive logic:

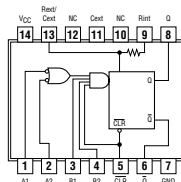
$Y = A$



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RETRIGGERABLE MONOSTABLE MULTIVIBRATORS



NC-No internal connection

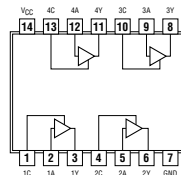
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126

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

positive logic:

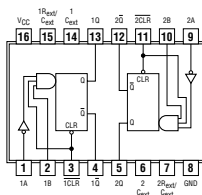
$Y = A$



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123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



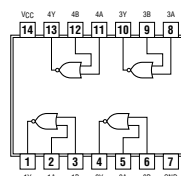
See page 282

128

SN54128...75-Ω LINE DRIVER SN74128...50-Ω LINE DRIVER

positive logic:

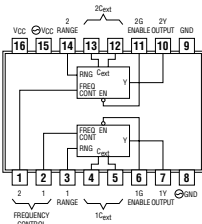
$Y = \overline{A + B}$



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124

DUAL VOLTAGE-CONTROLLED OSCILLATORS



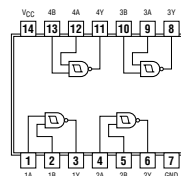
See page 283

132

QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT TRIGGER INPUTS

positive logic:

$Y = \overline{A \cdot B}$



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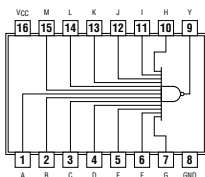
Pin Assignments

133

13-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$$



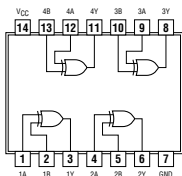
See page 287

136

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

positive logic:

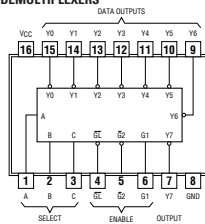
$$Y = A \cdot B = \bar{A}B + A\bar{B}$$



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137

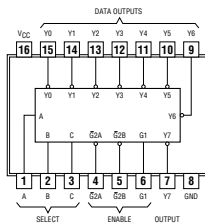
3-LINE TO 8-LINE DECODERS/DEMULTIPLERS WITH ADDRESS LATCHES



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138

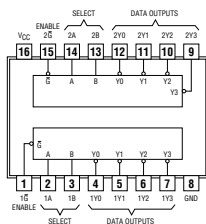
3-LINE TO 8-LINE DECODERS/DEMULTIPLERS



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139

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLERS



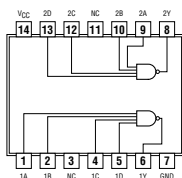
See page 292

140

DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

positive logic:

$$Y = ABCD$$

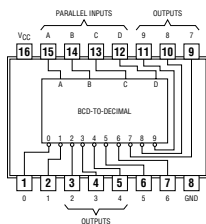


NC-No internal connection

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145

BCD-TO-DECIMAL DECODERS/DRIVERS

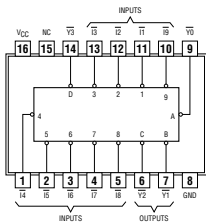


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Pin Assignments

147

10-LINE TO 4-LINE BCD PRIORITY ENCODER

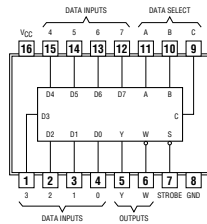


NC-No internal connection

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151

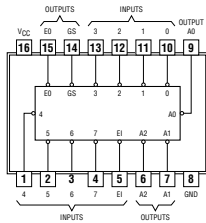
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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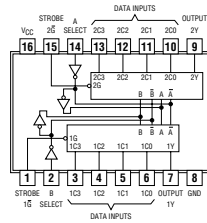
8-LINE TO 3-LINE PRIORITY ENCODERS



See page 298

153

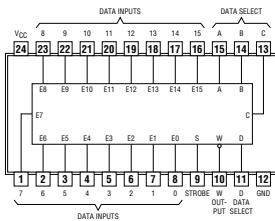
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 304

150

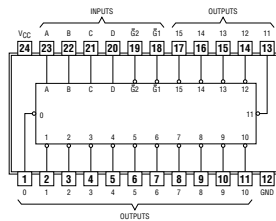
16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



See page 300

154

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS



See page 306

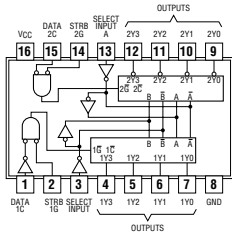
Pin Assignments

155

DUAL 2-LINE TO 4-LINE DECODERS/DEMULPLEXERS

156

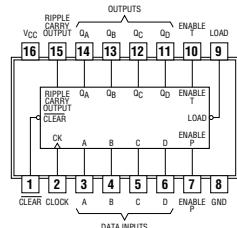
DUAL 2-LINE TO 4-LINE DECODERS/DEMULPLEXERS
WITH OPEN-COLLECTOR OUTPUTS



See page 308, 310

161

163
4-BIT SYNCHRONOUS BINARY COUNTERS

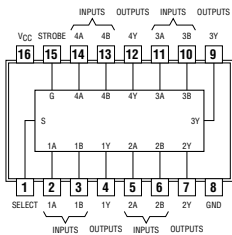


See page 318, 320

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158

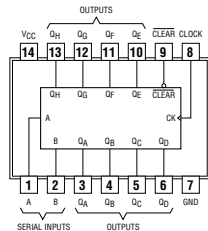
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 312, 314

164

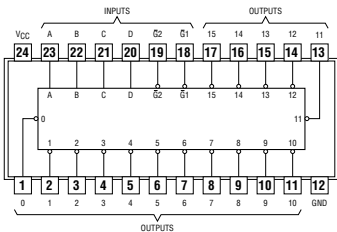
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS



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159

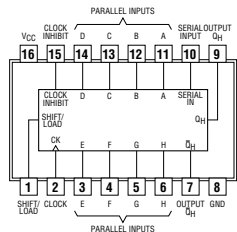
4-LINE TO 16-LINE DECODERS/DEMULPLEXERS
WITH OPEN-COLLECTOR OUTPUTS



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165

PARALLEL-LOAD 8-BIT SHIFT REGISTERS

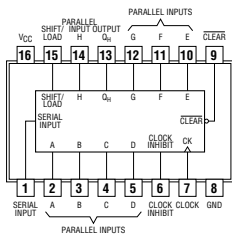


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Pin Assignments

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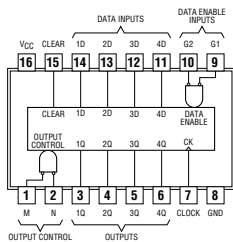
8-BIT PARALLEL-LOAD SHIFT REGISTERS



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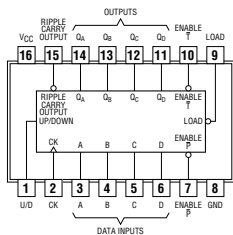
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS



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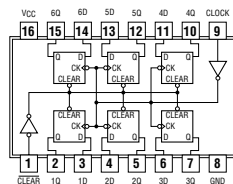
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS



See page 328

174

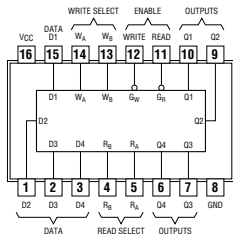
HEX D-TYPE FLIP-FLOPS WITH CLEAR



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170

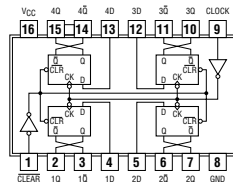
4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS



See page 330

175

QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

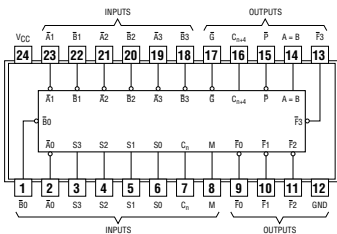


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Pin Assignments

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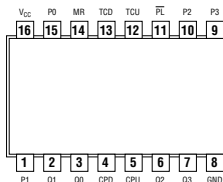
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS



See page 336

192

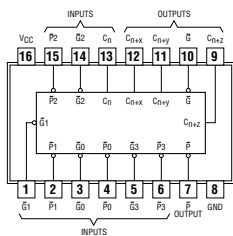
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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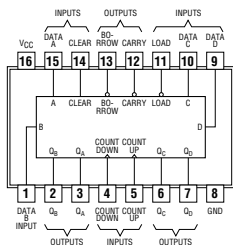
LOOK-AHEAD CARRY GENERATOR



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193

4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)



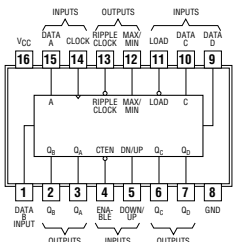
See page 346

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SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

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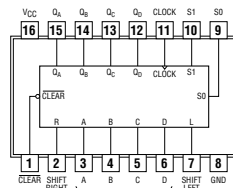
4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS



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194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

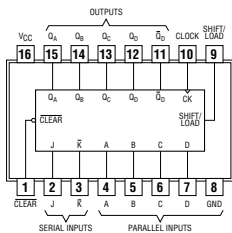


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Pin Assignments

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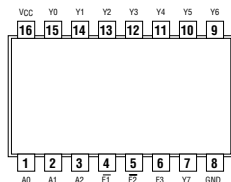
4-BIT PARALLEL-ACCESS SHIFT REGISTERS



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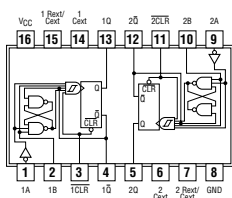
3-LINE TO 8-LINE DECODERS/DEMULPLEXERS



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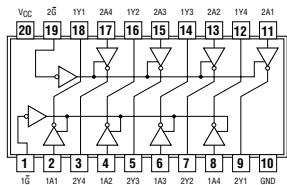
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



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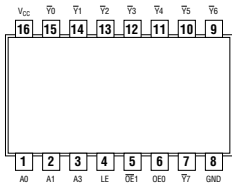
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



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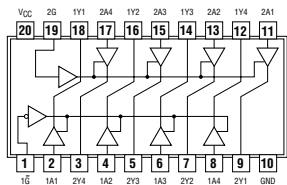
3-LINE TO 8-LINE DECODERS/DEMULPLEXERS WITH ADDRESS LATCHES



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OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

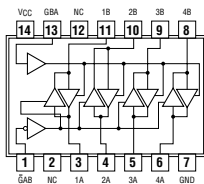


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Pin Assignments

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QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

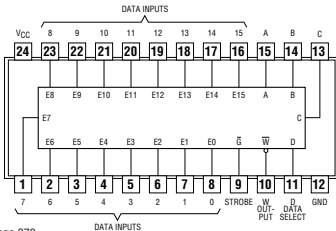


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NC-No internal connection

250

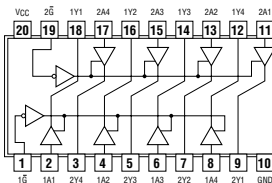
1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



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244

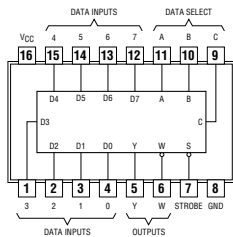
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



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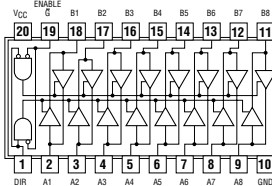
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



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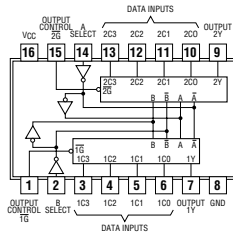
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



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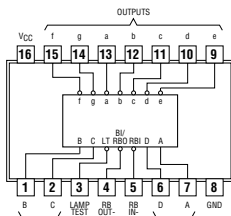
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



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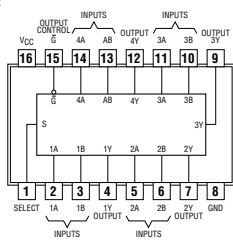
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

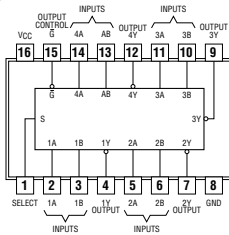


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Pin Assignments

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QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

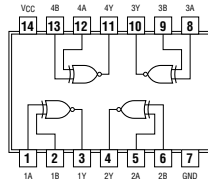


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QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-DRAIN OUTPUTS

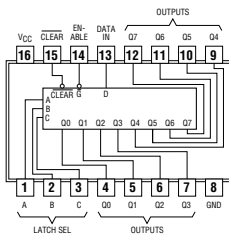
positive logic:
 $Y = A \oplus B$



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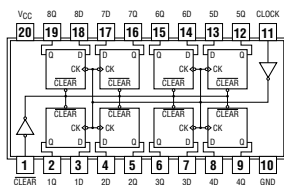
8-BIT ADDRESSABLE LATCHES



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OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

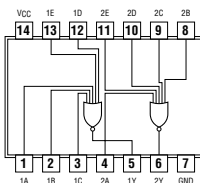


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DUAL 5-INPUT POSITIVE-NOR GATES

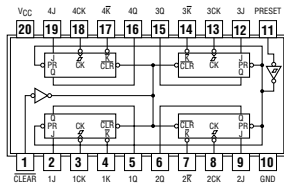
positive logic:
 $Y = A + B + C + D + E$



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QUADRUPLE J-K̄ FLIP-FLOPS

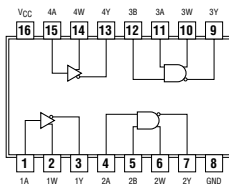


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QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

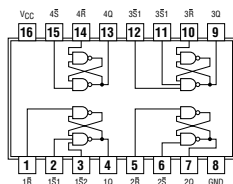
positive logic:
 $Y = \bar{A}, W = A$
 $Y = AB, W = AB$



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QUADRUPLE \bar{S} - \bar{R} LATCHES

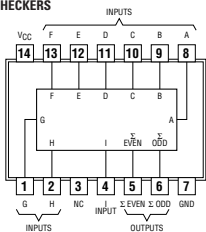


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Pin Assignments

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9-BIT PARITY GENERATORS/CHECKERS

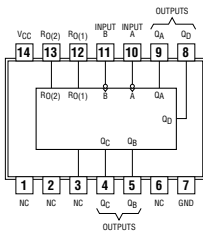


NC-No internal connection

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4-BIT BINARY COUNTERS

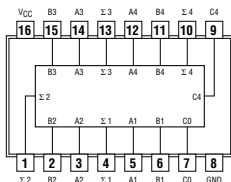


NC-No internal connection

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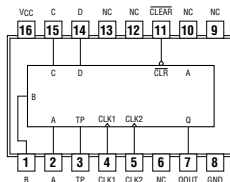
4-BIT BINARY FULL ADDERS WITH FAST CARRY



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PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

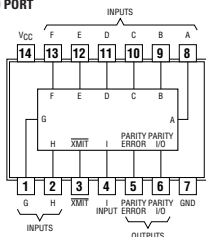


NC-No internal connection

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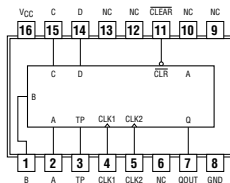
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT



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DIGITAL PHASE-LOCKED-LOOP FILTERS

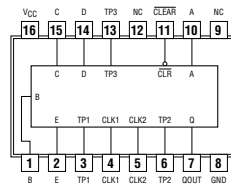


NC-No internal connection

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PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

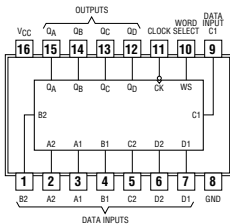


NC-No internal connection

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QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

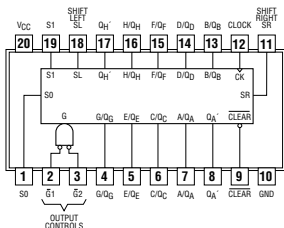


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Pin Assignments

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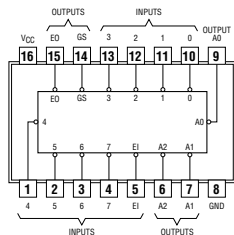
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS



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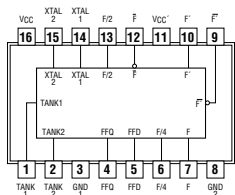
8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS



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CRYSTAL-CONTROLLED OSCILLATORS



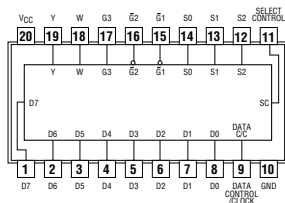
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8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT REGISTERS WITH 3-STATE OUTPUTS

356

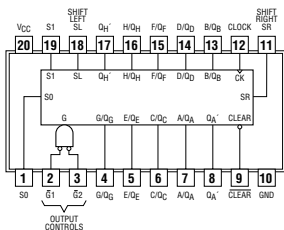
8-INPUT MULTIPLEXER/REGISTERS 3-STATE



See page 412, 414

323

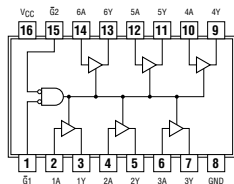
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS



See page 408

365

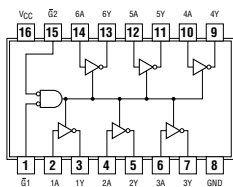
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



See page 416

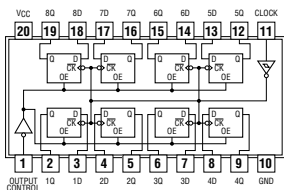
Pin Assignments

366 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



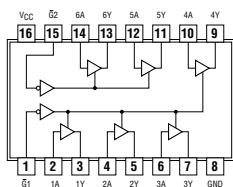
See page 417

374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



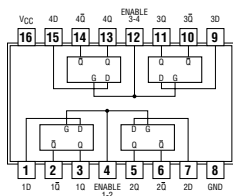
See page 422

367 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



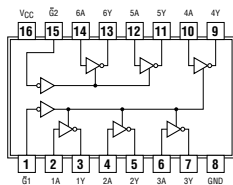
See page 418

375 4-BIT BISTABLE LATCHES



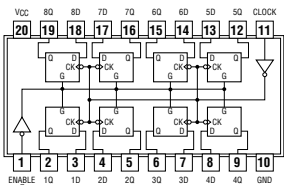
See page 424

368 HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



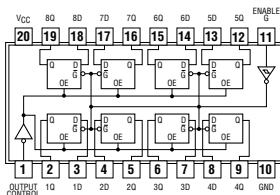
See page 419

377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE



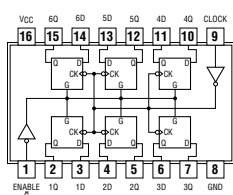
See page 425

373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 420

378 HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

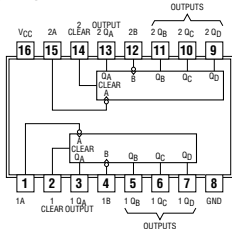


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Pin Assignments

390

DUAL 4-BIT DECADE COUNTERS

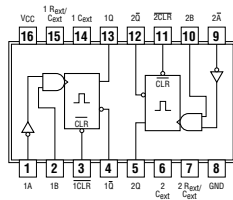


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423

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

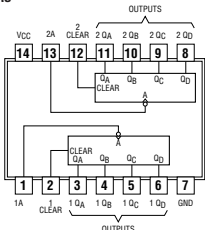
positive logic.
Y = A



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393

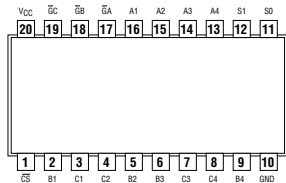
DUAL 4-BIT BINARY COUNTERS



See page 428

442

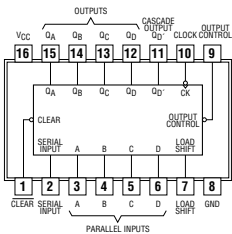
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS



See page 432

395

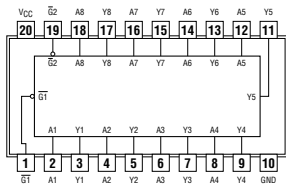
CASCADABLE SHIFT REGISTERS



See page 429

465

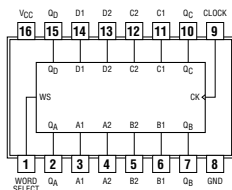
OCTAL BUFFERS WITH 3-STATE OUTPUTS



See page 433

399

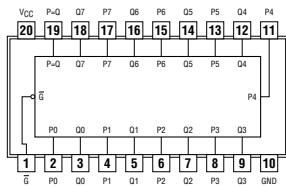
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE



See page 430

518

OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

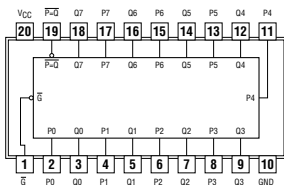


See page 433

Pin Assignments

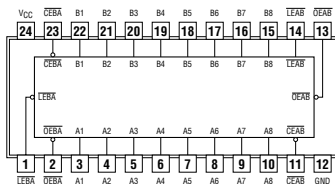
520 OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

521 8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS



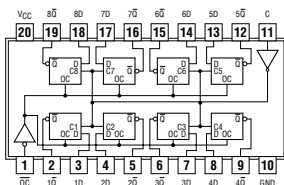
See page 434, 435

543 OCTAL REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS



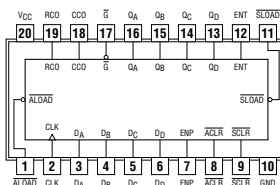
See page 440

533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



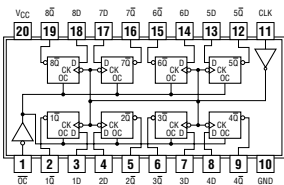
See page 436

561 SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS



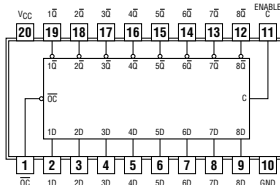
See page 442

534 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



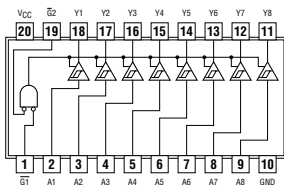
See page 437

563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



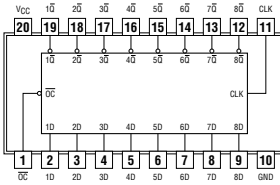
See page 444

540 541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 438, 439

564 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

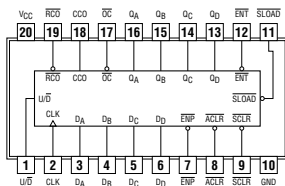


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Pin Assignments

569

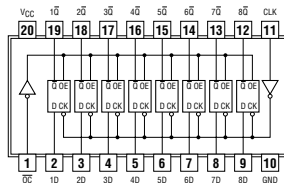
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS



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576

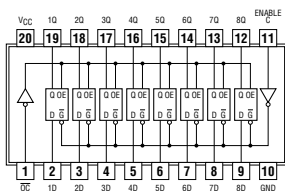
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



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573

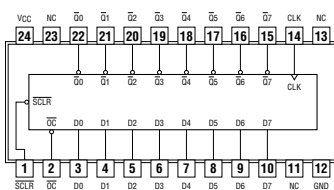
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



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577

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

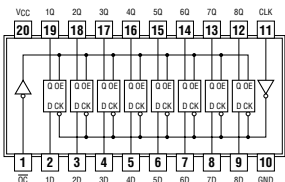


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NC-No internal connection

574

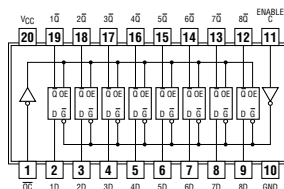
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



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580

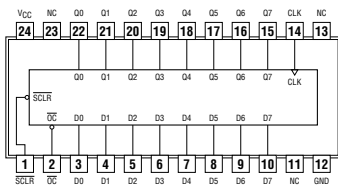
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



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575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

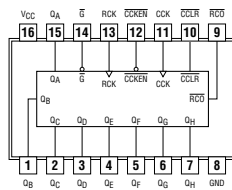


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NC-No internal connection

590

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

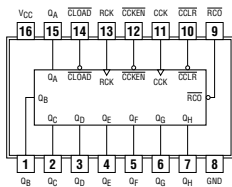


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Pin Assignments

592

8-BIT BINARY COUNTERS WITH INPUT REGISTERS



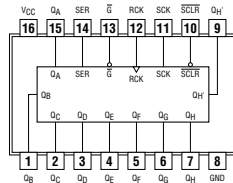
See page 458

595

8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

596

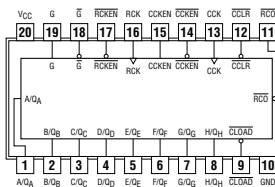
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES



See page 464, 466

593

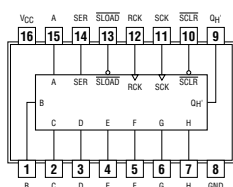
8-BIT BINARY COUNTERS WITH INPUT REGISTERS



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597

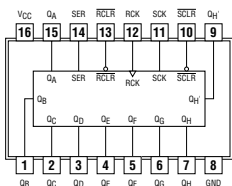
SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES



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594

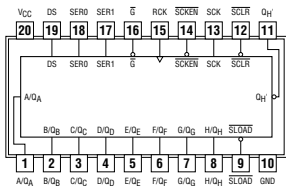
8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS



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598

8-BIT SHIFT REGISTERS WITH INPUT LATCHES



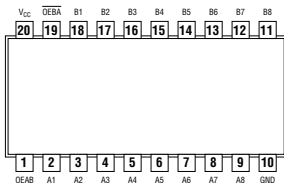
See page 470

Pin Assignments

620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

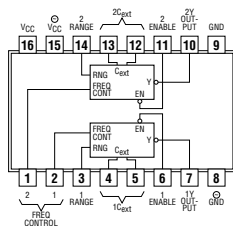
621 OCTAL BUS TRANSCEIVERS

623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



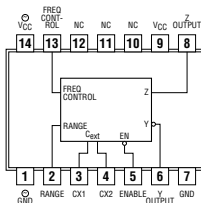
See page 472, 473, 474

629 DUAL VOLTAGE-CONTROLLED OSCILLATORS



See page 477

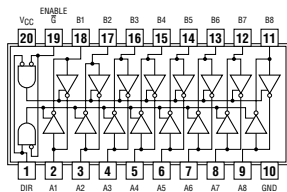
624 VOLTAGE-CONTROLLED OSCILLATORS



NC-No internal connection

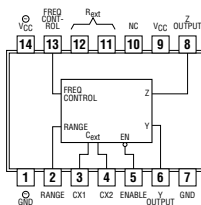
See page 475

638 OCTAL BUS TRANSCEIVERS



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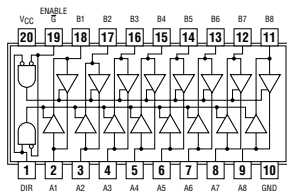
628 VOLTAGE-CONTROLLED OSCILLATORS



NC-No internal connection

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639 OCTAL BUS TRANSCEIVERS



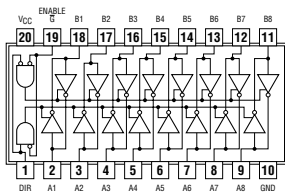
See page 479

640

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

642

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS



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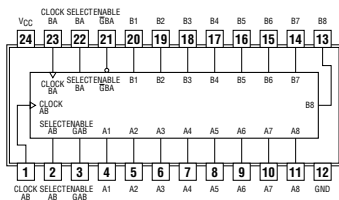
651

652

653

654

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



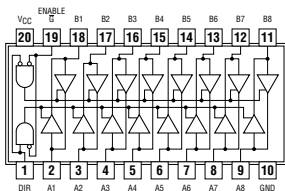
See page 490, 492, 494, 496

641

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

645

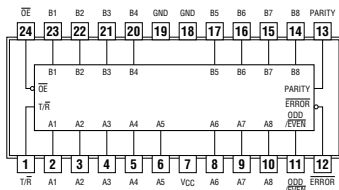
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



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657

OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



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646

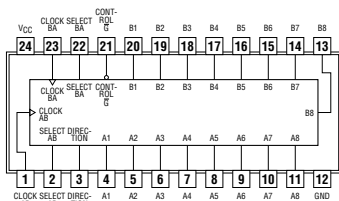
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

647

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

648

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

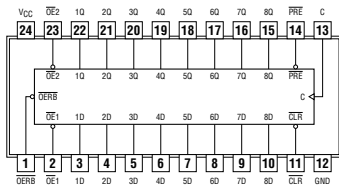


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666

667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

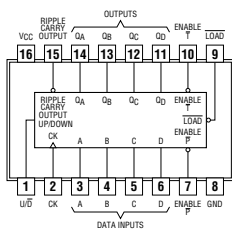


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Pin Assignments

669

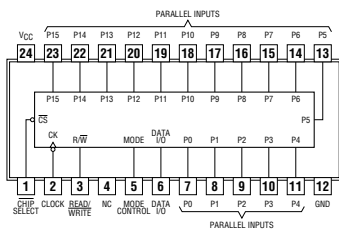
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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674

16-BIT SHIFT REGISTERS

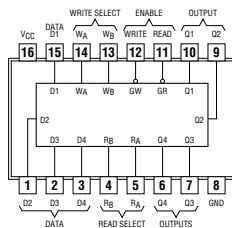


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NC-No internal connection

670

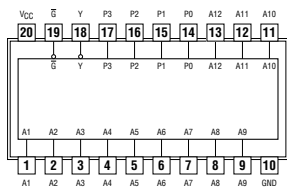
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS



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679

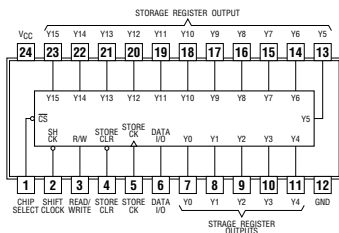
12-BIT ADDRESS COMPARATOR



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673

16-BIT SHIFT REGISTERS

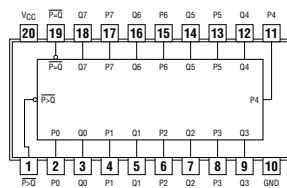


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684

8-BIT MAGNITUDE COMPARATORS

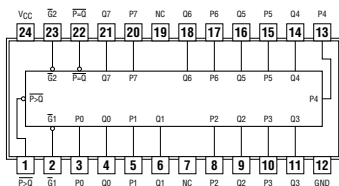


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Pin Assignments

686

8-BIT MAGNITUDE/IDENTITY COMPARATORS

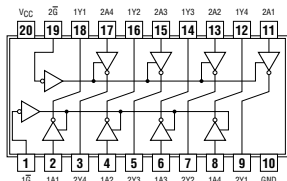


NC-No internal connection

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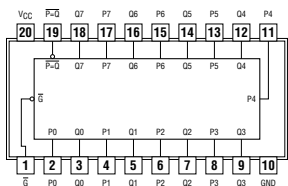
OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS



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688

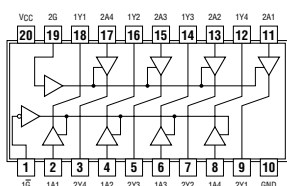
8-BIT IDENTITY COMPARATORS



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757

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

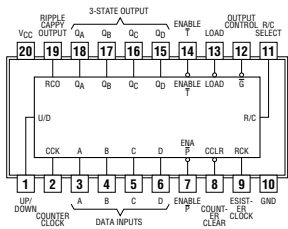


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699

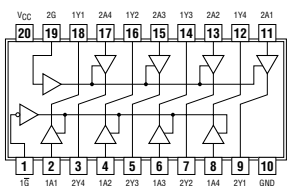
SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS



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760

OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS



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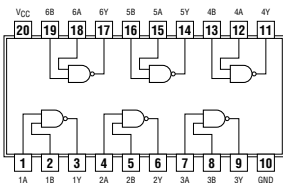
Pin Assignments

804

HEX 2-INPUT NAND DRIVERS

positive logic:

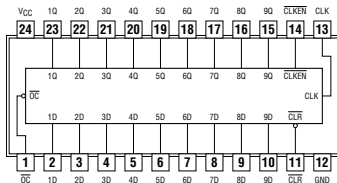
$$Y = A \cdot B$$



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823

9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



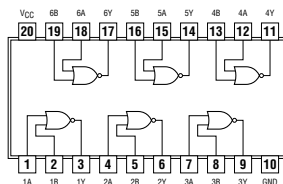
See page 530

805

HEX 2-INPUT NOR DRIVERS

positive logic:

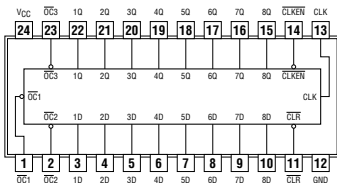
$$Y = A + B$$



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825

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



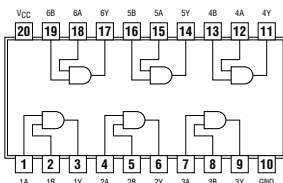
See page 531

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HEX 2-INPUT AND DRIVERS

positive logic:

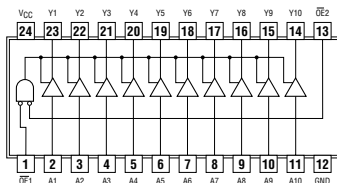
$$Y = A + B$$



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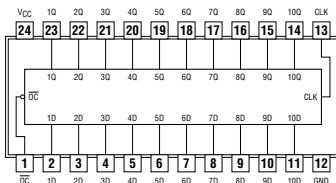
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 532

821

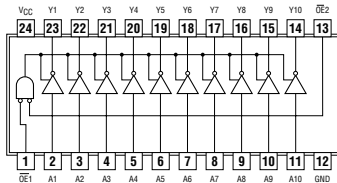
10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS



See page 529

828

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 532

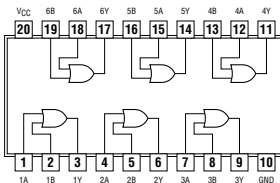
Pin Assignments

832

HEX 2-INPUT OR DRIVERS

positive logic:

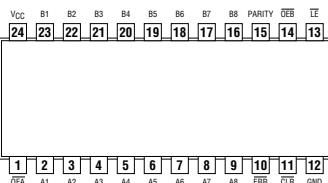
$$Y = A + B$$



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853

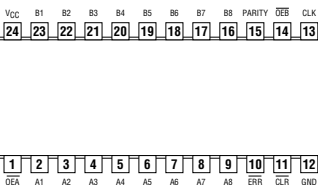
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 538

833

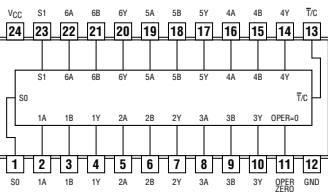
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 534

857

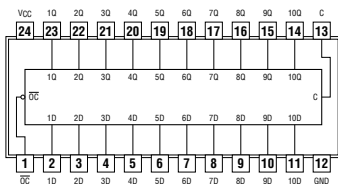
HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS



See page 540

841

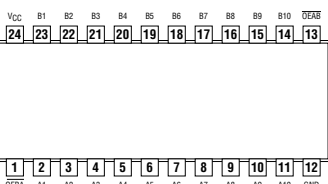
10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 536

861

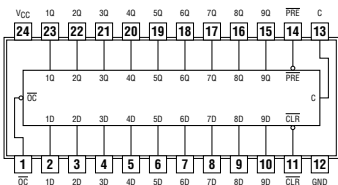
10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 542

843

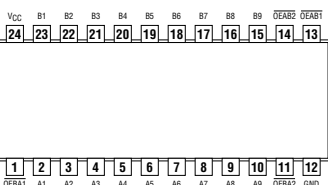
9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 537

863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

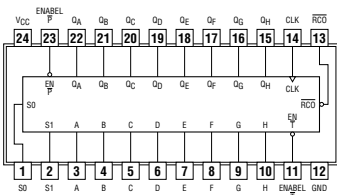


See page 543

867

869

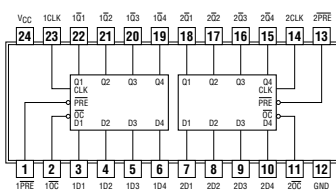
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS



See page 544, 546

876

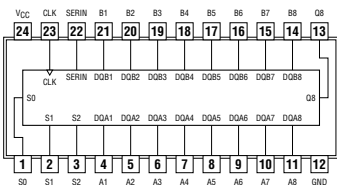
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 552

870

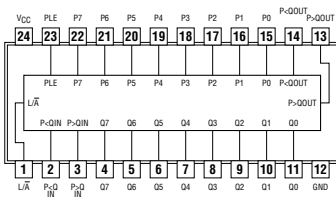
DUAL 16-BY 4-BIT REGISTER FILES



See page 548

885

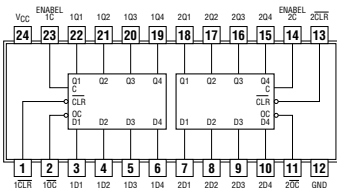
8-BIT MAGNITUDE COMPARATORS



See page 554

873

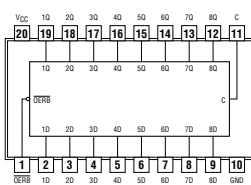
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 550

990

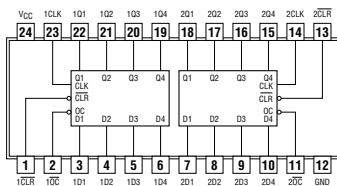
8-BIT D-TYPE TRANSPARENT READ-BACK LATCH



See page 556

874

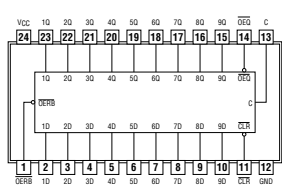
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 551

992

9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

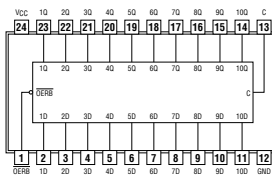


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Pin Assignments

994

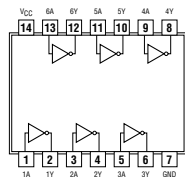
10-BIT D-TYPE TRANSPARENT READ-BACK LATCH



See page 558

1005

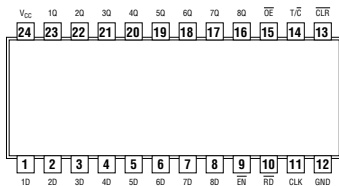
HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



See page 561

996

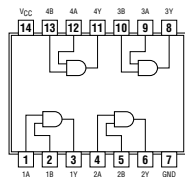
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES



See page 559

1008

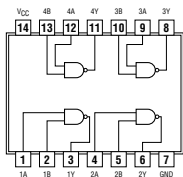
QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER



See page 561

1000

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

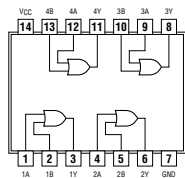


See page 560

1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

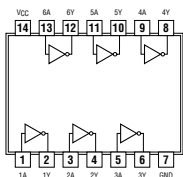
positive logic:
 $Y = A + B$



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1004

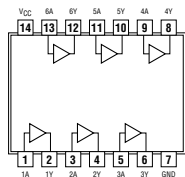
HEX INVERTING DRIVERS



See page 560

1034

HEX DRIVERS

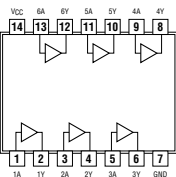


See page 562

Pin Assignments

1035

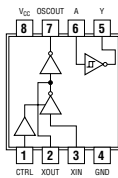
HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



See page 563

1404

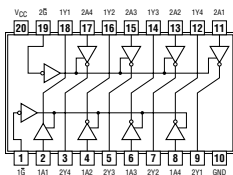
OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR



See page 565

1240

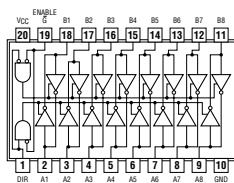
OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS



See page 563

1640

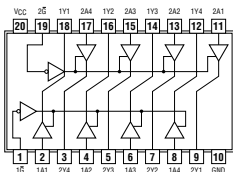
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 566

1244

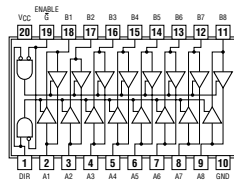
OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS



See page 564

1645

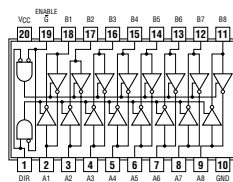
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 567

1245

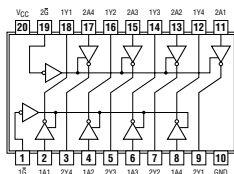
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 564

2240

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

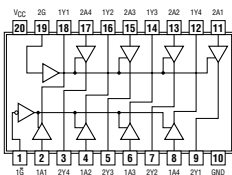


See page 568

Pin Assignments

2241

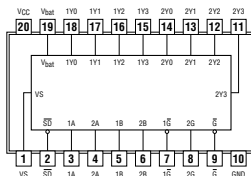
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



See page 569

2414

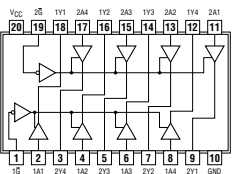
MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR



See page 573

2244

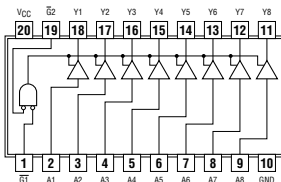
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



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2541

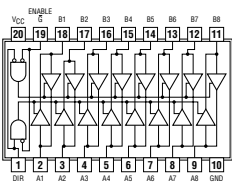
OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS



See page 574

2245

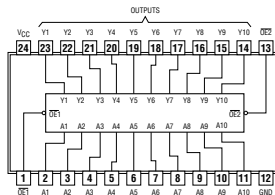
OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



See page 571

2827

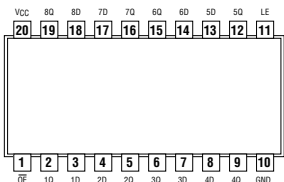
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 574

2373

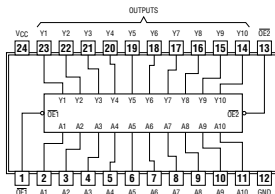
25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS



See page 572

2828

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING

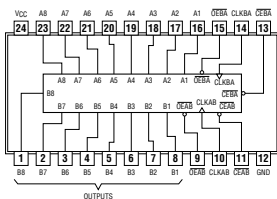


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Pin Assignments

2952

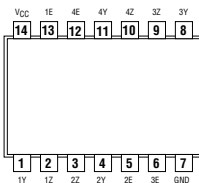
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



See page 576

4016

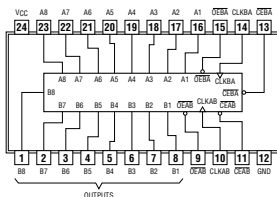
QUAD BILATERAL SWITCH



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2953

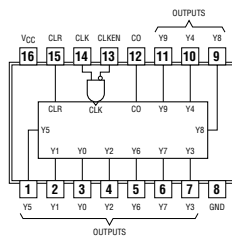
OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS



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4017

DECADE COUNTERS/DIVIDER

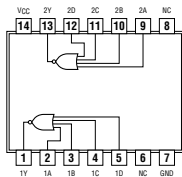


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4002

DUAL 4-INPUT POSITIVE-NOR GATES

positive logic:
 $Y = \overline{A + B + C + D}$

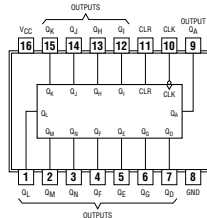


NC-No internal connection

See page 579

4020

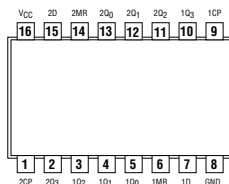
14-STAGE BINARY COUNTERS



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4015

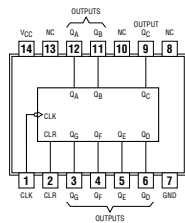
DUAL 4-STAGE STATIC SHIFT REGISTER



See page 580

4024

7-STAGE BINARY COUNTERS

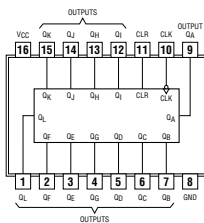


NC-No internal connection

See page 584

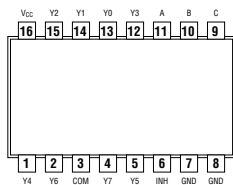
Pin Assignments

4040 12-STAGE BINARY COUNTERS



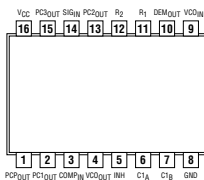
See page 585

4051 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



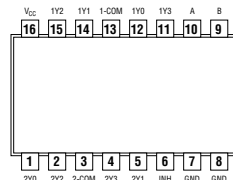
See page 589

4046 PHASE-LOCKED-LOOP WITH VCO



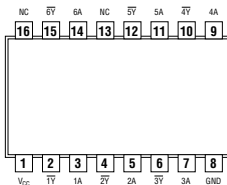
See page 586

4052 DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



See page 590

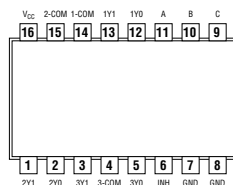
4049 HEX INVERTING BUFFERS



NC-No internal connection

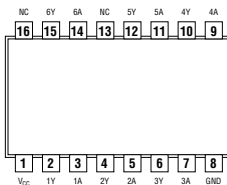
See page 588

4053 TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



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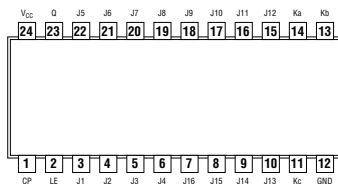
4050 HEX NON-INVERTING BUFFERS



NC-No internal connection

See page 588

4059 CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

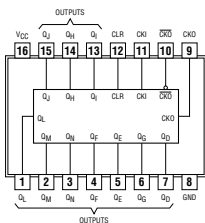


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Pin Assignments

4060

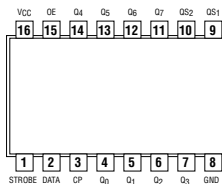
ASYNCHRONOUS 14-STAGE BINARY COUNTERS
AND OSCILLATORS



See page 593

4094

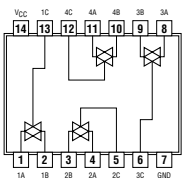
8-STAGE SHIFT AND STORE BUS REGISTER,
THREE-STATE



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4066

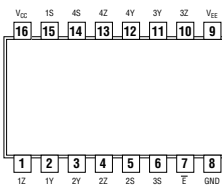
QUADRUPLE BILATERAL SWITCHES



See page 594

4316

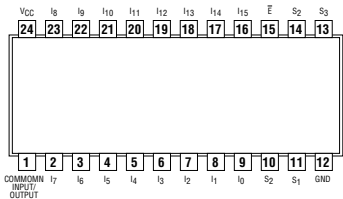
QUAD ANALOG SWITCH WITH LEVEL TRANSLATION



See page 598

4067

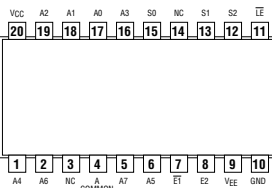
16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



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4351

ANALOG MULTIPLEXERS/DEMULTIPLEXERS
WITH LATCH



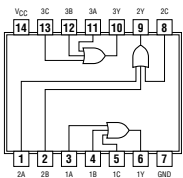
See page 599

NC-No internal connection

4075

TRIPLE 3-INPUT OR GATES

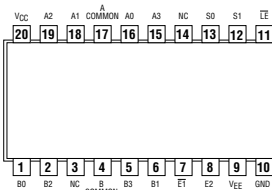
positive logic:
 $Y = A + B + C$



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4352

ANALOG MULTIPLEXERS/DEMULTIPLEXERS
WITH LATCH



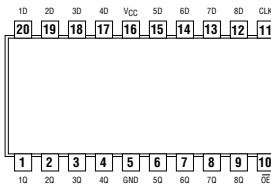
See page 600

NC-No internal connection

Pin Assignments

4374

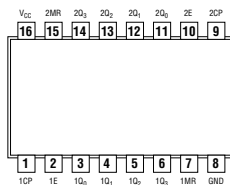
OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK
FLIP-FLOP WITH 3-STAE OUTPUTS



See page 601

4518

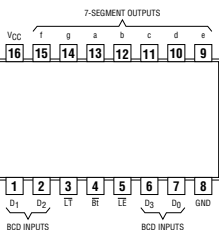
DUAL SYNCHRONOUS COUNTERS



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4511

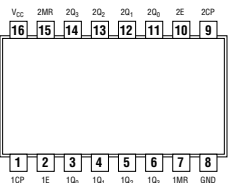
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



See page 602

4520

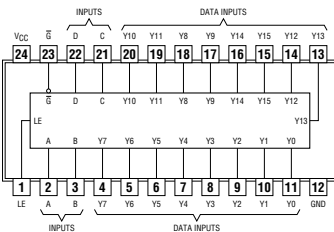
DUAL SYNCHRONOUS COUNTERS



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4514

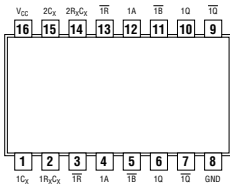
4-LINE TO 16-LINE DECODERS/DEMULTIPLXERS WITH INPUT LATCHES



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4538

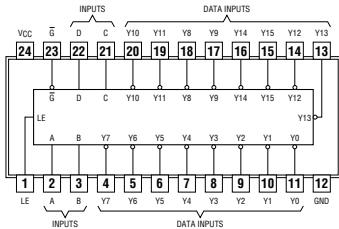
DUAL RETRIGGERABLE
PRECISION MONO STABLE MULTIVIBRATOR



See page 608

4515

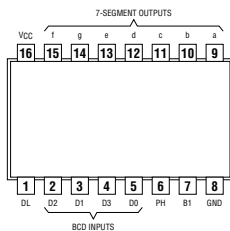
4-LINE TO 16-LINE DECODERS/DEMULTIPLXERS WITH INPUT LATCHES



See page 605

4543

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

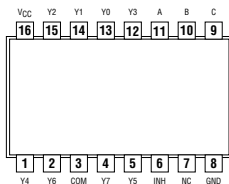


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Pin Assignments

4851

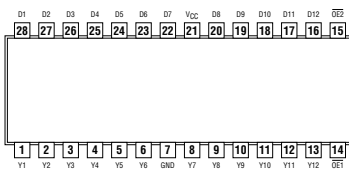
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL



See page 612

5402

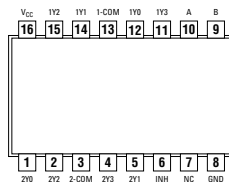
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



See page 615

4852

DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

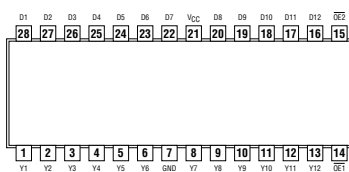


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NC-No internal connection

5403

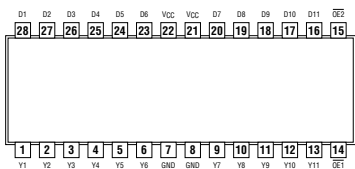
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



See page 615

5400

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

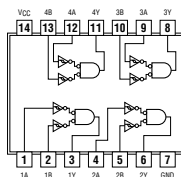


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7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

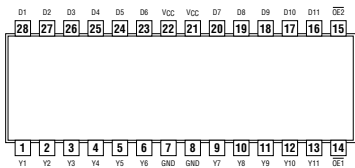
positive logic:
 $Y = A \cdot B$



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5401

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

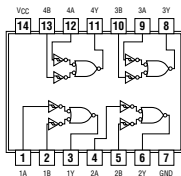


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7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:
 $Y = A + B$

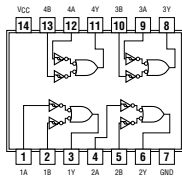


See page 616

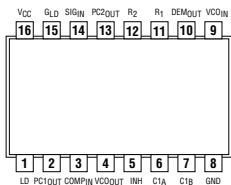
7032**QUADRUPLE POSITIVE-OR GATES
WITH SCHMITT-TRIGGER INPUTS**

positive logic:

$$Y = A + B$$



See page 617

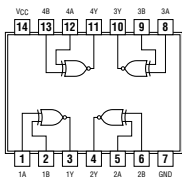
7046**PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR**

See page 618

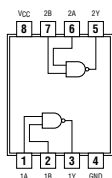
7266**QUAD 2-INPUT EXCLUSIVE-NOR GATES**

positive logic:

$$Y = \overline{A} \oplus \overline{B}$$



See page 619

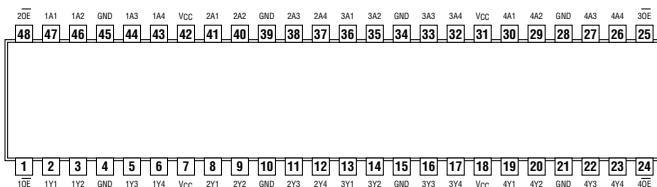
8003**DUAL 2-INPUT POSITIVE-NAND GATES**

See page 619

Pin Assignments

16240

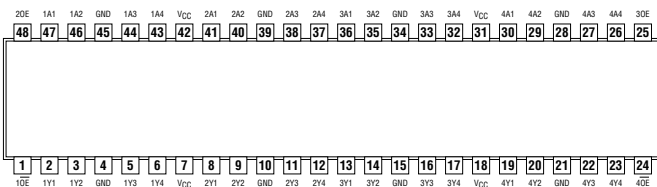
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 620

16241

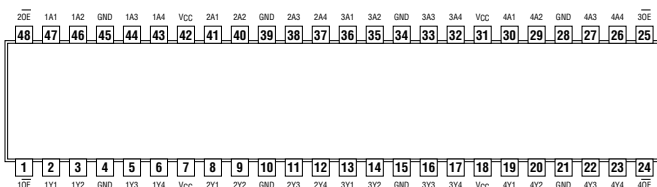
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 622

16244

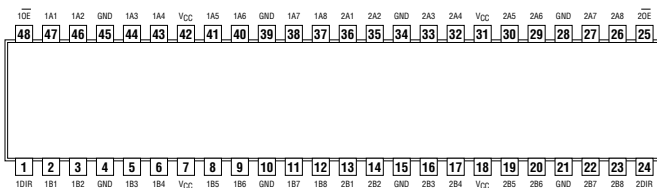
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 624

16245

16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

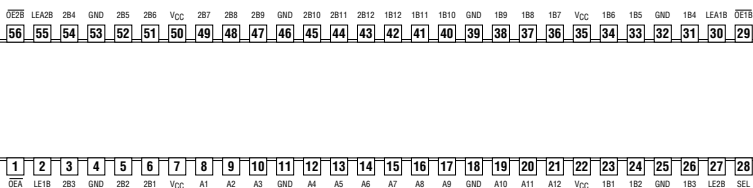


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Pin Assignments

16260

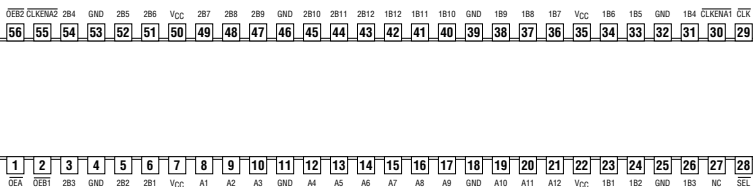
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH
WITH 3-STATE OUTPUTS



See page 628

16269

12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

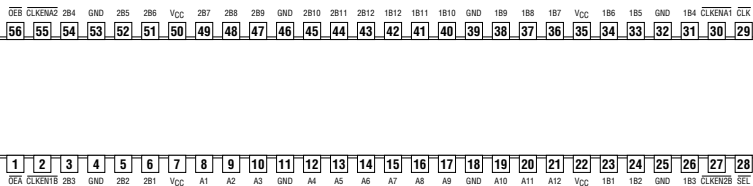


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NC-No internal connection

16270

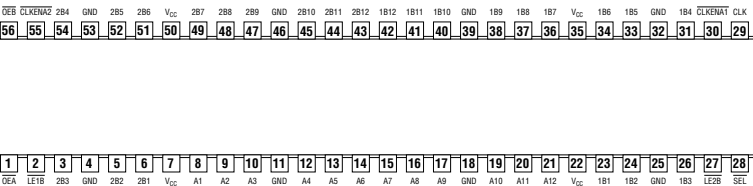
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



See page 632

16271

12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER
WITH 3-STATE OUTPUTS

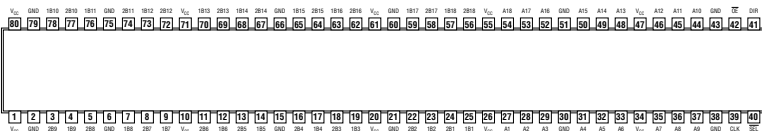


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Pin Assignments

16282

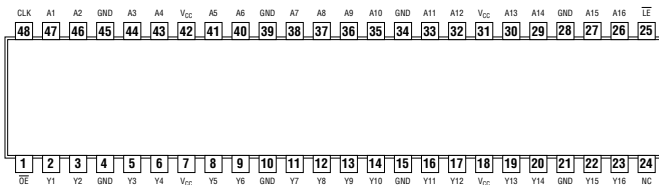
18-BIT TO 36-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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16344

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

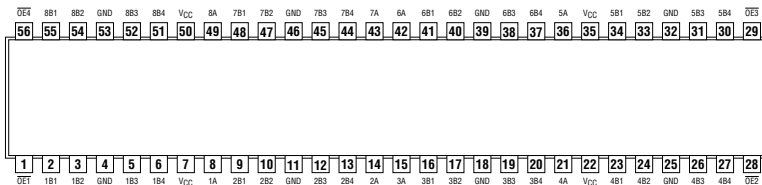


NC-No internal connection

See page 638

16344

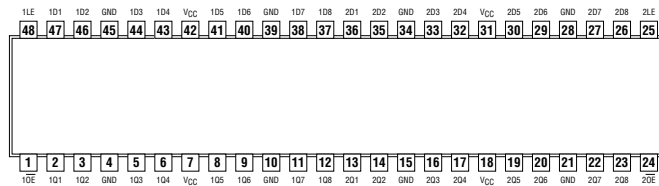
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



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16373

16-BIT TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

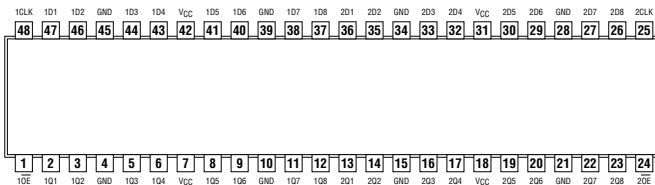


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Pin Assignments

16374

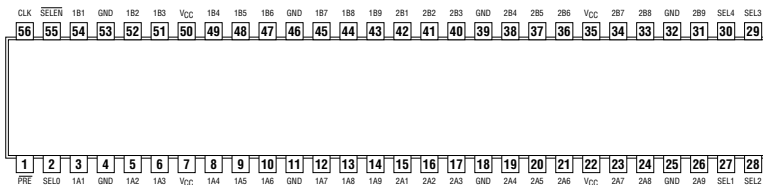
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



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16409

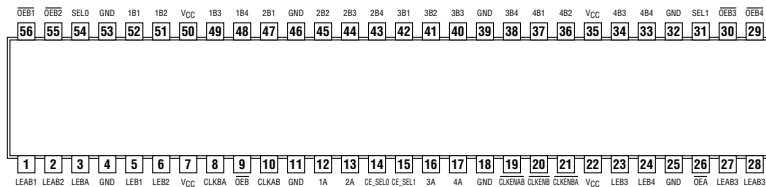
9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER
WITH 3-STATE OUTPUTS



See page 646

16460

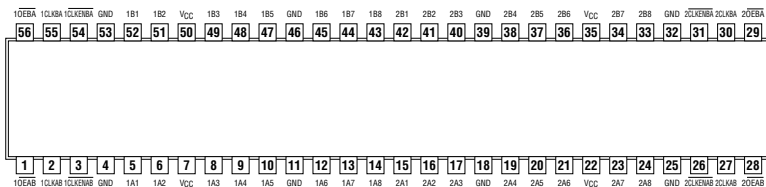
4-T0-1 MULTIPLEXED/DEMULPLEXED TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16470

16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

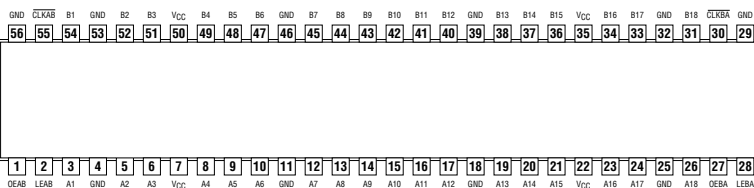


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Pin Assignments

16500

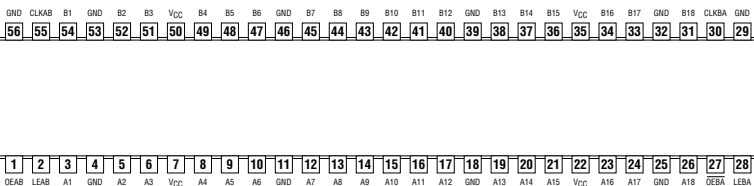
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16501

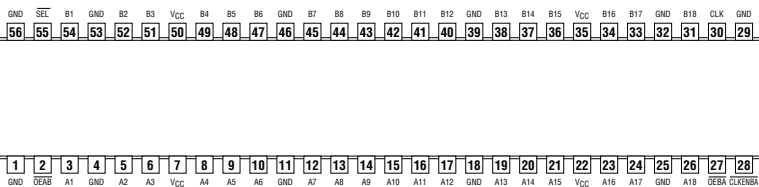
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16524

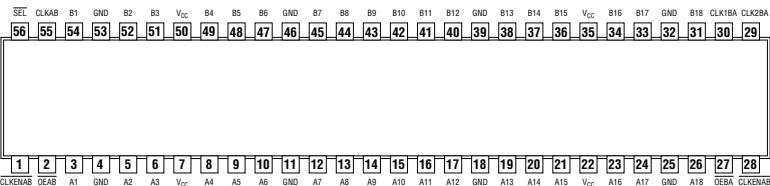
18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16525

18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

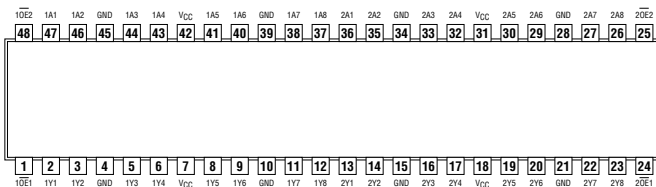


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Pin Assignments

16540

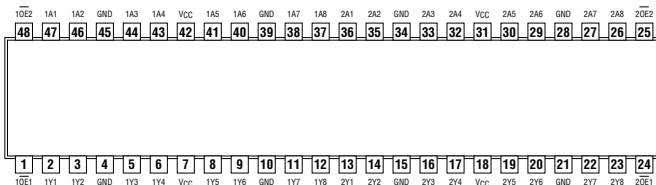
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16541

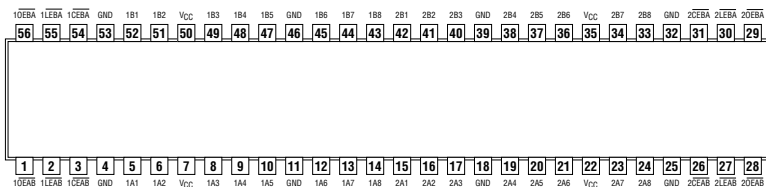
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 661

16543

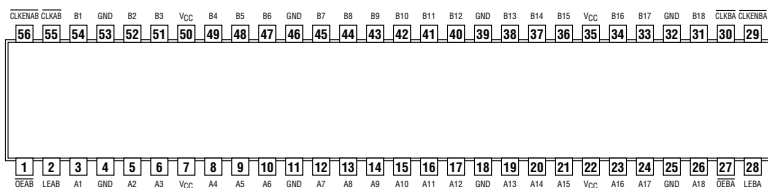
16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16600

18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

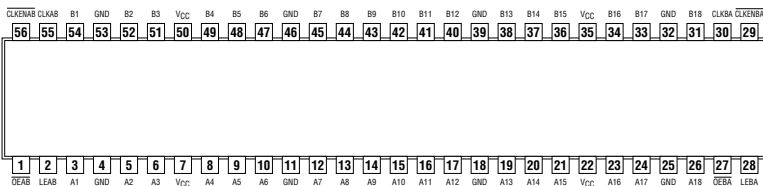


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Pin Assignments

16601

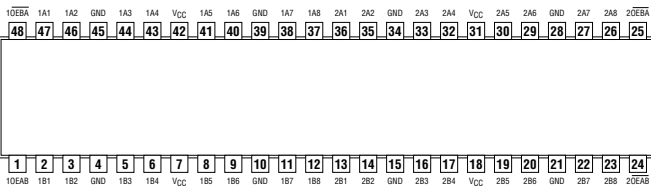
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16620

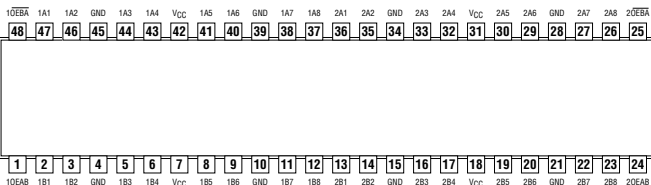
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16623

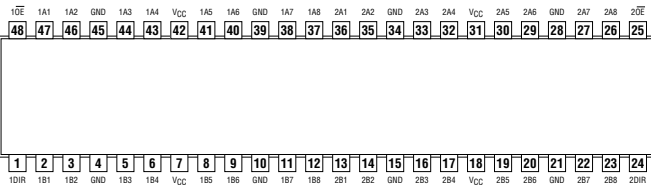
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16640

16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

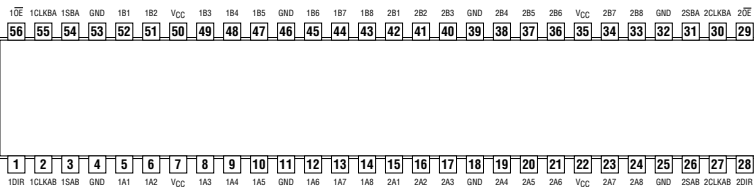


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Pin Assignments

16646

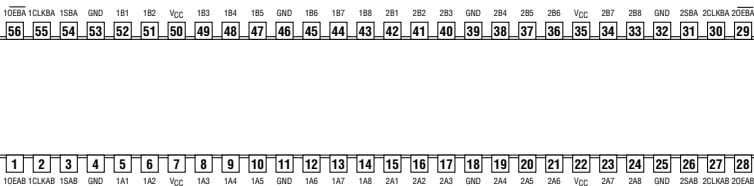
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16651

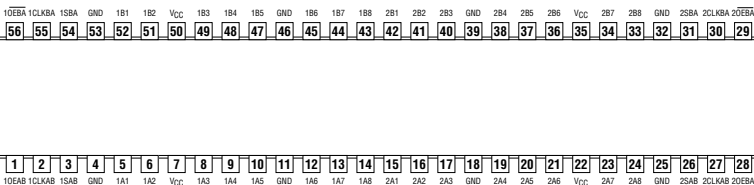
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16652

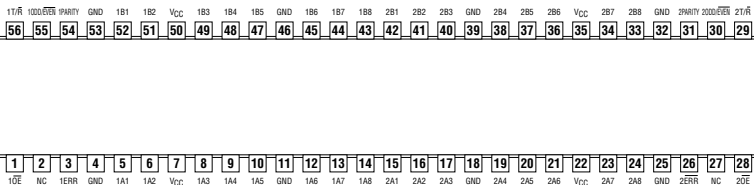
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16657

16-BIT TRANSCEIVERS
WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



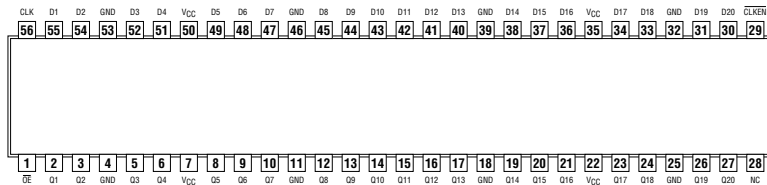
See page 678

NC-No internal connection

Pin Assignments

16721

20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

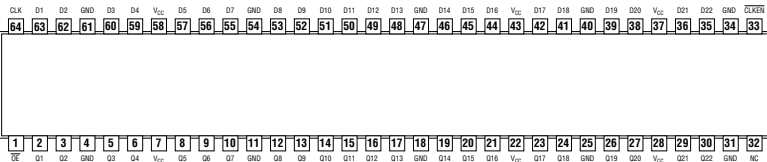


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NC-No internal connection

16722

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

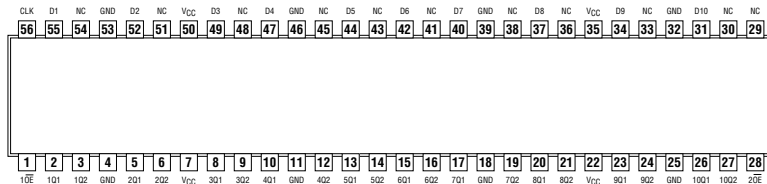


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NC-No internal connection

16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH DUAL OUTPUTS

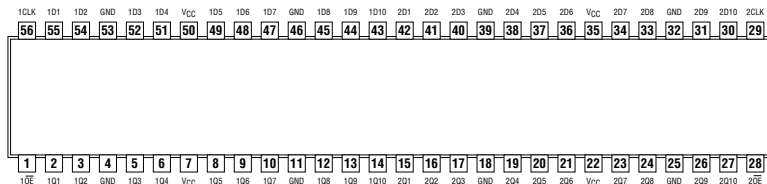


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NC-No internal connection

16821

20-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

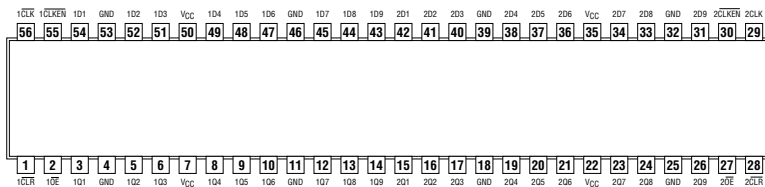


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Pin Assignments

16823

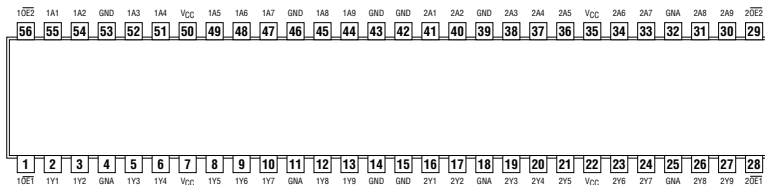
18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH DUAL OUTPUTS



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16825

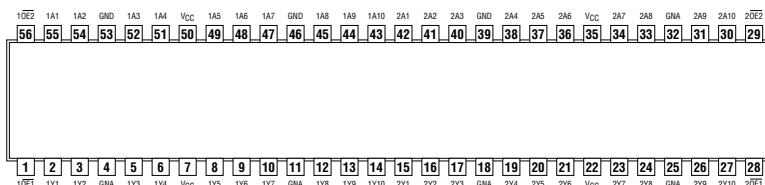
18-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16827

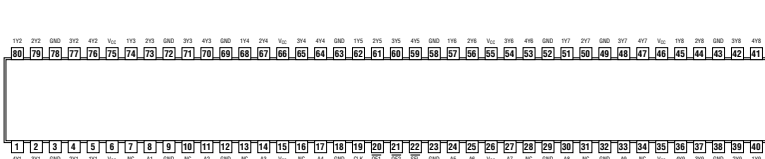
20-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16831

1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS



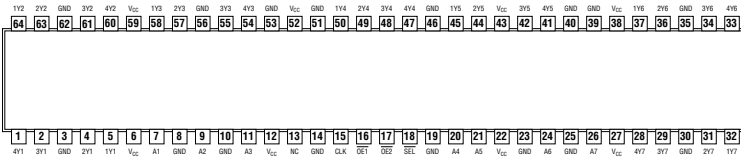
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NC-No internal connection

Pin Assignments

16832

**1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS**

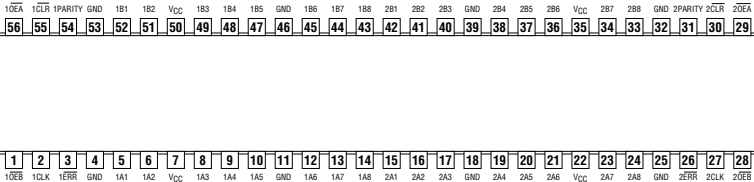


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NC-No internal connection

16833

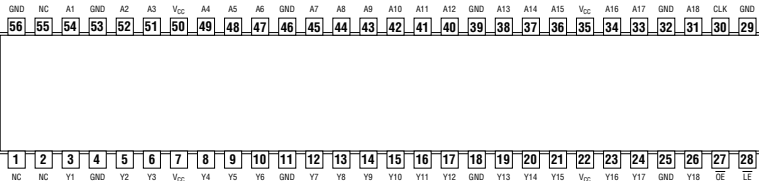
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



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16834

**16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS**

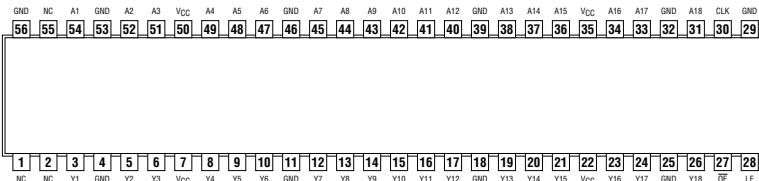


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NC-No internal connection

16835

**3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS**



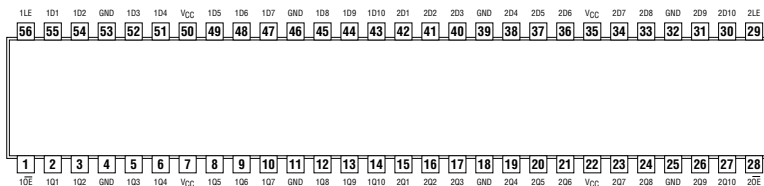
See page 693

NC-No internal connection

Pin Assignments

16841

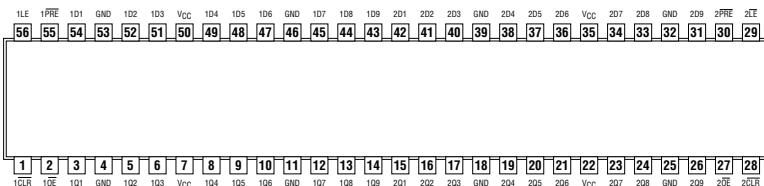
20-BIT BUS INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS



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16843

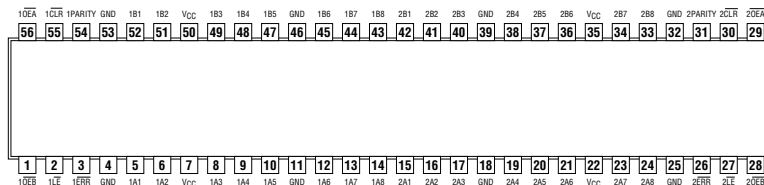
18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



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16853

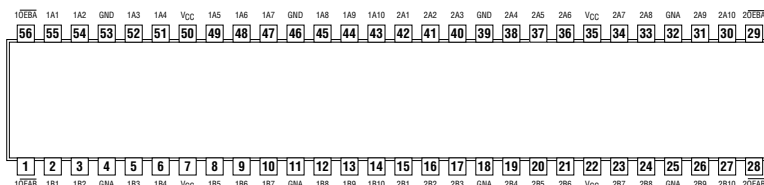
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



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16861

20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

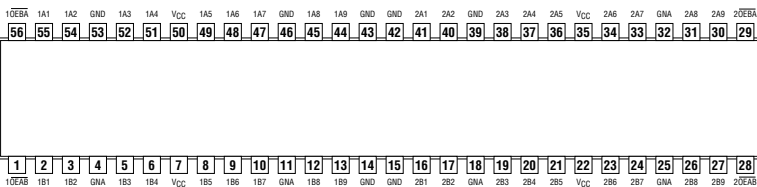


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Pin Assignments

16863

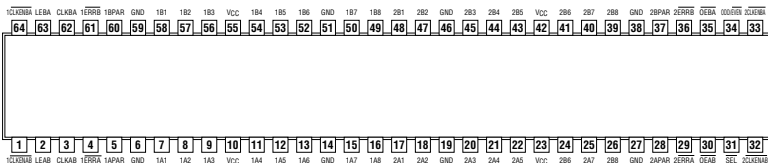
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16901

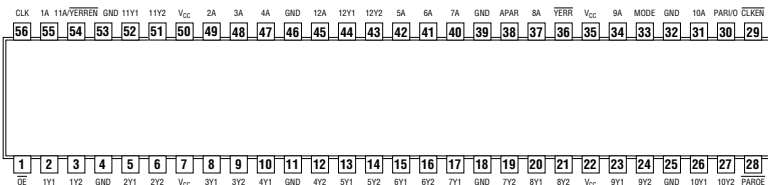
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS



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16903

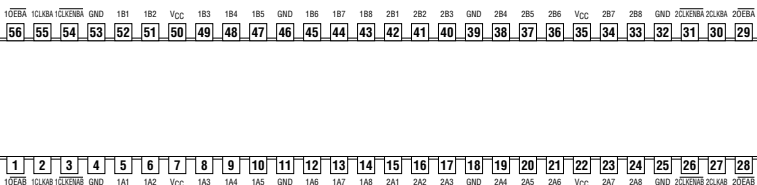
3.3-V 12-BIT UNIVERSAL BUS DRIVER
WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS



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16952

16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

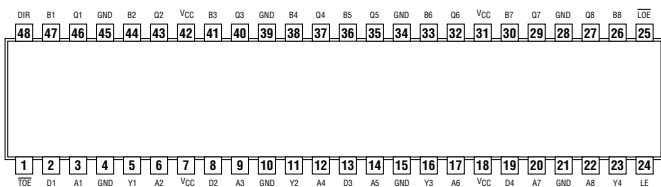


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Pin Assignments

16973

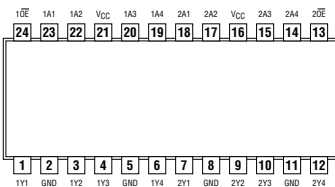
8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS



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25244

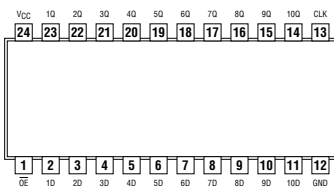
25-Ω OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



See page 708

29821

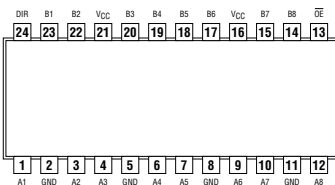
10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 711

25245

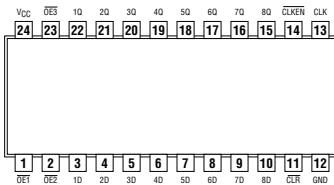
25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 709

29825

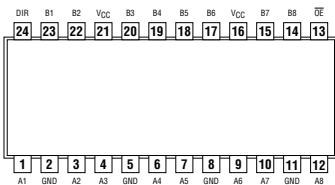
8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 712

25642

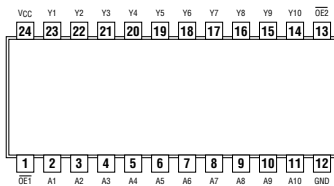
25-Ω OCTAL BUS TRANSCEIVER



See page 710

29827

29828
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

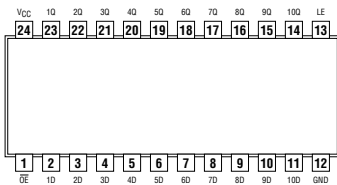


See page 713, 714

Pin Assignments

29841

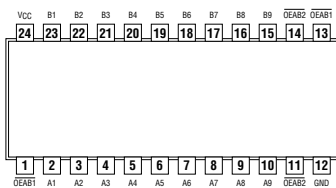
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 715

29864

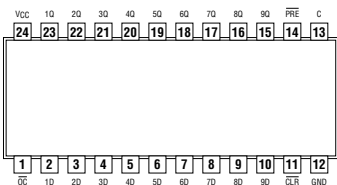
9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 721

29843

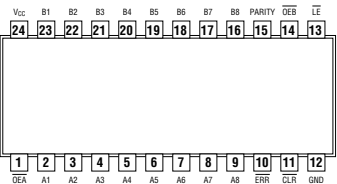
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 716

29854

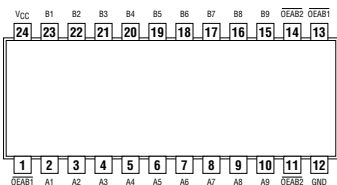
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



See page 718

29863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



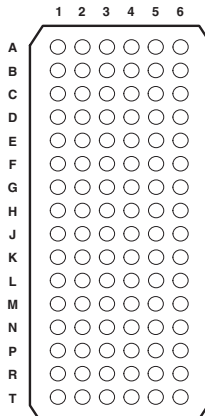
See page 720

Pin Assignments

32240

32-BIT BUFFER/DRIVER

GKE PACKAGE
(TOP VIEW)



terminal assignments

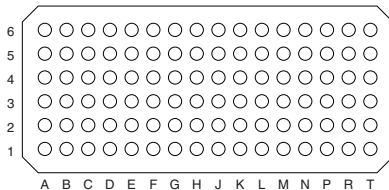
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|------------------|------------------|-----|-----|
| A | 1Y2 | 1Y1 | 1OE | 2OE | 1A1 | 1A2 |
| B | 1Y4 | 1Y3 | GND | GND | 1A3 | 1A4 |
| C | 2Y2 | 2Y1 | 1V _{CC} | 1V _{CC} | 2A1 | 2A2 |
| D | 2Y2 | 2Y3 | GND | GND | 2A3 | 2A4 |
| E | 3Y2 | 3Y1 | GND | GND | 3A1 | 3A2 |
| F | 3Y4 | 3Y3 | 1V _{CC} | 1V _{CC} | 3A3 | 3A4 |
| G | 4Y2 | 4Y1 | GND | GND | 4A1 | 4A2 |
| H | 4Y3 | 4Y4 | 4OE | 3OE | 4A4 | 4A3 |
| J | 5Y2 | 5Y1 | 5OE | 6OE | 5A1 | 5A2 |
| K | 5Y4 | 5Y3 | GND | GND | 5A3 | 5A4 |
| L | 6Y2 | 6Y1 | 2V _{CC} | 2V _{CC} | 6A1 | 6A2 |
| M | 6Y4 | 6Y3 | GND | GND | 6A3 | 6A4 |
| N | 7Y2 | 7Y1 | GND | GND | 7A1 | 7A2 |
| P | 7Y4 | 7Y3 | 2V _{CC} | 2V _{CC} | 7A3 | 7A4 |
| R | 8Y2 | 8Y1 | GND | GND | 8A1 | 8A2 |
| T | 8Y3 | 8Y4 | 8OE | 7OE | 8A4 | 8A3 |

See page 722

32244

32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



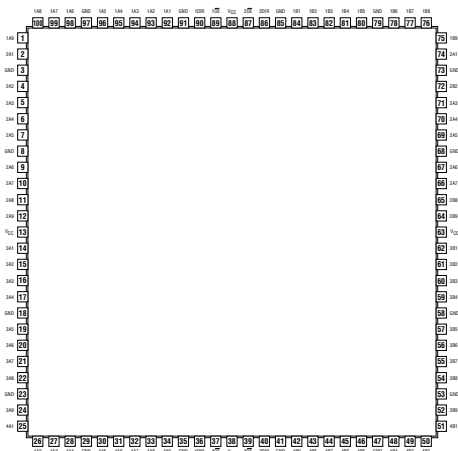
| | | | | | | | | | | | | | | | | |
|---|-----|-----|-----------------|-----|-----|-----------------|-----|-----|------|-----|-----------------|-----|-----|-----------------|-----|------|
| 6 | 1A2 | 1A4 | 2A2 | 2A4 | 3A2 | 3A4 | 4A2 | 4A3 | 5A2 | 5A4 | 6A2 | 6A4 | 7A2 | 7A4 | 8A2 | 8A3 |
| 5 | 1A1 | 1A3 | 2A1 | 2A3 | 3A1 | 3A3 | 4A1 | 4A4 | 5A1 | 5A3 | 6A1 | 6A3 | 7A1 | 7A3 | 8A1 | 8A4 |
| 4 | 2OE | GND | V _{CC} | GND | GND | V _{CC} | GND | 3OE | 6OE | GND | V _{CC} | GND | GND | V _{CC} | GND | 7OE |
| 3 | 1OE | GND | V _{CC} | GND | GND | V _{CC} | GND | 4OE | 5DIR | GND | V _{CC} | GND | GND | V _{CC} | GND | 8DIR |
| 2 | 1Y1 | 1Y3 | 2Y1 | 2Y3 | 3Y1 | 3Y3 | 4Y1 | 4Y4 | 5Y1 | 5Y3 | 6Y1 | 6Y3 | 7Y1 | 7Y3 | 8Y1 | 8Y4 |
| 1 | 1Y2 | 1Y4 | 2Y2 | 2Y4 | 3Y2 | 3Y4 | 4Y2 | 4Y3 | 5Y2 | 5Y4 | 6Y2 | 6Y4 | 7Y2 | 7Y4 | 8Y2 | 8Y3 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

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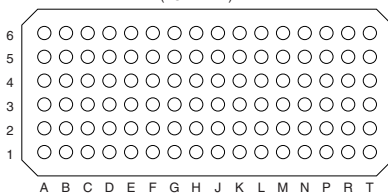
Pin Assignments

32245

32-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



GKE PACKAGE
(TOP VIEW)

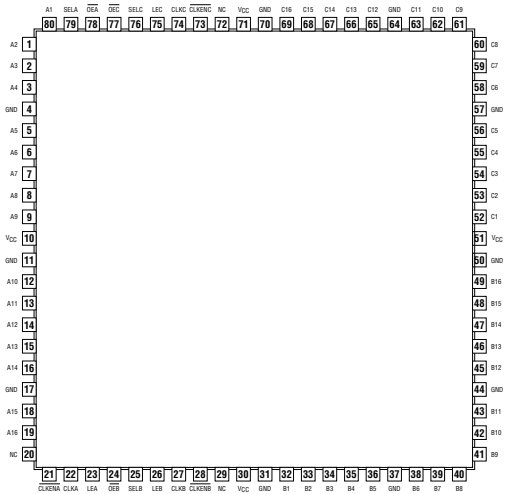


| | | | | | | | | | | | | | | | | |
|---|------------------|-----|----------|-----|-----|----------|-----|------------------|------------------|-----|----------|-----|-----|----------|-----|------------------|
| 6 | 1A2 | 1A4 | 1A6 | 1A8 | 2A2 | 2A4 | 2A6 | 2A7 | 3A2 | 3A4 | 3A6 | 3A8 | 4A2 | 4A4 | 4A6 | 4A7 |
| 5 | 1A1 | 1A3 | 1A5 | 1A7 | 2A1 | 2A3 | 2A5 | 2A8 | 3A1 | 3A3 | 3A5 | 3A7 | 4A1 | 4A3 | 4A5 | 4A8 |
| 4 | $\overline{1OE}$ | GND | V_{CC} | GND | GND | V_{CC} | GND | $\overline{2OE}$ | $\overline{3OE}$ | GND | V_{CC} | GND | GND | V_{CC} | GND | $\overline{4OE}$ |
| 3 | 1DIR | GND | V_{CC} | GND | GND | V_{CC} | GND | 2DIR | 3DIR | GND | V_{CC} | GND | GND | V_{CC} | GND | 4DIR |
| 2 | 1B1 | 1B3 | 1B5 | 1B7 | 2B1 | 2B3 | 2B5 | 2B8 | 3B1 | 3B3 | 3B5 | 3B7 | 4B1 | 4B3 | 4B5 | 4B8 |
| 1 | 1B2 | 1B4 | 1B6 | 1B8 | 2B2 | 2B4 | 2B6 | 2B7 | 3B2 | 3B4 | 3B6 | 3B8 | 4B2 | 4B4 | 4B6 | 4B7 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

Pin Assignments

32316

16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

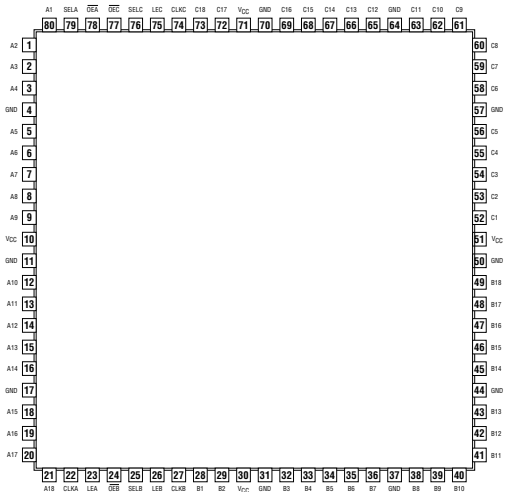


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NC-No internal connection

32318

18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS



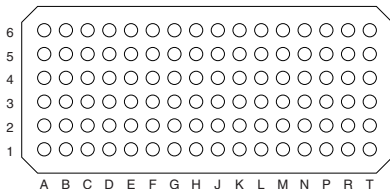
See page 730

Pin Assignments

32373

32-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



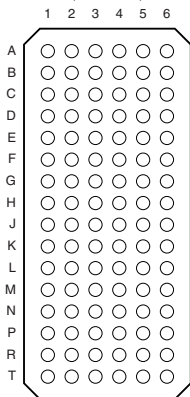
| | | | | | | | | | | | | | | | | |
|---|-----|-----|-----------------|-----|-----|-----------------|-----|-----|-----|-----|-----------------|-----|-----|-----------------|-----|-----|
| 6 | 1D2 | 1D4 | 1D6 | 1D8 | 2D2 | 2D4 | 2D6 | 2D7 | 3D2 | 3D4 | 3D6 | 3D8 | 4D2 | 4D4 | 4D6 | 4D7 |
| 5 | 1D1 | 1D3 | 1D5 | 1D7 | 2D1 | 2D3 | 2D5 | 2D8 | 3D1 | 3D3 | 3D5 | 3D7 | 4D1 | 4D3 | 4D5 | 4D8 |
| 4 | 1LE | GND | V _{CC} | GND | GND | V _{CC} | GND | 2LE | 3LE | GND | V _{CC} | GND | GND | V _{CC} | GND | 4LE |
| 3 | 1OE | GND | V _{CC} | GND | GND | V _{CC} | GND | 2OE | 3OE | GND | V _{CC} | GND | GND | V _{CC} | GND | 4OE |
| 2 | 1Q1 | 1Q3 | 1Q5 | 1Q7 | 2Q1 | 2Q3 | 2Q5 | 2Q8 | 3Q1 | 3Q3 | 3Q5 | 3Q7 | 4Q1 | 4Q3 | 4Q5 | 4Q8 |
| 1 | 1Q2 | 1Q4 | 1Q6 | 1Q8 | 2Q2 | 2Q4 | 2Q6 | 2Q7 | 3Q2 | 3Q4 | 3Q6 | 3Q8 | 4Q2 | 4Q4 | 4Q6 | 4Q7 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

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32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

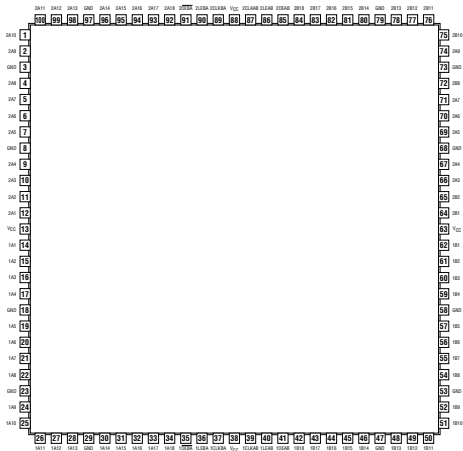
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|-----------------|-----------------|-----|-----|
| A | 1Q2 | 1Q1 | 1OE | 1CLK | 1D1 | 1D2 |
| B | 1Q4 | 1Q3 | GND | GND | 1D3 | 1D4 |
| C | 1Q6 | 1Q5 | V _{CC} | V _{CC} | 1D5 | 1D6 |
| D | 1Q8 | 1Q7 | GND | GND | 1D7 | 1D8 |
| E | 2Q2 | 2Q1 | GND | GND | 2D1 | 2D2 |
| F | 2Q4 | 2Q3 | V _{CC} | V _{CC} | 2D3 | 2D4 |
| G | 2Q6 | 2Q5 | GND | GND | 2D5 | 2D6 |
| H | 2Q8 | 2Q7 | 2OE | 2CLK | 2D7 | 2D8 |
| J | 3Q2 | 3Q1 | 3OE | 3CLK | 3D1 | 3D2 |
| K | 3Q4 | 3Q3 | GND | GND | 3D3 | 3D4 |
| L | 3Q6 | 3Q5 | V _{CC} | V _{CC} | 3D5 | 3D6 |
| M | 3Q8 | 3Q7 | GND | GND | 3D7 | 3D8 |
| N | 4Q2 | 4Q1 | GND | GND | 4D1 | 4D2 |
| P | 4Q4 | 4Q3 | V _{CC} | V _{CC} | 4D3 | 4D4 |
| R | 4Q6 | 4Q5 | GND | GND | 4D5 | 4D6 |
| T | 4Q7 | 4Q8 | 4OE | 4CLK | 4D8 | 4D7 |

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Pin Assignments

32501

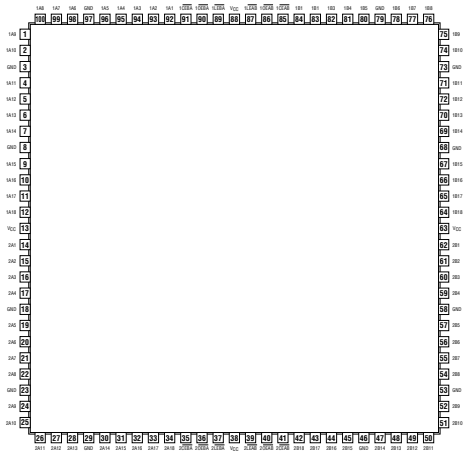
36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



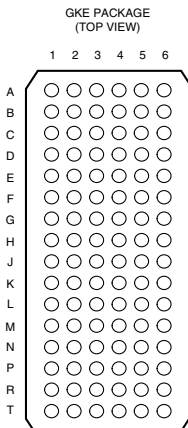
See page 736

32543

36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



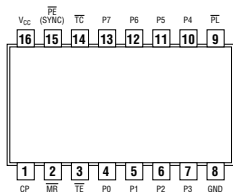
See page 738

32973**16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH
WITH EIGHT INDEPENDENT BUFFERS**

terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|----|---------------------------|---------------------------|-----|-----|
| A | 1A1 | D1 | 1 $\overline{\text{TOE}}$ | 1DIR | 1B1 | 1Q1 |
| B | 1A2 | Y1 | GND | GND | 1B2 | 1Q2 |
| C | 1A3 | D2 | V _{CC} | V _{CC} | 1B3 | 1Q3 |
| D | 1A4 | Y2 | GND | GND | 1B4 | 1Q4 |
| E | 1A5 | D3 | GND | GND | 1B5 | 1Q5 |
| F | 1A6 | Y3 | V _{CC} | V _{CC} | 1B6 | 1Q6 |
| G | 1A7 | D4 | GND | GND | 1B7 | 1Q7 |
| H | 1A8 | Y4 | 1LE | 1 $\overline{\text{LOE}}$ | 1B8 | 1Q8 |
| J | 2A1 | D5 | 2 $\overline{\text{TOE}}$ | 2DIR | 2B1 | 2Q1 |
| K | 2A2 | Y5 | GND | GND | 2B2 | 2Q2 |
| L | 2A3 | D6 | V _{CC} | V _{CC} | 2B3 | 2Q3 |
| M | 2A4 | Y6 | GND | GND | 2B4 | 2Q4 |
| N | 2A5 | D7 | GND | GND | 2B5 | 2Q5 |
| P | 2A6 | Y7 | V _{CC} | V _{CC} | 2B6 | 2Q6 |
| R | 2A7 | D8 | GND | GND | 2B7 | 2Q7 |
| T | 2A8 | Y8 | 2LE | 2 $\overline{\text{LOE}}$ | 2B8 | 2Q8 |

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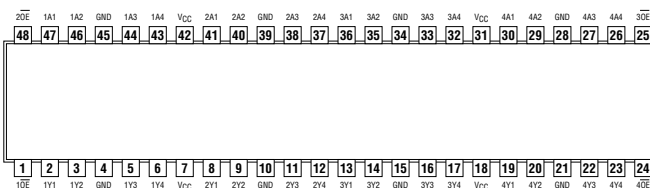
40103**8-STAGE SYNCHRONOUS DOWN COUNTERS**

See page 742

Pin Assignments

162240

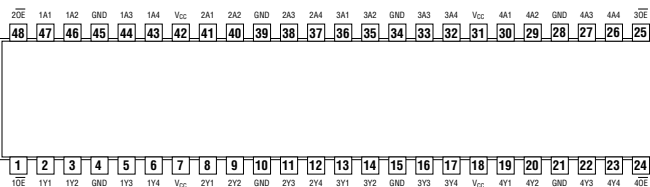
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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162241

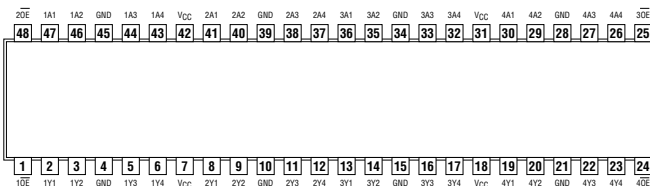
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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162244

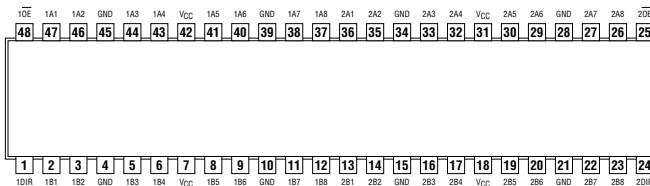
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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162245

16-BIT TRANSCEIVER
WITH 3-STATE OUTPUTS

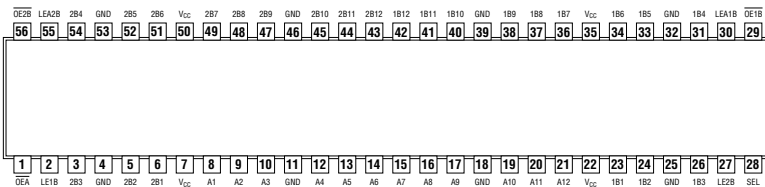


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Pin Assignments

162260

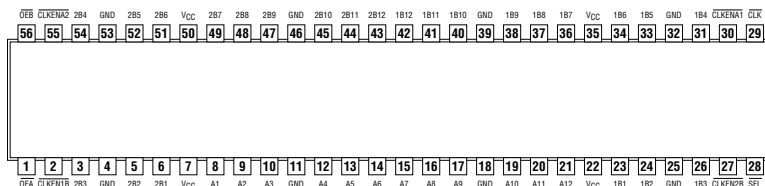
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH
WITH 3-STATE OUTPUTS



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162268

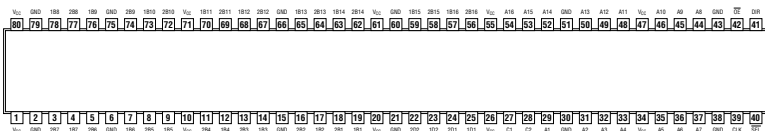
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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162280

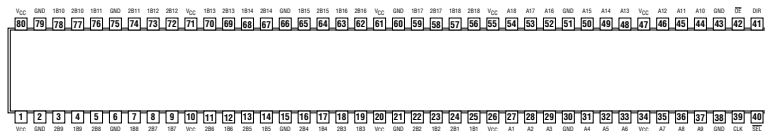
16-BIT TO 32-BIT REGISTERED BUS EXCHANGER
WITH BYTE MASKS AND 3-STATE OUTPUTS



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162282

18-BIT TO 36-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

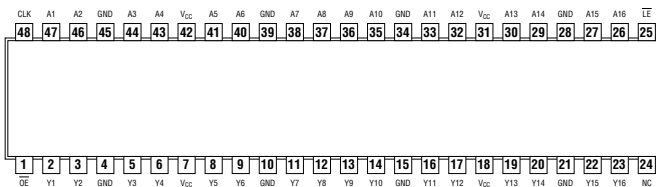


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Pin Assignments

162334

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

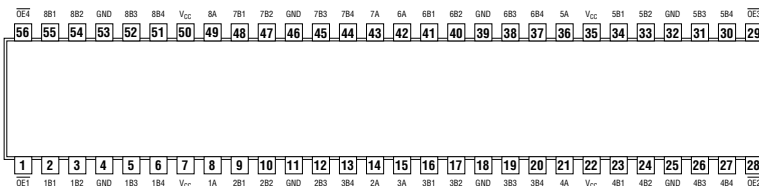


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NC-No internal connection

162344

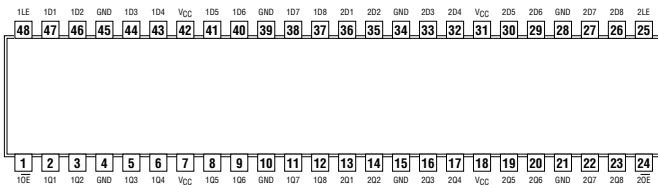
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



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162373

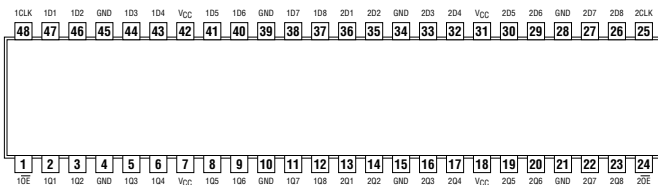
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS



See page 760

162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



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Pin Assignments

162460

4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|------------------|------|-----|------|------|-----------------|-------|-----------------|-------|-----|-----|-----|---------|---------|-----|-----|-----|--------------------|--------------------|--------------------|-----------------|------|------|-----|-----------------|------------------|------------------|
| OE _{B1} | OE _{B2} | SEL0 | GND | 1B1 | 1B2 | V _{CC} | 1B3 | 1B4 | 2B1 | GND | 2B2 | 2B3 | 2B4 | 3B1 | 3B2 | 3B3 | GND | 3B4 | 4B1 | 4B2 | V _{CC} | 4B3 | 4B4 | GND | SEL1 | OE _{B3} | OE _{B4} |
| 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| LEAB1 | LEAB2 | LEBA | GND | LEB1 | LEB2 | V _{CC} | CLKBA | OE _B | CLKAB | GND | 1A | 2A | OE_SEL0 | OE_SEL1 | 3A | 4A | GND | CLK _{ENB} | CLK _{ENB} | CLK _{ENB} | V _{CC} | LEB3 | LEBA | GND | OE _A | LEAB3 | LEAB3 |

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162500

18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|-------|----|-----|----|----|-----------------|----|----|----|-----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-------|------|
| GND | CLKAB | B1 | GND | B2 | B3 | V _{CC} | B4 | B5 | B6 | GND | B7 | B8 | B9 | B10 | B11 | B12 | GND | B13 | B14 | B15 | V _{CC} | B16 | B17 | GND | B18 | CLKBA | GND |
| 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| OEAB | LEAB | A1 | GND | A2 | A3 | V _{CC} | A4 | A5 | A6 | GND | A7 | A8 | A9 | A10 | A11 | A12 | GND | A13 | A14 | A15 | V _{CC} | A16 | A17 | GND | A18 | OEBA | LEBA |

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162501

18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|-------|----|-----|----|----|-----------------|----|----|----|-----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-------|------|
| GND | CLKAB | B1 | GND | B2 | B3 | V _{CC} | B4 | B5 | B6 | GND | B7 | B8 | B9 | B10 | B11 | B12 | GND | B13 | B14 | B15 | V _{CC} | B16 | B17 | GND | B18 | CLKBA | GND |
| 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| OEAB | LEAB | A1 | GND | A2 | A3 | V _{CC} | A4 | A5 | A6 | GND | A7 | A8 | A9 | A10 | A11 | A12 | GND | A13 | A14 | A15 | V _{CC} | A16 | A17 | GND | A18 | OEBA | LEBA |

See page 766

162525

18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

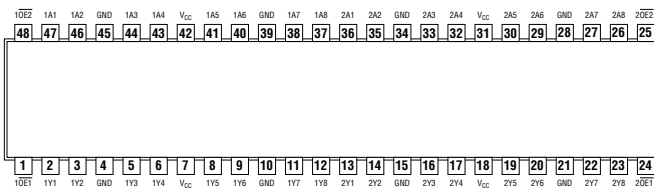
| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|-------|----|-----|----|----|-----------------|----|----|----|-----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|--------------------|--------------------|
| SEL | CLKAB | B1 | GND | B2 | B3 | V _{CC} | B4 | B5 | B6 | GND | B7 | B8 | B9 | B10 | B11 | B12 | GND | B13 | B14 | B15 | V _{CC} | B16 | B17 | GND | B18 | CLK _{ENB} | CLK _{ENB} |
| 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| CLK _{ENB} | OEAB | A1 | GND | A2 | A3 | V _{CC} | A4 | A5 | A6 | GND | A7 | A8 | A9 | A10 | A11 | A12 | GND | A13 | A14 | A15 | V _{CC} | A16 | A17 | GND | A18 | OEBA | CLK _{ENB} |

See page 768

Pin Assignments

162541

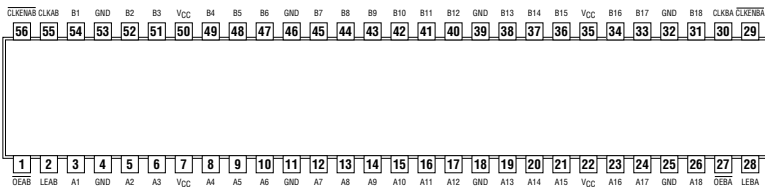
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 770

162601

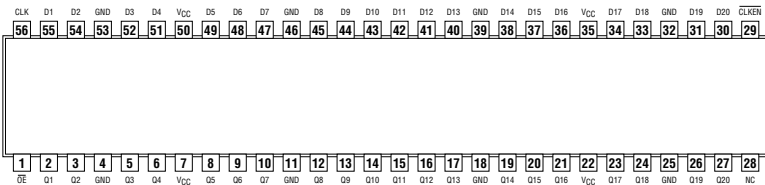
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 772

162721

3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

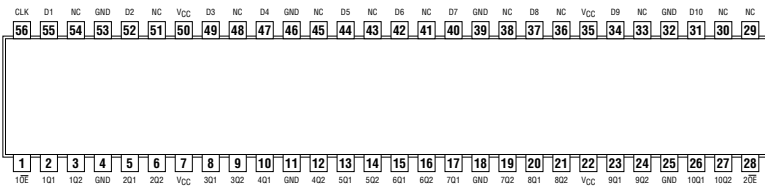


See page 774

NC-No internal connection

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS
AND 3-STATE OUTPUTS

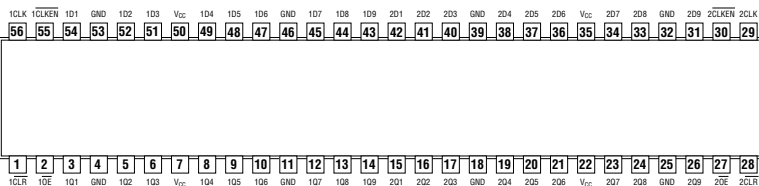


See page 775

NC-No internal connection

162823

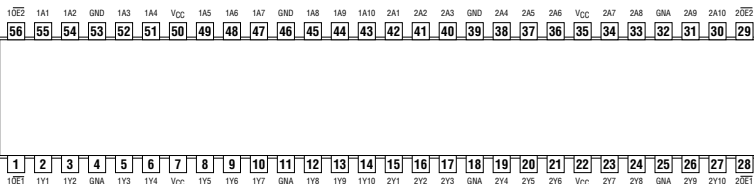
**18-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS**



See page 776

162825

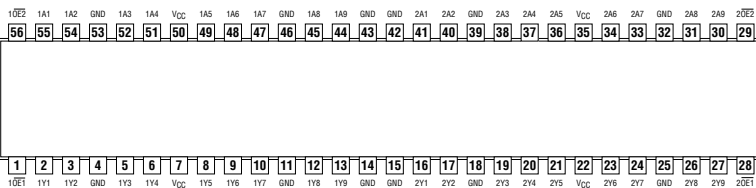
18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 777

162827

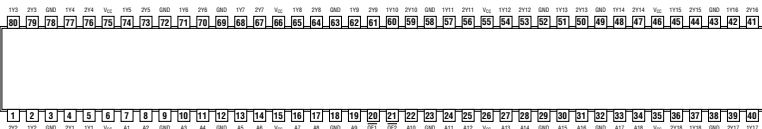
20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 778

162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

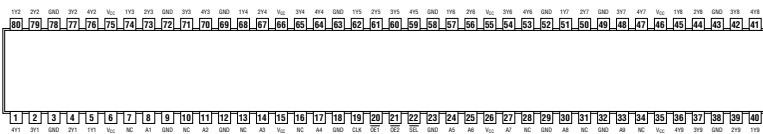


See page 779

Pin Assignments

162831

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

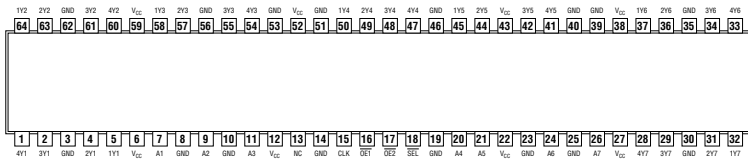


See page 780

NC-No internal connection

162832

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

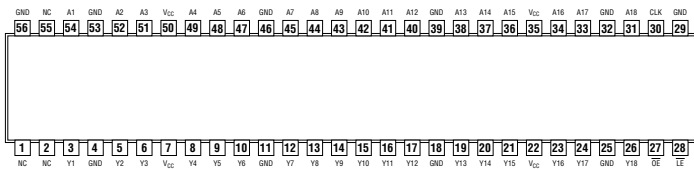


See page 781

162834

162835

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

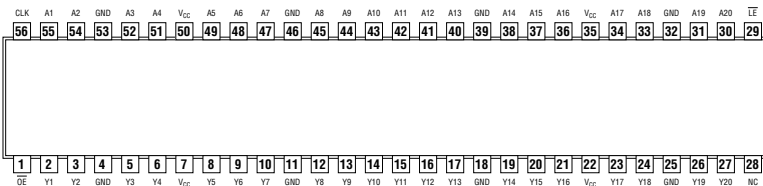


See page 782, 783

NC-No internal connection

162836

20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS



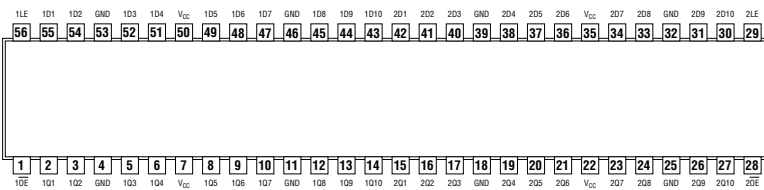
See page 784

NC-No internal connection

Pin Assignments

162841

20-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS



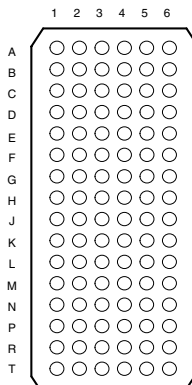
See page 785

Pin Assignments

322244

32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

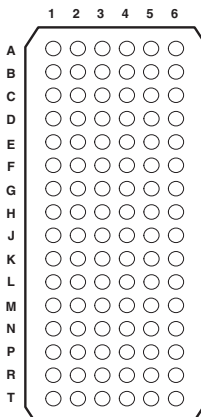
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|-------------------|-------------------|-----|-----|
| A | 1Y2 | 1Y1 | 1 \overline{OE} | 2 \overline{OE} | 1A1 | 1A2 |
| B | 1Y4 | 1Y3 | GND | GND | 1A3 | 1A4 |
| C | 2Y2 | 2Y1 | V _{CC} | V _{CC} | 2A1 | 2A2 |
| D | 2Y4 | 2Y3 | GND | GND | 2A3 | 2A4 |
| E | 3Y2 | 3Y1 | GND | GND | 3A1 | 3A2 |
| F | 3Y4 | 3Y3 | V _{CC} | V _{CC} | 3A3 | 3A4 |
| G | 4Y2 | 4Y1 | GND | GND | 4A1 | 4A2 |
| H | 4Y3 | 4Y4 | 4 \overline{OE} | 3 \overline{OE} | 4A4 | 4A3 |
| J | 5Y2 | 5Y1 | 5 \overline{OE} | 6 \overline{OE} | 5A1 | 5A2 |
| K | 5Y4 | 5Y3 | GND | GND | 5A3 | 5A4 |
| L | 6Y2 | 6Y1 | V _{CC} | V _{CC} | 6A1 | 6A2 |
| M | 6Y4 | 6Y3 | GND | GND | 6A3 | 6A4 |
| N | 7Y2 | 7Y1 | GND | GND | 7A1 | 7A2 |
| P | 7Y4 | 7Y3 | V _{CC} | V _{CC} | 7A3 | 7A4 |
| R | 8Y2 | 8Y1 | GND | GND | 8A1 | 8A2 |
| T | 8Y3 | 8Y4 | 8 \overline{OE} | 7 \overline{OE} | 8A4 | 8A3 |

See page 786

322374

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|-------------------|-----------------|-----|-----|
| A | 1Q2 | 1Q1 | 1 \overline{OE} | 1CLK | 1D1 | 1D2 |
| B | 1Q4 | 1Q3 | GND | GND | 1D3 | 1D4 |
| C | 1Q6 | 1Q5 | V _{CC} | V _{CC} | 1D5 | 1D6 |
| D | 1Q8 | 1Q7 | GND | GND | 1D7 | 1D8 |
| E | 2Q2 | 2Q1 | GND | GND | 2D1 | 2D2 |
| F | 2Q4 | 2Q3 | V _{CC} | V _{CC} | 2D3 | 2D4 |
| G | 2Q6 | 2Q6 | GND | GND | 2D5 | 2D6 |
| H | 2Q7 | 2Q8 | 2 \overline{OE} | 2CLK | 2D8 | 2D7 |
| J | 3Q2 | 3Q1 | 3 \overline{OE} | 3CLK | 3D1 | 3D2 |
| K | 3Q4 | 3Q3 | GND | GND | 3D3 | 3D4 |
| L | 3Q6 | 3Q5 | V _{CC} | V _{CC} | 3D5 | 3D6 |
| M | 3Q8 | 3Q7 | GND | GND | 3D7 | 3D8 |
| N | 4Q2 | 4Q1 | GND | GND | 4D1 | 4D2 |
| P | 4Q4 | 4Q3 | V _{CC} | V _{CC} | 4D3 | 4D4 |
| R | 4Q6 | 4Q5 | GND | GND | 4D5 | 4D6 |
| T | 4Q7 | 4Q8 | 4 \overline{OE} | 4CLK | 4D8 | 4D7 |

See page 787

**FUNCTION
AND
ELECTRICAL
CHARACTERISTICS**

Standard

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | CD74 AC | UNIT |
|-----------------|------------|------|------|----|------|------|------|---------|---------|----------|----------|-------|---------|---------|------|
| I _{CC} | MAX | 22 | 4.4 | 36 | 3 | 17.4 | 10.2 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | 0.02 | 0.08 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|--------|----------|----------|------|------|-------|-------|--------|---------|----------|----------|------|
| I _{CC} | MAX | 0.04 | 0.02 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|------------------|--------|--------|------------|-----|----|-----|-----|-----|-----|---------|---------|----------|
| t _{PLH} | A or B | Y | MAX | 22 | 15 | 4.5 | 11 | 4.5 | 6 | 23 | 27 | 25 |
| t _{PHL} | A or B | Y | MAX | 15 | 15 | 5 | 8 | 4 | 5.3 | 23 | 27 | 25 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT |
|------------------|--------|--------|------------|----------|-------|---------|---------|--------|----------|----------|-----|------|
| t _{PLH} | A or B | Y | MAX | 30 | 7.4 | 8.5 | 7.3 | 12.3 | 9.5 | 10.8 | 8.5 | 9 |
| t _{PHL} | A or B | Y | MAX | 30 | 6.8 | 7 | 7.3 | 8.8 | 8 | 13.2 | 8.5 | 9 |

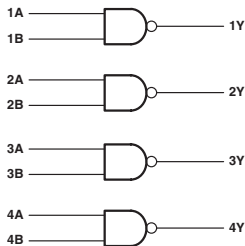
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|--------|--------|------------|-------|-------|--------|---------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 13 | 8.5 | 4.3 | 3 | 2.4 | 2 |
| t _{PHL} | A or B | Y | MAX | 13 | 8.5 | 4.3 | 3 | 2.4 | 2 |

UNIT:ns

01

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS**

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | HC | UNIT |
|-----------|------------|-----|-----|-----|----------|------|
| I_{CC} | MAX | 22 | 4.4 | 3 | 0.02 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | V_{CC} | V |
| I_{OL} | MAX | 16 | 8 | 8 | 4 | mA |

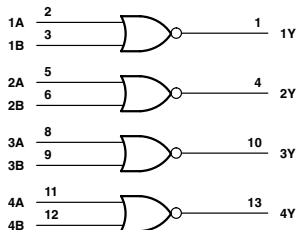
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | HC |
|-----------|--------|--------|------------|-----|----|-----|----|
| t_{PLH} | A or B | Y | MAX | 55 | 32 | 54 | 31 |
| t_{PHL} | A or B | Y | MAX | 15 | 28 | 28 | 25 |

UNIT:ns

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | UNIT |
|-----------|------------|------|------|----|------|------|----|---------|---------|----------|----------|------|
| I_{CC} | MAX | 27 | 5.4 | 45 | 4 | 20.1 | 13 | 0.02 | 0.04 | 0.02 | 0.04 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | mA |

| PARAMETER | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------|------------|-------|---------|--------|----------|------|------|-------|-------|--------|----------|----------|------|
| I_{CC} | MAX | 0.04 | 0.08 | 0.04 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -8 | -9 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|-----------|--------|--------|------------|-----|----|-----|-----|-----|-----|---------|---------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 22 | 15 | 5.5 | 12 | 4.5 | 6.5 | 23 | 27 | 25 | 32 |
| t_{PHL} | A or B | Y | MAX | 15 | 15 | 5.5 | 10 | 4.5 | 5.3 | 23 | 27 | 25 | 32 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V |
|-----------|--------|--------|------------|-------|---------|--------|----------|-----|------|-------|-------|--------|
| t_{PLH} | A or B | Y | MAX | 6.9 | 11.5 | 10.6 | 12.2 | 8.5 | 8.5 | 13 | 8.5 | 4.4 |
| t_{PHL} | A or B | Y | MAX | 6.4 | 11.5 | 8.7 | 12.2 | 8.5 | 8.5 | 13 | 8.5 | 4.4 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUC 1.8V | AUC 2.3V |
|-----------|--------|--------|------------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 2.4 | 2 |
| t_{PHL} | A or B | Y | MAX | 2.4 | 2 |

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS



$$Y = \overline{A \cdot B}$$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

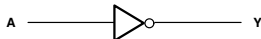
| PARAMETER | MAX or MIN | TTL | LS | S | ALS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|-----|-----|-----|-----|----------|----------|----------|------|
| I_{CC} | MAX | 22 | 4.4 | 36 | 4 | 0.02 | 0.04 | 0.04 | mA |
| V_{OH} | MAX | 5.5 | 8 | 5.5 | 8 | V_{CC} | V_{CC} | V_{CC} | V |
| I_{OL} | MAX | 16 | 0.1 | 20 | 0.1 | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | SN74 HC | CD74 HC | CD74 HCT |
|-----------|--------|--------|------------|-----|----|-----|-----|---------|---------|----------|
| t_{PLH} | A or B | Y | MAX | 45 | 32 | 7.5 | 50 | 31 | 30 | 36 |
| t_{PHL} | A or B | Y | MAX | 15 | 28 | 7 | 13 | 25 | 30 | 36 |

UNIT: ns

HEX INVERTERS



- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | UNIT |
|-----------------|------------|------|------|----|------|------|------|---------|---------|----------|----------|-------|---------|------|
| I _{CC} | MAX | 33 | 6.6 | 54 | 4.2 | 26.3 | 15.3 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|---------|--------|----------|----------|------|------|-------|-------|--------|---------|----------|----------|------|
| I _{CC} | MAX | 0.08 | 0.04 | 0.02 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|------------------|--------|--------|------------|-----|----|-----|-----|----|-----|---------|---------|----------|
| t _{PLH} | A or B | Y | MAX | 22 | 15 | 4.5 | 11 | 5 | 6 | 24 | 26 | 25 |
| t _{PHL} | A or B | Y | MAX | 15 | 15 | 5 | 8 | 4 | 5.3 | 24 | 26 | 25 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT |
|------------------|--------|--------|------------|----------|-------|---------|---------|--------|----------|----------|-----|------|
| t _{PLH} | A or B | Y | MAX | 29 | 7.1 | 7.5 | 6.5 | 9.7 | 9 | 9.3 | 8.5 | 8.5 |
| t _{PHL} | A or B | Y | MAX | 29 | 6 | 7 | 6.5 | 9.6 | 8.5 | 9.3 | 8.5 | 8.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|--------|--------|------------|-------|-------|--------|---------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 12 | 8.5 | 4.5 | 2.8 | 2.5 | 2.0 |
| t _{PHL} | A or B | Y | MAX | 12 | 8.5 | 4.5 | 2.8 | 2.5 | 2.0 |

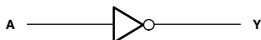
UNIT: ns

U04

HEX INVERTERS

- $Y = \bar{A}$
- Unbuffered Output

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | AHC | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------|------------|---------|---------|------|-------|-------|--------|----------|----------|------|
| I_{CC} | MAX | 0.02 | 0.04 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -4 | -4 | -8 | -6 | -12 | -24 | -8 | -9 | mA |
| I_{OL} | MAX | 4 | 4 | 8 | 6 | 12 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | AHC | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.3V |
|-----------|--------|--------|------------|---------|---------|-----|-------|-------|--------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 20 | 21 | 8 | 13 | 8 | 3.8 | 2.0 | 1.7 |
| t_{PHL} | A or B | Y | MAX | 20 | 21 | 8 | 13 | 8 | 3.8 | 2.0 | 1.7 |

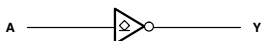
UNIT: ns

05

HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

- $Y = \bar{A}$

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | SN74 HC | CD74 AC | CD74 ACT | AHC | LV 3V | LV 5V | UNIT |
|-----------|------------|------|-----|------|-----|---------|---------|----------|------|-------|-------|------|
| I_{CC} | MAX | 33 | 6.6 | 54 | 4.2 | 0.02 | 0.08 | 0.08 | 0.02 | - | 0.02 | mA |
| I_{OH} | MAX | 0.25 | 0.1 | 0.25 | - | - | -24 | -24 | - | - | - | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | V_{CC} | 5.5 | 5.5 | 5.5 | V |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 4 | 24 | 24 | 8 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | SN74 HC | CD74 AC | CD74 ACT | AHC | LV 3V | LV 5V |
|-----------|--------|--------|------------|-----|----|-----|-----|---------|---------|----------|-----|-------|-------|
| t_{PLH} | A or B | Y | MAX | 55 | 32 | 7.5 | 54 | 29 | - | - | - | 12 | 8.5 |
| t_{PHL} | A or B | Y | MAX | 15 | 28 | 7 | 14 | 21 | - | - | - | 12 | 8.5 |
| t_{PLZ} | A | Y | MAX | - | - | - | - | - | 8.2 | 9.3 | 8.5 | - | - |
| t_{PZL} | A | Y | MAX | - | - | - | - | - | 6.5 | 10.8 | 8.5 | - | - |

UNIT: ns

06

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS

Logic Diagram



$$\bullet Y = \bar{A}$$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V | UNIT |
|-----------------|------------|------|------|----------|----------|-----------|-------------|-------------|------|
| I _{CC} | MAX | 51 | 60 | - | 0.02 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | 0.25 | 0.25 | - | ±0.0025 | - | - | - | mA |
| V _{OH} | MAX | 30 | 30 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | V |
| I _{OL} | MAX | 40 | 40 | 8 | 16 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V |
|------------------|--------|--------|------------|-----|----|----------|----------|-----------|-------------|-------------|
| t _{PLH} | A or B | Y | MAX | 15 | 15 | 12 | 8.5 | 3.7 | 2.8 | 1.3 |
| t _{PHL} | A or B | Y | MAX | 23 | 20 | 12 | 8.5 | 3.7 | 2.8 | 1.3 |

UNIT: ns

07

HEX BUFFERS/DRIVERS WITH OPEN-DRAIN
OUTPUTS

Logic Diagram



$$\bullet Y = A$$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V | UNIT |
|-----------------|------------|------|------|----------|----------|-----------|-------------|-------------|------|
| I _{CC} | MAX | 41 | 45 | - | 0.02 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | 0.25 | 0.25 | - | ±0.0025 | - | - | - | mA |
| V _{OH} | MAX | 30 | 30 | 5.5 | 5.5 | 5.5 | 3.6 | 3.6 | V |
| I _{OL} | MAX | 40 | 40 | 8 | 16 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V |
|------------------|--------|--------|------------|-----|----|----------|----------|-----------|-------------|-------------|
| t _{PLH} | A or B | Y | MAX | 15 | 10 | 12 | 8.5 | 2.9 | 2.3 | 1.3 |
| t _{PHL} | A or B | Y | MAX | 26 | 30 | 12 | 8.5 | 2.9 | 2.3 | 1.3 |

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-AND GATES



- $Y = A \cdot B$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | UNIT |
|-----------------|------------|------|------|----|------|----|------|---------|---------|----------|----------|-------|------|
| I _{CC} | MAX | 33 | 8.8 | 57 | 4 | 24 | 12.9 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | mA |

| PARAMETER | MAX or MIN | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3.3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|---------|---------|--------|----------|----------|------|------|-------|-------|----------|---------|----------|----------|------|
| I _{CC} | MAX | 0.02 | 0.08 | 0.04 | 0.02 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|------------------|--------|--------|------------|-----|----|-----|-----|-----|-----|---------|---------|----------|
| t _{PLH} | A or B | Y | MAX | 27 | 15 | 7 | 14 | 5.5 | 6.6 | 25 | 27 | 30 |
| t _{PHL} | A or B | Y | MAX | 19 | 20 | 7.5 | 10 | 5.5 | 6.3 | 25 | 27 | 30 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT |
|------------------|--------|--------|------------|----------|-------|---------|---------|--------|----------|----------|-----|------|
| t _{PLH} | A or B | Y | MAX | 38 | 6.9 | 8.5 | 8.7 | 9 | 10 | 12.9 | 9 | 9 |
| t _{PHL} | A or B | Y | MAX | 38 | 6.5 | 7.5 | 8.7 | 8.2 | 10 | 12.9 | 9 | 9 |

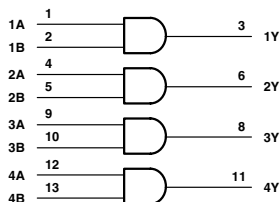
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V | LVC 3.3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|--------|--------|------------|-------|-------|----------|---------|----------|----------|
| t _{PLH} | A or B | Y | MAX | 14 | 9 | 4.1 | 2.9 | 2.3 | 1.8 |
| t _{PHL} | A or B | Y | MAX | 14 | 9 | 4.1 | 2.9 | 2.3 | 1.8 |

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

● $Y = A \cdot B$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | F | SN74 HC | UNIT |
|-----------|------------|-----|-----|------|-----|------|----------|------|
| I_{CC} | MAX | 33 | 8.8 | 57 | 4.2 | 26.3 | 15.3 | mA |
| I_{OH} | MAX | - | 0.1 | 0.25 | 0.1 | - | - | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | V_{CC} | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 4 | mA |

SWITCHING CHARACTERISTICS

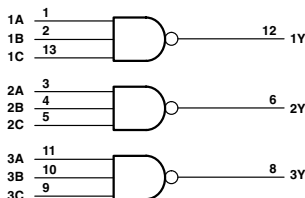
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | F | SN74 HC |
|-----------|--------|--------|------------|-----|----|----|-----|-----|---------|
| t_{PLH} | A or B | Y | MAX | 32 | 35 | 10 | 54 | 9.6 | 31 |
| t_{PHL} | A or B | Y | MAX | 24 | 35 | 10 | 15 | 4.8 | 25 |

UNIT: ns

TRIPLE 3-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE
(each gate)

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | CD74 AC | UNIT |
|-----------|------------|------|------|----|------|----|-----|---------|---------|----------|----------|-------|---------|---------|------|
| I_{CC} | MAX | 16.5 | 3.3 | 27 | 2.2 | 13 | 7.7 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | 0.02 | 0.08 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | ACT 11 | SN74 ACT | CD74 ACT | LV 3V | LV 5V | LVC 3V | ALVC 3V | UNIT |
|-----------|------------|--------|----------|----------|-------|-------|--------|---------|------|
| I_{CC} | MAX | 0.04 | 0.04 | 0.08 | - | 0.02 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -6 | -12 | -24 | -24 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 6 | 12 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|-----------|-----------|--------|------------|-----|----|-----|-----|-----|-----|---------|---------|----------|----------|
| t_{PLH} | A, B or C | Y | MAX | 22 | 15 | 4.5 | 11 | 4.5 | 6 | 24 | 30 | 19 | 36 |
| t_{PHL} | A, B or C | Y | MAX | 15 | 15 | 5 | 10 | 4.5 | 5.3 | 24 | 30 | 19 | 36 |

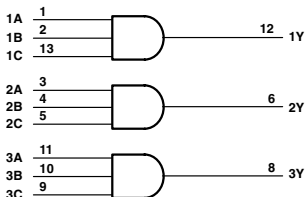
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | LV 3V | LV 5V | LVC 3V | ALVC 3V |
|-----------|-----------|--------|------------|-------|---------|---------|--------|----------|----------|-------|-------|--------|---------|
| t_{PLH} | A, B or C | Y | MAX | 6.7 | 8 | 12.2 | 8.9 | 10 | 13.5 | 13.5 | 9 | 4.9 | 3 |
| t_{PHL} | A, B or C | Y | MAX | 7 | 6.5 | 12.2 | 8.2 | 9.5 | 13.5 | 13.5 | 9 | 4.9 | 3 |

UNIT: ns

TRIPLE 3-INPUT POSITIVE-AND GATES

- $Y = A \cdot B \cdot C$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE
(each gate)

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | UNIT |
|-----------|------------|------|----|------|----|-----|---------|---------|----------|----------|-------|---------|------|
| I_{CC} | MAX | 6.6 | 42 | 3 | 18 | 9.7 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | 0.02 | mA |
| I_{OH} | MAX | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | -24 | mA |
| I_{OL} | MAX | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | ACT 11 | SN74 ACT | LV 3V | LV 5V | UNIT |
|-----------|------------|--------|----------|-------|-------|------|
| I_{CC} | MAX | 0.04 | 0.02 | - | 0.02 | mA |
| I_{OH} | MAX | -24 | -24 | -6 | -12 | mA |
| I_{OL} | MAX | 24 | 24 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|-----------|-----------|--------|------------|----|-----|-----|-----|-----|---------|---------|----------|----------|
| t_{PLH} | A, B or C | Y | MAX | 15 | 7 | 13 | 6 | 6.6 | 25 | 30 | 21 | 42 |
| t_{PHL} | A, B or C | Y | MAX | 20 | 7.5 | 10 | 5.5 | 6.5 | 25 | 30 | 21 | 42 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | SN74 AC | ACT 11 | SN74 ACT | LV 3V | LV 5V |
|-----------|-----------|--------|------------|-------|---------|--------|----------|-------|-------|
| t_{PLH} | A, B or C | Y | MAX | 6.5 | 8.5 | 9.6 | 10.5 | 14 | 9 |
| t_{PHL} | A, B or C | Y | MAX | 6.9 | 7.5 | 8.7 | 10.5 | 14 | 9 |

UNIT: ns

HEX SCHMITT-TRIGGER INVERTERS



- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | CD74 AC | SN74 ACT | CD74 ACT | AHC | AHCT | UNIT |
|-----------|------------|------|------|---------|---------|----------|----------|---------|---------|----------|----------|------|------|------|
| I_{CC} | MAX | 60 | 21 | 0.02 | 0.04 | 0.02 | 0.04 | 0.02 | 0.08 | 0.02 | 0.08 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -4 | -4 | -24 | -24 | -24 | -24 | -8 | -8 | mA |
| I_{OL} | MAX | 16 | 8 | 4 | 4 | 4 | 4 | 24 | 24 | 24 | 24 | 8 | 8 | mA |

| PARAMETER | MAX or MIN | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.5V | UNIT |
|-----------|------------|-------|-------|--------|---------|----------|----------|------|
| I_{CC} | MAX | - | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -6 | -12 | -24 | -24 | -8 | -9 | mA |
| I_{OL} | MAX | 6 | 12 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | CD74 AC | SN74 ACT | CD74 ACT |
|-----------|--------|--------|------------|-----|----|---------|---------|----------|----------|---------|---------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 22 | 22 | 31 | 41 | 40 | 57 | 11 | 10.5 | 12.5 | 14.5 |
| t_{PHL} | A or B | Y | MAX | 22 | 22 | 31 | 41 | 40 | 57 | 9.5 | 10.5 | 11 | 9.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.5V |
|-----------|--------|--------|------------|-----|------|-------|-------|--------|---------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 12 | 9 | 18.5 | 12 | 6.4 | 3.4 | 3.5 | 2.7 |
| t_{PHL} | A or B | Y | MAX | 12 | 9 | 18.5 | 12 | 6.4 | 3.4 | 3.5 | 2.7 |

UNIT: ns

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

● $Y = \bar{A}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

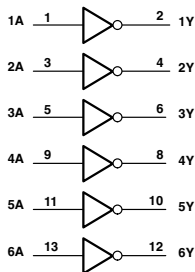
| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 51 | mA |
| V_{OH} | MAX | 15 | V |
| I_{OL} | MAX | 40 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|-----------|-------|--------|------------|-----|
| t_{PLH} | A | Y | MAX | 15 |
| t_{PHL} | A | Y | MAX | 23 |

UNIT: ns

Logic Diagram



17

HEX SCHMITT-TRIGGER BUFFER

● $Y = A$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | AUC 1.8V | AUC 2.5V | UNIT |
|-----------|------------|------|-------------|-------------|------|
| I_{CC} | MAX | 41 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | 0.25 | -8 | -9 | mA |
| I_{OL} | MAX | 40 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | AUC 1.8V | AUC 2.5V |
|-----------|-------|--------|------------|-----|-------------|-------------|
| t_{PLH} | A | Y | MAX | 15 | 2.4 | 1.9 |
| t_{PHL} | A | Y | MAX | 26 | 2.4 | 1.9 |

UNIT: ns

Logic Diagram



HEX SCHMITT-TRIGGER INVERTERS

- $Y = \overline{A}$
- P-N-P Input Reduce System Loading
($I_{IL} = -0.05\text{mA MAX}$)
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

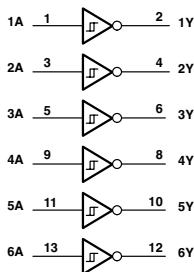
| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 30 | mA |
| I_{DH} | MAX | -0.4 | mA |
| I_{OL} | MAX | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-----------|--------|--------|------------|----|
| t_{PLH} | A or B | Y | MAX | 20 |
| t_{PHL} | A or B | Y | MAX | 30 |

UNIT: ns

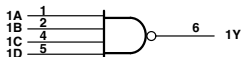
Logic Diagram



DUAL 4-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C \cdot D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE
(each gate)

| INPUTS | | | | OUTPUT Y |
|--------|---|---|---|-------------|
| A | B | C | D | |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------|------|----|------|-----|-----|------------|------------|-------------|------|
| I_{CC} | MAX | 11 | 2.2 | 18 | 1.5 | 8.7 | 5.1 | 0.02 | 0.04 | 0.04 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | mA |

| PARAMETER | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LV 3V | LV 5V | UNIT |
|-----------|------------|----------|------------|-----------|-------------|----------|----------|------|
| I_{CC} | MAX | 0.04 | 0.08 | 0.04 | 0.08 | - | 0.02 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -24 | -6 | -12 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 24 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|-----------|--------------|--------|------------|-----|----|-----|-----|-----|-----|------------|------------|-------------|
| t_{PLH} | A, B, C or D | Y | MAX | 22 | 15 | 4.5 | 11 | 5 | 6 | 28 | 30 | 42 |
| t_{PHL} | A, B, C or D | Y | MAX | 15 | 15 | 5 | 10 | 4.5 | 5.3 | 28 | 30 | 42 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LV 3V | LV 5V |
|-----------|--------------|--------|------------|----------|------------|-----------|-------------|----------|----------|
| t_{PLH} | A, B, C or D | Y | MAX | 6.7 | 12.2 | 9.1 | 13.5 | 11.5 | 8 |
| t_{PHL} | A, B, C or D | Y | MAX | 7.3 | 12.2 | 9.2 | 13.5 | 11.5 | 8 |

UNIT: ns

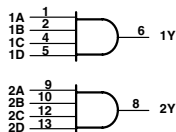
DUAL 4-INPUT POSITIVE-AND GATES

- $Y = A \cdot B \cdot C \cdot D$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE
(each gate)

| INPUTS | | | | OUTPUT |
|--------|---|---|---|--------|
| A | B | C | D | Y |
| H | H | H | H | H |
| L | X | X | X | L |
| X | L | X | X | L |
| X | X | L | X | L |
| X | X | X | L | L |

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | ACT 11 | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|----|-----|---------|---------|----------|-------|--------|-------|-------|------|
| I_{CC} | MAX | 4.4 | 2.3 | 12 | 7.3 | 0.02 | 0.04 | 0.04 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | -6 | -12 | mA |
| I_{OL} | MAX | 8 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | ACT 11 |
|-----------|--------------|--------|------------|----|-----|----|-----|---------|---------|----------|-------|--------|
| t_{PLH} | A, B, C or D | Y | MAX | 15 | 15 | 6 | 5.3 | 28 | 33 | 41 | 8.8 | 9.8 |
| t_{PHL} | A, B, C or D | Y | MAX | 20 | 10 | 6 | 5.5 | 28 | 33 | 41 | 6.9 | 8.9 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V |
|-----------|--------------|--------|------------|-------|-------|
| t_{PLH} | A, B, C or D | Y | MAX | 12 | 8 |
| t_{PHL} | A, B, C or D | Y | MAX | 12 | 8 |

UNIT: ns

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

- $Y = \overline{G(A + B + C + D)}$

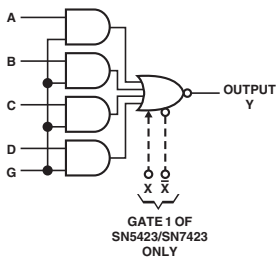
FUNCTION TABLE
(each gate)

| INPUTS | | | | | OUTPUT |
|--------|---|---|---|---|--------|
| A | B | C | D | G | Y |
| H | X | X | X | H | L |
| X | H | X | X | H | L |
| X | X | H | X | H | L |
| X | X | X | H | H | L |
| L | L | L | L | X | H |
| X | X | X | X | L | H |

Expander inputs are open.

H = high level, L = low level, X = irrelevant

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 19 | mA |
| I_{OH} | MAX | -0.8 | mA |
| I_{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

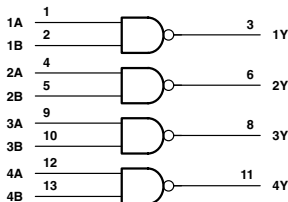
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|-----------|--------|--------|------------|-----|
| t_{PLH} | A or B | Y | MAX | 22 |
| t_{PHL} | A or B | Y | MAX | 15 |

UNIT: ns

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

$$\bullet Y = \overline{AB}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------|------------|-----|-----|------|
| I_{CC} | MAX | 22 | 4.4 | mA |
| V_{OH} | MAX | 15 | 15 | V |
| I_{OL} | MAX | 16 | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|-----------|--------|--------|------------|-----|----|
| t_{PLH} | A or B | Y | MAX | 24 | 32 |
| t_{PHL} | A or B | Y | MAX | 17 | 28 |

UNIT: ns

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TRIPLE 3-INPUT POSITIVE-NOR GATES

$$\bullet Y = \overline{A + B + C}$$

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE
(each gate)

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | ACT 11 | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|------|------|----|---------|---------|----------|-------|--------|-------|-------|------|
| I_{CC} | MAX | 26 | 6.8 | 4 | 17.1 | 12 | 0.02 | 0.04 | 0.04 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | -6 | -12 | mA |
| I_{OL} | MAX | 16 | 8 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 |
|-----------|-----------|--------|------------|-----|----|-----|-----|-----|---------|---------|----------|-------|
| t_{PLH} | A, B or C | Y | MAX | 15 | 15 | 15 | 5.5 | 5.5 | 23 | 29 | 35 | 7.7 |
| t_{PHL} | A, B or C | Y | MAX | 11 | 15 | 9 | 4.5 | 4.5 | 23 | 29 | 35 | 8.1 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT 11 | LV 3V | LV 5V |
|-----------|-----------|--------|------------|--------|-------|-------|
| t_{PLH} | A, B or C | Y | MAX | 10.1 | 14 | 9 |
| t_{PHL} | A, B or C | Y | MAX | 9.4 | 14 | 9 |

UNIT: ns

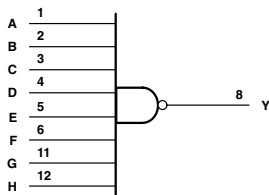
8-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

| INPUTS A-H | OUTPUT Y |
|----------------------|-------------|
| All inputs H | L |
| One or more inputs L | H |

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | ACT 11 | UNIT |
|-----------|------------|------|------|----|------|-----|----|------------|------------|-------------|----------|-----------|------|
| I_{CC} | MAX | 6 | 1.1 | 10 | 0.9 | 4.9 | 4 | 0.02 | 0.04 | 0.04 | 0.04 | 0.04 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | ACT 11 |
|-----------|----------|--------|------------|-----|----|---|-----|-----|-----|------------|------------|-------------|----------|-----------|
| t_{PLH} | A thru H | Y | MAX | 22 | 15 | 6 | 10 | 5 | 5.5 | 33 | 39 | 42 | 7.2 | 8.5 |
| t_{PHL} | A thru H | Y | MAX | 15 | 20 | 7 | 12 | 4.5 | 5 | 33 | 39 | 42 | 7.4 | 8.7 |

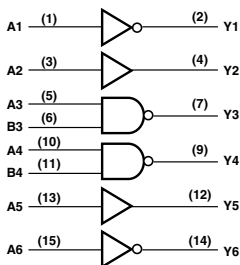
UNIT: ns

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DELAY ELEMENTS

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I_{OL} of 12/24mA
- P-N-P Inputs Reduce Fan-In ($I_{IL} = -0.2\text{mA MAX}$)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Range

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|-------------------|-----|---------|
| I_{CC} | MAX | 20 | mA |
| I_{OH} | Y3, Y4 outputs | MAX | -1.2 mA |
| | All other outputs | MAX | -0.4 mA |
| I_{OL} | Y3, Y4 outputs | MAX | 24 mA |
| | All other outputs | MAX | 8 mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-----------|------------------|--------|------------|----|
| t_{PLH} | A1, A6 | Y1, Y6 | MAX | 65 |
| t_{PHL} | | | | 45 |
| t_{PLH} | A2, A5 | Y2, Y5 | MAX | 80 |
| t_{PHL} | | | | 95 |
| t_{PLH} | A3, B3 A4, Y4 | Y3, Y4 | MAX | 15 |
| t_{PHL} | | | | 15 |

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-OR GATES



● $Y = A + B$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | UNIT |
|-----------|------------|------|------|----|------|------|------|---------|---------|----------|----------|-------|------|
| I_{CC} | MAX | 38 | 9.8 | 68 | 4.9 | 26.6 | 15.5 | 0.02 | 0.04 | 0.02 | 0.04 | 0.04 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | mA |

| PARAMETER | MAX or MIN | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------|------------|---------|---------|--------|----------|----------|------|------|-------|-------|--------|---------|----------|----------|------|
| I_{CC} | MAX | 0.02 | 0.08 | 0.04 | 0.02 | 0.08 | 0.02 | 0.02 | 0.02 | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -24 | -8 | -9 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|-----------|--------|--------|------------|-----|----|---|-----|-----|-----|---------|---------|----------|
| t_{PLH} | A or B | Y | MAX | 15 | 22 | 7 | 14 | 5.8 | 6.6 | 25 | 27 | 30 |
| t_{PHL} | A or B | Y | MAX | 22 | 22 | 7 | 12 | 5.8 | - | 25 | 27 | 30 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT |
|-----------|--------|--------|------------|----------|-------|---------|---------|--------|----------|----------|-----|------|
| t_{PLH} | A or B | Y | MAX | 36 | 6.7 | 8.5 | 9.5 | 9 | 10 | 12.1 | 8.5 | 9 |
| t_{PHL} | A or B | Y | MAX | 36 | 5.9 | 7.5 | 9.5 | 8 | 10 | 12.1 | 8.5 | 9 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|-----------|--------|--------|------------|-------|-------|--------|---------|----------|----------|
| t_{PLH} | A or B | Y | MAX | 13 | 8.5 | 3.8 | 2.8 | 2.5 | 2.1 |
| t_{PHL} | A or B | Y | MAX | 13 | 8.5 | 3.8 | 2.8 | 2.5 | 2.1 |

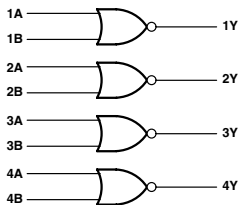
UNIT: ns

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QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

$$\bullet Y = \overline{A + B}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | UNIT |
|-----------|------------|------|------|-----|------|
| I_{CC} | MAX | 16.5 | 13.8 | 9 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | V |
| I_{OL} | MAX | 48 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS |
|-----------|--------|--------|------------|-----|----|-----|
| t_{PLH} | A or B | Y | MAX | 15 | 32 | 33 |
| t_{PHL} | A or B | Y | MAX | 18 | 28 | 12 |

UNIT: ns

34

HEX BUFFER GATE

$$\bullet Y = A$$

Logic Diagram

FUNCTION TABLE
(each gate)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AUC 1.8V | AUC 2.5V | UNIT |
|-----------|------------|-------------|-------------|------|
| I_{CC} | MAX | 0.01 | 0.01 | mA |
| I_{DH} | MAX | -8 | -9 | mA |
| I_{OL} | MAX | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUC 1.8V | AUC 2.5V |
|-----------|-------|--------|------------|-------------|-------------|
| t_{PLH} | A | Y | MAX | 2.4 | 1.8 |
| t_{PHL} | | | | 2.4 | 1.8 |

UNIT: ns

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HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

● Y = A

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

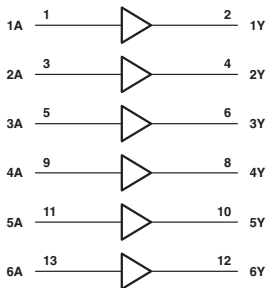
| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 63 | mA |
| V _{OH} | MAX | 5.5 | V |
| I _{OL} | MAX | 8 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 50 |
| t _{PHL} | A | Y | MAX | 14 |

UNIT: ns

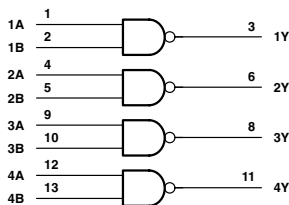
Logic Diagram



QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | F | UNIT |
|-----------|------------|------|------|----|------|-----|------|
| I_{CC} | MAX | 54 | 12 | 80 | 7.8 | 33 | mA |
| I_{OH} | MAX | -1.2 | -1.2 | -3 | -2.6 | -15 | mA |
| I_{OL} | MAX | 48 | 24 | 60 | 24 | 64 | mA |

SWITCHING CHARACTERISTICS

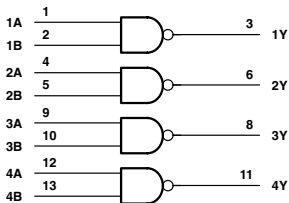
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | F |
|-----------|--------|--------|------------|-----|----|-----|-----|-----|
| t_{PLH} | A or B | Y | MAX | 22 | 24 | 6.5 | 8 | 6.5 |
| t_{PHL} | A or B | Y | MAX | 15 | 24 | 6.5 | 7 | 5 |

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | F | UNIT |
|-----------|------------|-----|-----|-----|-----|-----|------|
| I_{CC} | MAX | 54 | 12 | 80 | 7.8 | 30 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 4.5 | V |
| I_{OL} | MAX | 48 | 24 | 60 | 24 | 64 | mA |

SWITCHING CHARACTERISTICS

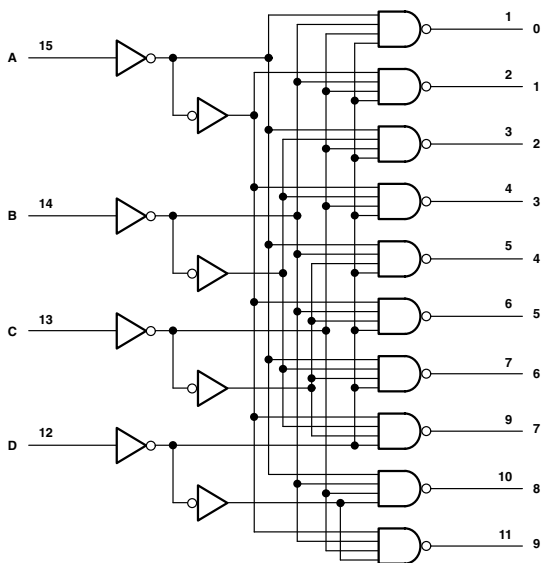
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | F |
|-----------|--------|--------|------------|-----|----|----|-----|-----|
| t_{PLH} | A or B | Y | MAX | 22 | 32 | 10 | 33 | 13 |
| t_{PHL} | A or B | Y | MAX | 18 | 28 | 10 | 12 | 5.5 |

UNIT: ns

4-LINE-TO-10-LINE DECODERS (1 of 10)

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
 - 3-Line to 8-Line Decoders
 - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| No. | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---------|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | L | H | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | L | H | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | L | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 56 | 13 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

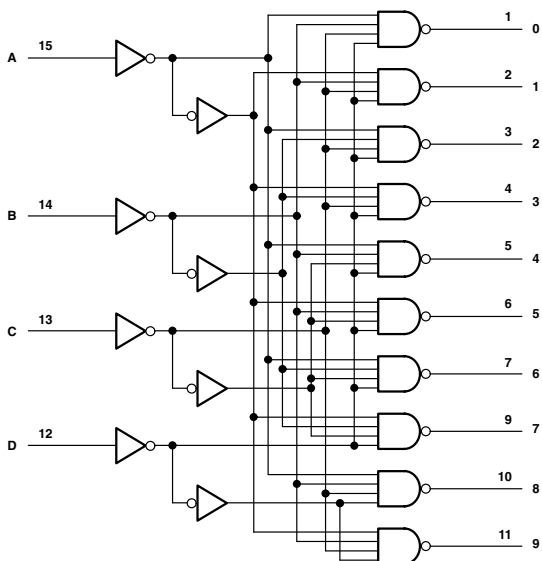
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|--------------------------|--------------|--------|------------|-----|----|---------|---------|----------|
| t_{PLH} 2Level - Logic | A, B, C or D | 0-9 | MAX | 25 | 25 | 38 | 45 | 53 |
| t_{PHL} 2Level - Logic | | 0-9 | | 25 | 25 | 38 | 45 | 53 |
| t_{PLH} 3Level - Logic | A, B, C or D | 0-9 | MAX | 30 | 30 | 38 | 45 | 53 |
| t_{PHL} 3Level - Logic | | 0-9 | | 30 | 30 | 38 | 45 | 53 |

UNIT: ns

BCD-TO-DECIMAL DECODERS/DRIVERS

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

Logic Diagram (SN74)



FUNCTION TABLE

| No. | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---------|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | L | H | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | L | H | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | L | H | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | L | H | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | L | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING C

| PARAMETER | MAX or MIN | TTL | UNIT |
|---------------------|------------|-----|------|
| I _{CC} | MAX | 70 | mA |
| V _O (on) | MAX | 0.9 | V |
| I _{OL} | MAX | 80 | mA |

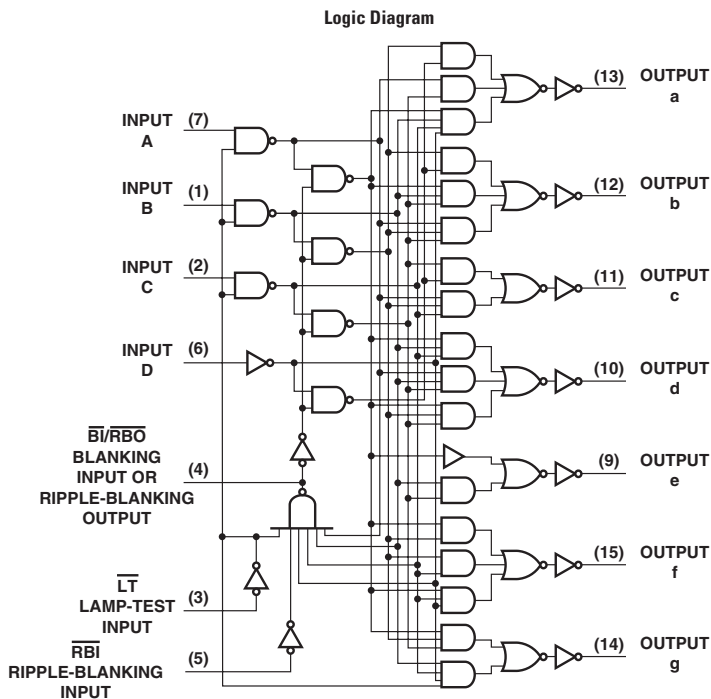
SWITCHING CHARACTERISTICS

| PARAMETER | MAX or MIN | TTL |
|------------------|------------|-----|
| t _{PLH} | MAX | 25 |
| t _{PHL} | | 25 |

UNIT: ns

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression



FUNCTION TABLE

| No. | INPUTS | | | | | | $\overline{\text{BI/RBO}}^\dagger$ | OUTPUTS | | | | | | |
|-----|------------------------|-------------------------|---|---|---|---|------------------------------------|---------|-----|-----|-----|-----|-----|-----|
| | $\overline{\text{LT}}$ | $\overline{\text{RBI}}$ | D | C | B | A | | a | b | c | d | e | f | g |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | ON |
| 1 | H | X | L | L | L | H | H | OFF | ON | ON | ON | OFF | OFF | OFF |
| 2 | H | X | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON |
| 3 | H | X | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON |
| 4 | H | X | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON |
| 5 | H | X | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON |
| 6 | H | X | L | H | H | L | H | OFF | OFF | ON | ON | ON | ON | ON |
| 7 | H | X | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF |
| 8 | H | X | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON |
| 9 | H | X | H | L | L | H | H | ON | ON | ON | OFF | OFF | ON | ON |
| 10 | H | X | H | L | H | L | H | OFF | ON | OFF | ON | ON | OFF | ON |
| 11 | H | X | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON |
| 12 | H | X | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON |
| 13 | H | X | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON |
| 14 | H | X | H | H | L | L | H | OFF | OFF | OFF | ON | ON | ON | ON |
| 15 | H | X | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| BI | X | X | X | X | X | X | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| RBI | L | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| LT | L | X | X | X | X | X | H | ON | ON | ON | ON | ON | ON | ON |

H = high level, L = low level, irrelevant

- NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open held at high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking input/ripple blanking output ($\overline{\text{BI/RBO}}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

† $\overline{\text{BI/RBO}}$ is wire AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBI}}$).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------|------------|------|-------|------|
| I_{CC} | MAX | 103 | 13 | mA |
| I_{OH} | MAX | -0.2 | -0.05 | mA |
| I_{OL} | MAX | 8 | 3.2 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|-----------|-------------------------|--------|------------|-----|-----|
| t_{OFF} | A | A to g | MAX | 100 | 100 |
| t_{ON} | A | A to g | MAX | 100 | 100 |
| t_{OFF} | $\overline{\text{RBI}}$ | A to g | MAX | 100 | 100 |
| t_{ON} | $\overline{\text{RBI}}$ | A to g | MAX | 100 | 100 |

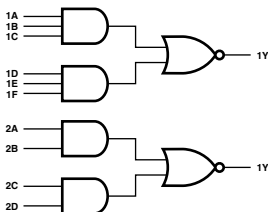
UNIT: ns

AND-OR-INVERT GATES

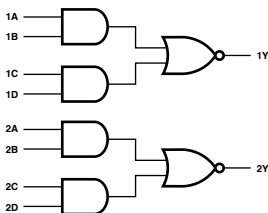
- '51, 'S51: $Y = \overline{AB + CD}$
- 'F51, 'LS51: $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
- 'HC51: $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

Logic Diagram

LS51



S51



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | F | SN74 HC | UNIT |
|-----------|------------|------|------|----|-----|------------|------|
| I_{CC} | MAX | 14 | 2.8 | 22 | 7.5 | 0.08 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -1 | -1 | -4 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 20 | 4 | mA |

SWITCHING CHARACTERISTICS

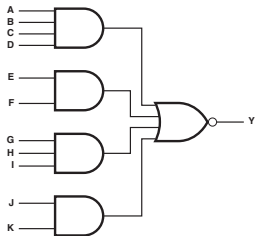
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | F | SN74 HC |
|-----------|-------|--------|------------|-----|----|-----|-----|------------|
| t_{PLH} | Any | Y | MAX | 22 | 20 | 5.5 | 6.5 | 35 |
| t_{PHL} | Any | Y | MAX | 15 | 20 | 5.5 | 4.5 | 35 |

UNIT: ns

4-2-3-2 INPUT AND-OR INVERT GATES

$$\bullet Y = \overline{ABCD + EF + GHI + JK}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | S | F | UNIT |
|-----------------|------------|----|-----|------|
| I _{CC} | MAX | 16 | 4.7 | mA |
| I _{OH} | MAX | -1 | -1 | mA |
| I _{OL} | MAX | 20 | 20 | mA |

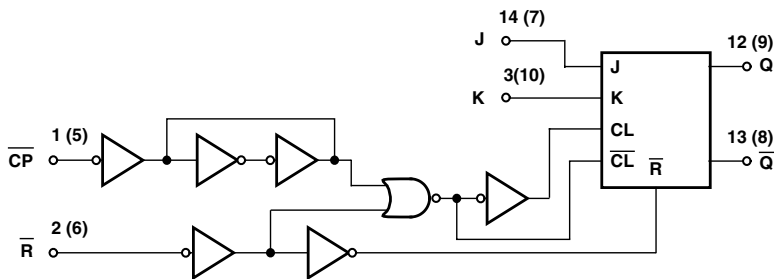
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | S | F |
|------------------|-------|--------|------------|-----|-----|
| t _{PLH} | Any | Y | MAX | 5.5 | 7 |
| t _{PHL} | Any | Y | MAX | 5.5 | 5.5 |

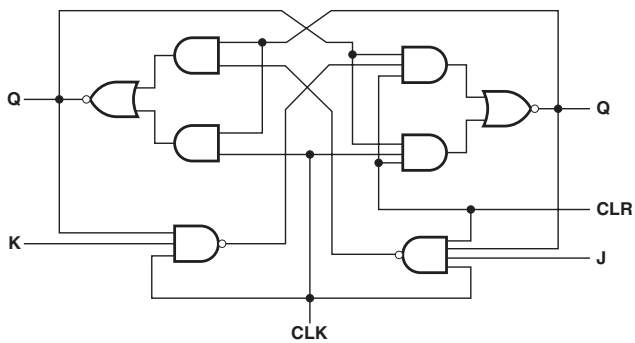
UNIT: ns

DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram



CD74HC/HCT73



SN74LS73

FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | |
|--------|-------|---|---|----------------|------------------------|
| CLEAR | CLOCK | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q ₀ | \bar{Q} ₀ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | TOGGLE |
| H | H | X | X | Q ₀ | \bar{Q} ₀ |

TRUTH TABLE (CD74)

| INPUTS | | | | OUTPUTS | |
|-----------|------------|---|---|-----------|-----------|
| \bar{R} | \bar{CP} | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | ↓ | L | L | No Change | No Change |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | Toggle |
| H | H | X | X | No Change | No Change |

NOTE:

H = High Level (Steady State)

L = Low Level (Steady State)

X = Irrelevant

↓ = High-to-Low Transition

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 20 | 6 | 0.04 | 0.08 | 0.08 | mA |
| I _{OH} | MAX | 16 | 8 | 4 | 4 | 4 | mA |
| I _{OL} | MAX | -0.4 | -0.4 | -4 | -4 | -4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

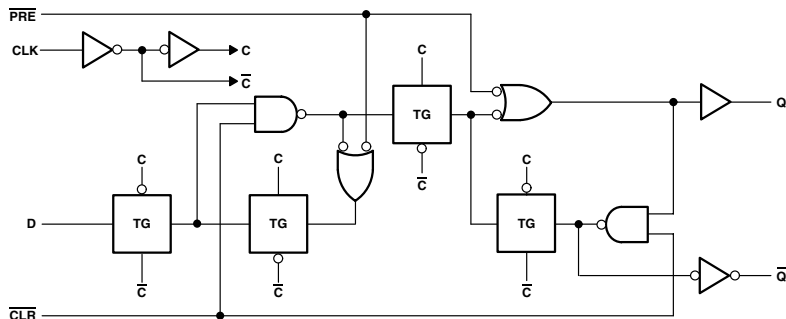
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|-------------------|----------------|------------|-----|------|---------|---------|----------|
| | | | | | | | | |
| f _{max} | | | MIN | 15 | 30 | 25 | 20 | 20 |
| t _w | CLOCK "L" | | MIN | 20 | - | 20 | - | - |
| | CLOCK "H" | | | 47 | 20 | 20 | - | - |
| | CP Pulse Wide | | | - | - | - | 24 | 24 |
| | CLEAR "L" | | | 25 | 20 | 20 | 24 | 27 |
| t _{su} | CLK | | MIN | 0 ↑ | 20 ↓ | 25 ↓ | - | - |
| | J,K to CP | | - | - | - | 24 | 24 | |
| t _h | CLK | | MIN | 0 ↓ | 0 ↓ | 0 ↓ | - | - |
| | J,K to \bar{CP} | | - | - | - | 3 | 3 | |
| t _{PLH} | \bar{CLEAR} | \bar{Q} | MAX | 25 | 20 | 39 | 44 | 51 |
| t _{PHL} | | | | - | 20 | 39 | 44 | 51 |
| t _{PLH} | \bar{CLEAR} | Q | MAX | - | 20 | 39 | 44 | 51 |
| t _{PHL} | | | | 40 | 20 | 39 | 44 | 51 |
| t _{PLH} | CLOCK | Q or \bar{Q} | MAX | 25 | 20 | 32 | - | - |
| t _{PHL} | | | | 40 | 20 | 32 | - | - |
| t _{PLH} | \bar{CP} | Q | MAX | - | - | - | 48 | 57 |
| t _{PHL} | | | | - | - | - | 48 | 57 |
| t _{PLH} | \bar{CP} | \bar{Q} | MAX | - | - | - | 48 | 54 |
| t _{PHL} | | | | - | - | - | 48 | 54 |

UNIT f_{max} : MHz, other : ns

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | |
|--------|-----|-------|---|----------------|-------------|
| PRE | CLR | CLOCK | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | \bar{Q}_0 |

† This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | UNIT |
|-----------------|------------|------|------|----|------|----|----|---------|---------|----------|----------|-------|---------|------|
| I _{CC} | MAX | 15 | 8 | 25 | 4 | 16 | 16 | 0.04 | 0.08 | 0.04 | 0.08 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V | UNIT |
|-----------------|------------|---------|--------|----------|----------|------|------|-------|-------|--------|----------|----------|------|
| I _{CC} | MAX | 0.08 | 0.04 | 0.02 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | 8 | 9 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | |
|------------------|----------|---------|-------------------|-----|----|------|------|------|------|---------|---------|----|
| f _{max} | | | MIN | 15 | 25 | 75 | 34 | 105 | 100 | 25 | 20 | |
| t _w | CLOCK'H' | | MIN | 30 | 25 | 6 | 14.5 | 4 | 4 | 20 | 24 | |
| | | | CLOCK'L' | MIN | 37 | - | 7.3 | 14.5 | 5.5 | 5 | 20 | 24 |
| | | | PRE, CLR 'L' | MIN | 30 | 25 | 7 | 15 | 4 | 4 | 25 | 24 |
| t _{su} | DATA | | MIN | 20 | 20 | 3 | 15 | 4.5 | 3 | 25 | 18 | |
| | | | PRE, CLR INACTIVE | MIN | 20 | - | - | 10 | 2 | 2 | 6 | - |
| t _h | | | MIN | 5 | 5 | 2 | 0 | 0 | 1 | 0 | 3 | |
| ↑P _{LH} | PRE | Q or Q̄ | MAX | 25 | 25 | 6 | 13 | 7.5 | 7.1 | 58 | 60 | |
| ↑P _{HL} | | | | 40 | 40 | 13.5 | 15 | 10.5 | 10.5 | 58 | 60 | |
| ↑P _{LH} | CLR | Q or Q̄ | MAX | 25 | 25 | 6 | 13 | 7.5 | 7.1 | 58 | 60 | |
| ↑P _{HL} | | | | 40 | 40 | 13.5 | 15 | 10.5 | 10.5 | 58 | 60 | |
| ↑P _{LH} | CLOCK | Q or Q̄ | MAX | 25 | 25 | 9 | 16 | 8 | 7.8 | 44 | 53 | |
| ↑P _{HL} | | | | 40 | 40 | 9 | 18 | 9 | 9.2 | 44 | 53 | |

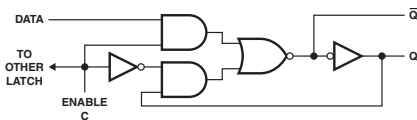
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HCT | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | |
|------------------|----------|---------|-------------------|----------|----------|-------|---------|---------|--------|----------|----------|-----|
| f _{max} | | | MIN | 22 | 16 | 125 | 125 | 110 | 100 | 125 | 85 | |
| t _w | CLOCK'H' | | MIN | 23 | 27 | 4 | 5 | 4.5 | 5 | 6 | 5.7 | |
| | | | CLOCK'L' | MIN | 23 | 27 | 4 | 5 | 4.5 | 5 | 6 | 5.7 |
| | | | PRE, CLR 'L' | MIN | 20 | 24 | 4 | 5 | 4 | 5 | 6 | 5 |
| t _{su} | DATA | | MIN | 15 | 18 | 3.5 | 3 | 3.5 | 4.5 | 3.5 | 4 | |
| | | | PRE, CLR INACTIVE | MIN | 0 | - | 1 | 0 | - | 2 | 0 | - |
| t _h | | | MIN | 0 | 3 | 0 | 0.5 | 0 | 0 | 1 | 0 | |
| ↑P _{LH} | PRE | Q or Q̄ | MAX | 44 | 60 | 7.1 | 10 | 10.5 | 9.6 | 10.5 | 11.5 | |
| ↑P _{HL} | | | | 44 | 60 | 9 | 10.5 | 11.5 | 12.5 | 11.5 | 12.5 | |
| ↑P _{LH} | CLR | Q or Q̄ | MAX | 44 | 60 | 7.1 | 10 | 10.5 | 9.6 | 10.5 | 11.5 | |
| ↑P _{HL} | | | | 44 | 60 | 9 | 10.5 | 11.5 | 12.5 | 11.5 | 12.5 | |
| ↑P _{LH} | CLOCK | Q or Q̄ | MAX | 35 | 53 | 8.2 | 10.5 | 10 | 9.4 | 13.0 | 9.5 | |
| ↑P _{HL} | | | | 35 | 53 | 7.5 | 10.5 | 10 | 8.8 | 11.5 | 9.5 | |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LV 3V | LV 5V | LVC 3V | AUC 1.8V | AUC 2.5V | |
|------------------|----------|---------|-------------------|------|------|-------|-------|--------|----------|----------|-----|
| f _{max} | | | MIN | 75 | 65 | 45 | 75 | 100 | 300 | 350 | |
| t _w | CLOCK'H' | | MIN | 5 | 5 | 7 | 5 | 3.3 | 0.5 | 0.5 | |
| | | | CLOCK'L' | MIN | 5 | 5 | 7 | 5 | 3.3 | 0.5 | 0.5 |
| | | | PRE, CLR 'L' | MIN | 5 | 5 | 7 | 5 | 3.3 | 1.5 | 1.5 |
| t _{su} | DATA | | MIN | 5 | 5 | 7 | 5 | 3 | 0.6 | 0.7 | |
| | | | PRE, CLR INACTIVE | MIN | 3 | 3.5 | 5 | 3 | 2 | 0.2 | 0.3 |
| t _h | | | MIN | 0.5 | 0 | 0.5 | 0.5 | 0 | 0.3 | 0.3 | |
| ↑P _{LH} | PRE | Q or Q̄ | MAX | 11 | 13 | 18 | 11 | 5.4 | 3.1 | 2.5 | |
| ↑P _{HL} | | | | 11 | 13 | 18 | 11 | 5.4 | 3.1 | 2.5 | |
| ↑P _{LH} | CLR | Q or Q̄ | MAX | 11 | 13 | 18 | 11 | 5.4 | 3 | 2.4 | |
| ↑P _{HL} | | | | 11 | 13 | 18 | 11 | 5.4 | 3 | 2.4 | |
| ↑P _{LH} | CLOCK | Q or Q̄ | MAX | 10.5 | 10 | 17.5 | 10.5 | 5.2 | 2.8 | 2.2 | |
| ↑P _{HL} | | | | 10.5 | 10 | 17.5 | 10.5 | 5.2 | 2.8 | 2.2 | |

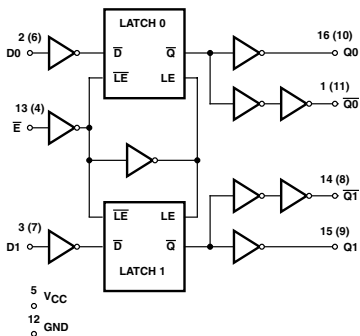
UNIT f_{max} : MHz, other : ns

4-BIT BISTABLE LATCHES

Logic Diagram



SN74LS75



CD74HC/HCT75

FUNCTION TABLE
(SN74)

| INPUTS | | OUTPUTS | |
|--------|---|---------|-------------|
| D | C | Q | \bar{Q} |
| L | H | L | H |
| H | H | H | L |
| X | L | Q_0 | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------|------|---------|---------|----------|------|
| I_{CC} | MAX | 53 | 12 | 0.04 | 0.08 | 0.08 | mA |
| I_{OH} | MAX | -0.4 | -0.4 | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 16 | 8 | 4 | 4 | 4 | mA |

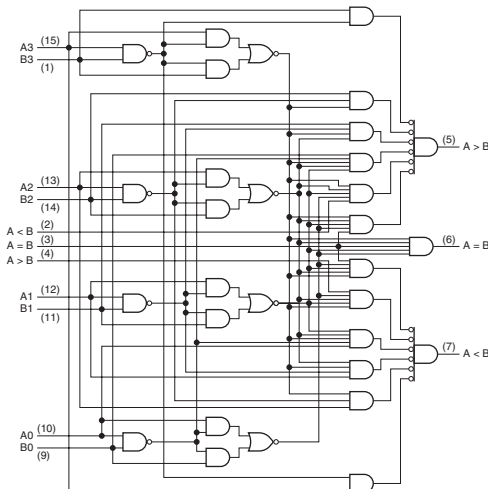
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|-----------|-------|-----------|------------|-----|----|---------|---------|----------|
| t_w | | | MIN | 20 | 20 | 20 | 24 | 24 |
| t_{su} | | | MIN | 20 | 20 | 25 | 18 | 18 |
| t_h | | | MIN | 5 | 5 | 5 | 3 | 3 |
| t_{PLH} | D | Q | MAX | 30 | 27 | 30 | 33 | 42 |
| t_{PHL} | D | \bar{Q} | MAX | 25 | 17 | 30 | 33 | 42 |
| t_{PLH} | D | Q | MAX | 40 | 20 | 30 | 39 | 42 |
| t_{PHL} | D | \bar{Q} | MAX | 15 | 15 | 30 | 39 | 42 |
| t_{PLH} | G | Q | MAX | 30 | 27 | 33 | 39 | 42 |
| t_{PHL} | G | \bar{Q} | MAX | 15 | 25 | 33 | 39 | 42 |
| t_{PLH} | G | Q | MAX | 30 | 30 | 33 | 39 | 45 |
| t_{PHL} | G | \bar{Q} | MAX | 15 | 15 | 33 | 39 | 45 |

UNIT: ns

4-BIT MAGNITUDE COMPARATORS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|------------------|--------|--------|--------|------------------|-----|-----|---------|-----|-----|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A>B | A<B | A=B | A>B | A<B | A=B |
| A3=B3 | X | X | X | X | X | X | H | L | L |
| A3<B3 | X | X | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | X | X | X | X | X | H | L | L |
| A3=B3 | A2=B2 | X | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | X | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | L | L | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | H | L | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | L | L | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | L | H | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | H | L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|-----|---------|---------|----------|------|
| I _{CC} | MAX | 88 | 20 | 115 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -1 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | Number of Gate Levels | MAX or MIN | TTL | LS | S | SN74 HC | CD74 HC | CD74 HCT |
|------------------|-----------------------|--------------|-----------------------|------------|-----|----|------|---------|---------|----------|
| t _{PLH} | Any A or B data input | A < B, A > B | 3 | MAX | 26 | 36 | 16 | 58 | 59 | 56 |
| | | A = B | 4 | MAX | 35 | 45 | 18 | 50 | 53 | 60 |
| t _{PHL} | Any A or B data input | A < B, A > B | 3 | MAX | 30 | 30 | 16.5 | 58 | 59 | 56 |
| | | A = B | 4 | MAX | 30 | 45 | 16.5 | 50 | 53 | 60 |
| t _{PLH} | A < B, A = B | A > B | 1 | MAX | 11 | 22 | 7.5 | 44 | 42 | 45 |
| | | A < B, A = B | 1 | | 17 | 17 | 8.5 | 44 | 42 | 45 |
| t _{PHL} | A = B | A = B | 2 | MAX | 20 | 20 | 10.5 | 37 | - | - |
| | | A = B | 2 | | 17 | 26 | 7.5 | 37 | - | - |
| t _{PLH} | A > B, A = B | A < B | 1 | MAX | 11 | 22 | 7.5 | 44 | 42 | 45 |
| | | A > B, A = B | 1 | | 17 | 17 | 8.5 | 44 | 42 | 45 |

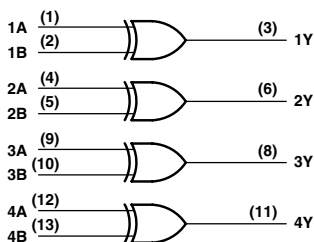
UNIT: ns

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

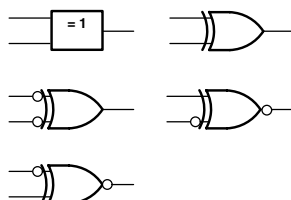
- $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

Logic Diagram (SN74)



Exclusive OR



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | SN74 AC | CD74 AC | ACT 11 | UNIT |
|-----------|------------|------|------|----|------|----|----|---------|---------|----------|-------|---------|---------|--------|------|
| I_{CC} | MAX | 50 | 10 | 75 | 5.9 | 38 | 28 | 0.02 | 0.04 | 0.04 | 0.04 | 0.02 | 0.08 | 0.04 | mA |
| I_{OH} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | 24 | 24 | mA |
| I_{OL} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | -24 | -24 | mA |

| PARAMETER | MAX or MIN | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | UNIT |
|-----------|------------|----------|----------|------|------|-------|-------|--------|------|
| I_{CC} | MAX | 0.04 | 0.08 | 0.02 | 0.02 | - | 0.02 | 0.01 | mA |
| I_{OH} | MAX | 24 | 24 | -10 | 8 | 6 | 12 | 24 | mA |
| I_{OL} | MAX | -24 | -24 | 10 | -8 | -6 | -12 | -24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 |
|----------------------|--------|--------|------------|-----|----|------|-----|-----|-----|---------|---------|----------|-------|
| t_{PLH} Input Low | A or B | Y | MAX | 23 | 23 | 10.5 | 17 | 7.5 | 6.5 | 25 | 36 | 48 | 7.6 |
| t_{PHL} Input Low | | Y | MAX | 17 | 17 | 10 | 12 | 6.5 | 6.5 | 25 | 36 | 48 | 6.8 |
| t_{PLH} Input High | A or B | Y | MAX | 30 | 30 | 10.5 | 17 | 6.5 | 8 | 25 | 36 | 48 | 7.6 |
| t_{PHL} Input High | | Y | MAX | 22 | 22 | 10 | 10 | 7 | 7.5 | 25 | 36 | 48 | 6.8 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V |
|----------------------|--------|--------|------------|---------|---------|--------|----------|----------|-----|------|-------|-------|--------|
| t_{PLH} Input Low | A or B | Y | MAX | 9 | 10.8 | 9.6 | 10 | 14.6 | 10 | 10 | 16.5 | 10 | 4.6 |
| t_{PHL} Input Low | | Y | MAX | 9.5 | 10.8 | 9 | 10.5 | 14.6 | 10 | 10 | 16.5 | 10 | 4.6 |
| t_{PLH} Input High | A or B | Y | MAX | 9 | 10.8 | 9.6 | 10 | 14.6 | 10 | 10 | 16.5 | 10 | 4.6 |
| t_{PHL} Input High | | Y | MAX | 9.5 | 10.8 | 9 | 10.5 | 14.6 | 10 | 10 | 16.5 | 10 | 4.6 |

UNIT: ns

DECADE COUNTER

FUNCTION TABLE

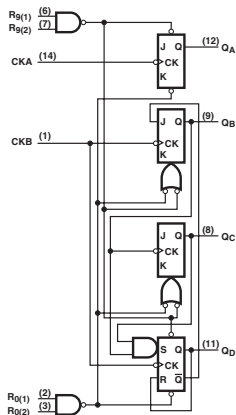
| Count | BCD COUNT SEQUENCE | | | |
|-------|--------------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | X | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

| Count | BI-QUINARY | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _A | Q _D | Q _C | Q _B |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

RESET/COUNT

| RESET INPUTS | | | | OUTPUTS | | | |
|--------------------|--------------------|--------------------|--------------------|----------------|----------------|----------------|----------------|
| R ₀ (1) | R ₀ (2) | R ₉ (1) | R ₉ (2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | | | | Count |
| L | X | L | X | | | | Count |
| L | X | X | L | | | | Count |
| X | L | L | X | | | | Count |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 39 | 15 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|----------------|---------------------------------|------------|-----|----|
| f _{max} | A | Q _A | MIN | 32 | 32 |
| | B | Q _B | | 16 | 16 |
| t _w | A | | MIN | 15 | 15 |
| | B | | | 30 | 30 |
| | RESET | | | 15 | 30 |
| t _{su} | RESET INACTIVE | | MIN | 25 | 25 |
| t _{PLH} | A | Q _A | MAX | 16 | 16 |
| t _{PHL} | | Q _B | | 18 | 18 |
| t _{PLH} | A | Q _D | MAX | 48 | 48 |
| t _{PHL} | | Q _B | | 50 | 50 |
| t _{PLH} | B | Q _B | MAX | 16 | 16 |
| t _{PHL} | | Q _C | | 21 | 21 |
| t _{PLH} | B | Q _C | MAX | 32 | 32 |
| t _{PHL} | | Q _C | | 35 | 35 |
| t _{PLH} | B | Q _C | MAX | 32 | 32 |
| t _{PHL} | | Q _C | | 35 | 35 |
| t _{PHL} | Set to 0 | Any | MAX | 40 | 40 |
| t _{PLH} | Set to 9 | Q _A , Q _D | MAX | 30 | 30 |
| | | Q _B , Q _C | | 40 | 40 |

UNIT f_{max} : MHz, other : ns

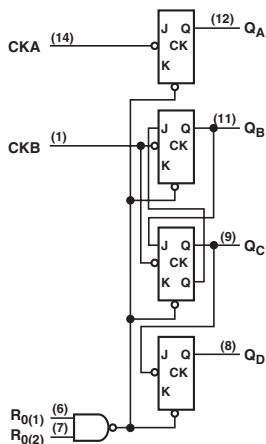
DIVIDE-BY-TWELVE DECODE COUNTERS

FUNCTION TABLE
COUNT SEQUENCE

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

RESET/COUNT

| RESET INPUTS | | OUTPUTS | | | |
|--------------|-------|----------------|----------------|----------------|----------------|
| R0(1) | R0(2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 39 | 15 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|----------------|----------------|------------|-----|----|
| f _{max} | A | Q _A | MIN | 32 | 32 |
| | B | Q _B | | 16 | 16 |
| t _w | A | | MIN | 15 | 15 |
| | B | | | 30 | 30 |
| | RESET | | | 15 | 30 |
| t _{su} | RESET INACTIVE | | MIN | 25 | 25 |
| t _{PLH} | A | Q _A | MAX | 16 | 16 |
| t _{PHL} | | | | 18 | 18 |
| t _{PLH} | A | Q _D | MAX | 48 | 48 |
| t _{PHL} | | | | 50 | 50 |
| t _{PLH} | B | Q _B | MAX | 16 | 16 |
| t _{PHL} | | | | 21 | 21 |
| t _{PLH} | B | Q _C | MAX | 16 | 16 |
| t _{PHL} | | | | 21 | 21 |
| t _{PLH} | B | Q _D | MAX | 32 | 32 |
| t _{PHL} | | | | 35 | 35 |
| t _{PHL} | Set to 0 | Any | MAX | 40 | 40 |

UNIT f_{max} : MHz, other : ns

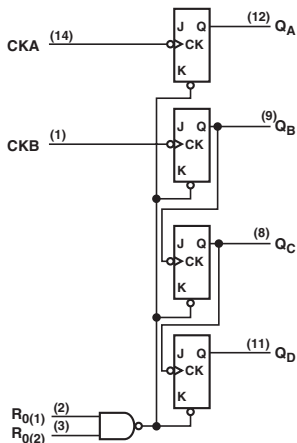
4-BIT BINARY COUNTERS

FUNCTION TABLE (SN74)
COUNT SEQUENCE

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

RESET/COUNT

| RESET INPUTS | | OUTPUTS | | | |
|--------------------|--------------------|----------------|----------------|----------------|----------------|
| R ₀ (1) | R ₀ (2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | L | L | L |
| L | X | | | | COUNT |
| X | L | | | | COUNT |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|----------|------|
| I _{CC} | MAX | 39 | 15 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

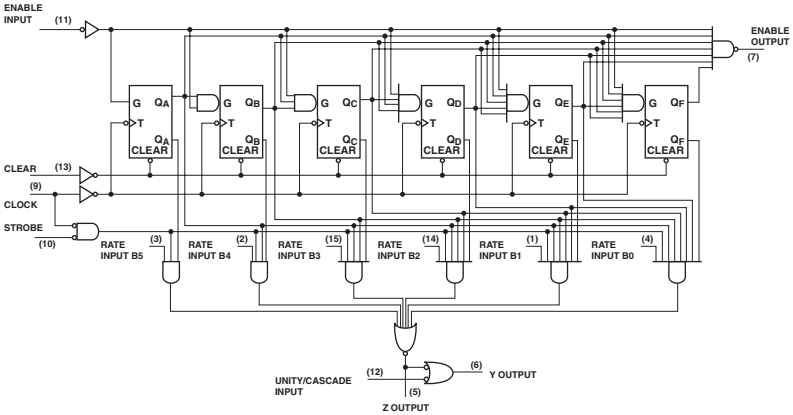
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT |
|------------------|---------------------------|---------------------------|------------|-----|----|---------|----------|
| f _{max} | A (CD74:CP ₀) | QA (CD74:Q ₀) | MIN | 32 | 32 | 20 | 20 |
| | B (CD:74CP1) | QB (CD74:Q ₁) | | 16 | 16 | 20 | 20 |
| t _w | A (CP ₀) | | MIN | 15 | 15 | 24 | 24 |
| | B (CP1) | | | 30 | 30 | 24 | 24 |
| | RESET | | | 15 | 30 | 24 | 24 |
| t _{su} | RESET INACTIVE | | MIN | 25 | 25 | - | - |
| t _{PLH} | CKA (CP ₀) | QA (Q ₀) | MAX | 16 | 16 | 38 | 51 |
| | | QB (Q ₁) | | 18 | 18 | 38 | 51 |
| t _{PLH} | CKA (CP ₀) | QC (Q ₂) | MAX | 70 | 70 | - | - |
| | | QD (Q ₃) | | 70 | 70 | - | - |
| t _{PHL} | CKB (CP1) | QB (Q ₁) | MAX | 16 | 16 | 41 | 51 |
| | | QC (Q ₂) | | 21 | 21 | 41 | 51 |
| t _{PLH} | CKB (CP1) | QC (Q ₂) | MAX | 32 | 32 | 56 | 69 |
| | | QD (Q ₃) | | 35 | 35 | 56 | 69 |
| t _{PHL} | CKB (CP1) | QD (Q ₃) | MAX | 51 | 51 | 74 | 87 |
| | | ANY | | 51 | 51 | 74 | 87 |
| t _{PHL} | Set to 0 | ANY | MAX | 40 | 40 | - | - |

UNIT f_{max} : MHz, other : ns

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

- Perform Fixed-Rate or Variable-Rate Frequency Division
- Typical Maximum Clock Frequency: 32MHz

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | |
|--------|--------|--------|--|---------------------------|-------------------|-----------------------------------|----|--------|
| CLEAR | ENABLE | STROBE | BINARY RATE B ₃ B ₂ B ₁ B ₀ | NUMBER OF CLOCK PULSES | UNITY/ CASCADE | LOGI LEVEL OR NUMBER OF PULSES | | |
| | | | | | | Y | Z | ENABLE |
| H | X | H | X X X X X X | X | H | L H | H | |
| L | L | L | L L L L L L L L | 64 | H | L | H | 1 |
| L | L | L | L L L L L L L H | 64 | H | 1 | 1 | 1 |
| L | L | L | L L L L L H L L | 64 | H | 2 | 2 | 1 |
| L | L | L | L L L L H L L L | 64 | H | 4 | 4 | 1 |
| L | L | L | L L H L L L L L | 64 | H | 8 | 8 | 1 |
| L | L | L | L H L L L L L L | 64 | H | 16 | 16 | 1 |
| L | L | L | H L L L L L L L | 64 | H | 32 | 32 | 1 |
| L | L | L | H H H H H H H H | 64 | H | 63 | 63 | 1 |
| L | L | L | H H H H H H H H | 64 | L | H | 63 | 1 |
| L | L | L | H L H L L L L L | 64 | H | 40 | 40 | 1 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

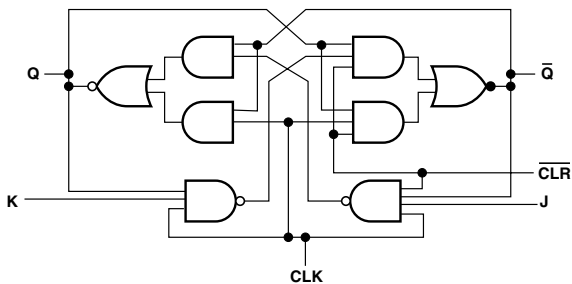
| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------------|------------|------|------|
| I _{cc} | MAX | 120 | mA |
| I _{oh} | MAX | 16 | mA |
| I _{ol} | MAX | -0.4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

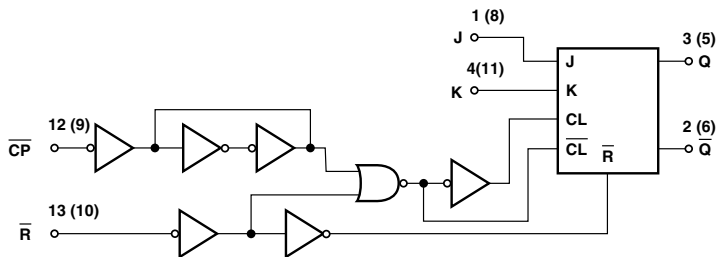
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|------------------|---------------|--------|------------|-----|
| f _{max} | A | QA | MIN | 25 |
| t _w | CLK | | MIN | 20 |
| | CLR | | MIN | 15 |
| t _{su} | Positive | | MIN | 25 |
| | Negative | | MIN | 0 |
| t _h | Positive | | MIN | 0 |
| | Negative | | MIN | 20 |
| †P _{LH} | ENABLE | ENABLE | MAX | 20 |
| †P _{HL} | | | MAX | 21 |
| †P _{LH} | STRB | Z | MAX | 18 |
| †P _{HL} | | | MAX | 23 |
| †P _{LH} | CLK | Y | MAX | 39 |
| †P _{HL} | | | MAX | 30 |
| †P _{LH} | CLK | Z | MAX | 18 |
| †P _{HL} | | | MAX | 26 |
| †P _{LH} | RATE | Z | MAX | 10 |
| †P _{HL} | | | MAX | 14 |
| †P _{LH} | UNITY /CAS | Y | MAX | 14 |
| †P _{HL} | | | MAX | 10 |
| †P _{LH} | STRB | Y | MAX | 30 |
| †P _{HL} | | | MAX | 33 |
| †P _{LH} | CLK | ENABLE | MAX | 30 |
| †P _{HL} | | | MAX | 33 |
| †P _{LH} | CLR | Y | MAX | 36 |
| †P _{HL} | | | MAX | 23 |
| †P _{LH} | RATE | Y | MAX | 23 |
| †P _{HL} | | | MAX | 23 |

 UNIT f_{max} : MHz, other : ns

Logic Diagram
SN74LS



Logic Diagram
CD74HC/HCT



FUNCTION TABLES
(SN74LS107A)

| INPUTS | | | | OUTPUTS | |
|--------|-----|---|---|----------------|-------------|
| CLR | CLK | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q ₀ | \bar{Q}_0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q ₀ | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{cc} | MAX | 20 | 6 | 0.04 | 0.08 | 0.08 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | 4 | mA |

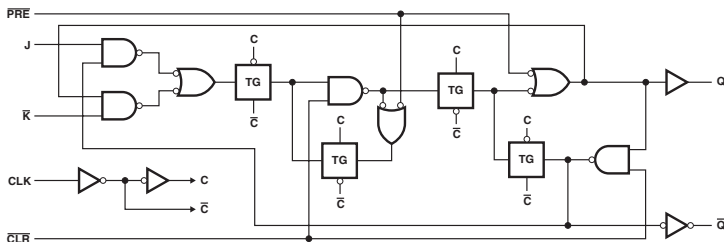
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|-----------------------------|-----------|------------|-----|----|---------|---------|----------|
| f _{max} | | | MIN | 15 | 30 | 25 | 20 | 19 |
| t _w | CLK H | | MIN | 20 | 20 | 20 | - | - |
| | CLK L | | MIN | 47 | - | 20 | - | - |
| | \bar{CP} | | MIN | - | - | - | 24 | 27 |
| | CLR L (or \bar{R}) | | MIN | 25 | 25 | 20 | 24 | 36 |
| t _{su} | J, K | | MIN | 0 | 20 | 25 | 30 | 30 |
| | CLR INACTIVE | | MIN | 0 | 25 | 25 | - | - |
| t _h | | | MIN | 0 | 0 | 0 | 3 | 5 |
| t _{PLH} | \bar{CLR} (or \bar{R}) | \bar{Q} | MAX | 25 | 20 | 39 | 47 | 57 |
| t _{PHL} | | Q | MAX | 40 | 20 | 39 | 47 | 57 |
| t _{PLH} | CLK | \bar{Q} | MAX | 25 | 20 | 32 | - | - |
| t _{PHL} | | Q | MAX | 40 | 20 | 32 | - | - |
| t _{PLH} | \bar{CP} | Q | MAX | - | - | - | 51 | 65 |
| t _{PHL} | | | MAX | - | - | - | 51 | 65 |
| t _{PLH} | \bar{CP} | \bar{Q} | MAX | - | - | - | 51 | 60 |
| t _{PHL} | | | MAX | - | - | - | 51 | 60 |

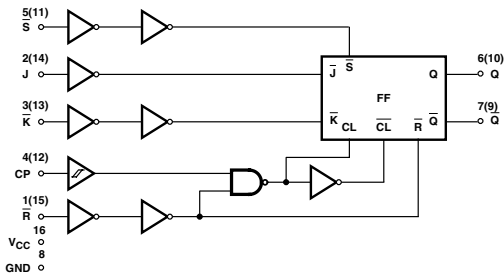
UNIT f_{max} : MHz, other : ns

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

Logic Diagram
SN74, CD74AC/ACT



Logic Diagram
CD74HC/HCT



FUNCTION TABLE
(SN74, CD74AC/ACT)

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-------|---|---|----------------|------------------------|
| PRE | CLR | CLOCK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | TOGGLE | |
| H | H | ↑ | L | H | Q ₀ | \bar{Q} ₀ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q ₀ | \bar{Q} ₀ |

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------|------------|------|------|------|----|----|---------|---------|----------|---------|----------|------|
| I_{CC} | MAX | 15 | 8 | 4 | 17 | 17 | 0.04 | 0.08 | 0.08 | 0.08 | 0.08 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | mA |
| I_{OL} | MAX | 16 | 4 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | mA |

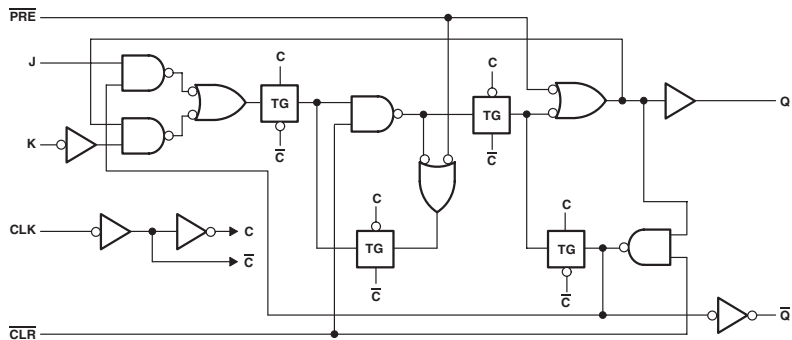
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|-----------|-------------------------|--------------|------------|-----|----|------|------|------|---------|---------|----------|
| fmax | | | MIN | 25 | 25 | 34 | 105 | 90 | 25 | 20 | 18 |
| tw | CLK H | | MIN | 20 | 25 | 14.5 | 4 | 4 | 20 | - | - |
| | CLK L | | MIN | 20 | - | 14.5 | 5.5 | 5 | 20 | - | - |
| | CP | | MIN | - | - | - | - | - | - | 24 | 27 |
| | PRE L | | MIN | 20 | 25 | 15 | 4 | 4 | 25 | - | - |
| | CLR L | | MIN | 20 | 25 | 15 | 4 | 4 | 25 | - | - |
| | R | | MIN | - | - | - | - | - | - | 24 | 27 |
| tsu | J, \bar{K} | | MIN | 10 | 25 | 15 | 5.5 | 3 | 25 | - | - |
| | PRE, CLR | | MIN | 10 | - | 10 | 2 | 2 | 6 | - | - |
| | J, K to CP | | MIN | - | - | - | - | - | - | 24 | 27 |
| th | | | MIN | 6 | 5 | 0 | 0 | 1 | 0 | 3 | 3 |
| TPHL | $\overline{\text{PRE}}$ | Q | MAX | 15 | 25 | 13 | 8 | 8 | 58 | - | - |
| | | \bar{Q} | MAX | 35 | 40 | 15 | 10.5 | 10.5 | 58 | - | - |
| TPHL | $\overline{\text{CLR}}$ | \bar{Q} | MAX | 15 | 25 | 13 | 8 | 8 | 58 | - | - |
| | | Q | MAX | 25 | 40 | 15 | 10.5 | 10.5 | 58 | - | - |
| TPHL | CLK | \bar{Q}, Q | MAX | 16 | 25 | 16 | 9 | 8 | 44 | - | - |
| | | | MAX | 28 | 40 | 18 | 9 | 9.2 | 44 | - | - |
| TPHL | $\overline{\text{CP}}$ | Q | MAX | - | - | - | - | - | - | 53 | 60 |
| | | | MAX | - | - | - | - | - | - | 53 | 60 |
| TPHL | $\overline{\text{CP}}$ | \bar{Q} | MAX | - | - | - | - | - | - | 53 | 60 |
| | | | MAX | - | - | - | - | - | - | 53 | 60 |
| TPHL | \bar{R} | Q | MAX | - | - | - | - | - | - | 56 | 68 |
| | | | MAX | - | - | - | - | - | - | 56 | 68 |
| TPHL | \bar{R} | \bar{Q} | MAX | - | - | - | - | - | - | 51 | 56 |
| | | | MAX | - | - | - | - | - | - | 51 | 56 |

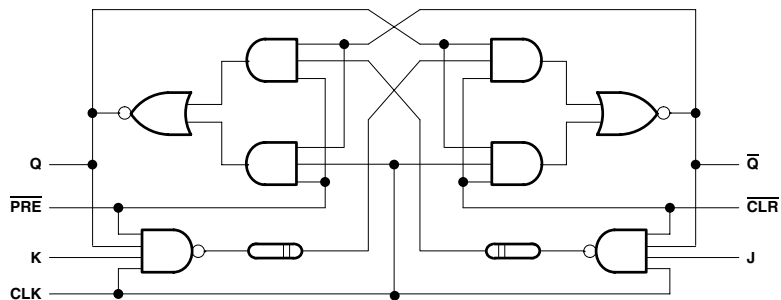
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 AC | CD74 ACT |
|-----------|-------------------------|--------------|------------|---------|----------|
| fmax | | | MIN | 100 | 100 |
| tw | CLK H | | MIN | 5 | 5 |
| | CLK L | | MIN | 5 | 5 |
| | CP | | MIN | - | - |
| | PRE L | | MIN | 4.5 | 5.5 |
| | CLR L | | MIN | 4.5 | 5.5 |
| | R | | MIN | - | - |
| tsu | J, \bar{K} | | MIN | 5.5 | 5.5 |
| | PRE, CLR | | MIN | - | 5.5 |
| | J, K to CP | | MIN | - | - |
| th | | | MIN | 0 | 0 |
| TPHL | $\overline{\text{PRE}}$ | Q | MAX | 12.2 | 12.2 |
| | | \bar{Q} | MAX | 12.2 | 12.2 |
| TPHL | $\overline{\text{CLR}}$ | \bar{Q} | MAX | 12.2 | 12.2 |
| | | Q | MAX | 12.2 | 12.2 |
| TPHL | CLK | \bar{Q}, Q | MAX | 10.3 | 10.3 |
| | | | MAX | 10.3 | 10.3 |
| TPHL | $\overline{\text{CP}}$ | Q | MAX | - | - |
| | | | MAX | - | - |
| TPHL | $\overline{\text{CP}}$ | \bar{Q} | MAX | - | - |
| | | | MAX | - | - |
| TPHL | \bar{R} | Q | MAX | - | - |
| | | | MAX | - | - |
| TPHL | \bar{R} | \bar{Q} | MAX | - | - |
| | | | MAX | - | - |

UNIT fmax : MHz, other : ns

Logic Diagram (SN74HC112)



Logic Diagram (SN74LVC112A)



FUNCTION TABLE (SN74)

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|------------------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | \bar{Q} ₀ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | \bar{Q} ₀ |

[†]The output levels in this configuration may not meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LVC 3V | UNIT |
|-----------------|------------|------|----|------|----|---------|---------|----------|---------|----------|--------|------|
| I _{CC} | MAX | 6 | 25 | 4.5 | 19 | 0.04 | 0.08 | 0.08 | 0.08 | 0.08 | 0.01 | mA |
| I _{OH} | MAX | -0.4 | -1 | -0.4 | -1 | -4 | -4 | -4 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 8 | 20 | 8 | 20 | 4 | 4 | 4 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

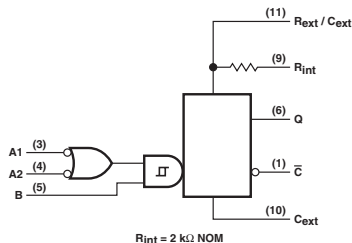
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LVC 3V |
|------------------|--|----------------|------------|----|-----|------|-----|---------|---------|----------|---------|----------|--------|
| f _{max} | | | MIN | 30 | 80 | 30 | 100 | 20 | 20 | 20 | 100 | 100 | 150 |
| t _w | PRE, CLR | | MIN | 25 | 8 | 10 | 5 | 25 | 24 | 27 | 4.5 | 4.5 | - |
| | CLK H | | MIN | 20 | 6 | 16.5 | 5 | 25 | - | - | 4.5 | 4.5 | 3.3 |
| | CLK L | | MIN | - | 6.5 | 16.5 | 5 | 25 | - | - | 4.5 | 4.5 | 3.3 |
| | CP | | MIN | - | - | - | - | - | 24 | 30 | - | - | - |
| t _{su} | DATA | | MIN | 20 | 7 | 22 | 5 | 25 | 24 | 24 | 4 | 4 | 2.3 |
| | PRE INACTIVE | | MIN | 25 | - | 20 | 5 | 25 | - | - | - | - | 1.1 |
| | CLR INACTIVE | | MIN | 20 | - | 20 | 5 | 25 | - | - | - | - | 1.1 |
| t _h | | | MIN | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 | 0 | 0.7 |
| t _{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \bar{Q} | MAX | 20 | 7 | 15 | 7.5 | 41 | - | - | 10.3 | 10.3 | 4.8 |
| t _{PHL} | | | MAX | 20 | 7 | 18 | 7.5 | 41 | - | - | 12.2 | 12.2 | 4.8 |
| t _{PLH} | CLK | Q or \bar{Q} | MAX | 20 | 7 | 15 | 7.5 | 31 | - | - | 10.3 | 10.3 | 5.9 |
| t _{PHL} | | | MAX | 20 | 7 | 19 | 7.5 | 31 | - | - | 12.2 | 12.2 | 5.9 |
| t _{PLH} | $\overline{\text{CP}}$ | Q or \bar{Q} | MAX | - | - | - | - | - | 53 | 53 | - | - | - |
| t _{PHL} | | | MAX | - | - | - | - | - | 53 | 53 | - | - | - |
| t _{PLH} | \bar{S} | Q or \bar{Q} | MAX | - | - | - | - | - | 47 | 48 | - | - | - |
| t _{PHL} | | | MAX | - | - | - | - | - | 47 | 48 | - | - | - |
| t _{PLH} | \bar{R} | Q or \bar{Q} | MAX | - | - | - | - | - | 54 | 56 | - | - | - |
| t _{PHL} | | | MAX | - | - | - | - | - | 54 | 56 | - | - | - |

UNIT f_{max}: MHz, other: ns

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Internal Timing Resistors ($2k\Omega$)
- Programmable Output Pulse Width with R_{ext}/C_{ext} : 40ns to 28s

Logic Diagram



- NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext} .
 2. To use the internal timing resistor, connect R_{int} to V_{CC} . For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------|----|---|----------------|----------------|
| A1 | A2 | B | Q | \bar{Q} |
| L | X | H | L | H |
| X | L | H | L [†] | H [†] |
| X | X | L | L [†] | H [†] |
| H | H | X | L [†] | H [†] |
| H | ↓ | H | | |
| ↓ | H | H | | |
| ↓ | ↓ | H | | |
| L | X | ↑ | | |
| X | L | ↑ | | |

See explanation of function table on page

[†] These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 40 | mA |
| I_{OH} | MAX | -0.4 | mA |
| I_{OL} | MAX | 16 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

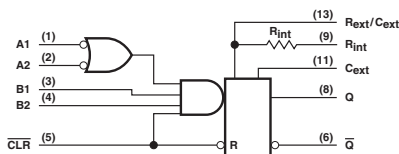
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|-------------|---|-----------|------------|-----|
| t_w (out) | Pulse width obtained with zero timing capacitance | | MIN | 50 |
| t_{PLH} | A | Q | MAX | 70 |
| t_{PHL} | B | | | 80 |
| t_{PLH} | A | \bar{Q} | MAX | 55 |
| t_{PHL} | B | | | 65 |

UNIT: NS

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle
- Internal Timing Resistors (5kΩ)

Logic Diagram



R_{int} is nominally 10 kΩ for '122 and 'LS122

FUNCTION TABLE

| CLEAR | INPUTS | | | | OUTPUTS | |
|-------|--------|----|---|----|---------|-----------|
| | A1 | A2 | B | B2 | Q | \bar{Q} |
| L | X | X | X | X | L | H |
| X | H | H | X | X | L† | H† |
| X | X | X | L | X | L† | H† |
| X | X | X | X | L | L† | H† |
| H | L | X | † | H | | |
| H | L | X | H | † | | |
| H | X | L | † | H | | |
| H | X | L | H | † | | |
| H | H | ↓ | H | H | | |
| H | ↓ | ↓ | H | H | | |
| H | ↓ | H | H | H | | |
| † | L | X | H | H | | |
| † | X | L | H | H | | |

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 66 | 11 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

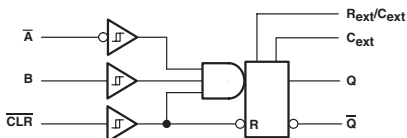
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|-------|-----------|------------|-----|----|
| t _w | | | MIN | 40 | 40 |
| t _{PLH} | A | Q | MAX | 33 | 33 |
| | B | | | 28 | 44 |
| t _{PHL} | A | \bar{Q} | MAX | 40 | 45 |
| | B | | | 36 | 56 |
| t _{PLH} | CLEAR | \bar{Q} | MAX | 27 | 27 |
| | | \bar{Q} | | 40 | 45 |

UNIT: NS

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUTS | |
|--------|---------------|---|----------------|----------------|
| CLEAR | \bar{A} (A) | B | Q | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L [†] | H [†] |
| X | X | L | L [†] | H [†] |
| H | L | ↑ | | |
| H | ↓ | H | | |
| ↑ | L | H | | |

See explanation of function table on page

[†] These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|---------|----------|------|-------|-------|-------|------|
| I_{CC} | MAX | 66 | 20 | 0.16 | 0.16 | 0.65 | 0.975 | 0.28 | 0.65 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -8 | -8 | -6 | -12 | mA |
| I_{OL} | MAX | 16 | 8 | 4 | 4 | 8 | 8 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

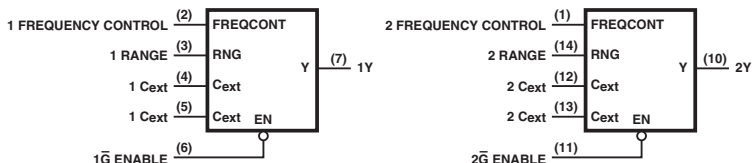
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT | AHC | AHCT | LV 3V | LV 5V |
|-----------|---------------|-----------|------------|-----|----|---------|----------|-----|------|-------|-------|
| t_W | | | MIN | 40 | 40 | 30 | 30 | 5 | 5 | 5 | 5 |
| t_{PLH} | \bar{A} (A) | Q | MAX | 33 | 33 | 90 | 90 | 16 | 12 | 27.5 | 16 |
| | B | | | 28 | 44 | 90 | 90 | 16 | 12 | 27.5 | 16 |
| t_{PHL} | \bar{A} (A) | \bar{Q} | MAX | 40 | 45 | 96 | 102 | 16 | 12 | 27.5 | 16 |
| | B | | | 36 | 56 | 96 | 102 | 16 | 12 | 27.5 | 16 |
| t_{PLH} | CLEAR (R) | Q | MAX | 40 | 45 | 65 | 72 | 13 | 14 | 22 | 13 |
| | | \bar{Q} | | 27 | 27 | 65 | 72 | 13 | 14 | 22 | 13 |

UNIT: NS

DUAL VOLTAGE-CONTROLLED OSCILLATORS

- Frequency Spectrum: 1Hz to 60MHz
- Typical f_{max} : 85MHz
- Typical Power Dissipation: 525mW

Block Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OP

| PARAMETER | MAX or MIN | S | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 150 | mA |
| I_{OH} | MAX | -1 | mA |
| I_{OL} | MAX | 20 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERIS

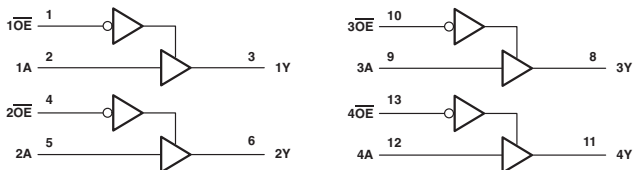
| PARAMETER | MAX or MIN | S |
|-----------|------------|----|
| f_o | MIN | 60 |

UNIT: NS

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)

FUNCTION TABLE
(SN74)
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | SN64 BCT | ABT | UNIT |
|-----------------|------------|------|------|-----|---------|---------|----------|----------|----------|----------|-----|------|
| I _{CC} | MAX | 54 | 20 | 40 | 0.08 | 0.16 | 0.08 | 0.16 | 49 | 49 | 30 | mA |
| I _{OH} | MAX | -5.2 | -2.6 | -15 | -6 | -6 | -6 | -6 | -15 | -15 | -32 | mA |
| I _{OL} | MAX | 16 | 24 | 64 | 6 | 6 | 6 | 6 | 64 | 64 | 60 | mA |

| PARAMETER | MAX or MIN | LVT 3V | LVTH 3V | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|--------|---------|------|------|-------|-------|-------|--------|---------|----------|----------|------|
| I _{CC} | MAX | 7 | 7 | 0.04 | 0.02 | 0.02 | 0.02 | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -32 | -8 | -8 | -8 | -16 | -16 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 64 | 64 | 8 | 8 | 8 | 16 | 16 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | SN64 BCT | ABT |
|------------------|-----------|--------|------------|-----|----|-----|---------|---------|----------|----------|----------|----------|-----|
| t _{PLH} | A | Y | MAX | 13 | 15 | 6.5 | 30 | 30 | 33 | 38 | 5.7 | 6 | 4.9 |
| t _{PHL} | | | MAX | 18 | 18 | 8 | 30 | 30 | 33 | 38 | 7.7 | 8 | 4.9 |
| t _{PZH} | \bar{G} | Y | MAX | 17 | 20 | 8.5 | 30 | 38 | 35 | 38 | 10.3 | 11.1 | 5.9 |
| t _{PZL} | | | MAX | 25 | 25 | 9 | 30 | 38 | 35 | 38 | 11.7 | 12.8 | 6.8 |
| t _{PHZ} | | | MAX | 8 | 20 | 6 | 30 | 38 | 33 | 42 | 8.9 | 9.4 | 6.2 |
| t _{PLZ} | | | MAX | 12 | 20 | 6 | 30 | 38 | 33 | 42 | 8.6 | 9.9 | 6.2 |

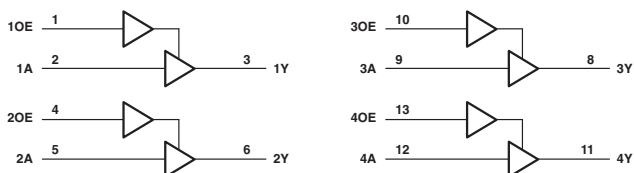
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVT 3V | LVTH 3V | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|-----------|--------|------------|--------|---------|-----|------|-------|-------|-------|--------|---------|----------|----------|
| t _{PLH} | A | Y | MAX | 4.0 | 3.5 | 8.5 | 8.5 | 13 | 8.5 | 10.5 | 4.8 | 2.8 | 2.6 | 2.1 |
| t _{PHL} | | | MAX | 3.9 | 3.9 | 8.5 | 8.5 | 13 | 8.5 | 10.5 | 4.8 | 2.8 | 2.6 | 2.1 |
| t _{PZH} | \bar{G} | Y | MAX | 4.7 | 4 | 8 | 8 | 13 | 8 | 9.5 | 5.4 | 3.5 | 2.8 | 2.3 |
| t _{PZL} | | | MAX | 4.7 | 4 | 8 | 8 | 13 | 8 | 9.5 | 5.4 | 3.5 | 2.8 | 2.3 |
| t _{PHZ} | | | MAX | 5.1 | 4.5 | 10 | 10 | 15 | 10 | 9 | 4.6 | 4 | 3.4 | 2.3 |
| t _{PLZ} | | | MAX | 4.5 | 4.5 | 10 | 10 | 15 | 10 | 9 | 4.6 | 4 | 3.4 | 2.3 |

UNIT: NS

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)


FUNCTION TABLE
(SN74)
 (each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 BCT | SN64 BCT | ABT | UNIT |
|-----------------|------------|------|------|-----|---------|---------|----------|----------|----------|-----|------|
| I _{CC} | MAX | 62 | 22 | 48 | 0.08 | 0.16 | 0.16 | 51 | 51 | 30 | mA |
| I _{OH} | MAX | -5.2 | -2.6 | -15 | -6 | -6 | -6 | -15 | -15 | -32 | mA |
| I _{OL} | MAX | 16 | 24 | 64 | 6 | 6 | 6 | 64 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | LVTH 3V | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|---------|------|------|-------|-------|--------|---------|----------|----------|------|
| I _{CC} | MAX | 7 | 0.04 | 0.02 | 0.02 | 0.02 | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -32 | -8 | -8 | -8 | -16 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 64 | 8 | 8 | 8 | 16 | 24 | 24 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 BCT | SN64 BCT | ABT |
|------------------|-------|--------|------------|-----|----|-----|---------|---------|----------|----------|----------|-----|
| t _{PLH} | A | Y | MAX | 13 | 15 | 7 | 30 | 30 | 36 | 6.3 | 6.3 | 6.3 |
| t _{PHL} | | | MAX | 18 | 18 | 8.5 | 30 | 30 | 36 | 7.4 | 7.4 | 5.7 |
| t _{PZH} | G | Y | MAX | 18 | 25 | 8.5 | 30 | 38 | 38 | 7.9 | 7.9 | 6.5 |
| t _{PZL} | | | MAX | 25 | 35 | 8.5 | 30 | 38 | 38 | 10.5 | 10.5 | 6.5 |
| t _{PHZ} | | | MAX | 16 | 25 | 7.5 | 30 | 38 | 42 | 10 | 10 | 6.8 |
| t _{PLZ} | | | MAX | 18 | 25 | 8 | 30 | 38 | 42 | 12.3 | 12.3 | 6.7 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|-------|--------|------------|---------|-----|------|-------|-------|--------|---------|----------|----------|
| t _{PLH} | A | Y | MAX | 3.8 | 8.5 | 8.5 | 13 | 8.5 | 4.7 | 3.1 | 2.6 | 2.1 |
| t _{PHL} | | | MAX | 3.9 | 8.5 | 8.5 | 13 | 8.5 | 4.7 | 3.1 | 2.6 | 2.1 |
| t _{PZH} | G | Y | MAX | 5.4 | 8 | 8 | 13 | 8 | 5.7 | 3.3 | 2.7 | 2.2 |
| t _{PZL} | | | MAX | 5.2 | 8 | 8 | 13 | 8 | 5.7 | 3.3 | 2.7 | 2.2 |
| t _{PHZ} | | | MAX | 3.8 | 10 | 10 | 15 | 10 | 6 | 3.7 | 3.3 | 2.2 |
| t _{PLZ} | | | MAX | 5.5 | 10 | 10 | 15 | 10 | 6 | 3.7 | 3.3 | 2.2 |

UNIT: ns

50-Ω LINE DRIVERS

$$\bullet Y = \overline{A + B}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|-------|------|
| I_{CC} | MAX | 57 | mA |
| I_{OH} | MAX | -42.4 | mA |
| I_{OL} | MAX | 48 | mA |

SWITCHING CHARACTERISTICS

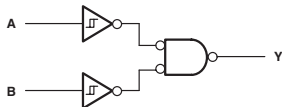
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|-----------|-------|--------|------------|-----|
| t_{PLH} | A, B | Y | MAX | 9 |
| t_{PHL} | A, B | Y | MAX | 12 |

UNIT: ns

QUADRUPLE POSITIVE-NAND GATES
WITH SCHMITT TRIGGER INPUTS

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | SN74 HC | CD74 HC | CD74 HCT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|----|------------|------------|-------------|------|------|----------|----------|------|
| I_{CC} | MAX | 40 | 14 | 68 | 0.02 | 0.04 | 0.04 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -1 | -4 | -4 | -4 | -8 | -8 | -6 | -12 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 4 | 4 | 4 | 8 | 8 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | SN74 HC | CD74 HC | CD74 HCT | AHC | AHCT |
|-----------|-------|--------|------------|-----|----|------|------------|------------|-------------|-----|------|
| t_{PLH} | A, B | Y | MAX | 22 | 22 | 10.5 | 31 | 38 | 50 | 11 | 10 |
| t_{PHL} | A, B | Y | MAX | 22 | 22 | 13 | 31 | 38 | 50 | 11 | 8 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V |
|-----------|-------|--------|------------|----------|----------|
| t_{PLH} | A, B | Y | MAX | 17.5 | 11 |
| t_{PHL} | A, B | Y | MAX | 17.5 | 11 |

UNIT: ns

13-INPUT POSITIVE-NAND GATES

$$\bullet Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

FUNCTION TABLE

| INPUTS A-H | OUTPUT Y |
|----------------------|-------------|
| All inputs H | L |
| One or more inputs L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION

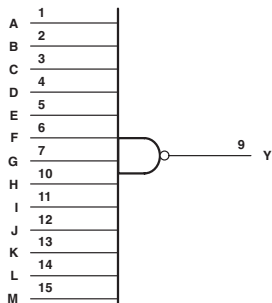
| PARAMETER | MAX or MIN | S | ALS | SN74 HC | UNIT |
|-----------------|------------|----|------|------------|------|
| I _{CC} | MAX | 10 | 0.34 | 0.02 | mA |
| I _{OH} | MAX | -1 | -0.4 | -4 | mA |
| I _{OL} | MAX | 20 | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | S | ALS | SN74 HC |
|------------------|--------|--------|------------|---|-----|------------|
| t _{PLH} | A to M | Y | MAX | 6 | 11 | 38 |
| t _{PHL} | A to M | Y | MAX | 7 | 25 | 38 |

UNIT: ns

Logic Diagram



136

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES
WITH OPEN COLLECTOR OUTPUTS

$$\bullet Y = A \oplus B = \overline{A}B + A\overline{B}$$

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

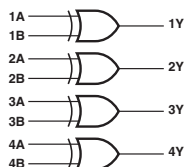
| PARAMETER | MAX or MIN | TTL | LS | ALS | AS | UNIT |
|-----------------|------------|-----|-----|-----|-----|------|
| I _{CC} | MAX | 50 | 10 | 5.9 | 31 | mA |
| V _{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I _{OL} | MAX | 16 | 8 | 8 | 20 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | AS |
|------------------|--------|----------------------|------------|-----|----|-----|------|
| t _{PLH} | A or B | Y (Other Output = L) | MAX | 18 | 30 | 50 | 12.5 |
| t _{PHL} | A or B | Y (Other Output = L) | MAX | 50 | 30 | 15 | 7.1 |
| t _{PLH} | A or B | Y (Other Output = L) | MAX | 22 | 30 | 50 | 11.4 |
| t _{PHL} | A or B | Y (Other Output = L) | MAX | 55 | 30 | 15 | 10.7 |

UNIT: ns

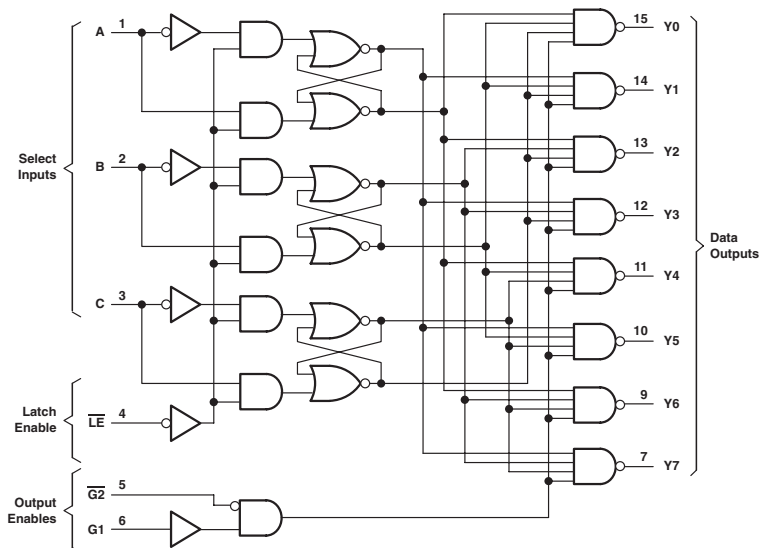
Logic Diagram



3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

- Incorporates Two Output Enables To Simplify Cascading

Logic Diagram (SN74ALS)



FUNCTION TABLE (SN74)

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|----|----|--------|---|---|--|----|----|----|----|----|----|----|
| ENABLE | | | SELECT | | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| LE | G1 | G2 | C | B | A | | | | | | | | |
| X | X | H | X | X | X | H | H | H | H | H | H | H | |
| X | L | X | X | X | X | H | H | H | H | H | H | H | |
| L | H | L | L | L | L | L | H | H | H | H | H | H | |
| L | H | L | L | L | H | H | L | H | H | H | H | H | |
| L | H | L | L | H | L | H | H | L | H | H | H | H | |
| L | H | L | L | H | H | H | H | L | H | H | H | H | |
| L | H | L | H | L | L | H | H | H | H | L | H | H | |
| L | H | L | H | L | H | H | H | H | H | L | H | H | |
| L | H | L | H | H | H | H | H | H | H | H | L | H | |
| L | H | L | H | H | H | H | H | H | H | H | H | L | |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | LVC 3V | UNIT |
|-----------------|------------|------|------|----|---------|---------|----------|----------|--------|------|
| I _{cc} | MAX | 18 | 11 | 24 | 0.08 | 0.16 | 0.08 | 0.16 | 0.01 | mA |
| I _{oh} | MAX | -0.4 | -0.4 | -2 | -4 | -4 | -4 | -4 | -24 | mA |
| I _{ol} | MAX | 8 | 8 | 20 | 4 | 4 | 4 | 4 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | LVC 3V |
|------------------|-----------------------|----------------------|------------|----|-----|------|---------|---------|----------|----------|--------|
| t _{PLH} | SELECT | Y (CD74: \bar{Y}) | MAX | 24 | 20 | 12.5 | 48 | 54 | 48 | 57 | - |
| t _{PHL} | | | MAX | 38 | 20 | 12.5 | 48 | 54 | 48 | 57 | - |
| t _{PLH} | $\bar{G2}$ | Y (CD74: \bar{Y}) | MAX | 21 | 12 | 8 | 36 | 44 | 36 | 56 | - |
| t _{PHL} | | | MAX | 27 | 15 | 8.5 | 36 | 44 | 36 | 56 | - |
| t _{PLH} | G1 | Y (CD74: \bar{Y}) | MAX | 21 | 17 | 10 | 36 | 44 | 36 | 53 | - |
| t _{PHL} | | | MAX | 27 | 15 | 9 | 36 | 44 | 36 | 53 | - |
| t _{PLH} | \bar{LE} (CD74: LE) | Y (CD74: \bar{Y}) | MAX | 27 | 22 | 13.5 | 48 | 57 | 52 | 66 | - |
| t _{PHL} | | | MAX | 38 | 20 | 14 | 48 | 57 | 52 | 66 | - |

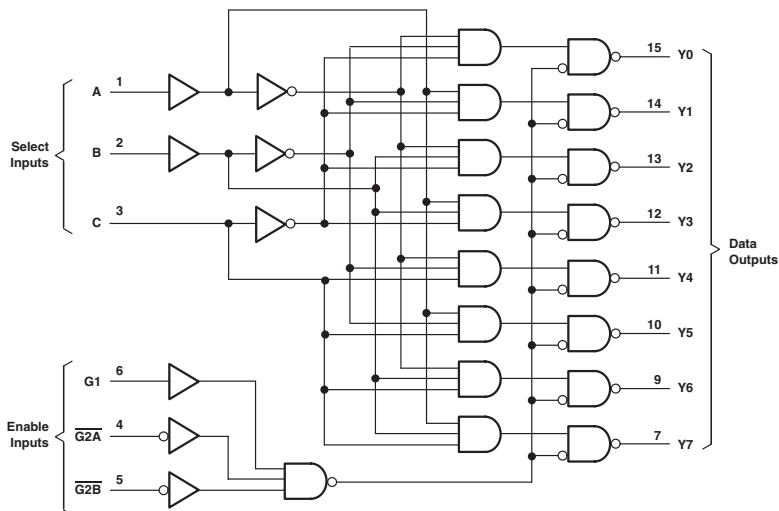
UNIT:ns

LVC:Preview

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXRS

- 3 Enable Inputs to Simplify Cascading and /or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



FUNCTION TABLE (SN74)

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---------------|-----|-----|---------------|---|---|---------|----|----|----|----|----|----|----|
| G1 | G2A | G2B | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | H | H | H | H | H | L | H | H | H |
| H | L | L | H | H | L | H | H | H | H | H | L | H | H |
| H | L | L | H | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | UNIT |
|-----------------|------------|------|----|------|----|----|---------|---------|----------|----------|------|
| I _{CC} | MAX | 10 | 74 | 10 | 20 | 20 | 0.08 | 0.16 | 0.08 | 0.16 | mA |
| I _{OH} | MAX | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 4 | mA |

| PARAMETER | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | UNIT |
|-----------------|------------|-------|---------|--------|----------|------|------|-------|-------|-------|--------|------|
| I _{CC} | MAX | 0.04 | 0.16 | 0.04 | 0.16 | 0.04 | 0.04 | 0.02 | 0.02 | 0.01 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -24 | -8 | -8 | -6 | -12 | -8 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 24 | 8 | 8 | 6 | 12 | 8 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|------------------|---------|------------|------------|----|----|-----|-----|-----|---------|---------|----------|----------|
| t _{PLH} | A, B, C | Y (CD74:Y) | MAX | 27 | 12 | 22 | 10 | 8.5 | 45 | 45 | 45 | 53 |
| t _{PHL} | | | MAX | 39 | 12 | 18 | 9.5 | 9 | 45 | 45 | 45 | 53 |
| t _{PLH} | G2 | Y (CD74:Y) | MAX | 26 | 11 | 17 | 7.5 | 8 | 39 | 53 | 42 | 53 |
| t _{PHL} | | | MAX | 38 | 11 | 17 | 8.5 | 7.5 | 39 | 53 | 42 | 53 |
| t _{PLH} | G1 | Y (CD74:Y) | MAX | 26 | 11 | 17 | 10 | 9 | 39 | 53 | 42 | 53 |
| t _{PHL} | | | MAX | 38 | 11 | 17 | 10 | 8.5 | 39 | 53 | 42 | 53 |

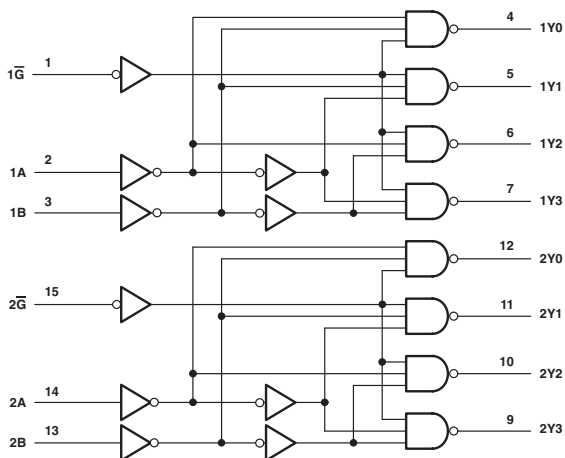
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V |
|------------------|---------|------------|------------|-------|---------|--------|----------|------|------|-------|-------|-------|--------|
| t _{PLH} | A, B, C | Y (CD74:Y) | MAX | 8.1 | 11 | 9.8 | 12 | 11.5 | 13 | 18 | 11.5 | 14 | 6.7 |
| t _{PHL} | | | MAX | 8.8 | 11 | 9.7 | 12 | 11.5 | 13 | 18 | 11.5 | 14 | 6.7 |
| t _{PLH} | G2 | Y (CD74:Y) | MAX | 8.3 | 10 | 8.9 | 10.5 | 11.5 | 12 | 17 | 11.5 | 13 | 6.5 |
| t _{PHL} | | | MAX | 8.3 | 10 | 8.9 | 10.5 | 11.5 | 12 | 17 | 11.5 | 13 | 6.5 |
| t _{PLH} | G1 | Y (CD74:Y) | MAX | 7.5 | 11 | 9.3 | 11 | 11.5 | 11.5 | 18.5 | 11.5 | 12 | 5.8 |
| t _{PHL} | | | MAX | 7.7 | 11 | 9.8 | 11 | 11.5 | 11.5 | 18.5 | 11.5 | 12 | 5.8 |

UNIT: ns

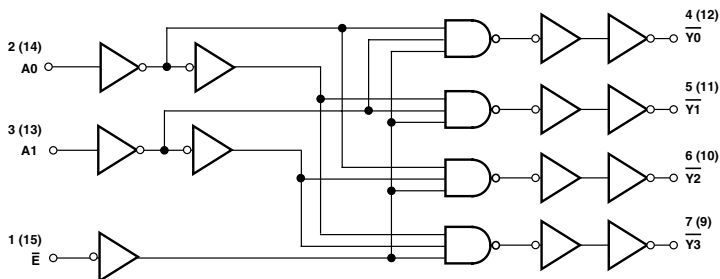
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Incorporate Two Enable Inputs to Simplify Cascading and /or Data Reception
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



Logic Diagram (CD74HC/HCT)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUTS | | | |
|----------------|--------|---|---------|----|----|----|
| ENABLE | SELECT | | Y0 | Y1 | Y2 | Y3 |
| \overline{G} | B | A | | | | |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | CD74 AC | ACT 11 | UNIT |
|-----------------|------------|------|----|------|---------|---------|----------|----------|---------|--------|------|
| I _{CC} | MAX | 11 | 90 | 13 | 0.08 | 0.16 | 0.08 | 0.16 | 0.16 | 0.08 | mA |
| I _{OH} | MAX | -0.4 | -1 | -0.4 | -4 | -4 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 8 | 20 | 8 | 4 | 4 | 4 | 4 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | UNIT |
|-----------------|------------|----------|------|------|-------|-------|--------|------|
| I _{CC} | MAX | 0.16 | 0.04 | 0.02 | - | 0.02 | 0.01 | mA |
| I _{OH} | MAX | -24 | -8 | -8 | -6 | -12 | -24 | mA |
| I _{OL} | MAX | 24 | 8 | 8 | 6 | 12 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | CD74 AC | ACT 11 |
|------------------|--------------------------|---------------------------|------------|----|----|-----|---------|---------|----------|----------|---------|--------|
| t _{PLH} | SELECT | Y (CD74: \overline{Y}) | MAX | 29 | 12 | 14 | 44 | 44 | 43 | 51 | 10.5 | 8.5 |
| t _{PHL} | SELECT | Y (CD74: Y) | MAX | 38 | 12 | 14 | 44 | 44 | 43 | 51 | 10.5 | 8.5 |
| t _{PLH} | \overline{G} (CD74: E) | Y (CD74: Y) | MAX | 24 | 8 | 14 | 44 | 41 | 43 | 51 | 10.5 | 7.9 |
| t _{PHL} | \overline{G} (CD74: E) | Y (CD74: Y) | MAX | 32 | 10 | 15 | 44 | 41 | 43 | 51 | 10.5 | 7.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V |
|------------------|--------------------------|---------------------------|------------|----------|------|------|-------|-------|--------|
| t _{PLH} | SELECT | Y (CD74: \overline{Y}) | MAX | 11.5 | 10.5 | 10.5 | 16.5 | 10.5 | 6.2 |
| t _{PHL} | SELECT | Y (CD74: Y) | MAX | 11.5 | 10.5 | 10.5 | 16.5 | 10.5 | 6.2 |
| t _{PLH} | \overline{G} (CD74: E) | Y (CD74: Y) | MAX | 12 | 9.5 | 9.5 | 14.5 | 9.5 | 4.7 |
| t _{PHL} | \overline{G} (CD74: E) | Y (CD74: Y) | MAX | 12 | 9.5 | 9.5 | 14.5 | 9.5 | 4.7 |

UNIT: ns

DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

$$\bullet Y = \overline{ABCD}$$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

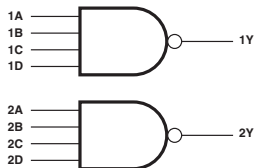
| PARAMETER | MAX or MIN | S | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 44 | mA |
| I_{OH} | MAX | -40 | mA |
| I_{OL} | MAX | 60 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | S |
|-----------|------------|--------|------------|-----|
| t_{PLH} | A, B, C, D | Y | MAX | 6.5 |
| t_{PHL} | | | MAX | 6.5 |

UNIT: ns

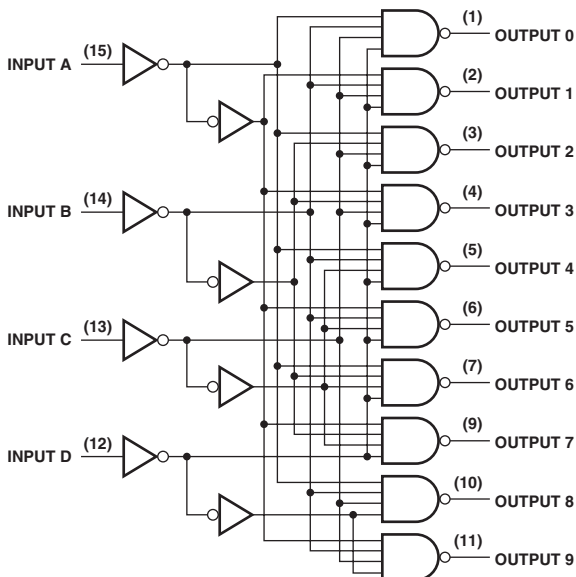
Logic Diagram



BCD-TO-DECIMAL DECODERS/DRIVERS

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

Logic Diagram



FUNCTION TABLE

| No. | INPUTS | | | | OUTPUTS | | | | | | | | | | |
|---------|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERAT

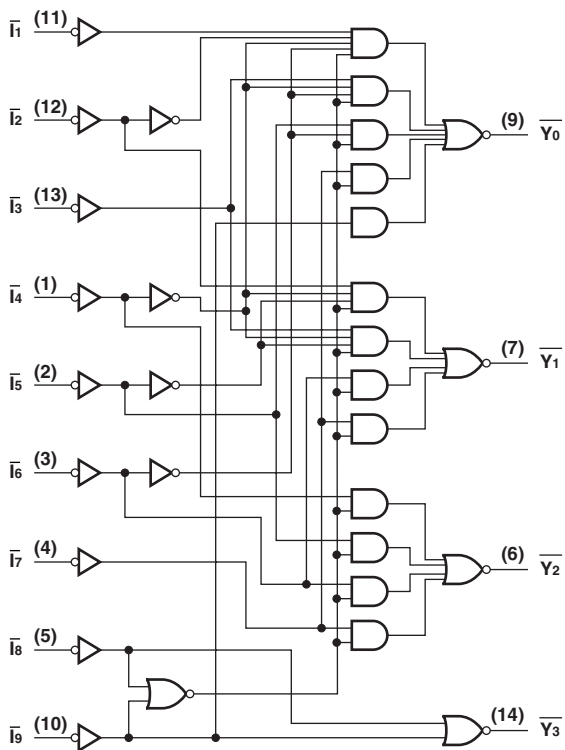
| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-------------|------------|-----|----|------|
| I_{CC} | MAX | 70 | 13 | mA |
| V_o (OFF) | MAX | 15 | 15 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | MAX or MIN | TTL | LS |
|-----------|------------|-----|----|
| t_{PLH} | MAX | 50 | 50 |
| t_{PHL} | MAX | 50 | 50 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| I ₁ | I ₂ | I ₃ | I ₄ | I ₅ | I ₆ | I ₇ | I ₈ | I ₉ | V ₀ | V ₁ | V ₂ | V ₃ |
| H | H | H | H | H | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | X | X | L | L | H | H | L |
| X | X | X | X | X | X | X | L | H | L | H | H | H |
| X | X | X | X | X | L | H | H | H | L | L | L | L |
| X | X | X | X | L | H | H | H | H | H | L | L | H |
| X | X | X | L | H | H | H | H | H | H | L | H | H |
| X | X | L | H | H | H | H | H | H | H | L | L | L |
| X | L | H | H | H | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

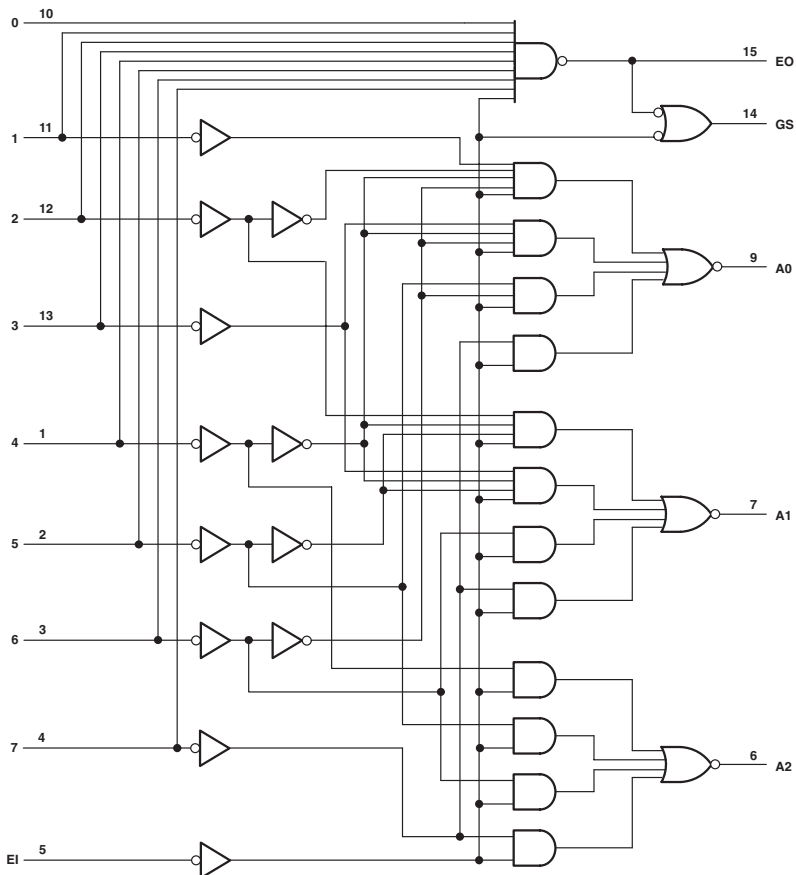
| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 70 | 20 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|------------|-----|----|---------|---------|----------|
| t _{PLH} | MAX | 19 | 33 | 48 | 48 | 53 |
| t _{PHL} | MAX | 19 | 23 | 48 | 48 | 53 |

UNIT:ns

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| EI | INPUTS | | | | | | | OUTPUTS | | | | | |
|----|--------|---|---|---|---|---|---|---------|----|----|----|----|----|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | EO |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | L | H | L | L | L | H | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | L | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | L | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | UNIT |
|-----------------|------------|------|------|---------|------|
| I _{CC} | MAX | 60 | 20 | 0.08 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | mA |

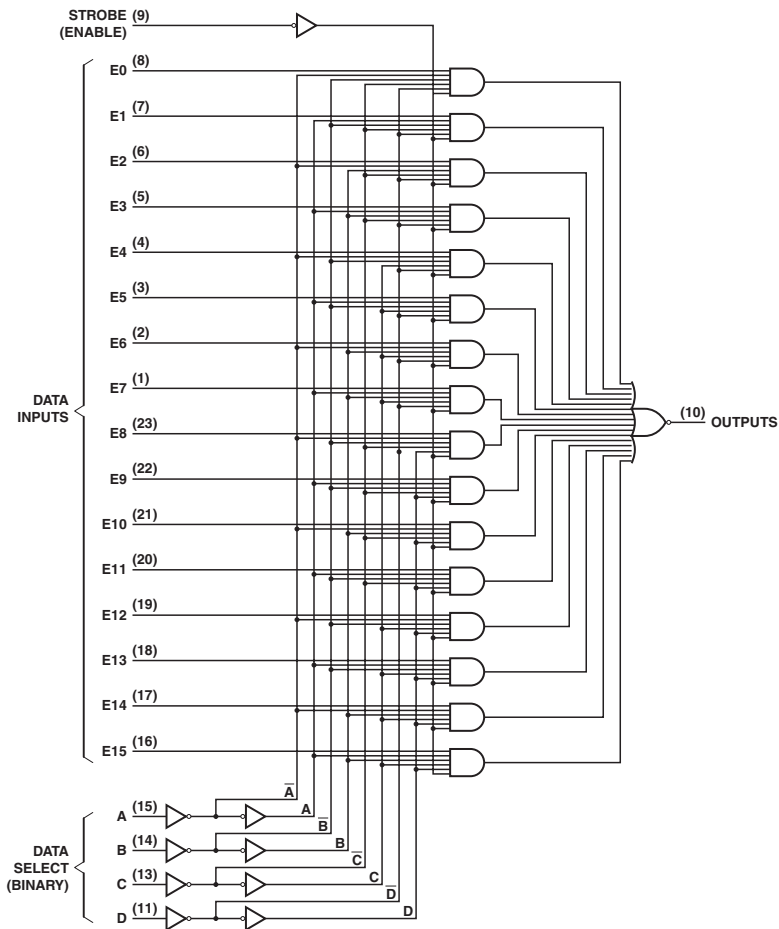
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | WAVEFORM | MAX or MIN | TTL | LS | SN74 HC |
|------------------|--------|--------------|---------------------|------------|-----|----|---------|
| t _{PLH} | 1 to 7 | A0, A1 or A2 | In-phase output | MAX | 15 | 18 | 45 |
| | | | | | 14 | 25 | 45 |
| t _{PHL} | 1 to 7 | A0, A1 or A2 | Out-of-phase output | MAX | 19 | 36 | 45 |
| | | | | | 19 | 29 | 45 |
| t _{PLH} | 0 to 7 | E0 | Out-of-phase output | MAX | 10 | 18 | 38 |
| | | | | | 25 | 40 | 38 |
| t _{PHL} | 0 to 7 | GS | In-phase output | MAX | 30 | 55 | 48 |
| | | | | | 25 | 21 | 48 |
| t _{PLH} | EI | A0, A1 or A2 | In-phase output | MAX | 15 | 25 | 49 |
| | | | | | 15 | 25 | 49 |
| t _{PHL} | EI | GS | In-phase output | MAX | 12 | 17 | 36 |
| | | | | | 15 | 36 | 36 |
| t _{PLH} | EI | E0 | In-phase output | MAX | 15 | 21 | 41 |
| | | | | | 30 | 35 | 41 |

UNIT: ns

16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | STROBE \bar{G} | OUTPUT W |
|--------|---|---|---|---|---------------------|-------------|
| SELECT | | | | | | |
| D | C | B | A | | | |
| X | X | X | X | H | H | |
| L | L | L | L | L | E0 | |
| L | L | L | H | L | E1 | |
| L | L | H | L | L | E2 | |
| L | L | H | H | L | E3 | |
| L | H | L | L | L | E4 | |
| L | H | L | H | L | E5 | |
| L | H | H | L | L | E6 | |
| L | H | H | H | L | E7 | |
| H | L | L | L | L | E8 | |
| H | L | L | H | L | E9 | |
| H | L | H | L | L | E10 | |
| H | L | H | H | L | E11 | |
| H | H | L | L | L | E12 | |
| H | H | L | H | L | E13 | |
| H | H | H | L | L | E14 | |
| H | H | H | H | L | E15 | |

NOTES:

H = High Level, L = Low Level, X = irrelevant

E0, E1 ... E15 = the complement of the level of the respective E input

D0, D1 ... D7 = the level of the D respective input

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------------|------------|------|------|
| I _{cc} | MAX | 48 | mA |
| I _{oh} | MAX | -0.8 | mA |
| I _{ol} | MAX | 16 | mA |

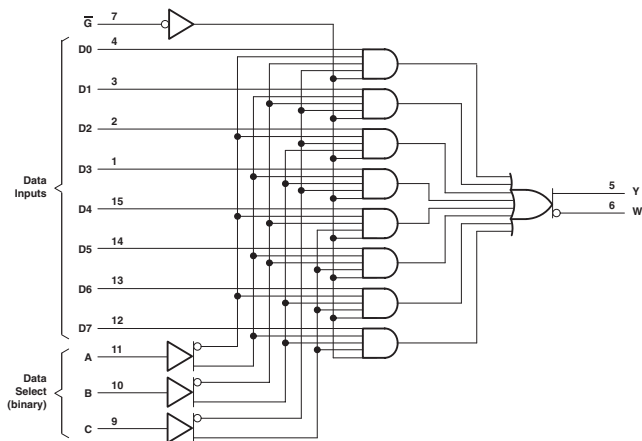
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|------------------|---------------------------|--------|------------|-----|
| t _{PLH} | A, B, C or D | W | MAX | 35 |
| | | | | 33 |
| t _{PHL} | Strobe \bar{G} | W | MAX | 24 |
| | | | | 30 |
| t _{PLH} | E0 thru E15 or E0 thru D7 | W | MAX | 14 |
| | | | | 20 |

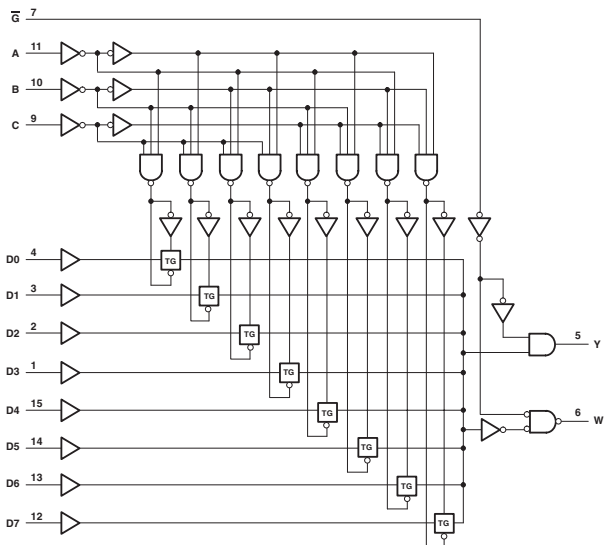
UNIT:ns

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74ALS, AS, F, CD74AC/ACT)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | | |
|--------|---|---|-----------|---------|------------|--|
| SELECT | | | | Y | W | |
| C | B | A | \bar{G} | | | |
| X | X | X | H | L | H | |
| L | L | L | L | D0 | $\bar{D0}$ | |
| L | L | H | L | D1 | $\bar{D1}$ | |
| L | H | L | L | D2 | $\bar{D2}$ | |
| L | H | H | L | D3 | $\bar{D3}$ | |
| H | L | L | L | D4 | $\bar{D4}$ | |
| H | L | H | L | D5 | $\bar{D5}$ | |
| H | H | L | L | D6 | $\bar{D6}$ | |
| H | H | H | L | D7 | $\bar{D7}$ | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------|------|------|----|------|-----|----|---------|---------|----------|---------|----------|------|
| I _{CC} | MAX | 48 | 10 | 70 | 12 | 30 | 21 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -2.6 | -15 | -1 | -6 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 24 | 48 | 24 | 6 | 4 | 4 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

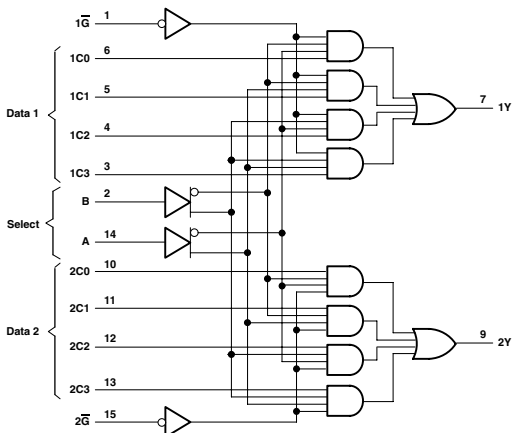
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------------------------|------------------------|------------|-----|----|------|-----|------|------|---------|---------|----------|
| t _{PLH} | A, B or C | Y | MAX | 38 | 43 | 18 | 18 | 14.5 | 12 | 63 | 56 | 62 |
| t _{PHL} | (CD74HC/HCT: Sn) | | | 38 | 30 | 18 | 24 | 15 | 9 | 63 | 56 | 62 |
| t _{PLH} | A, B or C | W (CD74HC: \bar{Y}) | MAX | 26 | 23 | 15 | 24 | 12 | 9.5 | 63 | 62 | 65 |
| t _{PHL} | (CD74HC/HCT: Sn) | | | 30 | 32 | 13.5 | 23 | 12 | 7.5 | 63 | 62 | 65 |
| t _{PLH} | D0 to D7 | Y | MAX | 20 | 32 | 16.5 | 10 | 10.5 | 7.5 | 49 | 51 | 57 |
| t _{PHL} | (CD74HC/HCT: In) | | | 27 | 26 | 18 | 15 | 11 | 7.5 | 49 | 51 | 57 |
| t _{PLH} | D0 to D7 | W (CD74HC: \bar{Y}) | MAX | 14 | 21 | 13 | 15 | 6.5 | 7 | 49 | 56 | 54 |
| t _{PHL} | (CD74HC/HCT: In) | | | 14 | 20 | 12 | 15 | 4.5 | 5 | 49 | 56 | 54 |
| t _{PLH} | \bar{G} | Y | MAX | 33 | 42 | 12 | 18 | 14 | 10.5 | 32 | 42 | 44 |
| t _{PHL} | (CD74HC/HCT: \bar{E}) | | | 33 | 32 | 12 | 19 | 11 | 7.5 | 32 | 42 | 44 |
| t _{PLH} | \bar{G} | W (CD74HC: \bar{Y}) | MAX | 21 | 24 | 7 | 19 | 6 | 7 | 32 | 44 | 54 |
| t _{PHL} | (CD74HC/HCT: \bar{E}) | | | 23 | 30 | 7 | 23 | 10 | 6 | 32 | 44 | 54 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 AC | CD74 ACT |
|------------------|--------------------------|------------------------|------------|---------|----------|
| t _{PLH} | A, B or C | Y | MAX | 18.2 | 20.2 |
| t _{PHL} | (CD74HC/HCT: Sn) | | | 18.2 | 20.2 |
| t _{PLH} | A, B or C | W (CD74HC: \bar{Y}) | MAX | 19.6 | 21.6 |
| t _{PHL} | (CD74HC/HCT: Sn) | | | 19.6 | 21.6 |
| t _{PLH} | D0 to D7 | Y | MAX | 13.5 | 15.5 |
| t _{PHL} | (CD74HC/HCT: In) | | | 13.5 | 15.5 |
| t _{PLH} | D0 to D7 | W (CD74HC: \bar{Y}) | MAX | 14.9 | 16.9 |
| t _{PHL} | (CD74HC/HCT: In) | | | 14.9 | 16.9 |
| t _{PLH} | \bar{G} | Y | MAX | 12.2 | 12.1 |
| t _{PHL} | (CD74HC/HCT: \bar{E}) | | | 12.2 | 12.1 |
| t _{PLH} | \bar{G} | W (CD74HC: \bar{Y}) | MAX | 13.5 | 13.5 |
| t _{PHL} | (CD74HC/HCT: \bar{E}) | | | 13.5 | 13.5 |

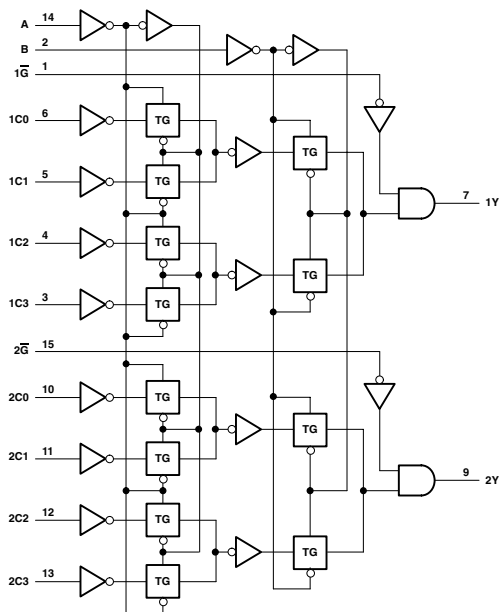
UNIT: ns

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74ALS, AS, F, LS)



Logic Diagram (SN74HC, HCT, CD74AC, ACT)



FUNCTION TABLE (SN74)

| SELECT INPUTS | | DATA INPUTS | | | STROBE | | OUTPUTS | |
|---------------|---|-------------|----|----|--------|---|---------|--|
| B | A | C0 | C1 | C2 | C3 | G | Y | |
| X | X | X | X | X | X | H | L | |
| L | L | L | X | X | X | L | L | |
| L | L | H | X | X | X | L | H | |
| L | H | X | L | X | X | L | L | |
| L | H | X | H | X | X | L | H | |
| H | L | X | X | L | X | L | L | |
| H | L | X | X | H | X | L | H | |
| H | H | X | X | X | L | L | L | |
| H | H | X | X | X | H | L | H | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------|------|------|----|------|-----|----|---------|---------|----------|---------|----------|------|
| I _{cc} | MAX | 60 | 10 | 70 | 14 | 33 | 20 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -2.6 | -15 | -1 | -6 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 24 | 48 | 20 | 6 | 4 | 4 | 24 | 24 | mA |

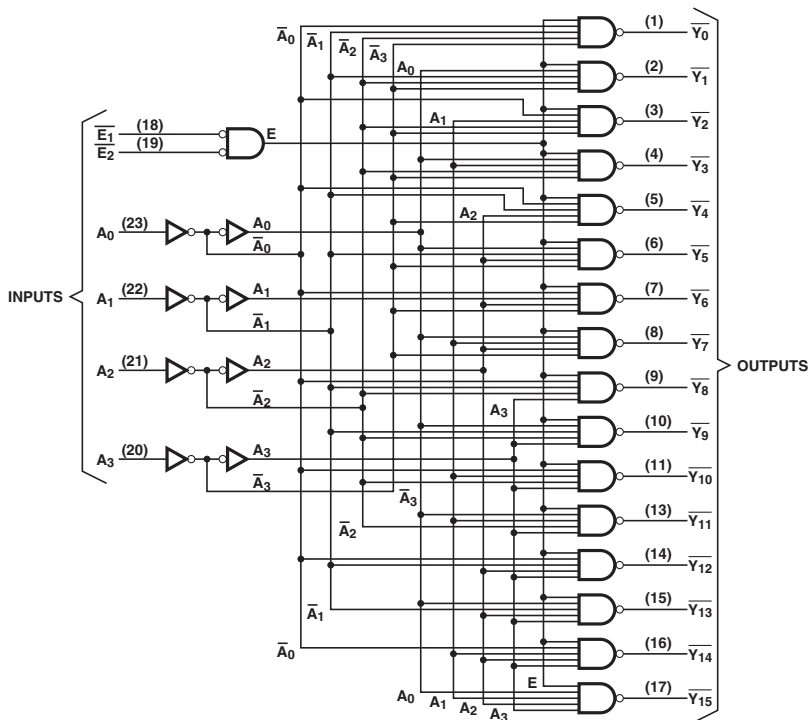
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------|--------|------------|-----|----|------|-----|------|------|---------|---------|----------|
| t _{PLH} | DATA | Y | MAX | 18 | 15 | 9 | 10 | 7 | 8 | 35 | 44 | 51 |
| | | | MAX | 23 | 26 | 9 | 15 | 8 | 7.5 | 35 | 44 | 51 |
| t _{PHL} | SELECT | Y | MAX | 34 | 29 | 18 | 21 | 12.5 | 12 | 38 | 48 | 51 |
| | | | MAX | 34 | 38 | 18 | 21 | 11 | 10.5 | 38 | 48 | 51 |
| t _{PLH} | STROBE | Y | MAX | 30 | 24 | 15 | 18 | 11.5 | 10.5 | 24 | 36 | 41 |
| | | | MAX | 23 | 32 | 13.5 | 18 | 9 | 8 | 24 | 36 | 41 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 AC | CD74 ACT |
|------------------|--------|--------|------------|---------|----------|
| t _{PLH} | DATA | Y | MAX | 13.3 | 18 |
| | | | MAX | 13.3 | 18 |
| t _{PHL} | SELECT | Y | MAX | 20 | 22 |
| | | | MAX | 20 | 22 |
| t _{PLH} | STROBE | Y | MAX | 11.8 | 12.6 |
| | | | MAX | 11.8 | 12.6 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|
| E ₁ | E ₂ | A ₃ | A ₂ | A ₁ | A ₀ | Y ₀ | Y ₁ | Y ₂ | Y ₃ | Y ₄ | Y ₅ | Y ₆ | Y ₇ | Y ₈ | Y ₉ | Y ₁₀ | Y ₁₁ | Y ₁₂ | Y ₁₃ | Y ₁₄ | Y ₁₅ | |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | ALS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 56 | 23 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | 24 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | -0.4 | 4 | 4 | 4 | mA |

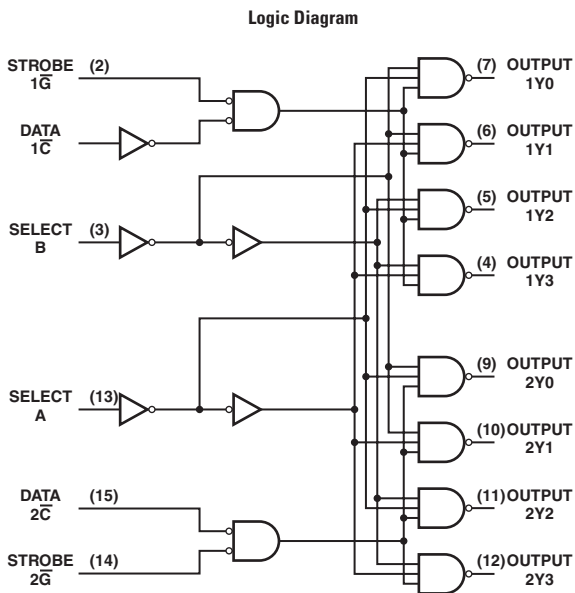
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | ALS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|---------|------------------------------|------------|-----|-----|---------|---------|----------|
| t _{PLH} | Address | 0 to 15 (CD74: Y0 to Y15) | MAX | 36 | 12 | 45 | 53 | 53 |
| t _{PHL} | | | | 33 | 12 | 45 | 53 | 53 |
| t _{PLH} | Enable | 0 to 15 (CD74: Y0 to Y15) | MAX | 30 | 12 | 45 | 53 | 51 |
| t _{PHL} | | | | 27 | 12 | 45 | 53 | 51 |

UNIT: ns

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Totem Pole



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | |
|--------|---|--------|------|---------|-----|-----|-----|
| SELECT | | STROBE | DATA | | | | |
| B | A | 1G | 1C | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| X | X | X | L | H | H | H | H |

| INPUTS | | | | OUTPUTS | | | |
|--------|---|--------|------|---------|-----|-----|-----|
| SELECT | | STROBE | DATA | | | | |
| B | A | 2G | 2C | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | L | L | H | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| X | X | X | H | H | H | H | H |

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | | | | | |
|--------|---|---|----------------|---------|-----|-----|-----|-----|-----|-----|-----|
| SELECT | | | STROBE or DATA | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C† | B | A | G‡ | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | X | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

† C = inputs 1C and 2C connected together

‡ G = inputs 1G and 2G connected together

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | UNIT |
|-----------------|------------|------|------|------|------|
| I _{CC} | MAX | 40 | 10 | 13 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | mA |

SWITCHING CHARACTERISTICS

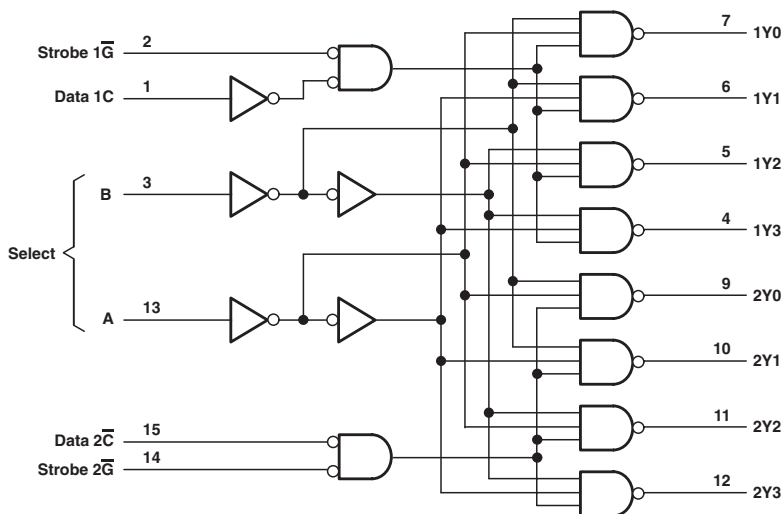
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS |
|------------------|--------|--------|------------|-----|----|-----|
| t _{PLH} | A or B | Y | MAX | 32 | 26 | 14 |
| t _{PHL} | A or B | | | 32 | 30 | 12 |
| t _{PLH} | 1C | Y | MAX | 24 | 27 | 12 |
| t _{PHL} | 1C | | | 30 | 27 | 14 |

UNIT: ns

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Open-Collector

Logic Diagram



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | |
|--------|---|--------|------|---------|-----|-----|-----|
| SELECT | | STROBE | DATA | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| B | A | 1G | 1C | | | | |
| X | X | H | X | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| X | X | X | L | H | H | H | H |

| INPUTS | | | | OUTPUTS | | | |
|--------|---|--------|------|---------|-----|-----|-----|
| SELECT | | STROBE | DATA | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| B | A | 2G | 2C | | | | |
| X | X | H | X | H | H | H | H |
| L | L | L | L | L | L | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| X | X | X | H | H | H | H | H |

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | | | | | |
|--------|---|---|----------------|---------|-----|-----|-----|-----|-----|-----|-----|
| SELECT | | | STROBE or DATA | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C† | B | A | G‡ | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | X | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

† C = inputs 1C and 2C connected together

‡ G = inputs 1G and 2G connected together

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | UNIT |
|-----------------|------------|-----|-----|-----|------|
| I _{CC} | MAX | 40 | 10 | 9 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | mA |
| V _{OH} | MAX | 5.5 | 5.5 | 5.5 | mA |

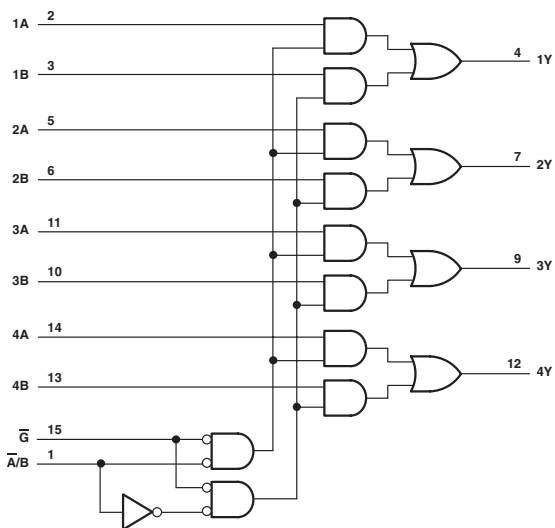
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS |
|------------------|----------------|--------|------------|-----|----|-----|
| t _{PLH} | 2C 1G or 2G | Y | MAX | 23 | 40 | 38 |
| | | | | 30 | 51 | 22 |
| t _{PHL} | A or B | Y | MAX | 34 | 46 | 55 |
| | | | | 34 | 51 | 25 |
| t _{PLH} | 1C | Y | MAX | 27 | 48 | 50 |
| | | | | 33 | 48 | 23 |

UNIT: ns

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74LV/SN74HC)



FUNCTION TABLE (SN74)

| INPUTS | | A | | B | | OUTPUT |
|--------|--------|---|---|---|---|--------|
| STROBE | SELECT | A | B | A | B | |
| H | X | X | X | X | X | L |
| L | L | L | L | X | X | L |
| L | L | L | L | H | X | H |
| L | H | H | X | L | L | L |
| L | H | X | H | X | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | UNIT |
|-----------------|------------|------|------|----|------|----|----|---------|---------|----------|------|
| I _{CC} | MAX | 48 | 16 | 78 | 11 | 28 | 23 | 0.08 | 0.16 | 0.08 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -6 | -4 | -6 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 6 | 4 | 6 | mA |

| PARAMETER | MAX or MIN | CD74 HCT | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | UNIT |
|-----------------|------------|----------|---------|----------|------|------|-------|-------|--------|------|
| I _{CC} | MAX | 0.16 | 0.16 | 0.16 | 0.04 | 0.02 | - | 0.0.2 | 0.01 | mA |
| I _{OH} | MAX | -4 | -24 | -24 | -8 | -8 | -6 | -12 | -24 | mA |
| I _{OL} | MAX | 4 | 24 | 24 | 8 | 8 | 6 | 12 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|------------------|--------|--------|------------|-----|----|------|-----|------|-----|---------|---------|----------|
| t _{PLH} | DATA | Y | MAX | 14 | 14 | 7.5 | 14 | 6 | 6.5 | 32 | 38 | 35 |
| | | | | 14 | 14 | 6.5 | 12 | 5.5 | 7 | 32 | 38 | 35 |
| t _{PHL} | STROBE | Y | MAX | 20 | 20 | 12.5 | 20 | 10.5 | 11 | 29 | 41 | 33 |
| | | | | 21 | 21 | 12 | 13 | 7.5 | 7 | 29 | 41 | 33 |
| t _{PLH} | SELECT | Y | MAX | 23 | 23 | 15 | 24 | 11 | 11 | 31 | 44 | 40 |
| | | | | 27 | 27 | 15 | 17 | 10 | 8 | 31 | 44 | 40 |

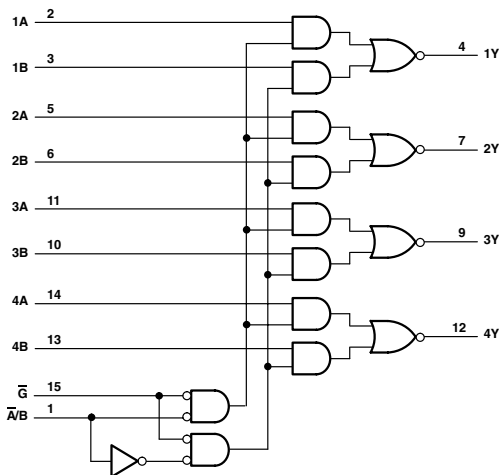
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V |
|------------------|--------|--------|------------|----------|---------|----------|------|------|-------|-------|--------|
| t _{PLH} | DATA | Y | MAX | 38 | 8.5 | 9.5 | 9.5 | 9.8 | 15 | 9.5 | 5.2 |
| | | | | 38 | 8.5 | 9.5 | 9.5 | 9.8 | 15 | 9.5 | 5.2 |
| t _{PHL} | STROBE | Y | MAX | 41 | 13.5 | 13.5 | 12 | 12 | 19.5 | 12 | 6.5 |
| | | | | 41 | 13.5 | 13.5 | 12 | 12 | 19.5 | 12 | 6.5 |
| t _{PLH} | SELECT | Y | MAX | 44 | 14.5 | 14.5 | 11.5 | 12 | 19 | 11.5 | 6.8 |
| | | | | 44 | 14.5 | 14.5 | 11.5 | 12 | 19 | 11.5 | 6.8 |

UNIT: ns

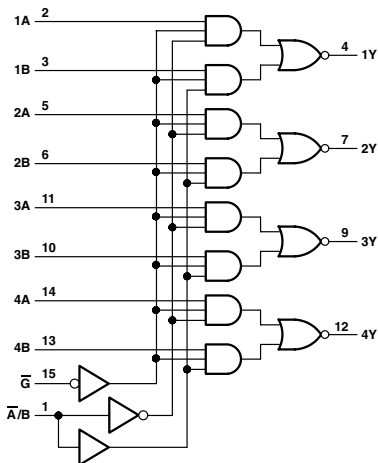
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

- Buffered Inputs and Outputs

Logic Diagram (SN74HC, ALS, LS)



Logic Diagram (SN74AS)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUT |
|--------|--------|---|---|--------|
| STROBE | SELECT | A | B | |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|----|------|------|----|---------|---------|----------|------|
| I _{CC} | MAX | 11 | 81 | 10 | 22.5 | 15 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.4 | -1 | -0.4 | -2 | -1 | -6 | -4 | -4 | mA |
| I _{OL} | MAX | 8 | 20 | 8 | 20 | 20 | 6 | 4 | 4 | mA |

| PARAMETER | MAX or MIN | CD74 AC | CD74 ACT | AHC | AHCT | UNIT |
|-----------------|------------|---------|----------|------|------|------|
| I _{CC} | MAX | 0.16 | 0.16 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -24 | -24 | -8 | -8 | mA |
| I _{OL} | MAX | 24 | 24 | 8 | 8 | mA |

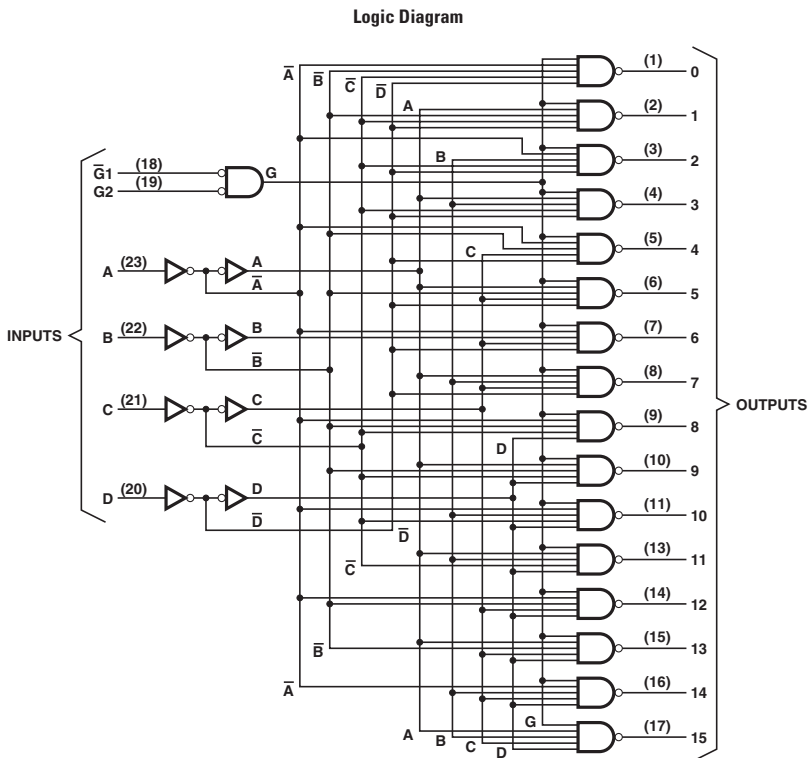
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------|--------|------------|----|------|-----|------|-----|---------|---------|----------|
| t _{PLH} | DATA | Y | MAX | 12 | 6 | 15 | 5 | 7 | 32 | 42 | 42 |
| | | | | 15 | 6 | 8 | 4.5 | 4.5 | 32 | 42 | 42 |
| t _{PHL} | STROBE | Y | MAX | 17 | 11.5 | 18 | 6.5 | 7 | 29 | 48 | 48 |
| | | | | 24 | 12 | 18 | 10 | 6.5 | 29 | 48 | 48 |
| t _{PLH} | SELECT | Y | MAX | 20 | 12 | 18 | 9.5 | 9.5 | 31 | 45 | 45 |
| | | | | 24 | 12 | 18 | 10.5 | 7 | 31 | 45 | 45 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 AC | CD74 ACT | AHC | AHCT |
|------------------|--------|--------|------------|---------|----------|------|------|
| t _{PLH} | DATA | Y | MAX | 8 | 9.2 | 9.5 | 9.8 |
| | | | | 8 | 9.2 | 9.5 | 9.8 |
| t _{PHL} | STROBE | Y | MAX | 11.9 | 12.4 | 12 | 12 |
| | | | | 11.9 | 12.4 | 12 | 12 |
| t _{PLH} | SELECT | Y | MAX | 12.9 | 13.5 | 11.5 | 12 |
| | | | | 12.9 | 13.5 | 11.5 | 12 |

UNIT: ns

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS



FUNCTION TABLE

| | | INPUTS | | | | OUTPUTS | | | | | | | | | | | | | | | | |
|----|----|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|---|
| G1 | G2 | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | L | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 56 | mA |
| I _{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

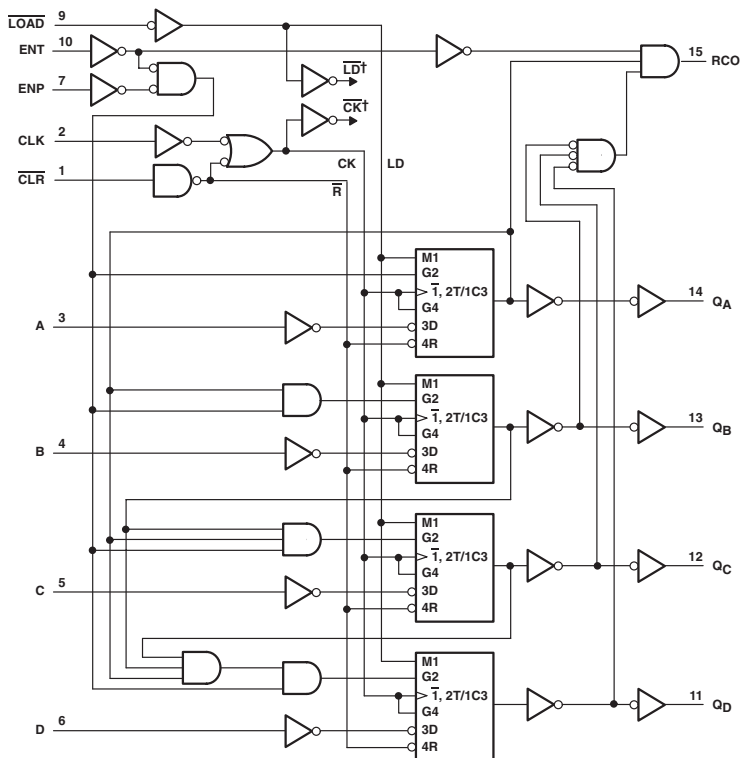
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|------------------|--------|--------|------------|-----|
| t _{PLH} | INPUT | ANY | MAX | 36 |
| t _{PHL} | | | | 36 |
| t _{PLH} | STROBE | ANY | MAX | 25 |
| t _{PHL} | | | | 36 |

UNIT: ns

4-BIT SYNCHRONOUS BINARY COUNTERS

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74)



† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

FUNCTION TABLE (SN74)

| INPUTS | | | | | OUTPUTS | | | | FUNCTION |
|--------|------|-----|-----|-----|---------|----|----|----|--------------|
| CLR | LOAD | ENP | ENT | CLK | QA | QB | QC | QD | |
| L | X | X | X | X | L | L | L | L | Reset to "0" |
| H | L | X | X | | A | B | C | D | Preset Data |
| H | H | X | L | | | | | | No Change |
| H | H | L | X | | | | | | No Change |
| H | H | H | H | | | | | | Count up |
| H | X | X | X | | | | | | No Change |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|------|----|----|---------|---------|----------|---------|----------|-------|-------|------|
| I _{CC} | MAX | 101 | 32 | 21 | 53 | 55 | 0.08 | 0.16 | 0.16 | 0.08 | 0.08 | - | 0.02 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | -2 | -1 | 4 | -4 | -4 | -24 | -24 | -6 | -12 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 20 | 20 | -4 | 4 | 4 | 24 | 24 | -6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT |
|------------------|----------------|-------------------------------|------------|-----|----|-----|------|------|---------|---------|----------|
| f _{max} | | | MIN | 25 | 25 | 40 | 75 | 90 | 25 | 20 | 20 |
| t _w | CLOCK | | MIN | 25 | 25 | - | - | 7 | 20 | 24 | 24 |
| | CLEAR | | | 20 | 20 | 15 | 8 | 5 | 20 | 30 | 30 |
| t _{su} | INPUT | | MIN | 20 | 20 | 15 | 8 | 5 | 38 | 18 | 15 |
| | ENABLE | | | 20 | 20 | 15 | 8 | 11.5 | 43 | 15 | 20 |
| | LOAD | | | 25 | 20 | 15 | 8 | 11.5 | 34 | 18 | 18 |
| | CLEAR INACTIVE | | | 20 | 25 | 10 | 8 | - | 31 | - | - |
| | | | | | 0 | 3 | 0 | 0 | 2 | 0 | 3 |
| t _{th} | | | MIN | 0 | 3 | 0 | 0 | 2 | 0 | 3 | 5 |
| t _{PLH} | CLOCK | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | 35 | 35 | 20 | 16.5 | 15 | 54 | 56 | 63 |
| t _{PHL} | | | | 35 | 35 | 20 | 12.5 | 15 | 54 | 56 | 63 |
| t _{PLH} | CLOCK | ANY Q | MAX | 25 | 24 | 15 | 7 | 9.5 | 51 | 56 | 59 |
| t _{PHL} | | | | 29 | 27 | 20 | 13 | 11 | 51 | 56 | 59 |
| t _{PLH} | ENABLE | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | 16 | 14 | 13 | 9 | 8.5 | 49 | 36 | 48 |
| t _{PHL} | | | | 16 | 14 | 13 | 8.5 | 8.5 | 49 | 36 | 48 |
| t _{PHL} | CLEAR | ANY Q | MAX | 38 | 28 | 24 | 13 | 13 | 53 | 63 | 75 |
| | | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | - | - | 23 | 12.5 | 11.5 | 55 | 63 | 75 |

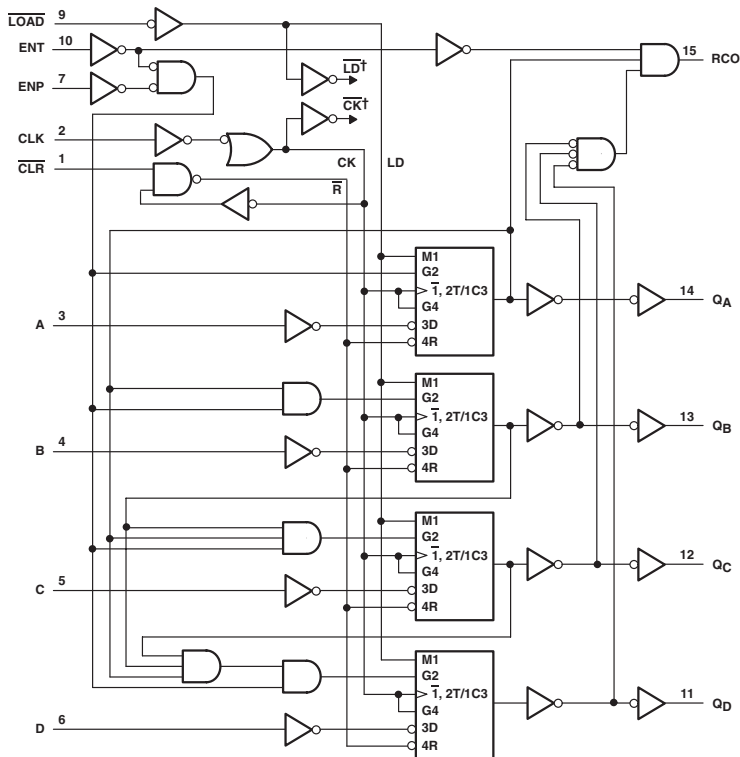
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 AC | CD74 ACT | LV 3V | LV 5V |
|------------------|----------------|-------------------------------|------------|---------|----------|-------|-------|
| f _{max} | | | MIN | 90 | 80 | 50 | 85 |
| t _w | CLOCK | | MIN | 5.5 | 6.2 | 5 | 5 |
| | CLEAR | | | 5 | 6 | 5 | 5 |
| t _{su} | INPUT | | MIN | 5 | 5 | 6.5 | 4.5 |
| | ENABLE | | | - | - | 9 | 6 |
| | LOAD | | | 6 | 6 | 9.5 | 6 |
| | CLEAR INACTIVE | | | - | - | 2.5 | 1.5 |
| | | | | | 0 | 0 | 1 |
| t _{th} | | | MIN | 0 | 0 | 1 | 1 |
| t _{PLH} | CLOCK | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | 16.7 | 16.7 | 23.5 | 14 |
| t _{PHL} | | | | 16.7 | 16.7 | 23.5 | 14 |
| t _{PLH} | CLOCK | ANY Q | MAX | 16.5 | 16.5 | 18.5 | 11.5 |
| t _{PHL} | | | | 16.5 | 16.5 | 18.5 | 11.5 |
| t _{PLH} | ENABLE | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | 10.3 | 10.8 | 18 | 11.5 |
| t _{PHL} | | | | 10.3 | 10.8 | 18 | 11.5 |
| t _{PHL} | CLEAR | ANY Q | MAX | 16.5 | 16.5 | 19.5 | 12.5 |
| | | RIPPLE CARRY (CD74HC/HCT: TC) | MAX | 16.5 | 16.5 | 19 | 12 |

UNIT f_{max} : MHz, other : ns

4-BIT SYNCHRONOUS BINARY COUNTERS

- Synchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74LV)



† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

FUNCTION TABLE (SN74)

| INPUTS | | | | | OUTPUTS | | | | FUNCTION |
|--------|------|-----|-----|-----|---------|----|----|----|--------------|
| CLR | LOAD | ENP | ENT | CLK | QA | QB | QC | QD | |
| L | X | X | X | X | L | L | L | L | Reset to "0" |
| H | L | X | X | X | A | B | C | D | Preset data |
| H | H | X | L | | | | | | No change |
| H | H | L | X | | | | | | No change |
| H | H | H | H | | | | | | Count up |
| H | X | X | X | | | | | | No change |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|-----|------|----|----|---------|---------|----------|---------|----------|-------|-------|------|
| I _{cc} | MAX | 101 | 32 | 160 | 21 | 53 | 55 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | - | 0.02 | mA |
| I _{oh} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | 4 | -4 | -4 | -24 | -24 | -6 | -12 | mA |
| I _{ol} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | -4 | 4 | 4 | 24 | 24 | -6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC |
|------------------|--------|--------------|------------|-----|----|----|------|------|------|---------|
| f _{max} | | | MIN | 25 | 25 | 40 | 40 | 75 | 90 | 25 |
| t _w | CLOCK | | MIN | 25 | 25 | 10 | - | - | 7 | 20 |
| | CLEAR | | | 20 | 20 | 10 | 12.5 | 6.7 | - | - |
| t _{su} | INPUT | | MIN | 20 | 20 | 4 | 15 | 8 | 5 | 38 |
| | ENABLE | | | 20 | 20 | 12 | 15 | 8 | 11.5 | 43 |
| | LOAD | | | 25 | 20 | 14 | 15 | 8 | 11.5 | 34 |
| | CLEAR | | | 20 | 20 | 14 | 15 | 12 | - | 40 |
| | | | | | 0 | 3 | 3 | 0 | 0 | 2 |
| t _{th} | | | MIN | 0 | 3 | 3 | 0 | 0 | 2 | 0 |
| t _{PLH} | CLOCK | RIPPLE CARRY | MAX | 35 | 35 | 25 | 20 | 16.5 | 15 | 54 |
| t _{PHL} | | | | 35 | 35 | 25 | 20 | 12.5 | 15 | 54 |
| t _{PLH} | CLOCK | ANY Q | MAX | 25 | 24 | 15 | 15 | 7 | 9.5 | 51 |
| t _{PHL} | | | | 29 | 27 | 15 | 20 | 13 | 11 | 51 |
| t _{PLH} | ENABLE | RIPPLE CARRY | MAX | 16 | 14 | 15 | 13 | 9 | 8.5 | 49 |
| t _{PHL} | | | | 16 | 14 | 15 | 13 | 8.5 | 8.5 | 49 |

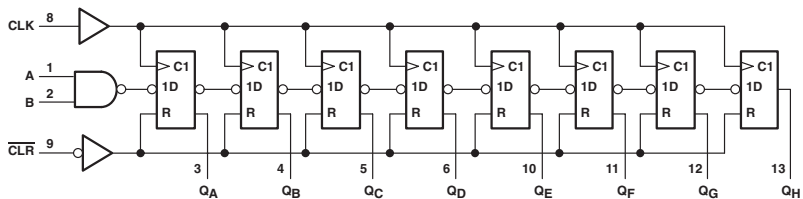
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LV 3V | LV 5V |
|------------------|--------|--------------|------------|---------|----------|---------|----------|-------|-------|
| f _{max} | | | MIN | 20 | 20 | 90 | 80 | 50 | 85 |
| t _w | CLOCK | | MIN | 24 | 24 | 5.5 | 6.2 | 5 | 5 |
| | CLEAR | | | - | - | - | - | - | - |
| t _{su} | INPUT | | MIN | 18 | 15 | 5 | 5 | 6.5 | 4.5 |
| | ENABLE | | | 15 | 20 | 5 | 6 | 9 | 6 |
| | LOAD | | | 18 | 18 | 6 | 7.5 | 9.5 | 6 |
| | CLEAR | | | 20 | 20 | 6 | 7.5 | 4 | 3.5 |
| | | | | | 3 | 5 | 0 | 0 | 1 |
| t _{th} | | | MIN | 3 | 5 | 0 | 0 | 1 | 1 |
| t _{PLH} | CLOCK | RIPPLE CARRY | MAX | 56 | 63 | 16.7 | 16.7 | 23.5 | 14 |
| t _{PHL} | | | | 56 | 63 | 16.7 | 16.7 | 23.5 | 14 |
| t _{PLH} | CLOCK | ANY Q | MAX | 56 | 59 | 16.5 | 16.5 | 18.5 | 11.5 |
| t _{PHL} | | | | 56 | 59 | 16.5 | 16.5 | 18.5 | 11.5 |
| t _{PLH} | ENABLE | RIPPLE CARRY | MAX | 36 | 48 | 10.3 | 10.8 | 18 | 11.5 |
| t _{PHL} | | | | 36 | 48 | 10.3 | 10.8 | 18 | 11.5 |

UNIT f_{max} : MHz, other : ns

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | | | |
|--------|-------|---|---|-----------------|-----------------|-----|-----------------|
| CLEAR | CLOCK | A | B | Q _A | Q _B | ... | Q _H |
| L | X | X | X | L | L | L | L |
| H | L | X | X | Q _{A0} | Q _{B0} | ... | Q _{H0} |
| H | ↑ | H | H | H | Q _{An} | ... | Q _{Gn} |
| H | ↑ | L | X | L | Q _{An} | ... | Q _{Gn} |
| H | ↑ | X | L | L | Q _{An} | ... | Q _{Gn} |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|------|---------|---------|----------|---------|----------|-------|-------|------|
| I _{CC} | MAX | 54 | 27 | 24 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | - | 0.02 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -0.4 | -4 | -4 | -4 | -24 | -24 | -6 | -12 | mA |
| I _{OL} | MAX | 8 | 8 | 8 | 4 | 4 | 4 | 24 | 24 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|------------------|---------|--------|------------|-----|----|-----|---------|---------|----------|---------|----------|
| f _{max} | | | MIN | 25 | 25 | 50 | 25 | 20 | 18 | 7.5 | 7.0 |
| t _w | CLR "L" | | MIN | 20 | 20 | 16 | 25 | 18 | 27 | 4.5 | 4.5 |
| | | | MIN | 20 | 20 | 10 | 20 | 24 | 27 | 6.7 | 7.1 |
| | | | MIN | 20 | 20 | 10 | 20 | 24 | 27 | 6.7 | 7.1 |
| | | | MIN | 20 | 20 | 10 | 20 | 24 | 27 | 6.7 | 7.1 |
| t _{su} | DATA | | MIN | 15 | 15 | 6 | 25 | 18 | 18 | 2.5 | 2.5 |
| | | | MIN | 20 | 20 | 8 | 25 | 18 | 18 | 2.5 | 2.5 |
| t _h | | | MIN | 5 | 5 | 2 | 5 | 4 | 4 | 2.5 | 3 |
| t _{PHL} | CLEAR | Q | MAX | 42 | 36 | 20 | 51 | 42 | 57 | 13.9 | 15.8 |
| t _{PLH} | CLOCK | Q | MAX | 30 | 27 | 16 | 44 | 51 | 54 | 12.5 | 14.9 |
| | | | MAX | 37 | 32 | 17 | 44 | 51 | 54 | 12.5 | 14.9 |

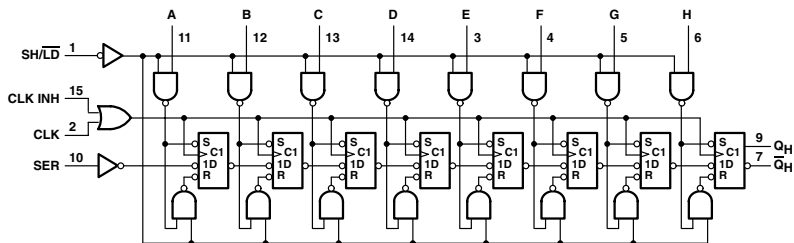
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV 3V | LV 5V |
|------------------|---------|--------|------------|-------|-------|
| f _{max} | | | MIN | 45 | 75 |
| t _w | CLR "L" | | MIN | 5 | 5 |
| | | | MIN | 5 | 5 |
| | | | MIN | 5 | 5 |
| | | | MIN | 5 | 5 |
| t _{su} | DATA | | MIN | 6 | 4.5 |
| | | | MIN | 2.5 | 2.5 |
| t _h | | | MIN | 0 | 1 |
| t _{PHL} | CLEAR | Q | MAX | 18.5 | 12.5 |
| t _{PLH} | CLOCK | Q | MAX | 18.5 | 12.5 |
| | | | MAX | 18.5 | 12.5 |

UNIT f_{max} : MHz, other : ns

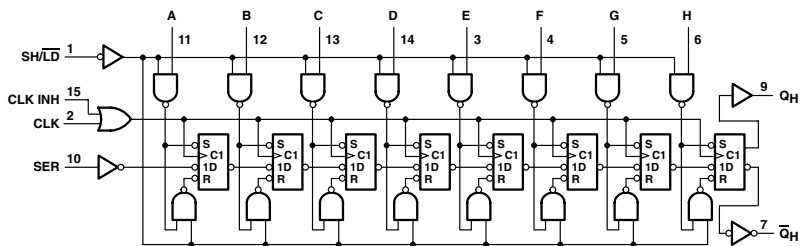
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs: Serial (QH, \bar{Q}_H)
- Direct Overriding Load (Data) Inputs
- Parallel-to-Serial Data Conversion

Logic Diagram (SN74LV, ALS, LS)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

| SHIFT/ LOAD | CLOCK INHIBIT | INPUTS | | | INTERNAL OUTPUTS | | OUTPUT Q _H |
|----------------|------------------|--------|--------|-------------------|---------------------|-----------------|------------------------------|
| | | CLOCK | SERIAL | PARALLEL A...H | Q _A | Q _B | |
| L | X | X | X | a...h | a | b | h |
| H | L | L | X | X | Q _{A0} | Q _{B0} | Q _{H0} |
| H | L | ↑ | H | X | H | Q _{An} | Q _{Gn} |
| H | L | ↑ | L | X | L | Q _{An} | Q _{Gn} |
| H | H | X | X | X | Q _{A0} | Q _{B0} | Q _{H0} |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|------|------------|------------|-------------|----------|----------|------|
| I _{cc} | MAX | 63 | 30 | 24 | 0.08 | 0.16 | 0.16 | - | 0.02 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | -4 | -4 | -4 | -6 | -12 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 4 | 4 | 4 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

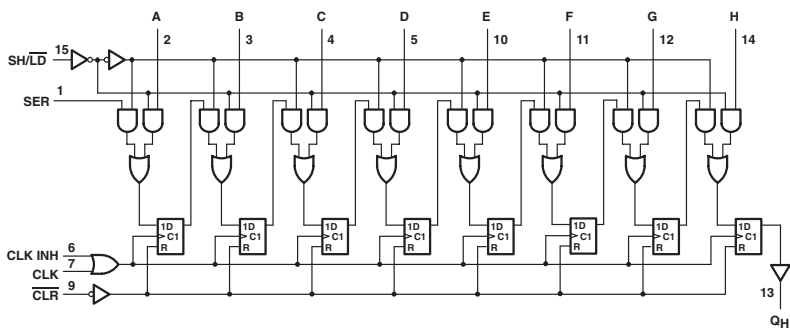
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|------------------|---|---|--------|------------|-----|----|-----|------------|------------|-------------|----------|----------|
| f _{max} | | | | MIN | 20 | 25 | 45 | 25 | 20 | 18 | 50 | 85 |
| t _w | CLOCK (CD74: CP) | High | | MIN | 25 | 15 | 11 | 20 | 24 | 27 | 7 | 4 |
| | | Low | | MIN | 25 | 25 | 11 | 20 | 24 | 27 | 7 | 4 |
| | SH/ $\overline{\text{LD}}$ 'L' (CD74: $\overline{\text{PL}}$) | High | | MIN | 15 | 25 | - | - | - | - | - | - |
| | | Low | | MIN | 15 | 17 | 12 | 20 | 24 | 30 | 9 | 6 |
| t _{su} | CLK INH (CD74: $\overline{\text{CE}}$) | | | MIN | 30 | 30 | 11 | 25 | 24 | 30 | 5 | 3.5 |
| | DATA | | | | 10 | 10 | 10 | 25 | 24 | 30 | 8.5 | 5 |
| | SER (CD74: DS) | | | | 20 | 20 | 10 | 10 | 24 | 30 | 6 | 4 |
| | SH/ $\overline{\text{LD}}$ 'H' | | | | 45 | 45 | 10 | 20 | - | - | 6 | 4 |
| t _h | | | | MIN | 0 | 0 | 4 | 5 | 11 | 11 | 0.5 | 1 |
| t _{PLH} | CLOCK (CD74: CP) | Q _H or $\overline{\text{Q}}_{H}$ (CD74: Q ₇ or $\overline{\text{Q}}_{7}$) | | MAX | 24 | 25 | 13 | 38 | 50 | 60 | 16.9 | 13.5 |
| t _{PHL} | | | | | 31 | 25 | 14 | 38 | 50 | 60 | 16.9 | 13.5 |
| t _{PLH} | SH/ $\overline{\text{LD}}$ (CD74: $\overline{\text{PL}}$) | Q _H or $\overline{\text{Q}}_{H}$ (CD74: Q ₇ or $\overline{\text{Q}}_{7}$) | | MAX | 31 | 35 | 20 | 38 | 53 | 60 | 22 | 13.5 |
| t _{PHL} | | | | | 40 | 35 | 22 | 38 | 53 | 60 | 22 | 13.5 |
| t _{PLH} | H (CD74: D ₇) | Q _H (CD74: Q ₇) | | MAX | 17 | 25 | 13 | 38 | 45 | 53 | 20 | 12.5 |
| t _{PHL} | | | | | 36 | 30 | 16 | 38 | 45 | 53 | 20 | 12.5 |
| t _{PLH} | H (CD74: D ₇) | $\overline{\text{Q}}_{H}$ (CD74: $\overline{\text{Q}}_{7}$) | | MAX | 27 | 30 | 15 | 38 | 45 | 53 | 20 | 12.5 |
| t _{PHL} | | | | | 27 | 25 | 16 | 38 | 45 | 53 | 20 | 12.5 |

UNIT f_{max} : MHz, other : ns

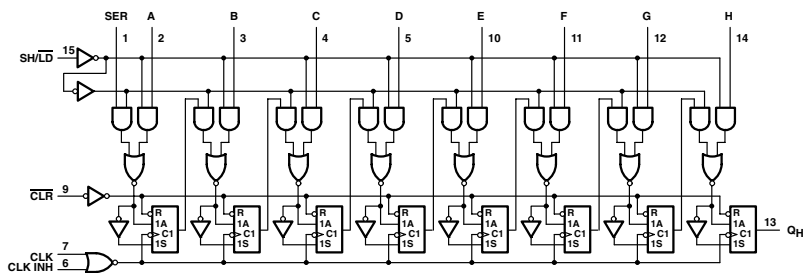
8-BIT PARALLEL-LOAD SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram (SN74LV, HC)



Logic Diagram (SN74ALS, LS)



FUNCTION TABLE (SN74)

| CLEAR | INPUTS | | | | | | INTERNAL OUTPUTS | | | OUTPUT |
|-------|------------|---------------|-------|--------|----------|-----|------------------|-----|--|--------|
| | SHIFT/LOAD | CLOCK INHIBIT | CLOCK | SERIAL | PARALLEL | QA | QB | QH | | |
| | | | | | A...H | | | | | |
| L | X | X | X | X | X | L | L | L | | |
| H | X | L | L | X | X | QA0 | QB0 | QH0 | | |
| H | L | L | ↑ | X | a...h | a | b | h | | |
| H | H | L | ↑ | H | X | H | QAn | QGn | | |
| H | H | L | ↑ | L | X | L | QAn | QGn | | |
| H | X | H | ↑ | X | X | QA0 | QB0 | QH0 | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | F | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|------|----|---------|---------|----------|-------|-------|------|
| I _{CC} | MAX | 127 | 32 | 24 | 60 | 0.08 | 0.16 | 0.16 | - | 0.02 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | -1 | -4 | -4 | -4 | -6 | -12 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 20 | 4 | 4 | 4 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

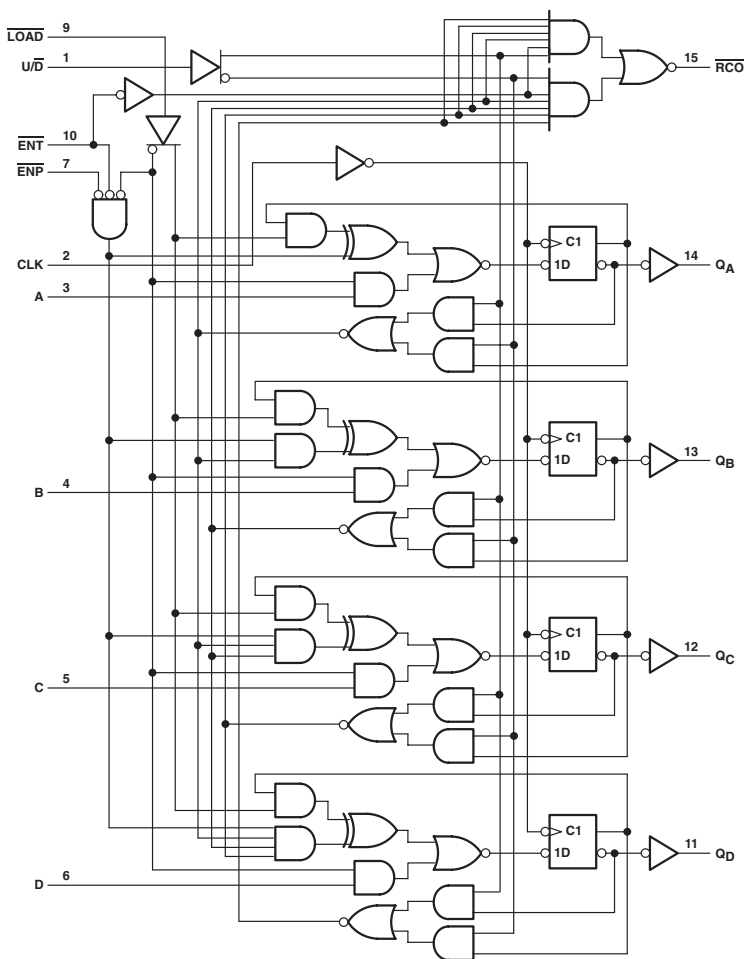
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | F | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|------------------|------------------|-------|--------|------------|-------|----|-----|-----|---------|---------|----------|-------|-------|
| f _{max} | | | | MIN | 25 | 25 | 45 | 110 | 25 | 20 | 16 | 50 | 85 |
| t _w | CLOCK (CD74: CP) | | | MIN | 20 | 20 | 10 | 3.5 | 20 | 24 | 30 | 7 | 4 |
| | | | | | 20 | 25 | 9 | 4 | 25 | 30 | 53 | 7 | 5 |
| t _{su} | Mode Control | | | MIN | 30 | 30 | 16 | 4 | 36 | 44 | 45 | 6 | 4 |
| | DATA | | | | 20 | 20 | 7 | 3 | 20 | 24 | 24 | 6 | 4.5 |
| t _h | | | | MIN | 0 | 0 | 3 | 0 | 0 | 1 | 0 | 0 | 1 |
| t _{PHL} | | CLEAR | QH | MAX | 35 | 30 | 14 | 9.5 | 30 | 48 | 60 | 18.5 | 12 |
| t _{PHL} | | | | | CLOCK | QH | MAX | 30 | 25 | 13 | 14 | 38 | 48 |
| t _{PLH} | | | | | | | | 26 | 20 | 12 | 9 | 38 | 48 |

UNIT: f_{max} - MHz; other - ns

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | S | ALS | AS | F | UNIT |
|-----------------|------------------|------------|------|-----|------|----|----|------|
| I _{CC} | | MAX | 45 | 160 | 25 | 63 | 52 | mA |
| I _{OH} | \overline{RCO} | MAX | -0.4 | -1 | -0.4 | -2 | -1 | mA |
| | Q | MAX | -1.2 | -1 | -0.4 | -2 | -1 | mA |
| I _{OL} | \overline{RCO} | MAX | 8 | 20 | 8 | 20 | 20 | mA |
| | Q | MAX | 24 | 20 | 8 | 20 | 20 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

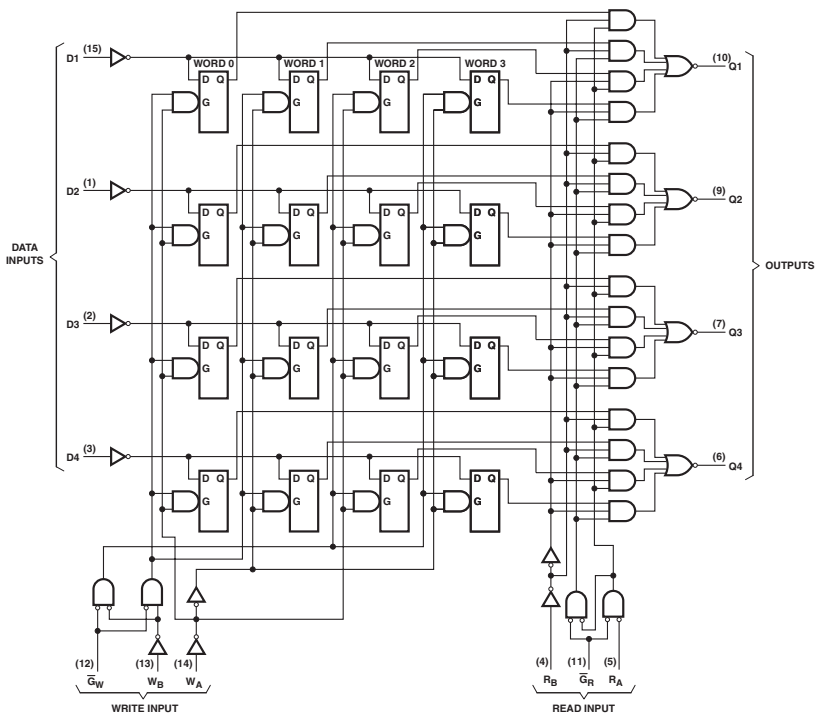
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F |
|------------------|-------------------|------------------|------------|----|----|-----|------|------|
| f _{max} | | | MIN | 20 | 40 | 40 | 75 | 90 |
| t _{PLH} | CLK | \overline{RCO} | MAX | 40 | 21 | 20 | 16.5 | 17 |
| | | | | 25 | 28 | 20 | 13 | 12.5 |
| t _{PLH} | CLK | ANY Q | MAX | 25 | 15 | 15 | 13 | 9.5 |
| | | | | 25 | 15 | 20 | 7 | 13 |
| t _{PLH} | \overline{ENT} | \overline{RCO} | MAX | 25 | 12 | 13 | 9 | 7 |
| | | | | 20 | 25 | 16 | 9 | 9 |
| t _{PLH} | U/ \overline{D} | \overline{RCO} | MAX | 35 | 15 | 19 | 12 | 12.5 |
| | | | | 25 | 22 | 19 | 13 | 12 |

UNIT f_{max} : MHz, other : ns

4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits

Logic Diagram



WRITE FUNCTION TABLE

| WRITE INPUTS | | | OUTPUTS | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| W _B | W _A | W _Y | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | Q ₀ | Q ₀ | Q ₀ |
| L | H | L | Q ₀ | Q = D | Q ₀ | Q ₀ |
| H | L | L | Q ₀ | Q ₀ | Q = D | Q ₀ |
| H | H | L | Q ₀ | Q ₀ | Q ₀ | Q = D |
| X | X | H | Q ₀ | Q ₀ | Q ₀ | Q ₀ |

READ FUNCTION TABLE

| READ INPUTS | | | OUTPUTS | | | |
|----------------|----------------|----------------|---------|------|------|------|
| R _B | R _A | R _R | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|-----|-----|------|
| I _{CC} | MAX | 150 | 40 | mA |
| V _{OH} | MAX | 5.5 | 5.5 | V |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

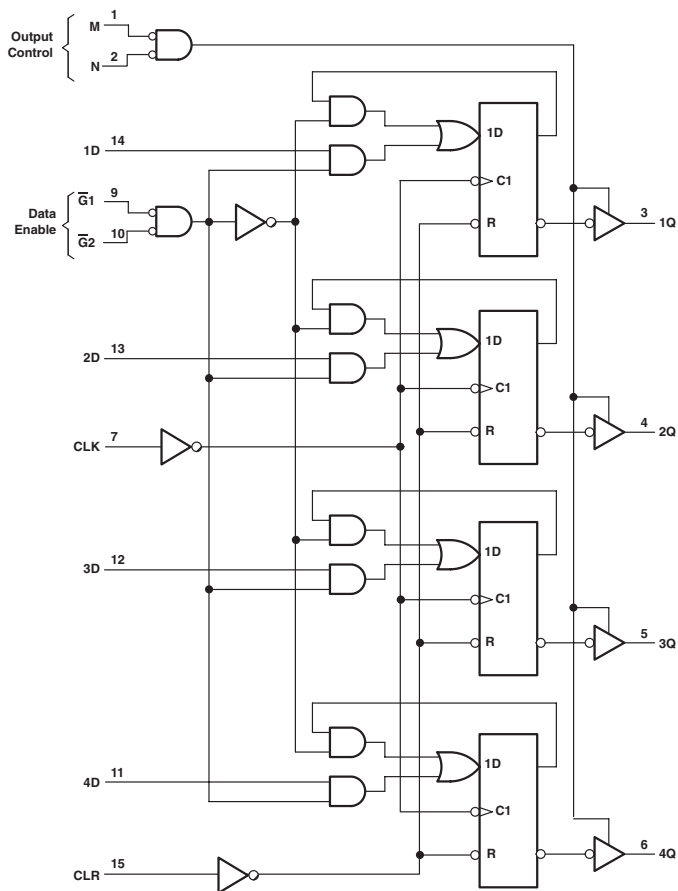
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|-----------------|--------|------------|-----|----|
| f _{max} | | | MIN | | |
| t _w | | | MIN | 25 | 25 |
| t _{su} | D | | MIN | 10 | 10 |
| | W | | | 15 | 15 |
| t _h | D | | MIN | 15 | 15 |
| | W | | | 5 | 5 |
| t _{PLH} | READ ENABLE | Q | MAX | 15 | 30 |
| t _{PHL} | | | | 30 | 30 |
| t _{PLH} | READ SELECT | Q | MAX | 35 | 40 |
| t _{PHL} | | | | 40 | 40 |
| t _{PLH} | WRITE ENABLE | Q | MAX | 40 | 45 |
| t _{PHL} | | | | 45 | 40 |
| t _{PLH} | DATA | Q | MAX | 30 | 45 |
| t _{PHL} | | | | 45 | 35 |

 UNIT f_{max} : MHz, other : ns

4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly
- Fully Independent Clock Virtually

Logic Diagram (SN74LS)



FUNCTION TABLE (SN74LS)

| CLEAR | CLOCK | INPUTS | | | OUTPUT Q |
|-------|-------|------------|--------------|-----------|----------------|
| | | DATA G1 | ENABLE G2 | DATA D | |
| H | X | X | X | X | L |
| L | L | X | X | X | Q ₀ |
| L | ↑ | H | X | X | Q ₀ |
| L | ↑ | X | H | X | Q ₀ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|------------|------------|-------------|------|
| I _{CC} | MAX | 72 | 24 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -5.2 | -2.6 | -6 | -6 | -6 | mA |
| I _{OL} | MAX | 16 | 24 | 6 | 6 | 6 | mA |

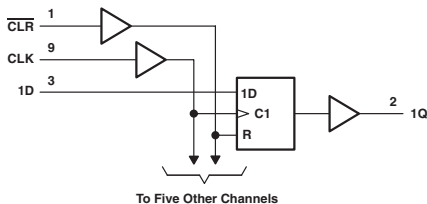
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|---------------------|--------|------------|-----|----|------------|------------|-------------|
| f _{max} | | | MIN | 25 | 25 | 25 | 20 | 13 |
| t _w | | | MIN | 20 | 25 | 20 | 24 | 38 |
| t _{su} | DATA ENABLE | | MIN | 17 | 35 | 25 | 18 | 18 |
| | DATA | | MIN | 10 | 17 | 25 | 18 | 27 |
| | CLR INACTIVE | | MIN | 10 | 10 | 23 | - | - |
| t _h | DATA ENABLE | | MIN | 2 | 0 | 0 | 0 | 0 |
| | DATA | | MIN | 10 | 3 | 0 | 3 | 0 |
| t _{PHL} | CLEAR | Q | MAX | 27 | 35 | 38 | 53 | 66 |
| t _{PLH} | CLOCK (CD74: CP) | Q | MAX | 43 | 25 | 38 | 60 | 60 |
| t _{PHL} | | | | 31 | 30 | 38 | 60 | 60 |
| t _{PZH} | ENABLE | Q | MAX | 30 | 23 | 38 | 45 | 45 |
| t _{PZL} | | | | 30 | 27 | 38 | 45 | 45 |
| t _{PHZ} | DISABLE | Q | MAX | 14 | 20 | 38 | 45 | - |
| t _{PHZ} | | | | 20 | 17 | 38 | 45 | - |

UNIT f_{max} : MHz, other : ns

HEX D-TYPE FLIP-FLOPS WITH CLEAR

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT |
|--------|-------|---|----------------|
| CLEAR | CLOCK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| L | L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|------|------|-----|------|----|----|---------|---------|------|
| I _{CC} | MAX | 65 | 26 | 144 | 19 | 45 | 55 | 0.08 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | mA |

| PARAMETER | MAX or MIN | CD74 HCT | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|----------|---------|----------|------|------|-------|-------|------|
| I _{CC} | MAX | 0.16 | 0.16 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I _{OH} | MAX | -4 | -24 | -24 | -8 | -8 | -6 | -12 | mA |
| I _{OL} | MAX | 4 | 24 | 24 | 8 | 8 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

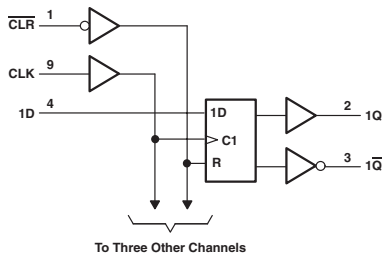
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC |
|------------------|--------------|--------|------------|-----|----|----|-----|-----|-----|---------|---------|
| f _{max} | | | MIN | 25 | 30 | 75 | 50 | 100 | 80 | 25 | 20 |
| t _w | CLR (MR) LOW | | MIN | 20 | 20 | 10 | 10 | 5 | 5 | 20 | 24 |
| | | | MIN | 20 | 20 | 7 | 10 | 4 | 4 | 20 | 24 |
| | | | MIN | 20 | 20 | 7 | 10 | 6 | 6 | 20 | 24 |
| t _{su} | DATA INPUT | | MIN | 20 | 20 | 5 | 10 | 4 | 4.5 | 25 | 18 |
| | | | MIN | 25 | 25 | 5 | 6 | 6 | 5 | 25 | - |
| | | | MIN | 5 | 5 | 3 | 0 | 1 | 1 | 0 | 5 |
| t _{PH} | CLR (MR) | ANY Q | MAX | 25 | - | - | 18 | - | - | 40 | 45 |
| t _{PHL} | CLR (MR) | ANY Q | MAX | 35 | 35 | 22 | 23 | 14 | 15 | 40 | 45 |
| t _{PH} | CLK (CP) | ANY Q | MAX | 30 | 30 | 12 | 15 | 8 | 9 | 40 | 50 |
| t _{PHL} | CLK (CP) | ANY Q | MAX | 35 | 30 | 17 | 17 | 10 | 11 | 40 | 50 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V |
|------------------|--------------|--------|------------|----------|---------|----------|------|------|-------|-------|
| f _{max} | | | MIN | 17 | 95 | 80 | 80 | 65 | 50 | 80 |
| t _w | CLR (MR) LOW | | MIN | 38 | 4 | 4 | 5 | 5 | 5 | 5 |
| | | | MIN | 30 | 5.2 | 6.2 | 5 | 5 | 5 | 5 |
| | | | MIN | 30 | 5.2 | 6.2 | 5 | 5 | 5 | 5 |
| t _{su} | DATA INPUT | | MIN | 24 | 2 | 2 | 4.5 | 5 | 6 | 4.5 |
| | | | MIN | - | - | - | 2.5 | 3.5 | 3 | 2.5 |
| | | | MIN | 5 | 3 | 2.5 | 0.5 | 0 | 0 | 0.5 |
| t _{PH} | CLR (MR) | ANY Q | MAX | 66 | 14.5 | 15.5 | - | - | 17 | 11 |
| t _{PHL} | CLR (MR) | ANY Q | MAX | 66 | 14.5 | 15.5 | 11 | 13 | 17 | 11 |
| t _{PH} | CLK (CP) | ANY Q | MAX | 60 | 13.5 | 14 | 10.5 | 10 | 16.5 | 10.5 |
| t _{PHL} | CLK (CP) | ANY Q | MAX | 60 | 13.5 | 14 | 10.5 | 10 | 16.5 | 10.5 |

UNIT f_{max} : MHz, other : ns

QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

- Complementary Outputs (Q , \bar{Q})
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUTS | |
|--------|------------|---|---------|-------------|
| CLR | CLOCK | D | Q | \bar{Q} |
| L | X | X | L | H |
| H | \uparrow | H | H | L |
| H | \uparrow | L | L | H |
| H | L | X | Q_0 | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | AC 11 | CD74 AC | CD74 ACT | UNIT |
|-----------|------------|------|------|----|------|----|----|---------|---------|----------|-------|---------|----------|------|
| I_{CC} | MAX | 45 | 18 | 96 | 14 | 34 | 34 | 0.08 | 0.16 | 0.16 | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -1 | -0.4 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 16 | 8 | 20 | 8 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | LV 3V | LV 5V | UNIT |
|-----------|------------|-------|-------|------|
| I_{CC} | MAX | - | 0.02 | mA |
| I_{OH} | MAX | -6 | -12 | mA |
| I_{OL} | MAX | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | AS | F | SN74 HC | CD74 HC |
|-----------|---------------------------|----------------------|------------|-----|----|----|-----|-----|-----|---------|---------|
| f_{max} | | | MIN | 25 | 30 | 75 | 50 | 100 | 100 | 25 | 20 |
| t_w | \overline{CLR} (MR) LOW | CLK (CP) HIGH | MIN | 20 | 20 | 10 | 10 | 5 | 5 | 20 | 24 |
| | | | | 20 | 20 | 7 | 10 | 4 | 4 | 20 | 24 |
| | | | | 20 | 20 | 7 | 10 | 5 | 5 | 20 | 24 |
| t_{su} | DATA INPUT | CLR (MR) INACTIVE | MIN | 20 | 20 | 5 | 10 | 3 | 3 | 25 | 24 |
| | | | | 25 | 25 | 5 | 6 | 6 | 5 | 25 | - |
| t_h | | | MIN | 5 | 5 | 3 | 0 | 1 | 1 | 0 | 5 |
| t_{PLH} | \overline{CLR} (MR) | ANY Q or \bar{Q} | MAX | 25 | 30 | 15 | 18 | 9 | 9 | 38 | 53 |
| t_{PHL} | \overline{CLR} (MR) | ANY Q or \bar{Q} | MAX | 35 | 30 | 22 | 23 | 13 | 13 | 38 | 53 |
| t_{PLH} | CLK (CP) | ANY Q or \bar{Q} | MAX | 30 | 25 | 12 | 15 | 7.5 | 7.5 | 38 | 53 |
| t_{PHL} | CLK (CP) | ANY Q or \bar{Q} | MAX | 35 | 25 | 17 | 17 | 10 | 9.5 | 38 | 53 |

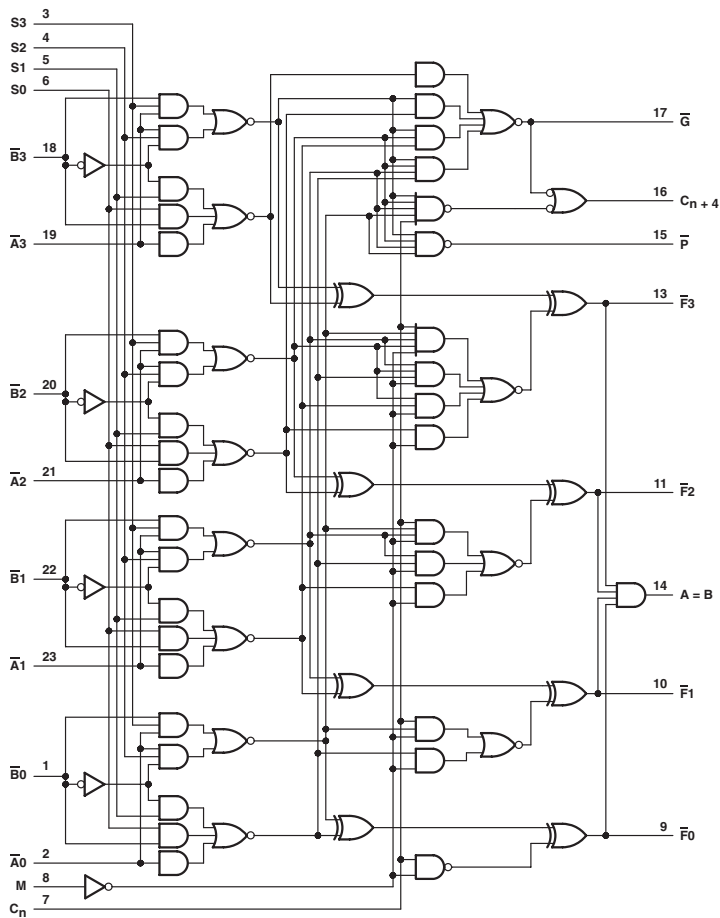
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | AC 11 | CD74 AC | CD74 ACT | LV 3V | LV 5V |
|-----------|---------------------------|--------------------------------|------------|----------|-------|---------|----------|-------|-------|
| f_{max} | | | MIN | 16 | 125 | 100 | 114 | 45 | 75 |
| t_w | \overline{CLR} (MR) LOW | CLK (CP) HIGH | MIN | 30 | 4 | 4 | 4 | 5 | 5 |
| | | | | 30 | 4 | 5 | 5 | 5 | 5 |
| | | | | 30 | 4 | 5 | 5 | 5 | 5 |
| t_{su} | DATA INPUT | \overline{CLR} (MR) INACTIVE | MIN | 30 | 5.5 | 2 | 2 | 5 | 4 |
| | | | | - | 5.5 | - | - | 5 | 5 |
| t_h | | | MIN | 5 | 0.5 | 2 | 2 | 1 | 1 |
| t_{PLH} | \overline{CLR} (MR) | ANY Q or \bar{Q} | MAX | 53 | 6.8 | 12.2 | 13 | 15.5 | 9.5 |
| t_{PHL} | \overline{CLR} (MR) | ANY Q or \bar{Q} | MAX | 53 | 9.3 | 12.2 | 13 | 15.5 | 9.5 |
| t_{PLH} | CLK (CP) | ANY Q or \bar{Q} | MAX | 50 | 6.9 | 12.2 | 11.5 | 17 | 10.5 |
| t_{PHL} | CLK (CP) | ANY Q or \bar{Q} | MAX | 50 | 9.3 | 12.2 | 11.5 | 17 | 10.5 |

UNIT f_{max} : MHz, other : ns

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects

Logic Diagram



FUNCTION TABLE (ACTIVE LOW)

| SELECTION | ACTIVE-LOW DATA | | |
|-----------|----------------------------|----------------------------------|------------------------------------|
| | M = H LOGIC FUNCTION | M = L: ARITHMETIC OPERATIONS | |
| | | C _n = L (no carry) | C _n = H (with carry) |
| L L L L | $F = \overline{A}$ | F = A MINUS 1 | F = A |
| L L L H | $F = \overline{AB}$ | F = AB MINUS 1 | F = AB |
| L L H L | $F = \overline{A+B}$ | F = AB MINUS 1 | F = AB |
| L L H H | F = 1 | F = MINUS 1(2's COMP) | F = 0 |
| L H L L | $F = \overline{A+B}$ | F = A PLUS (A + B) | F = A PLUS (A + B) PLUS 1 |
| L H L H | $F = \overline{B}$ | F = AB PLUS (A + B) | F = AB PLUS (A + B) PLUS 1 |
| L H H L | $F = \overline{A \odot B}$ | F = A MINUS B MINUS 1 | F = A MINUS B |
| L H H H | $F = \overline{A+B}$ | F = A + B | F = (A + B) PLUS 1 |
| H L L L | $F = \overline{AB}$ | F = A PLUS (A + B) | F = A PLUS (A + B) PLUS 1 |
| H L L H | $F = \overline{A \odot B}$ | F = A PLUS B | F = A PLUS B PLUS 1 |
| H L H L | F = B | F = AB PLUS (A + B) | F = AB PLUS (A + B) PLUS 1 |
| H L H H | F = A + B | F = (A + B) | F = (A + B) PLUS 1 |
| H H L L | F = 0 | F = A PLUS A* | F = A PLUS A PLUS 1 |
| H H L H | $F = \overline{AB}$ | F = AB PLUS A | F = AB PLUS A PLUS 1 |
| H H H L | $F = \overline{AB}$ | F = AB PLUS A | F = AB PLUS A PLUS 1 |
| H H H H | F = A | F = A | F = A PLUS 1 |

*Each bit is shifted to the next more significant position.

FUNCTION TABLE (ACTIVE HIGH)

| SELECTION | ACTIVE-HIGH DATA | | |
|-----------|----------------------------|----------------------------------|------------------------------------|
| | M = H LOGIC FUNCTION | M = L: ARITHMETIC OPERATIONS | |
| | | C _n = H (no carry) | C _n = L (with carry) |
| L L L L | F = A | F = A | F = A PLUS 1 |
| L L L H | $F = \overline{A+B}$ | F = A + B | F = (A + B) PLUS 1 |
| L L H L | $F = \overline{AB}$ | F = A + B | F = (A + B) PLUS 1 |
| L L H H | F = 0 | F = MINUS 1(2's COMPL) | F = 0 |
| L H L L | $F = \overline{AB}$ | F = A PLUS AB | F = A PLUS AB PLUS 1 |
| L H L H | $F = \overline{B}$ | F = (A + B) PLUS AB | F = (A + B) PLUS AB PLUS 1 |
| L H H L | $F = \overline{A \odot B}$ | F = A MINUS B MINUS 1 | F = A MINUS B |
| L H H H | $F = \overline{AB}$ | F = AB MINUS 1 | F = AB |
| H L L L | $F = \overline{A+B}$ | F = A PLUS AB | F = A PLUS AB PLUS 1 |
| H L L H | $F = \overline{A \odot B}$ | F = A PLUS B | F = A PLUS B PLUS 1 |
| H L H L | F = B | F = (A + B) PLUS AB | F = (A + B) PLUS AB PLUS 1 |
| H L H H | F = AB | F = AB MINUS 1 | F = AB |
| H H L L | F = 1 | F = A PLUS A* | F = A PLUS A PLUS 1 |
| H H L H | $F = \overline{AB}$ | F = (A + B) PLUS A | F = (A + B) PLUS A PLUS 1 |
| H H H L | $F = \overline{AB}$ | F = (A + B) PLUS A | F = (A + B) PLUS A PLUS 1 |
| H H H H | F = A | F = A MINUS 1 | F = A |

*Each bit is shifted to the next more significant position.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | TTL | LS | S | AS | UNIT |
|-----------------|---|------------|------|------|-----|-----|------|
| I _{CC} | | MAX | 150 | 37 | 220 | 200 | mA |
| I _{OH} | All outputs except \overline{A} , \overline{B} \overline{G} | MAX | -0.8 | -0.4 | -1 | -2 | mA |
| | | | - | - | - | -3 | mA |
| I _{OL} | All outputs except \overline{G} | MAX | 16 | 8 | 20 | 20 | mA |
| | | | 16 | 8 | 20 | 48 | mA |

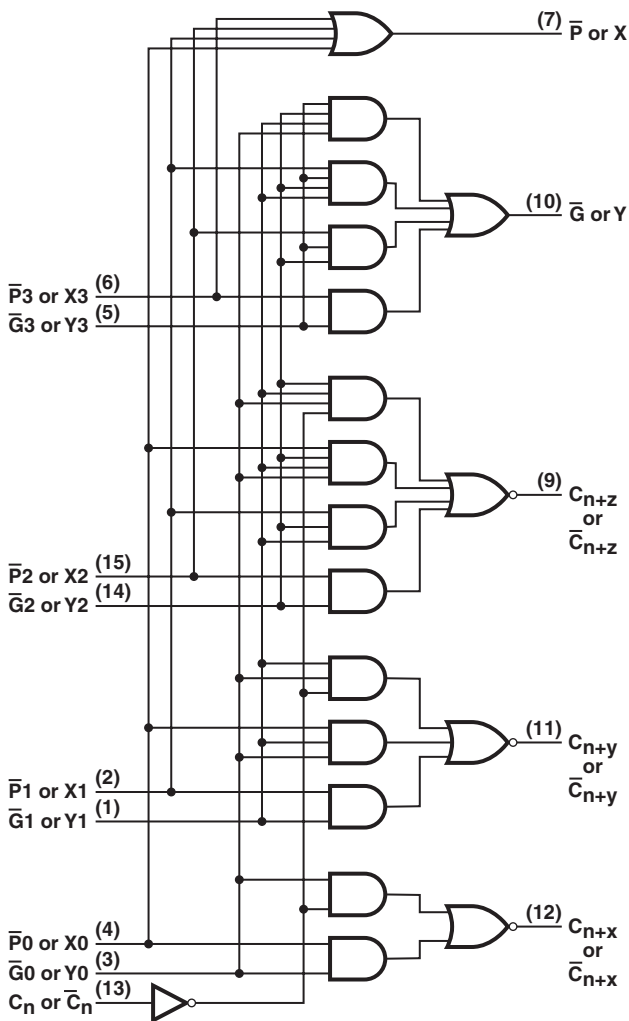
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | AS |
|------------------|-------------------------------------|--------------------|------------|-----|----|------|-----|
| t _{PLH} | C _n | C _n + 4 | MAX | 18 | 27 | 10.5 | 9 |
| | | | | 19 | 20 | 10.5 | 9 |
| t _{PLH} | \overline{A} , \overline{B} | C _n + 4 | MAX | 43 | 38 | 18.5 | 12 |
| | | | | 41 | 38 | 18.5 | 12 |
| t _{PLH} | C _n | \overline{F} | MAX | 19 | 26 | 12 | 9 |
| | | | | 18 | 20 | 12 | 9 |
| t _{PLH} | \overline{A}_1 , \overline{B}_1 | \overline{F}_1 | MAX | 42 | 32 | 16.5 | 9.5 |
| | | | | 32 | 20 | 16.5 | 8 |

UNIT: ns

LOOK-AHEAD CARRY GENERATOR

Logic Diagram



FUNCTION TABLE

\bar{G} OUTPUTS

| INPUTS | | | | | | OUTPUT | |
|------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------|
| \bar{G}_3 | \bar{G}_2 | \bar{G}_1 | \bar{P}_3 | \bar{P}_2 | \bar{P}_1 | \bar{P}_0 | \bar{G} |
| L | X | X | X | X | X | X | L |
| X | L | X | X | L | X | X | L |
| X | X | L | X | L | L | X | L |
| X | X | X | L | L | L | L | L |
| All other combinations | | | | | | | H |

\bar{P} OUTPUTS

| INPUTS | | | | OUTPUT |
|------------------------|-------------|-------------|-------------|-----------|
| \bar{P}_3 | \bar{P}_2 | \bar{P}_1 | \bar{P}_0 | \bar{P} |
| L | L | L | L | L |
| All other combinations | | | | H |

C_{n+x} OUTPUTS

| INPUTS | | | OUTPUT |
|------------------------|-------------|-------|-----------|
| \bar{G}_0 | \bar{P}_0 | C_n | C_{n+x} |
| L | X | X | H |
| X | L | H | H |
| All other combinations | | | L |

C_{n+y} OUTPUTS

| INPUTS | | | | | OUTPUT |
|------------------------|-------------|-------------|-------------|-------|-----------|
| \bar{G}_1 | \bar{G}_0 | \bar{P}_1 | \bar{P}_0 | C_n | C_{n+y} |
| L | X | X | X | X | H |
| X | L | L | X | X | H |
| X | X | L | L | H | H |
| All other combinations | | | | | L |

C_{n+z} OUTPUTS

| INPUTS | | | | | | OUTPUT | |
|------------------------|-------------|-------------|-------------|-------------|-------------|--------|-----------|
| \bar{G}_2 | \bar{G}_1 | \bar{G}_0 | \bar{P}_2 | \bar{P}_1 | \bar{P}_0 | C_n | C_{n+z} |
| L | X | X | X | X | X | X | H |
| X | L | X | L | X | X | X | H |
| X | X | L | L | L | X | X | H |
| X | X | X | L | L | L | H | H |
| All other combinations | | | | | | | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | S | AS | UNIT |
|-----------|------------|------|-----|----|------|
| I_{CC} | MAX | 72 | 109 | 36 | mA |
| I_{OH} | MAX | -0.8 | -1 | -2 | mA |
| I_{OL} | MAX | 16 | 20 | 20 | mA |

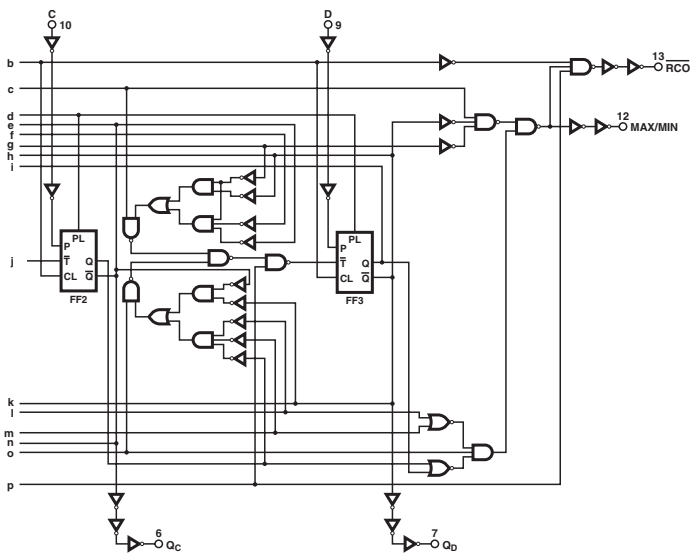
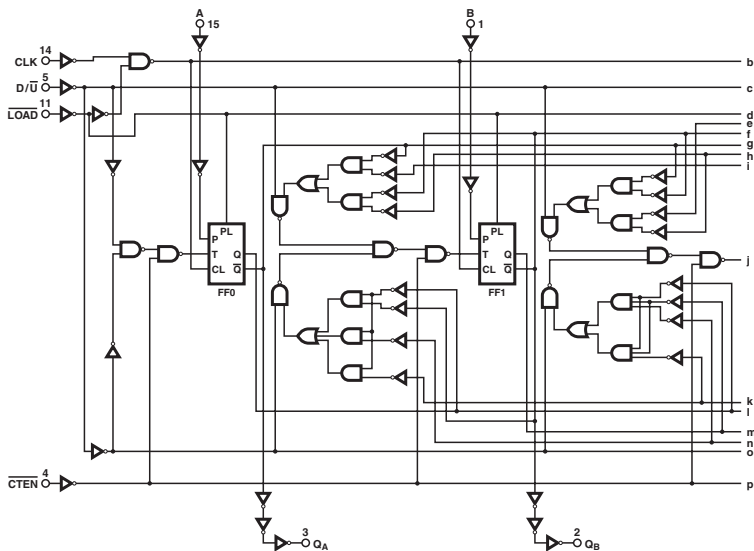
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | S | AS |
|-----------|------------------|------------------------------------|------------|------|------|------|
| t_{PLH} | C_n | $C_n + X, C_n + Y$ or $C_n + Z$ | MAX | 10 | 10 | 10 |
| t_{PHL} | | | | 10.5 | 10.5 | 9.5 |
| t_{PLH} | P or \bar{G} | $C_n + X, C_n + Y$ or $C_n + Z$ | MAX | 7 | 7 | 10.5 |
| t_{PHL} | | | | 7 | 7 | 6 |
| t_{PLH} | P or \bar{G} | \bar{G} | MAX | 7.5 | 7.5 | 12 |
| t_{PHL} | | | | 10.5 | 10.5 | 8 |
| t_{PLH} | \bar{P} | \bar{P} | MAX | 6.5 | 6.5 | 7.5 |
| t_{PHL} | | | | 10 | 10 | 6 |

UNIT: ns

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | FUNCTION |
|--------|------|--------------|-----------------------|---------------------|
| LOAD | CTEN | D/ \bar{U} | CLK | |
| H | L | L | $\overline{\text{J}}$ | Count up |
| H | L | H | $\overline{\text{J}}$ | Count down |
| L | X | X | X | Asynchronous preset |
| H | H | X | X | No change |

D/ \bar{U} or CTEN should be changed only when clock is high.

X = Don't care

$\overline{\text{J}}$ Low-to-high clock transition

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|------|------|------|---------|---------|------|
| I _{CC} | MAX | 105 | 35 | 22 | 0.08 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

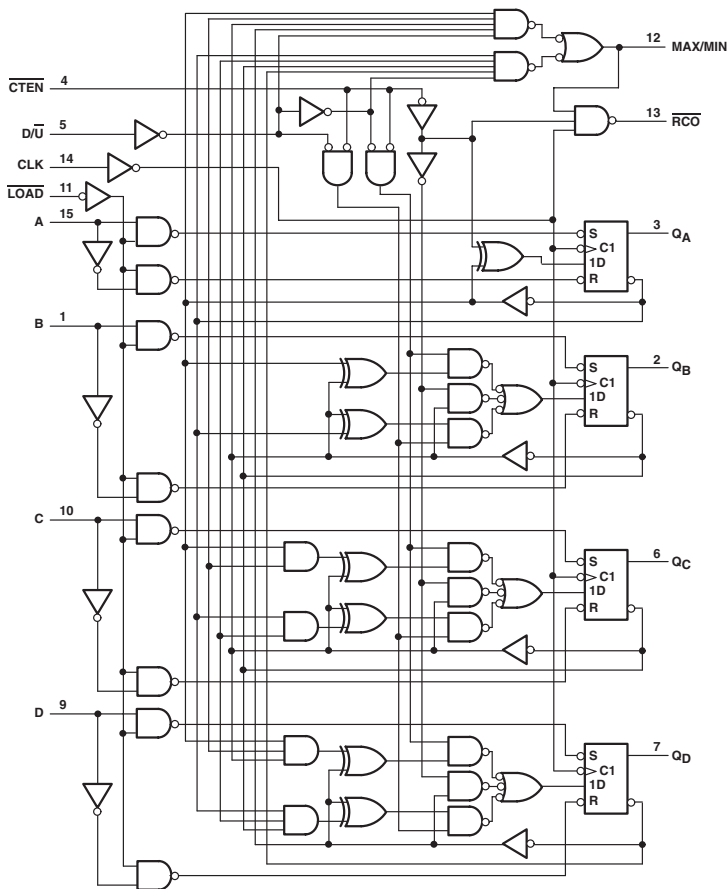
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC |
|------------------|--------------------------|-------------------------|------------|-----|----|-----|---------|---------|
| f _{max} | | | MIN | 20 | 20 | 25 | 17 | 20 |
| t _w | CLK | | MIN | 25 | 25 | 20 | 30 | 30 |
| | LOAD | | | 35 | 35 | 20 | 30 | 24 |
| t _{su} | Data, high or low | | MIN | 20 | 20 | 20 | 38 | 18 |
| t _h | Data hold time | | MIN | 0 | 5 | 5 | 5 | 2 |
| t _{PLH} | $\overline{\text{LOAD}}$ | Q | MAX | 33 | 33 | 30 | 66 | 59 |
| | | | | 50 | 50 | 30 | 66 | 59 |
| t _{PHL} | DATA | Q | MAX | 22 | 32 | 21 | 60 | 53 |
| | | | | 50 | 40 | 21 | 60 | 53 |
| t _{PLH} | CLK | $\overline{\text{RCO}}$ | MAX | 20 | 20 | 20 | 30 | 38 |
| | | | | 24 | 24 | 20 | 30 | 38 |
| t _{PHL} | CLK | Q | MAX | 24 | 24 | 18 | 48 | 51 |
| | | | | 36 | 36 | 18 | 48 | 51 |
| t _{PLH} | CLK | MAX/MIN | MAX | 42 | 42 | 31 | 63 | 63 |
| | | | | 52 | 52 | 31 | 63 | 63 |
| t _{PHL} | D/ \bar{U} | $\overline{\text{RCO}}$ | MAX | 45 | 45 | 37 | 57 | 45 |
| | | | | 45 | 45 | 28 | 57 | 45 |
| t _{PLH} | D/ \bar{U} | MAX/ MIN | MAX | 33 | 33 | 25 | 48 | 50 |
| | | | | 33 | 33 | 25 | 48 | 50 |

UNIT f_{max} : MHz other : ns

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control

Logic Diagram (SN74HC)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 105 | 35 | 22 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -0.4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 4 | 4 | 4 | mA |

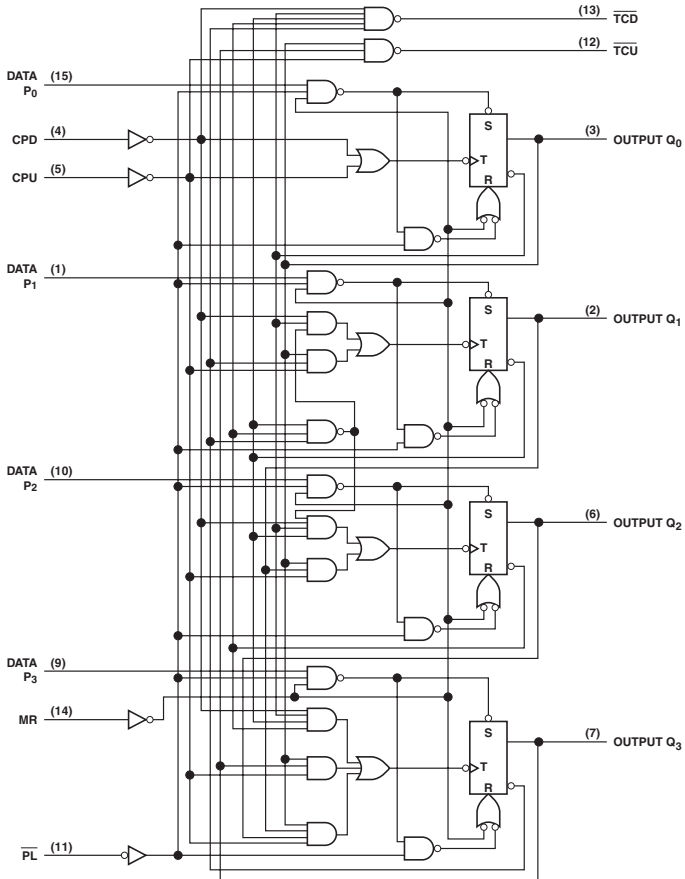
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------------------|------------------|------------|-----|----|------|---------|---------|----------|
| f _{max} | | | MIN | 20 | 20 | 30 | 17 | 20 | 20 |
| t _w | CLK | | MIN | 25 | 25 | 16.5 | 30 | 30 | 30 |
| | LOAD low | | | 35 | 35 | 20 | 30 | 24 | 24 |
| t _{su} | DATA | | MIN | 20 | 20 | 20 | 38 | 18 | 18 |
| t _h | DATA | | MIN | 0 | 5 | 5 | 5 | 2 | 2 |
| t _{PLH} | LOAD | QA, QB QC, QD | MAX | 33 | 33 | 30 | 66 | 59 | 60 |
| t _{PHL} | | | | 50 | 50 | 30 | 66 | 59 | 60 |
| t _{PLH} | DATA A, B, C, D | QA, QB QC, QD | MAX | 22 | 32 | 21 | 60 | 53 | 57 |
| t _{PHL} | | | | 50 | 40 | 21 | 60 | 53 | 57 |
| t _{PLH} | CLK | RIPPLE CLK | MAX | 20 | 20 | 20 | 30 | 38 | 53 |
| t _{PHL} | | | | 24 | 24 | 20 | 30 | 38 | 53 |
| t _{PLH} | CLK | QA, QB QC, QD | MAX | 24 | 24 | 18 | 48 | 51 | 41 |
| t _{PHL} | | | | 36 | 36 | 18 | 48 | 51 | 41 |
| t _{PLH} | CLK | MAX or MIN | MAX | 42 | 42 | 31 | 63 | 63 | 63 |
| t _{PHL} | | | | 52 | 52 | 31 | 63 | 63 | 63 |
| t _{PLH} | D \bar{U} | RIPPLE CLK | MAX | 45 | 45 | 37 | 57 | 45 | 45 |
| t _{PHL} | | | | 45 | 45 | 28 | 57 | 45 | 45 |
| t _{PLH} | D \bar{U} | MAX or MIN | MAX | 33 | 33 | 25 | 48 | 50 | 57 |
| t _{PHL} | | | | 33 | 33 | 25 | 48 | 50 | 57 |

UNIT f_{max} : MHz, other : ns

PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Logic Diagram



TRUE TABLE

| CLOCK UP | CLOCK DOWN | RESET | PARALLEL LOAD | FANCTION |
|----------|------------|-------|---------------|--------------------|
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Reset |
| X | X | L | L | Load Preset inputs |

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------------|------------|---------|------|
| I _{CC} | MAX | 0.16 | mA |
| I _{OH} | MAX | -4 | mA |
| I _{OL} | MAX | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

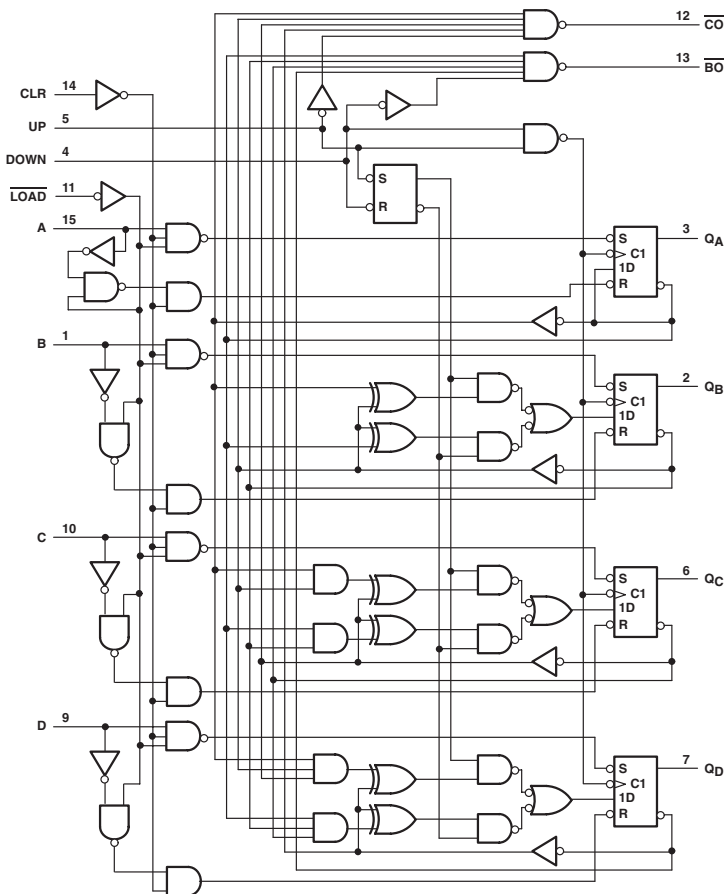
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|------------------|------------------------|----------------|------------|------------------|
| t _w | CPU, CPD | | MIN | 35 |
| | PL | | | 24 |
| | MR | | | 30 |
| t _{su} | P _n to PL | | MIN | 24 |
| t _h | P _n to PL | | MIN | 0 |
| | CPD to CPU, CPD to CPU | | | 24 |
| | t _{PLH} | CPU | | TCU |
| t _{PHL} | | | 38 | |
| t _{PLH} | CPD | TCD | MAX | 38 |
| | | | | t _{PHL} |
| t _{PLH} | CPU | Q _n | MAX | 65 |
| | | | | t _{PHL} |
| t _{PLH} | CPD | Q _n | MAX | 65 |
| | | | | t _{PHL} |
| t _{PLH} | PL | Q _n | MAX | 66 |
| | | | | t _{PHL} |
| t _{PHL} | MR | Q _n | MAX | 60 |

UNIT:ns

4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | F | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|------|----|---------|---------|----------|------|
| I _{CC} | MAX | 102 | 34 | 22 | 54 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.4 | -0.4 | -0.4 | -1 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 8 | 20 | 4 | 4 | 4 | mA |

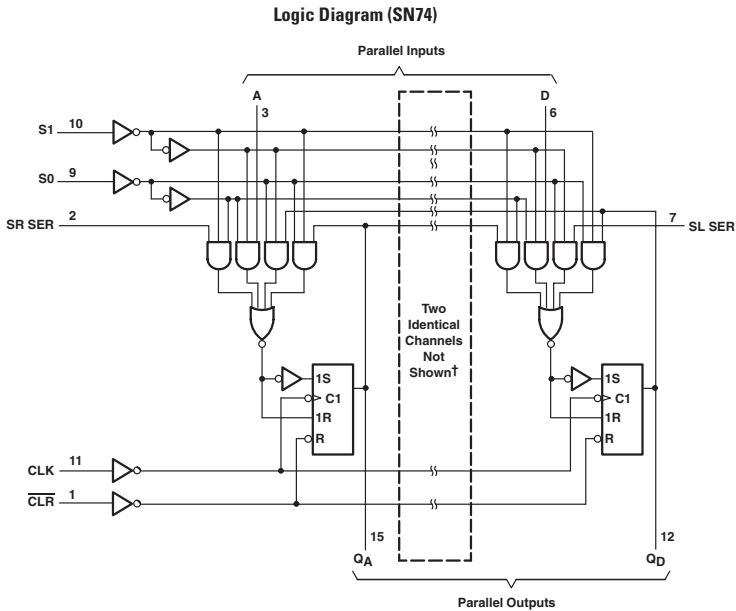
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | F | SN74 HC | CD74 HC | CD74 HCT | |
|------------------|----------------------------------|-----------------|------------|-----|----|-----|----|---------|---------|----------|----|
| f _{max} | | | MIN | 25 | 25 | 30 | 85 | 17 | 17 | 15 | |
| t _w | | | MIN | 20 | 20 | 20 | 4 | 30 | 30 | 35 | |
| t _{su} | | | DATA | MIN | 20 | 20 | 20 | 3.5 | 28 | 22 | 22 |
| t _h | | | DATA | MIN | 0 | 5 | 5 | 2.5 | 5 | 0 | 0 |
| t _{PLH} | UP (CD74: CPU) | \overline{CO} | MAX | 26 | 26 | 16 | 9 | 41 | 38 | 41 | |
| t _{PHL} | | | | 24 | 24 | 18 | 9 | 41 | 38 | 41 | |
| t _{PLH} | DOWN (CD74: CPD) | \overline{BO} | MAX | 24 | 24 | 16 | 9 | 41 | 38 | 41 | |
| t _{PHL} | | | | 24 | 24 | 18 | 9 | 41 | 38 | 41 | |
| t _{PLH} | UP or DOWN (CD74: CPU or CPD) | ANY Q | MAX | 38 | 38 | 19 | 9 | 63 | 65 | 60 | |
| t _{PHL} | | | | 47 | 47 | 17 | 13 | 63 | 65 | 60 | |
| t _{PLH} | LOAD (CD74: PL) | ANY Q | MAX | 40 | 40 | 30 | 11 | 65 | 66 | 69 | |
| t _{PHL} | | | | 40 | 40 | 28 | 13 | 65 | 66 | 69 | |
| t _{PHL} | CLR (CD74: MR) | ANY Q | MAX | 35 | 35 | 17 | 12 | 60 | 60 | 65 | |

UNIT f_{max} : MHz, other : ns

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts



† I/O ports not shown: Q_B (14) and Q_C (13)

FUNCTION TABLE (SN74)

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|--------|------|----|-------|--------|-------|----------|---|---|---|-----------------|-----------------|-----------------|-----------------|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | Q _A | Q _B | Q _C | Q _D |
| | S1 | S0 | | LEFT | RIGHT | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | X | X | X | X | H | Q _{An} | Q _{Bn} | Q _{Cn} |
| H | L | H | ↑ | X | L | X | X | X | X | L | Q _{An} | Q _{Bn} | Q _{Cn} |
| H | H | L | ↑ | H | X | X | X | X | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | H |
| H | H | L | ↑ | L | X | X | X | X | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | L |
| H | L | L | X | X | X | X | X | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | AS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|-----|----|---------|---------|----------|------|
| I _{CC} | MAX | 63 | 23 | 135 | 53 | 0.1 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -2 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 20 | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

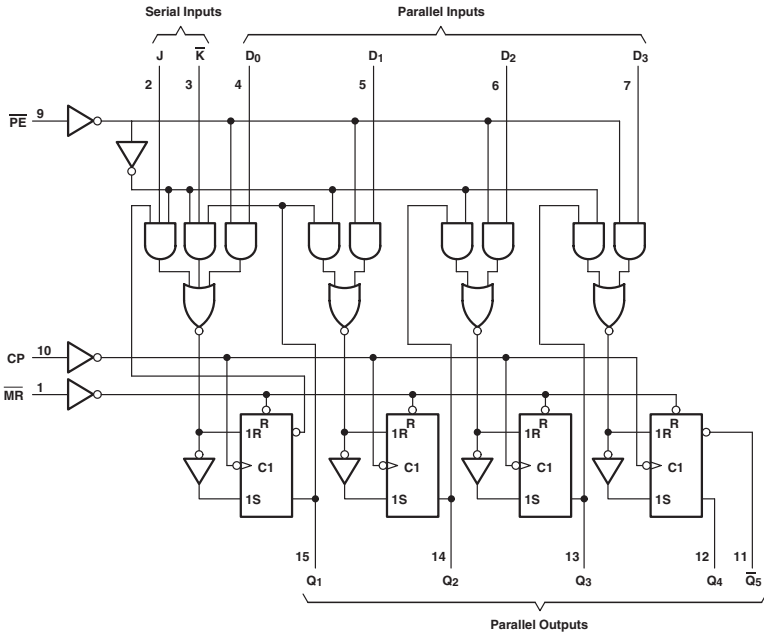
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | AS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--|--------|------------|-----|----|------|-----|---------|---------|----------|
| f _{max} | | | MIN | 25 | 25 | 70 | 80 | 25 | 20 | 18 |
| t _w | $\overline{\text{CLR}}$ (MR) CLK (CP) "H" CLK (CP) "L" | | MIN | 20 | 20 | 12 | 4.5 | 20 | 24 | 24 |
| | | | | 20 | 20 | 7 | 4 | 20 | 24 | 24 |
| | | | | 20 | 20 | 7 | 7 | 20 | 24 | 24 |
| t _{su} | Mode Control DATA CLR (MR) INACTIVE | | MIN | 30 | 30 | 11 | 9.5 | 25 | 24 | 30 |
| | | | | 20 | 20 | 5 | 4 | 25 | 21 | 21 |
| | | | | 25 | 25 | 9 | 6 | - | - | - |
| t _h | | | MIN | 0 | 0 | 3 | 0.5 | 0 | 0 | 0 |
| t _{PHL} | $\overline{\text{CLEAR}}$ (MR) | ANY | MAX | 30 | 30 | 18.5 | 12 | 38 | 42 | 60 |
| t _{PLH} | CLOCK (CP) | ANY | MAX | 22 | 22 | 12 | 7 | 36 | 53 | 56 |
| | | | | 26 | 26 | 16.5 | 7 | 36 | 53 | 56 |

 UNIT f_{max} : MHz, other : ns

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



TRUTH TABLE

| OPERATING MODES | INPUTS | | | | | | OUTPUT | | | | |
|---------------------------|-----------------|----|-----------------|---|----------------|----|----------------|----------------|----------------|----------------|------------------|
| | \overline{MR} | CP | \overline{PE} | J | \overline{K} | Dn | Q ₀ | Q ₁ | Q ₂ | Q ₃ | \overline{Q}_3 |
| Asynchronous Reset | L | X | X | X | X | X | L | L | L | L | H |
| Shift, Set First Stage | H | ↑ | h | h | h | X | H | q ₀ | q ₁ | q ₂ | \overline{q}_2 |
| Shift, Reset First Stage | H | ↑ | h | l | l | X | L | q ₀ | q ₁ | q ₂ | \overline{q}_2 |
| Shift, Toggle First Stage | H | ↑ | h | h | l | X | q ₀ | q ₀ | q ₁ | q ₂ | \overline{q}_2 |
| Shift, Retain First Stage | H | ↑ | h | l | h | X | q ₀ | q ₀ | q ₁ | q ₂ | \overline{q}_2 |
| Parallel Load | H | ↑ | l | X | X | dn | d ₀ | d ₁ | d ₂ | d ₃ | \overline{d}_2 |

H = High Voltage Level

L = Low Voltage Level,

X = Don't Care

↑ = Transition from Low to High Level

l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,

dn (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | AS | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|------|------|-----|----|---------|---------|------|
| I _{CC} | MAX | 63 | 21 | 109 | 57 | 0.1 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -1 | -2 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 20 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

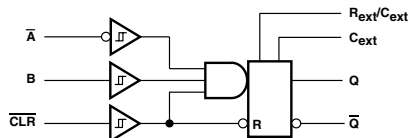
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | AS | SN74 HC | CD74 HC | |
|------------------|-------|-----------------|--------|------------|------------------------|------|------|------|---------|---------|---|
| f _{max} | | | | MIN | 30 | 30 | 70 | 70 | 25 | 20 | |
| t _w | Clock | \overline{MR} | | MIN | 16 | 16 | 7 | 4 | 20 | 24 | |
| | | | | | 12 | 12 | 12 | 7.2 | 20 | 24 | |
| t _{su} | | \overline{PE} | | MIN | 25 | 25 | 11 | 8 | 25 | 30 | |
| | | | | | Serial & Parallel Data | 20 | 15 | 5 | 3.5 | 25 | - |
| | | | | | Clear Inactive Data | 25 | 25 | 9 | 6 | 25 | - |
| | | | | | TRELEASE | MAX | 10 | 20 | 6 | - | - |
| t _h | | | | MIN | 0 | 0 | 3 | 1 | 0 | 3 | |
| t _{PHL} | | \overline{MR} | QA, QD | MAX | 30 | 30 | 18.5 | 11.5 | 38 | 45 | |
| t _{PLH} | Clock | MAX | | 22 | 22 | 12 | 8.5 | 36 | 53 | | |
| t _{PHL} | | MAX | | 26 | 26 | 16.5 | 10.5 | 36 | 53 | | |

UNIT f_{max} : MHz, other : ns

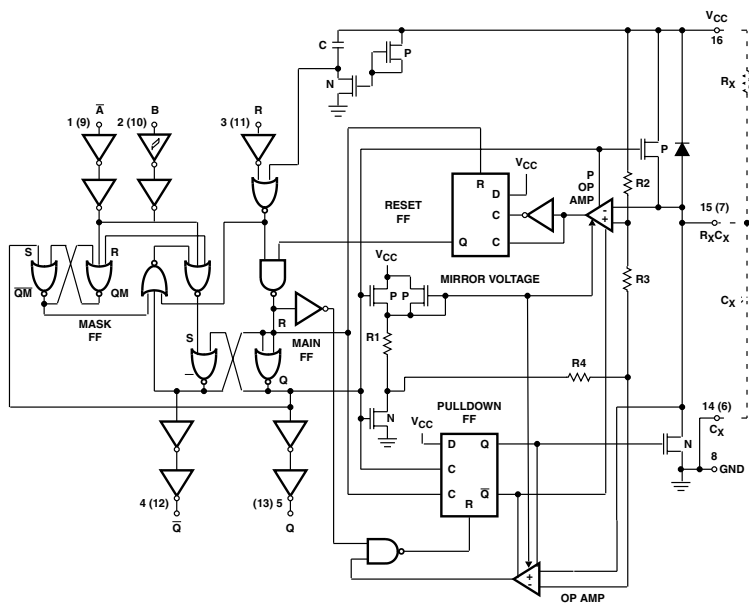
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Overriding Clear Terminates Outputs Pulse

Logic Diagram (SN74LV)



Logic Diagram (CD74HC/HCT)



FUNCTION TABLE
(each monostable multivibrator)

| INPUTS | | | OUTPUTS | |
|----------------|---|---|--------------|--------------|
| CLR | A | B | Q | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | \uparrow | \downarrow |
| H | ↓ | H | \downarrow | \uparrow |
| ↑ [†] | L | H | \downarrow | \uparrow |

[†] Pulsed-output patterns are tested during AC switching at 25°C with $R_{ext} = 2\text{ k}\Omega$ and $C_{ext} = 80\text{ pF}$.

[‡] This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to CLR going high. This latch is conditioned by taking either A high or B low while CLR is inactive (high).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

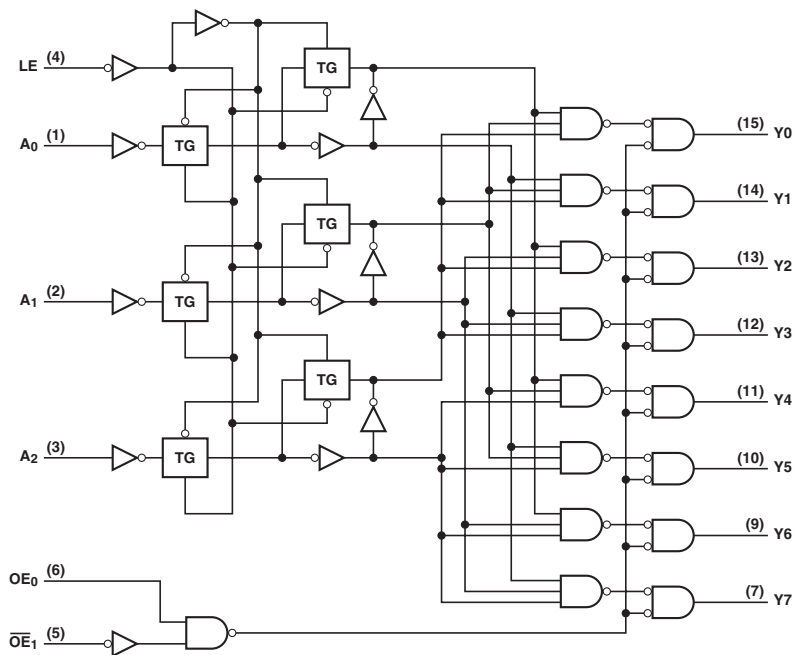
| PARAMETER | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|---------|----------|-------|-------|------|
| I_{CC} | MAX | 80 | 27 | 0.16 | 0.16 | 0.28 | 0.65 | mA |
| I_{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -6 | -12 | mA |
| I_{OL} | MAX | 16 | 8 | 4 | 4 | 6 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|-----------|------------------------|-----------|------------|-----|----|---------|----------|-------|-------|
| t_{PLH} | A (HC, LV: \bar{A}) | Q | MAX | 70 | 70 | 63 | 63 | 27.5 | 16 |
| | B | | | 55 | 55 | 63 | 63 | 27.5 | 16 |
| t_{PHL} | A (HC, LV: \bar{A}) | \bar{Q} | MAX | 80 | 80 | 51 | 51 | 27.5 | 16 |
| | B | | | 65 | 65 | 51 | 51 | 27.5 | 16 |
| t_{PHL} | Clear | Q | MAX | 27 | 55 | 48 | 57 | 22 | 13 |
| | | \bar{Q} | | 40 | 65 | 54 | 56 | 22 | 13 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | | |
|--------|-----|-----|----|----|---------|--|----|----|----|----|----|----|----|
| LE | OEO | OE1 | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | L | L | L | L | L | L | L | L |
| X | L | X | X | X | X | L | L | L | L | L | L | L | L |
| L | H | L | L | L | L | H | L | L | L | L | L | L | L |
| L | H | L | L | L | H | L | H | L | L | L | L | L | L |
| L | H | L | L | H | L | L | L | H | L | L | L | L | L |
| L | H | L | L | H | H | L | L | L | H | L | L | L | L |
| L | H | L | H | L | L | L | L | L | L | H | L | L | L |
| L | H | L | H | L | H | L | L | L | L | L | H | L | L |
| L | H | L | H | H | H | L | L | L | L | L | L | L | H |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

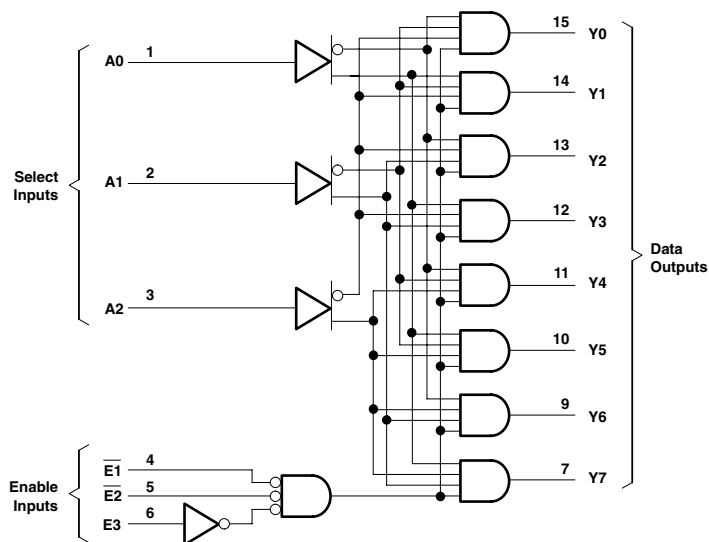
| PARAMETER | MAX or MIN | SN74 | CD74 | CD74 | UNIT |
|-----------------|------------|------|------|------|------|
| | | HC | HC | HCT | |
| I _{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 | CD74 | CD74 |
|------------------|-----------------|--------|------------|------|------|------|
| | | | | HC | HC | HCT |
| t _w | LE Pulse Width | | MIN | 20 | 15 | 15 |
| t _{su} | An to LE | | MIN | 19 | 15 | 15 |
| t _h | An to LE | | MIN | 5 | 9 | 5 |
| t _{PLH} | An | Y | MAX | 48 | 48 | 57 |
| t _{PHL} | | | | 48 | 48 | 57 |
| t _{PLH} | OE ₀ | Y | MAX | 44 | 44 | 60 |
| t _{PHL} | | | | 44 | 44 | 60 |
| t _{PLH} | OE ₁ | Y | MAX | 44 | 44 | 53 |
| t _{PHL} | | | | 44 | 44 | 53 |

UNIT:ns

Logic Diagram (CD74AC/ACT)



FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|----|----|---------|----|----|---------|----|----|----|----|----|----|----|
| ENABLE | | | ADDRESS | | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| E3 | E2 | E1 | A2 | A1 | A0 | | | | | | | | |
| X | X | H | X | X | X | L | L | L | L | L | L | L | L |
| L | X | X | X | X | X | L | L | L | L | L | L | L | L |
| X | H | X | X | X | X | L | L | L | L | L | L | L | L |
| H | L | L | L | L | L | H | L | L | L | L | L | L | L |
| H | L | L | L | L | H | L | L | L | L | L | L | L | L |
| H | L | L | L | H | L | L | L | L | H | L | L | L | L |
| H | L | L | L | H | H | L | L | L | L | H | L | L | L |
| H | L | L | H | L | L | L | L | L | L | H | L | L | L |
| H | L | L | H | L | H | L | L | L | L | L | H | L | L |
| H | L | L | H | H | L | L | L | L | L | L | L | H | L |
| H | L | L | H | H | H | L | L | L | L | L | L | L | H |

Note: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------|---------|----------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 4 | 4 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

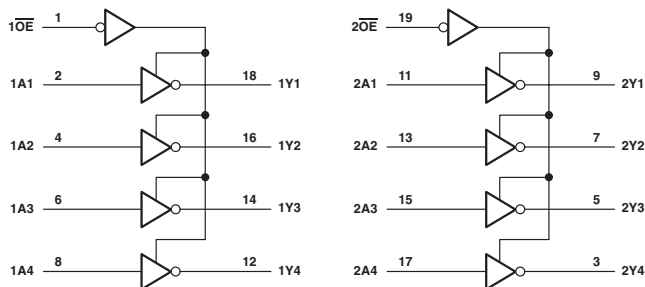
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|------------------|----------------------|--------|------------|---------|----------|---------|----------|
| t _{PLH} | Address | Y | MAX | 45 | 53 | 15 | 15.6 |
| | | | | 45 | 53 | 15 | 15.6 |
| t _{PHL} | E1, E2 (G2A, G2B) | Y | MAX | 60 | 60 | 11.9 | 14.2 |
| | | | | 60 | 60 | 11.9 | 14.2 |
| t _{PLH} | E3 (G1) | Y | MAX | 60 | 60 | 16.6 | 13.6 |
| | | | | 60 | 60 | 16.6 | 13.6 |

UNIT:ns

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT240 T_A : -40 to 85°C

Logic Diagram (SN74)

FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| OE | A | |
| L | H | L |
| L | L | H |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | ALS A-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | UNIT |
|-----------|------------|-----|-----|-----|------------|-----|-----|------------|------------|-------------|-------------|-------------|------|------|
| I_{CC} | MAX | 27 | 135 | 11 | 11 | 17 | 29 | 0.08 | 0.16 | 0.08 | 0.16 | 31 | 0.25 | mA |
| I_{CCL} | MAX | 44 | 150 | 23 | 23 | 75 | 75 | 0.08 | 0.16 | 0.08 | 0.16 | 71 | 30 | mA |
| I_{CCZ} | MAX | 50 | 150 | 25 | 25 | 38 | 63 | 0.08 | 0.16 | 0.08 | 0.16 | 9 | 0.25 | mA |
| I_{OH} | MAX | -15 | -15 | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | mA |
| I_{OL} | MAX | 24 | 64 | 24 | 48 | 64 | 64 | 6 | 6 | 6 | 6 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | LVT 3V | LVTH 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------|------------|-----------|------------|----------|------------|------------|-----------|-------------|-------------|------|------|----------|----------|------|
| I_{CC} | MAX | 0.19 | 0.19 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{CCL} | MAX | 5 | 5 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{CCZ} | MAX | 0.19 | 0.19 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{OH} | MAX | -32 | -32 | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | -16 | mA |
| I_{OL} | MAX | 64 | 64 | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | 16 | mA |

| PARAMETER | MAX or MIN | LVC 3V | LVCZ 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------|------------|-----------|------------|-------------|-------------|--------------|--------------|------|
| I_{CC} | MAX | 0.01 | 0.1 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{CCL} | MAX | 0.01 | 0.1 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{CCZ} | MAX | 0.01 | 0.1 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I_{OL} | MAX | 24 | 24 | 8 | 9 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | ALS A-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|-----------|------------|----------------------|------------|----|----|-----|---------|-----|-----|---------|---------|----------|----------|
| t_{PLH} | A | Y (CD74: \bar{Y}) | MAX | 14 | 7 | 9 | 9 | 6.5 | 8 | 25 | 30 | 32 | 33 |
| t_{PHL} | | | | 18 | 7 | 9 | 9 | 6.5 | 5.7 | 25 | 30 | 32 | 33 |
| t_{PZH} | $\bar{0E}$ | Y (CD74: \bar{Y}) | MAX | 23 | 10 | 13 | 13 | 6.4 | 6.1 | 38 | - | 44 | - |
| t_{PZL} | | | | 30 | 15 | 18 | 18 | 9 | 10 | 38 | - | 44 | - |
| t_{PHZ} | $\bar{0E}$ | Y (CD74: \bar{Y}) | MAX | 25 | 9 | 10 | 10 | 5 | 6.3 | 38 | - | 44 | - |
| t_{PLZ} | | | | 20 | 15 | 12 | 12 | 9.5 | 9.5 | 38 | - | 44 | - |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | ABT | LVT 3V | LVTH 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT |
|-----------|------------|----------------------|------------|----------|-----|--------|---------|-------|---------|---------|--------|----------|----------|
| t_{PLH} | A | Y (CD74: \bar{Y}) | MAX | 5.6 | 4.8 | 3.8 | 3.8 | 8.4 | 7 | 6.5 | 10.6 | 9.5 | 7.8 |
| t_{PHL} | | | | 4 | 4.8 | 4 | 4 | 7.2 | 6.5 | 6.5 | 8.7 | 8.5 | 7.8 |
| t_{PZH} | $\bar{0E}$ | Y (CD74: \bar{Y}) | MAX | 8.8 | 5.2 | 4.6 | 4.6 | 9.2 | 8 | 10.9 | 12.5 | 9.5 | 12.2 |
| t_{PZL} | | | | 10.5 | 6.2 | 4.4 | 4.4 | 8.7 | 8.5 | 10.9 | 12.3 | 10.5 | 12.2 |
| t_{PHZ} | $\bar{0E}$ | Y (CD74: \bar{Y}) | MAX | 8.1 | 6.4 | 4.4 | 4.4 | 6.6 | 9.5 | 10.9 | 10 | 10.5 | 12.2 |
| t_{PLZ} | | | | 9.5 | 5.8 | 4.3 | 4.3 | 7.7 | 9.5 | 10.9 | 10.8 | 10.5 | 12.2 |

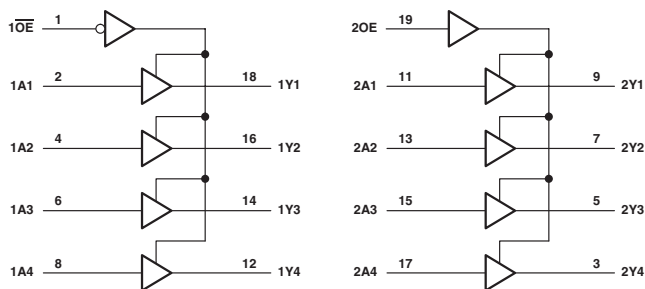
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LV 3V | LV 5V | LVC 3V | LVCZ 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|-----------|------------|--------|------------|------|------|-------|-------|--------|---------|----------|----------|-----------|-----------|
| t_{PLH} | A | Y | MAX | 8.5 | 9.5 | 12.5 | 8.5 | 6.5 | 6.5 | 2.1 | 1.6 | 2.1 | 1.6 |
| t_{PHL} | | | | 8.5 | 9.5 | 12.5 | 8.5 | 6.5 | 6.5 | 2.1 | 1.6 | 2.1 | 1.6 |
| t_{PZH} | $\bar{0E}$ | Y | MAX | 10.5 | 13 | 16 | 10.5 | 8 | 8 | 2.7 | 2 | 2.7 | 2 |
| t_{PZL} | | | | 10.5 | 13 | 16 | 10.5 | 8 | 8 | 2.7 | 2 | 2.7 | 2 |
| t_{PHZ} | $\bar{0E}$ | Y | MAX | 10.5 | 13 | 17 | 15.5 | 7 | 7 | 4 | 2 | 4 | 2 |
| t_{PLZ} | | | | 10.5 | 13 | 17 | 15.5 | 7 | 7 | 4 | 2 | 4 | 2 |

UNIT: ns

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- CD74AC/ACT241 T_A : -40 to 85°C

Logic Diagram (SN74)

FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 BCT | ABT | LVTH 3V | SN74 AC | UNIT |
|-----------------|------------|-----|-----|-----|-----|-----|---------|---------|----------|----------|------|---------|---------|------|
| ICCH | MAX | 27 | 160 | 18 | 35 | 60 | 0.08 | 0.16 | 0.16 | 43 | 0.25 | 0.19 | 0.04 | mA |
| ICCL | MAX | 46 | 180 | 26 | 90 | 90 | 0.08 | 0.16 | 0.16 | 85 | 30 | 5 | 0.04 | mA |
| ICcz | MAX | 54 | 180 | 30 | 56 | 90 | 0.08 | 0.16 | 0.16 | 10 | 0.25 | 0.19 | 0.04 | mA |
| I _{OH} | MAX | -15 | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -15 | -32 | -32 | -24 | mA |
| I _{OL} | MAX | 24 | 64 | 24 | 64 | 64 | 6 | 6 | 6 | 64 | 64 | 64 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 AC | SN74 ACT | CD74 ACT | UNIT |
|-----------------|------------|---------|----------|----------|------|
| ICCH | MAX | 0.16 | 0.04 | 0.08 | mA |
| ICCL | MAX | 0.16 | 0.04 | 0.08 | mA |
| ICcz | MAX | 0.16 | 0.04 | 0.08 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 BCT |
|------------------|------------------|----------------------|------------|----|----|-----|------|-----|---------|---------|----------|----------|
| t _{PLH} | A | Y (CD74: \bar{Y}) | MAX | 18 | 9 | 11 | 6.2 | 6.2 | 29 | 33 | 38 | 4.9 |
| | | | | 18 | 9 | 10 | 6.2 | 6.5 | 29 | 33 | 38 | 5.9 |
| t _{PZH} | $\overline{10E}$ | Y (CD74: \bar{Y}) | MAX | 23 | 12 | 21 | 9 | 6.7 | 38 | - | - | 8.7 |
| | | | | 30 | 15 | 21 | 7.5 | 8 | 38 | - | - | 9.4 |
| t _{PHZ} | $\overline{10E}$ | Y (CD74: \bar{Y}) | MAX | 25 | 9 | 10 | 6 | 7 | 38 | - | - | 8.1 |
| | | | | 20 | 15 | 15 | 9 | 7 | 38 | - | - | 9.9 |
| t _{PZH} | 20E | Y (CD74: \bar{Y}) | MAX | 23 | 12 | 21 | 10.5 | 6.7 | 38 | - | - | 8.7 |
| | | | | 30 | 15 | 21 | 8.5 | 8 | 38 | - | - | 9.4 |
| t _{PHZ} | 20E | Y (CD74: \bar{Y}) | MAX | 25 | 9 | 10 | 7 | 7 | 38 | - | - | 8.1 |
| | | | | 20 | 15 | 15 | 12 | 7 | 38 | - | - | 9.9 |

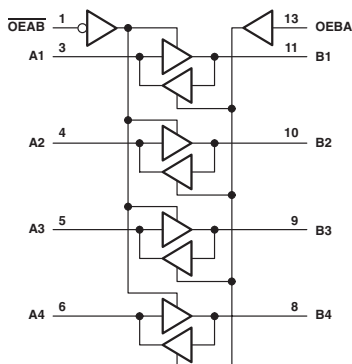
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | SN74 AC | CD74 AC | SN74 ACT | CD74 ACT |
|------------------|------------------|----------------------|------------|-----|---------|---------|---------|----------|----------|
| t _{PLH} | A | Y (CD74: \bar{Y}) | MAX | 4.6 | 3.5 | 7.5 | 7.5 | 9.5 | 8.7 |
| | | | | 4.6 | 3.4 | 7.5 | 7.5 | 8.5 | 8.7 |
| t _{PZH} | $\overline{10E}$ | Y (CD74: \bar{Y}) | MAX | 6.8 | 4.5 | 9.5 | 10.9 | 9.5 | 12.2 |
| | | | | 6.8 | 4.4 | 9.5 | 10.9 | 10.5 | 12.2 |
| t _{PHZ} | $\overline{10E}$ | Y (CD74: \bar{Y}) | MAX | 7.1 | 4.5 | 10.5 | 10.9 | 10.5 | 12.2 |
| | | | | 5.9 | 4.7 | 10.5 | 10.9 | 10.5 | 12.2 |
| t _{PZH} | 20E | Y (CD74: \bar{Y}) | MAX | 6.8 | 4.5 | 9.5 | 10.9 | 9.5 | 12.2 |
| | | | | 6.8 | 4.4 | 9.5 | 10.9 | 10.5 | 12.2 |
| t _{PHZ} | 20E | Y (CD74: \bar{Y}) | MAX | 7.1 | 4.5 | 10.5 | 10.9 | 10.5 | 12.2 |
| | | | | 5.9 | 4.7 | 10.5 | 10.9 | 10.5 | 12.2 |

UNIT: ns

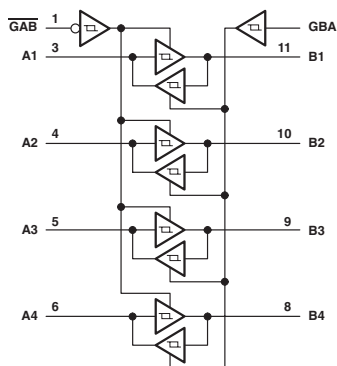
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading

Logic Diagram (SN74ALS)



Logic Diagram (SN74LS)



FUNCTION TABLE (SN74)

| INPUTS | | OPERATION |
|--------------|-----|-----------------------|
| $\bar{G}A$ B | GBA | |
| L | L | A to B |
| H | H | B to A |
| H | L | Isolation |
| L | H | Latch A and B (A = B) |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-------------------|------------|-----|-----|----|---------|---------|----------|------|
| I _{CC} H | MAX | 38 | 25 | 44 | 0.08 | 0.16 | 0.16 | mA |
| I _{CC} L | MAX | 50 | 30 | 74 | 0.08 | 0.16 | 0.16 | mA |
| I _{CC} Z | MAX | 54 | 32 | 56 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -15 | -15 | - | - | -6 | -6 | mA |
| I _{OL} | MAX | 24 | 24 | 64 | 6 | 6 | 6 | mA |

SWITCHING CHARACTERISTICS

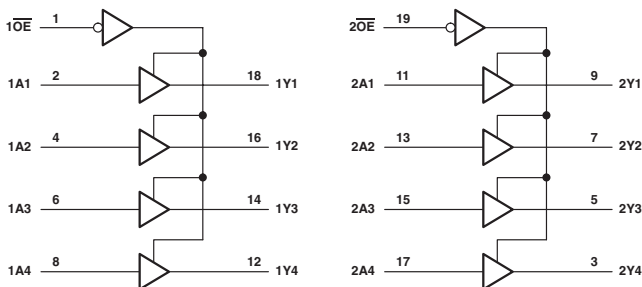
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------------|--------|------------|----|-----|------|---------|---------|----------|
| t _{PLH} | A or B | A or B | MAX | 18 | 11 | 7.5 | 25 | 27 | 33 |
| t _{PHL} | A or B | A or B | MAX | 18 | 11 | 6.5 | 25 | 27 | 33 |
| t _{PZH} | $\bar{G}A$ B | B | MAX | 23 | 20 | 9 | 38 | 45 | 51 |
| t _{PZL} | | | | 30 | 20 | 7.5 | 38 | 45 | 51 |
| t _{PHZ} | $\bar{G}A$ B | B | MAX | 25 | 14 | 6.5 | 38 | 45 | 53 |
| t _{PLZ} | | | | 20 | 22 | 9 | 38 | 45 | 53 |
| t _{PZH} | GAB | A | MAX | 23 | 20 | 10.5 | 38 | 45 | 51 |
| t _{PZL} | | | | 30 | 20 | 8.5 | 38 | 45 | 51 |
| t _{PHZ} | GAB | A | MAX | 25 | 14 | 7 | 38 | 45 | 53 |
| t _{PLZ} | | | | 20 | 22 | 11 | 38 | 45 | 53 |

UNIT: ns

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT244 T_A : -40 to 85°C

Logic Diagram (SN74)

FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | ALS C-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | SN64 BCT | UNIT |
|-----------|------------|-----|-----|-----|------------|-----|-----|------------|------------|-------------|-------------|-------------|-------------|------|
| I_{CC} | MAX | 27 | 160 | 17 | 17 | 34 | 60 | 0.08 | 0.16 | 0.08 | 0.16 | 40 | 40 | mA |
| I_{CCL} | MAX | 46 | 180 | 24 | 24 | 90 | 90 | 0.08 | 0.16 | 0.08 | 0.16 | 80 | 80 | mA |
| I_{CCZ} | MAX | 54 | 180 | 27 | 27 | 54 | 90 | 0.08 | 0.16 | 0.08 | 0.16 | 10 | 10 | mA |
| I_{OH} | MAX | -15 | -15 | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -15 | mA |
| I_{OL} | MAX | 24 | 64 | 24 | 48 | 64 | 64 | 6 | 6 | 6 | 6 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | ABT | LVT 3V | LVTH 3V | LVTZ 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | UNIT |
|-----------|------------|------|-----------|------------|------------|----------|------------|------------|-----------|-------------|-------------|------|------|----------|------|
| I_{CC} | MAX | 0.25 | 0.19 | 0.19 | 0.225 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | mA |
| I_{CCL} | MAX | 30 | 5 | 5 | 15 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | mA |
| I_{CCZ} | MAX | 0.25 | 0.19 | 0.19 | 0.225 | 0.08 | 0.04 | 0.08 | 0.08 | 0.04 | 0.08 | 0.04 | 0.04 | - | mA |
| I_{OH} | MAX | -32 | -32 | -32 | -32 | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | mA |
| I_{OL} | MAX | 64 | 64 | 64 | 64 | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | mA |

| PARAMETER | MAX or MIN | LV 5V | LV-AT 3 | LVC 3V | LVCH 3V | LVCZ 3V | ALVC 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------|------------|----------|------------|-----------|------------|------------|------------|-------------|-------------|-------------|--------------|--------------|------|
| I_{CC} | MAX | 0.02 | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{CCL} | MAX | 0.02 | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{CCZ} | MAX | 0.02 | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I_{OH} | MAX | -16 | -16 | -24 | -24 | -24 | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I_{OL} | MAX | 16 | 16 | 24 | 24 | 24 | 24 | 24 | 8 | 9 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | ALS C-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT |
|-----------|-----------------|--------|------------|----|----|-----|---------|-----|-----|---------|---------|----------|
| t_{PLH} | A | Y | MAX | 18 | 9 | 10 | 10 | 6.2 | 6.2 | 29 | 33 | 35 |
| t_{PHL} | | | | 18 | 9 | 10 | 10 | 6.2 | 6.5 | 29 | 33 | 35 |
| t_{PZH} | $\overline{0E}$ | Y | MAX | 23 | 12 | 20 | 20 | 9 | 6.7 | 38 | - | 44 |
| t_{PZL} | | | | 30 | 15 | 20 | 20 | 7.5 | 8 | 38 | - | 44 |
| t_{PHZ} | $\overline{0E}$ | Y | MAX | 25 | 9 | 10 | 10 | 6 | 7 | 38 | - | 44 |
| t_{PLZ} | | | | 20 | 15 | 13 | 13 | 9 | 7 | 38 | - | 44 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | SN74 BCT | SN64 BCT | ABT | LVT 3V | LVTH 3V | LVTZ 3V | AC 11 | SN74 AC | CD74 AC |
|-----------|-----------------|--------|------------|----------|----------|----------|-----|--------|---------|---------|-------|---------|---------|
| t_{PLH} | A | Y | MAX | 38 | 5 | 5.3 | 4.6 | 3.5 | 3.5 | 4.1 | 7.3 | 7.5 | 7.5 |
| t_{PHL} | | | | 38 | 5.5 | 6 | 4.6 | 3.3 | 3.3 | 4.1 | 6.9 | 7.5 | 7.5 |
| t_{PZH} | $\overline{0E}$ | Y | MAX | - | 8.7 | 9 | 5.1 | 4.5 | 4.5 | 5.2 | 8.5 | 8 | 10.9 |
| t_{PZL} | | | | - | 8.9 | 9.4 | 6.1 | 4.4 | 4.4 | 5.2 | 8.5 | 8.5 | 10.9 |
| t_{PHZ} | $\overline{0E}$ | Y | MAX | - | 7.7 | 8 | 6.6 | 4.4 | 4.4 | 5.6 | 7.3 | 9.5 | 10.9 |
| t_{PLZ} | | | | - | 8.9 | 9.8 | 5.7 | 4.4 | 4.4 | 5.1 | 8.2 | 9.5 | 10.9 |

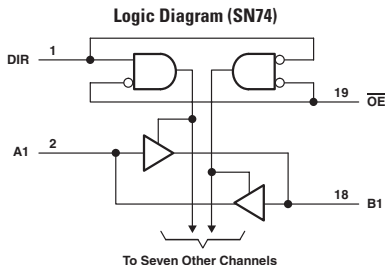
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | LVCH 3V |
|-----------|-----------------|--------|------------|--------|----------|----------|------|------|-------|-------|-------|--------|---------|
| t_{PLH} | A | Y | MAX | 9.9 | 10 | 8.7 | 8.5 | 9.5 | 13.5 | 8.5 | 9.5 | 5.9 | 5.9 |
| t_{PHL} | | | | 9.2 | 10 | 8.7 | 8.5 | 9.5 | 13.5 | 8.5 | 9.5 | 5.9 | 5.9 |
| t_{PZH} | $\overline{0E}$ | Y | MAX | 12.5 | 9.5 | 12.2 | 10.5 | 13 | 16 | 10.5 | 13 | 7.6 | 7.6 |
| t_{PZL} | | | | 11.4 | 10.5 | 12.2 | 10.5 | 13 | 16 | 10.5 | 13 | 7.6 | 7.6 |
| t_{PHZ} | $\overline{0E}$ | Y | MAX | 10.4 | 10.5 | 12.2 | 10.5 | 13 | 18 | 15.5 | 13 | 6.5 | 5.8 |
| t_{PLZ} | | | | 11.2 | 10.5 | 12.2 | 10.5 | 13 | 18 | 15.5 | 13 | 6.5 | 5.8 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCZ 3V | ALVC 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|-----------|-----------------|--------|------------|---------|---------|----------|----------|----------|-----------|-----------|
| t_{PLH} | A | Y | MAX | 5.9 | 2.8 | 2.8 | 2.5 | 1.9 | 2.5 | 1.9 |
| t_{PHL} | | | | 5.9 | 2.8 | 2.8 | 2.5 | 1.9 | 2.5 | 1.9 |
| t_{PZH} | $\overline{0E}$ | Y | MAX | 7.6 | 4.5 | 4.5 | 3.1 | 2.3 | 3.1 | 2.3 |
| t_{PZL} | | | | 7.6 | 4.5 | 4.5 | 3.1 | 2.3 | 3.1 | 2.3 |
| t_{PHZ} | $\overline{0E}$ | Y | MAX | 6.5 | 4.2 | 4.2 | 4.2 | 2.3 | 4.2 | 2.3 |
| t_{PLZ} | | | | 6.5 | 4.2 | 4.2 | 4.2 | 2.3 | 4.2 | 2.3 |

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

| ENABLE G | DIRECTION CONTROL DIR | OPERATION |
|----------|-----------------------|-----------------|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | SN64 BCT | ABT | ABTH | UNIT |
|--------------------------|------------|-----|-----|---------|-----|-----|---------|---------|----------|----------|----------|----------|------|------|------|
| I _{CCH} | MAX | 70 | 45 | 45 | 97 | 90 | 0.08 | 0.16 | 0.08 | 0.16 | 57 | 57 | 0.25 | 0.25 | mA |
| I _{CCL} | MAX | 90 | 55 | 55 | 143 | 120 | 0.08 | 0.16 | 0.08 | 0.16 | 90 | 90 | 30 | 30 | mA |
| I _{CCZ} | MAX | 95 | 58 | 58 | 123 | 110 | 0.08 | 0.16 | 0.08 | 0.16 | 15 | 15 | 0.25 | 0.25 | mA |
| I _{OH} (A port) | MAX | -15 | -15 | -15 | -15 | -3 | -6 | -4 | -6 | -4 | -3 | -3 | -32 | -32 | mA |
| I _{OH} (B port) | MAX | -15 | -15 | -15 | -15 | -15 | 6 | -4 | -6 | -4 | -15 | -15 | -32 | -32 | mA |
| I _{OL} (A port) | MAX | 24 | 24 | 48 | 64 | 24 | -6 | 4 | 6 | 4 | 24 | 24 | 64 | 64 | mA |
| I _{OL} (B port) | MAX | 24 | 24 | 48 | 64 | 64 | 6 | 4 | 6 | 4 | 64 | 64 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | LVT 3V | LVTH 3V | LVTR 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|--------------------------|------------|--------|---------|---------|-------|---------|---------|--------|----------|----------|------|------|-------|-------|------|
| I _{CCH} | MAX | 0.19 | 0.19 | 0.19 | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I _{CCL} | MAX | 5 | 5 | 12 | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I _{CCZ} | MAX | 0.19 | 0.19 | 0.19 | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I _{OH} (A port) | MAX | -32 | -32 | -12 | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | -16 | mA |
| I _{OH} (B port) | MAX | -32 | -32 | -32 | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | -16 | mA |
| I _{OL} (A port) | MAX | 64 | 64 | 32 | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | 16 | mA |
| I _{OL} (B port) | MAX | 64 | 64 | 32 | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | 16 | mA |

| PARAMETER | MAX or MIN | LV-AT | LVC 3V | LVCH 3V | LVCZ 3V | ALVC 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|--------------------------|------------|-------|--------|---------|---------|---------|----------|----------|----------|-----------|-----------|------|
| I _{CCH} | MAX | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I _{CCL} | MAX | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I _{CCZ} | MAX | 0.02 | 0.01 | 0.01 | 0.1 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I _{OH} (A port) | MAX | -16 | -24 | -24 | -24 | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I _{OH} (B port) | MAX | -16 | -24 | -24 | -24 | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I _{OL} (A port) | MAX | 16 | 24 | 24 | 24 | 24 | 24 | 8 | 9 | 8 | 9 | mA |
| I _{OL} (B port) | MAX | 16 | 24 | 24 | 24 | 24 | 24 | 8 | 9 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|-----------|-----------------|--------|------------|----|-----|---------|-----|-----|---------|---------|----------|----------|----------|
| t_{PLH} | A, B | B, A | MAX | 12 | 10 | 10 | 7.5 | 7 | 26 | 33 | 28 | 39 | 7 |
| t_{PHL} | | | | 12 | 10 | 10 | 7 | 7 | 26 | 33 | 28 | 39 | 7 |
| t_{PZH} | $\overline{0E}$ | A, B | MAX | 40 | 20 | 20 | 9 | 8 | 58 | 45 | 58 | 48 | 10.9 |
| t_{PZL} | | | | 40 | 20 | 20 | 8.5 | 9 | 58 | 45 | 58 | 48 | 11.6 |
| t_{PHZ} | $\overline{0E}$ | A, B | MAX | 28 | 10 | 10 | 5.5 | 7.5 | 50 | 45 | 50 | 45 | 9.3 |
| t_{PLZ} | | | | 25 | 15 | 15 | 9.5 | 7.5 | 50 | 45 | 50 | 45 | 9.1 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN64 BCT | ABT | ABTH | LVT 3V | LVTH 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT |
|-----------|-----------------|--------|------------|----------|-----|------|--------|---------|-------|---------|---------|--------|----------|
| t_{PLH} | A, B | B, A | MAX | 7 | 3.6 | 3.6 | 3.5 | 3.5 | 9.5 | 7 | 8.5 | 10 | 8 |
| t_{PHL} | | | | 7 | 3.9 | 3.9 | 3.5 | 3.5 | 6.9 | 7 | 8.5 | 9.1 | 9 |
| t_{PZH} | $\overline{0E}$ | A, B | MAX | 10.9 | 5.6 | 5.6 | 5.5 | 5.5 | 11.4 | 9 | 14 | 13.2 | 11 |
| t_{PZL} | | | | 11.6 | 6.2 | 6.2 | 5.5 | 5.5 | 9.5 | 9.5 | 14 | 12.9 | 12 |
| t_{PHZ} | $\overline{0E}$ | A, B | MAX | 9.3 | 5.9 | 5.9 | 5.9 | 5.9 | 9.5 | 10 | 14 | 12.9 | 11 |
| t_{PLZ} | | | | 9.1 | 4.5 | 4.5 | 5 | 5 | 10.4 | 10 | 14 | 13.9 | 11 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | LVCH 3V | LVCZ 3V | ALVC 3V |
|-----------|-----------------|--------|------------|----------|-----|------|-------|-------|-------|--------|---------|---------|---------|
| t_{PLH} | A, B | B, A | MAX | 10 | 8.5 | 9.5 | 13.5 | 8.5 | 9.5 | 6.3 | 6.3 | 6.3 | 3.4 |
| t_{PHL} | | | | 10 | 8.5 | 9.5 | 13.5 | 8.5 | 9.5 | 6.3 | 6.3 | 6.3 | 3.4 |
| t_{PZH} | $\overline{0E}$ | A, B | MAX | 14 | 12 | 16 | 19 | 12 | 16 | 8.5 | 8.5 | 8.5 | 5.5 |
| t_{PZL} | | | | 14 | 12 | 16 | 19 | 12 | 16 | 8.5 | 8.5 | 8.5 | 5.5 |
| t_{PHZ} | $\overline{0E}$ | A, B | MAX | 14.4 | 11 | 16.5 | 22 | 16 | 16.5 | 7.5 | 7.5 | 7.5 | 5.5 |
| t_{PLZ} | | | | 14.4 | 11 | 16.5 | 22 | 16 | 16.5 | 7.5 | 7.5 | 7.5 | 5.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|-----------|-----------------|--------|------------|----------|----------|----------|-----------|-----------|
| t_{PLH} | A, B | B, A | MAX | 3.4 | 2.2 | 1.8 | 2.2 | 1.8 |
| t_{PHL} | | | | 3.4 | 2.2 | 1.8 | 2.2 | 1.8 |
| t_{PZH} | $\overline{0E}$ | A, B | MAX | 5.5 | 3 | 2.4 | 3 | 2.4 |
| t_{PZL} | | | | 5.5 | 3 | 2.4 | 3 | 2.4 |
| t_{PHZ} | $\overline{0E}$ | A, B | MAX | 5.5 | 4 | 2.6 | 4 | 2.6 |
| t_{PLZ} | | | | 5.5 | 4 | 2.6 | 4 | 2.6 |

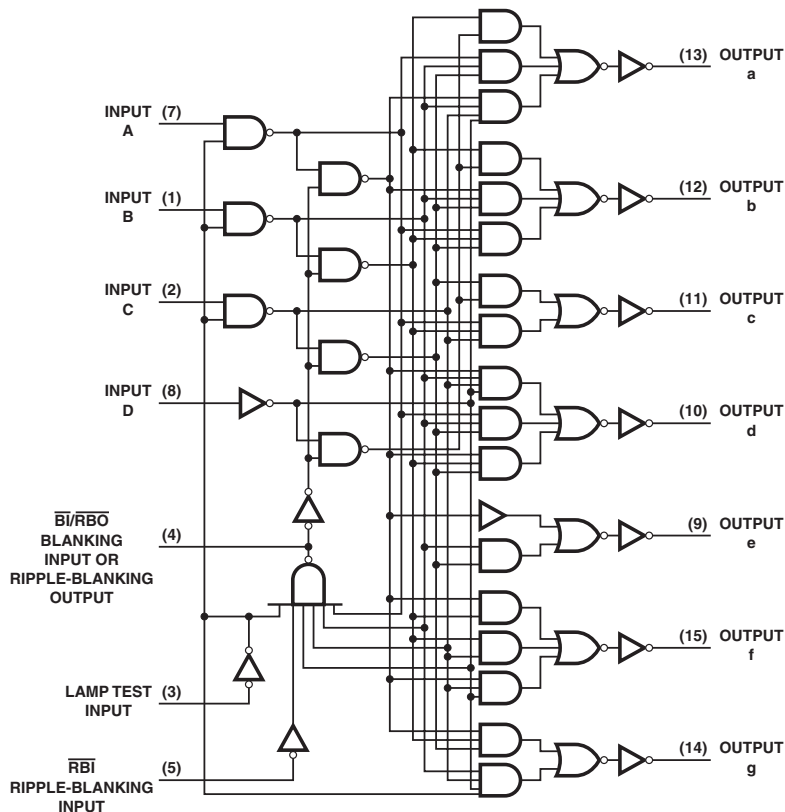
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTR 3V |
|-----------|-----------------|--------|------------|---------|
| t_{PLH} | A | B | MAX | 4.2 |
| | B | A | | 4.4 |
| t_{PHL} | A | B | MAX | 4.6 |
| | B | A | | 4.1 |
| t_{PZH} | $\overline{0E}$ | B | MAX | 5.5 |
| | | A | | 6 |
| t_{PZL} | $\overline{0E}$ | B | MAX | 6.6 |
| | | A | | 6.4 |
| t_{PHZ} | $\overline{0E}$ | B | MAX | 6.1 |
| | | A | | 5.8 |
| t_{PLZ} | $\overline{0E}$ | B | MAX | 5.2 |
| | | A | | 5.2 |

UNIT: ns

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



FUNCTION TABLE

| DECIMAL OR FUNCTION | INPUTS | | | | | $\overline{\text{BI/RBO}}$ | OUTPUTS | | | | | | | |
|---------------------------|------------------------|-------------------------|---|---|---|----------------------------|---------|-----|-----|-----|-----|-----|-----|-----|
| | $\overline{\text{LT}}$ | $\overline{\text{RBI}}$ | D | C | B | | A | a | b | c | d | e | f | g |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF |
| 1 | H | X | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF |
| 2 | H | X | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON |
| 3 | H | X | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON |
| 4 | H | X | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON |
| 5 | H | X | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON |
| 6 | H | X | L | H | H | L | H | ON | OFF | ON | ON | ON | ON | ON |
| 7 | H | X | L | H | H | H | H | ON | ON | ON | ON | OFF | OFF | OFF |
| 8 | H | X | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON |
| 9 | H | X | H | L | L | H | H | ON | ON | ON | ON | OFF | ON | ON |
| 10 | H | X | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON |
| 11 | H | X | H | L | H | H | H | OFF | OFF | ON | ON | OFF | ON | ON |
| 12 | H | X | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON |
| 13 | H | X | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON |
| 14 | H | X | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON |
| 15 | H | X | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| $\overline{\text{BI}}$ | X | X | X | X | X | X | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| $\overline{\text{RBI}}$ | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| LT | L | X | X | X | X | X | H | ON | ON | ON | ON | ON | ON | ON |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | TTL | LS | UNIT |
|-------------|----------------------------|------------|------|-------|------|
| I_{CC} | | MAX | 103 | 13 | mA |
| V_o (off) | a thru g | MAX | 15 | 15 | V |
| I_o (on) | | MAX | 40 | 24 | mA |
| I_{OH} | $\overline{\text{BI/RBO}}$ | MAX | -0.2 | -0.05 | mA |
| I_{OL} | | MAX | 8 | 3.2 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

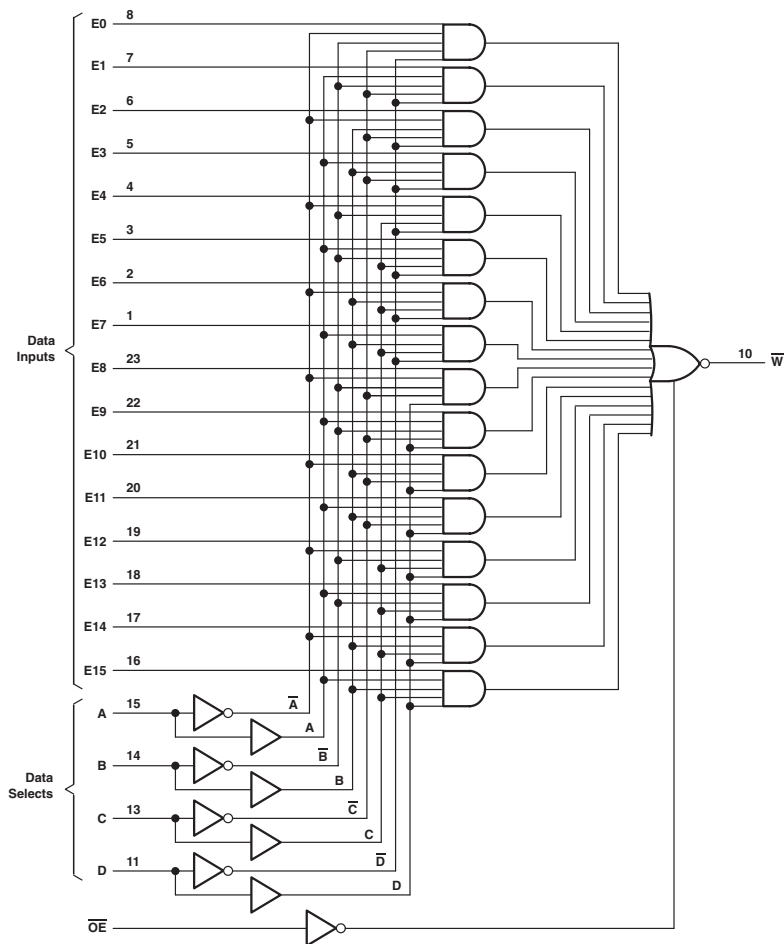
| PARAMETER | | MAX or MIN | TTL | LS |
|-----------|-------------------------------|------------|-----|-----|
| t_{off} | INPUT A | MIN | 100 | 100 |
| t_{on} | | | 100 | 100 |
| t_{off} | INPUT $\overline{\text{RBI}}$ | MIN | 100 | 100 |
| t_{on} | | | 100 | 100 |

UNIT: ns

1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
 - Boolean Function Generator
 - Parallel-to-Serial Converter
 - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

| \overline{OE} | INPUTS | | | | | OUTPUT | |
|-----------------|--------|---|---|---|-----|----------------|--|
| | A | B | C | D | Ei | \overline{W} | |
| L | L | L | L | L | E0 | E0 | |
| L | H | L | L | L | E1 | E1 | |
| L | L | H | L | L | E2 | E2 | |
| L | H | H | L | L | E3 | E3 | |
| L | L | L | H | L | E4 | E4 | |
| L | H | L | H | L | E5 | E5 | |
| L | L | H | H | L | E6 | E6 | |
| L | H | H | H | L | E7 | E7 | |
| L | L | L | L | H | E8 | E8 | |
| L | H | L | L | H | E9 | E9 | |
| L | L | H | L | H | E10 | E10 | |
| L | H | H | L | H | E11 | E11 | |
| L | L | L | H | H | E12 | E12 | |
| L | H | L | H | H | E13 | E13 | |
| L | L | H | H | H | E14 | E14 | |
| L | H | H | H | H | E15 | E15 | |
| H | X | X | X | X | X | Z | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 50 | mA |
| I _{OH} | MAX | -15 | mA |
| I _{OL} | MAX | 48 | mA |

SWITCHING CHARACTERISTICS

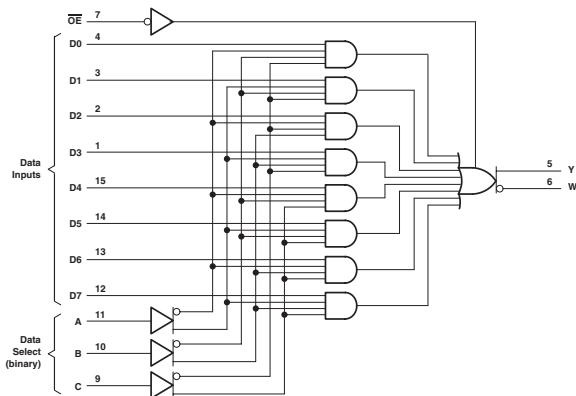
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS |
|------------------|-----------------|----------------|------------|------|
| t _{PLH} | DATA | \overline{W} | MAX | 8 |
| | | | | 7 |
| t _{PHL} | SELECT | \overline{W} | MAX | 13 |
| | | | | 10.5 |
| t _{PZH} | \overline{OE} | \overline{W} | MAX | 7 |
| | | | | 9 |
| t _{PHZ} | \overline{OE} | \overline{W} | MAX | 6 |
| | | | | 6.5 |

UNIT: ns

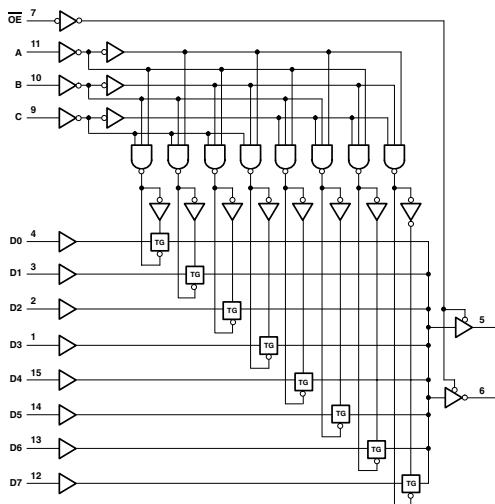
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '151
- 3-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

Logic Diagram (SN74ALS,F)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | | | | | | | |
|--------|---|---|--------------|---------|----|----|----|----|----|----|----|
| SELECT | | | STROBE OE | Y | W | | | | | | |
| C | B | A | | | D0 | D1 | D2 | D3 | D4 | D5 | D6 |
| X | X | X | H | Z | Z | | | | | | |
| L | L | L | L | D0 | D0 | | | | | | |
| L | L | H | L | D1 | D1 | | | | | | |
| L | H | L | L | D2 | D2 | | | | | | |
| L | H | H | L | D3 | D3 | | | | | | |
| H | L | L | L | D4 | D4 | | | | | | |
| H | L | H | L | D5 | D5 | | | | | | |
| H | H | L | L | D6 | D6 | | | | | | |
| H | H | H | L | D7 | D7 | | | | | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | S | ALS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 AC | CD74 AC | UNIT |
|-----------------|------------|------|------|------|------|----|------------|------------|-------------|------------|------------|------|
| I _{CC} | MAX | 62 | 12 | 85 | 14 | 24 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -5.2 | -2.6 | -6.5 | -2.6 | -3 | -6 | -4 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 24 | 24 | 6 | 4 | 4 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

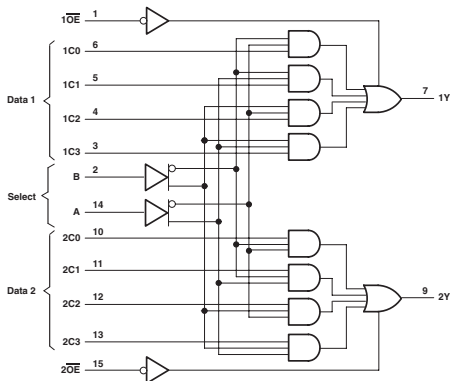
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | ALS | F | SN74 HC | CD74 HC | CD74 HCT | SN74 AC | CD74 AC |
|------------------|--|----------------------|------------|-----|----|------|-----|------|------------|------------|-------------|------------|------------|
| t _{PLH} | A, B, C (CD74: S ₀ , S ₁ , S ₂) | Y | MAX | 45 | 45 | 18 | 18 | 9.5 | 51 | 74 | 63 | 18.2 | 18.2 |
| t _{PHL} | | | | 45 | 45 | 19.5 | 24 | 7.5 | 51 | 74 | 63 | 18.2 | 18.2 |
| t _{PLH} | A, B, C (CD74: S ₀ , S ₁ , S ₂) | W (CD74: \bar{Y}) | MAX | 33 | 33 | 15 | 24 | 12.5 | 51 | 74 | 63 | 19.6 | 19.6 |
| t _{PHL} | | | | 33 | 33 | 13.5 | 23 | 9 | 51 | 74 | 63 | 19.6 | 19.6 |
| t _{PLH} | ANY D (CD74: ANYI) | Y | MAX | 28 | 28 | 12 | 10 | 7 | 49 | 53 | 53 | 13.5 | 13.5 |
| t _{PHL} | | | | 28 | 28 | 12 | 15 | 5 | 49 | 53 | 53 | 13.5 | 13.5 |
| t _{PLH} | ANY D (CD74: ANYI) | W (CD74: \bar{Y}) | MAX | 15 | 15 | 7 | 15 | 8 | 49 | 53 | 53 | 14.9 | 14.9 |
| t _{PHL} | | | | 15 | 15 | 7 | 15 | 8 | 49 | 53 | 53 | 14.9 | 14.9 |
| t _{PZH} | \bar{G} | Y | MAX | 27 | 45 | 19.5 | 15 | 7 | 36 | 42 | 45 | 13.5 | 13.5 |
| t _{PZL} | | | | 40 | 40 | 21 | 15 | 6.5 | 36 | 42 | 45 | 13.5 | 13.5 |
| t _{PZH} | \bar{G} | W (CD74: \bar{Y}) | MAX | 27 | 27 | 19.5 | 15 | 6 | 36 | 42 | 45 | 13.5 | 13.5 |
| t _{PZL} | | | | 40 | 40 | 21 | 15 | 4.5 | 36 | 42 | 45 | 13.5 | 13.5 |
| t _{PHZ} | \bar{G} | Y | MAX | 8 | 45 | 8.5 | 10 | 8.5 | 49 | 42 | 45 | 13.5 | 13.5 |
| t _{PLZ} | | | | 23 | 25 | 14 | 10 | 8 | 49 | 42 | 45 | 13.5 | 13.5 |
| t _{PHZ} | \bar{G} | W (CD74: \bar{Y}) | MAX | 8 | 55 | 8.5 | 10 | 5.5 | 49 | 42 | 45 | 13.5 | 13.5 |
| t _{PLZ} | | | | 23 | 25 | 14 | 10 | 4.5 | 49 | 42 | 45 | 13.5 | 13.5 |

UNIT: ns

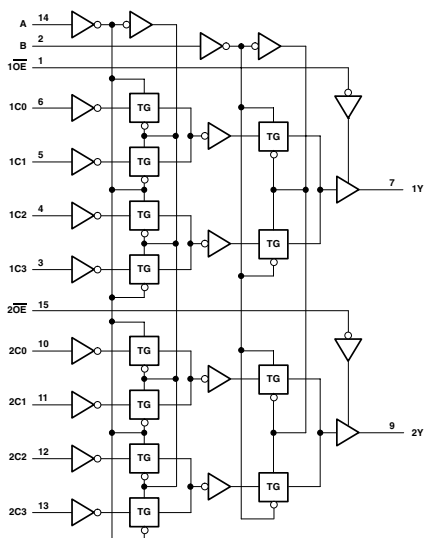
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

Logic Diagram (SN74ALS, AS, F)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

| SELECT INPUTS | | DATA INPUTS | | | | OUTPUT CONTROL | OUTPUT |
|---------------|---|-------------|----|----|----|-----------------|--------|
| B | A | C0 | C1 | C2 | C3 | \overline{OE} | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------|------|------|-----|----|---------|---------|----------|---------|----------|------|
| I _{CC} | MAX | 14 | 14 | 33 | 23 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -2.6 | -15 | -3 | -6 | -6 | -4 | -24 | -24 | mA |
| I _{OL} | MAX | 8 | 24 | 48 | 24 | 6 | 6 | 4 | 24 | 24 | mA |

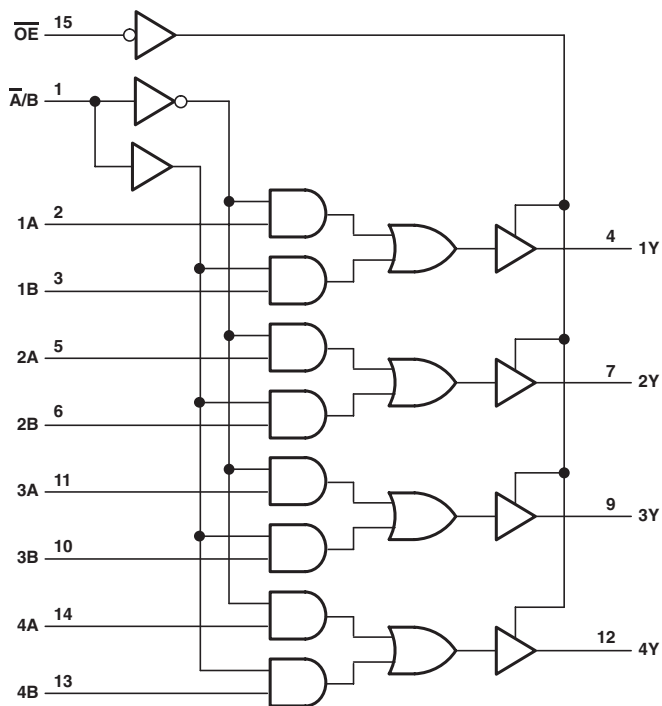
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|------------------|-----------------|--------|------------|----|-----|------|----|---------|---------|----------|---------|----------|
| t _{PLH} | DATA | Y | MAX | 25 | 10 | 7.5 | 8 | 35 | 53 | 57 | 13.3 | 18 |
| | | | | 20 | 14 | 8 | 7 | 35 | 53 | 57 | 13.3 | 18 |
| t _{PHL} | SELECT | Y | MAX | 45 | 21 | 13.5 | 13 | 38 | 53 | 60 | 20 | 22 |
| | | | | 32 | 21 | 11.5 | 10 | 38 | 53 | 60 | 20 | 22 |
| t _{PZH} | \overline{OE} | Y | MAX | 28 | 14 | 12.5 | 9 | 25 | 33 | 45 | 11.5 | 12.6 |
| | | | | 23 | 16 | 11.5 | 9 | 25 | 33 | 45 | 11.5 | 12.6 |
| t _{PHZ} | \overline{OE} | Y | MAX | 41 | 10 | 6 | 6 | 38 | 45 | 45 | 11.5 | 12.6 |
| | | | | 27 | 14 | 7 | 7 | 38 | 45 | 45 | 11.5 | 12.6 |

UNIT: ns

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)


FUNCTION TABLE (SN74)

| OUTPUT CONTROL OE | INPUTS | | | OUTPUT Y |
|----------------------|---------------|---|---|-------------|
| | SELECT A/B | A | B | |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | AC 11 | CD74 AC | ACT 11 | UNIT |
|-----------------|------------|------|------|------|------|----|------------|------------|-------------|-------------|----------|------------|-----------|------|
| I _{CC} | MAX | 19 | 87 | 14 | 31.9 | 23 | 0.08 | 0.16 | 0.08 | 0.16 | 0.08 | 0.16 | 0.08 | mA |
| I _{OH} | MAX | -2.6 | -6.5 | -2.6 | -15 | -3 | -6 | -6 | -6 | -6 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 20 | 24 | 48 | 24 | 6 | 6 | 6 | 6 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 ACT | LVC 3V | UNIT |
|-----------------|------------|-------------|-----------|------|
| I _{CC} | MAX | 0.16 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

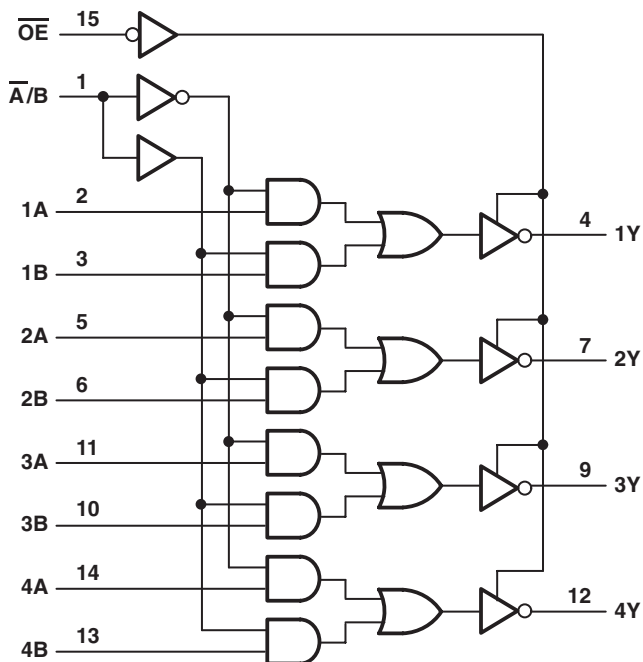
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT |
|------------------|-----------------|--------|------------|----|------|-----|-----|-----|------------|------------|-------------|-------------|
| t _{PLH} | DATA | ANY | MAX | 13 | 7.5 | 10 | 5.5 | 7 | 25 | 45 | 38 | 50 |
| t _{PHL} | | | | 15 | 6.5 | 12 | 6 | 6.5 | 25 | 45 | 38 | 50 |
| t _{PLH} | SELECT | ANY | MAX | 21 | 15 | 18 | 11 | 15 | 25 | 53 | 38 | 57 |
| t _{PHL} | | | | 24 | 15 | 22 | 10 | 9.5 | 25 | 53 | 38 | 57 |
| t _{PZH} | \overline{OE} | Y | MAX | 30 | 19.5 | 16 | 7.5 | 8.5 | 38 | 45 | 38 | 45 |
| t _{PZL} | | | | 30 | 21 | 18 | 9.5 | 8.5 | 38 | 45 | 38 | 45 |
| t _{PHZ} | \overline{OE} | Y | MAX | 30 | 8.5 | 10 | 6.5 | 7 | 38 | 45 | 38 | 45 |
| t _{PLZ} | | | | 25 | 14 | 15 | 7 | 7 | 38 | 45 | 38 | 45 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LVC 3V |
|------------------|-----------------|--------|------------|----------|------------|-----------|-------------|-----------|
| t _{PLH} | DATA | ANY | MAX | 6.4 | 9.3 | 6.9 | 10.7 | 4.6 |
| t _{PHL} | | | | 7.2 | 9.3 | 8.7 | 10.7 | 4.6 |
| t _{PLH} | SELECT | ANY | MAX | 7.2 | 13.4 | 8.2 | 15.4 | 6.4 |
| t _{PHL} | | | | 7.9 | 13.4 | 9.4 | 15.4 | 6.4 |
| t _{PZH} | \overline{OE} | Y | MAX | 6.5 | 14.7 | 7.3 | 16.1 | 5.6 |
| t _{PZL} | | | | 8.6 | 14.7 | 9.6 | 16.1 | 5.6 |
| t _{PHZ} | \overline{OE} | Y | MAX | 7.6 | 14.7 | 8.4 | 16.1 | 4.3 |
| t _{PLZ} | | | | 7.6 | 14.7 | 8.5 | 16.1 | 4.3 |

UNIT: ns

QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)


FUNCTION TABLE

| OUTPUT CONTROL OE | INPUTS | | | OUTPUT Y |
|----------------------|-----------------------------|---|---|-------------|
| | SELECT \bar{A}/\bar{B} | A | B | |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 ACT | UNIT |
|-----------------|------------|------|------|------|------|----|------------|------------|-------------|-------------|------|
| I _{CC} | MAX | 16 | 87 | 13 | 25.2 | 23 | 0.08 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -6.5 | -2.6 | -15 | -3 | -6 | -6 | -6 | -24 | mA |
| I _{OL} | MAX | 8 | 20 | 24 | 48 | 24 | 6 | 6 | 6 | 24 | mA |

SWITCHING CHARACTERISTICS

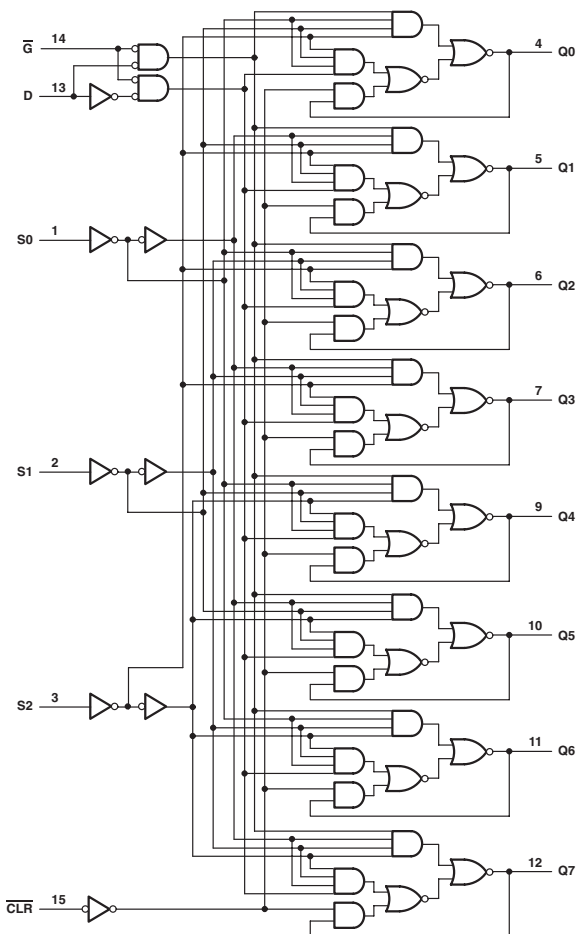
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 ACT |
|------------------|-----------|--------|------------|----|------|-----|-----|-----|------------|------------|-------------|-------------|
| t _{PLH} | DATA | Y | MAX | 12 | 6 | 8 | 5 | 6 | 25 | 24 | 34 | 10.7 |
| | | | | 17 | 6 | 7 | 4 | 5.5 | 25 | 24 | 34 | 10.7 |
| t _{PHL} | SELECT | Y | MAX | 21 | 12 | 25 | 9.5 | 9.5 | 25 | 35 | 43 | 15.4 |
| | | | | 24 | 12 | 20 | 10 | 11 | 25 | 35 | 43 | 15.4 |
| t _{PZH} | \bar{G} | Y | MAX | 30 | 19.5 | 18 | 8 | 8.5 | 38 | 35 | 35 | 16.1 |
| | | | | 30 | 21 | 18 | 10 | 8.5 | 38 | 35 | 35 | 16.1 |
| t _{PHZ} | \bar{G} | Y | MAX | 30 | 8.5 | 10 | 6 | 7 | 38 | 38 | 38 | 16.1 |
| | | | | 25 | 14 | 18 | 6.5 | 7 | 38 | 38 | 38 | 16.1 |

UNIT: ns

8-BIT ADDRESSABLE LATCHES

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

Logic Diagram (SN74ALS)



LATCH SELECTION

| SELECT INPUTS | | | LATCH ADDRESSED |
|---------------|---|---|-----------------|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

FUNCTION TABLE (SN74)

| INPUTS | | OUTPUT OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|--------|-----------|---------------------------|-------------------|---|
| CLEAR | \bar{G} | | | |
| H | L | D | Q ₀ | Addressable latch Memory 8-line demultiplexer Clear |
| H | H | Q ₀ | Q ₀ | |
| L | L | D | L | |
| L | H | L | L | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 90 | 36 | 22 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | 16 | 8 | 8 | 4 | 4 | 4 | mA |
| I _{OL} | MAX | -0.8 | -0.4 | -0.4 | -4 | -4 | -4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|---|----------------------|--------|------------|-----|----|-----|---------|---------|----------|
| t _w | \bar{G} (CDHC/HCT: $\bar{L}\bar{E}$) | | | MIN | 15 | 17 | 15 | 20 | 21 | 27 |
| | CLR (CDHC/HCT: MR) | | | | 15 | 10 | 10 | 20 | 21 | 27 |
| t _{su} | DATA | | | MIN | 15 | 20 | 15 | 19 | 24 | 26 |
| | ADDRESS | | | | 5 | 17 | 15 | 19 | 24 | 26 |
| t _h | DATA | | | MIN | 0 | 0 | 0 | 5 | 0 | 0 |
| | ADDRESS | | | | 20 | 0 | 0 | 5 | 0 | 0 |
| t _{PLH} | | CLEAR (CDHC/HCT: MR) | Any Q | MAX | 25 | 18 | 12 | 38 | 47 | 59 |
| t _{PHL} | | DATA | Any Q | MAX | 24 | 30 | 19 | 33 | 56 | 59 |
| t _{PLH} | | | | | 20 | 20 | 12 | 33 | - | 59 |
| t _{PLH} | | ADDRESS | Any Q | MAX | 28 | 27 | 22 | 50 | 56 | 61 |
| t _{PHL} | | | | | 28 | 20 | 12 | 50 | - | 61 |
| t _{PHL} | | ENABLE | Any Q | MAX | 20 | 24 | 20 | 43 | 51 | 57 |
| t _{PHL} | | | | | 20 | 24 | 13 | 43 | - | 57 |

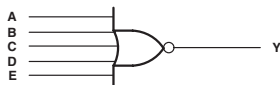
UNIT: ns

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DUAL 5-INPUT POSITIVE-NOR GATES

$$\bullet Y = \overline{A + B + C + D + E}$$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | S | F | UNIT |
|-----------|------------|----|-----|------|
| I_{CC} | MAX | 45 | 9.5 | mA |
| I_{OH} | MAX | -1 | -1 | mA |
| I_{OL} | MAX | 20 | 20 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | S | F |
|-----------|---------------|--------|------------|-----|-----|
| t_{PLH} | A, B, C, D, E | Y | MAX | 5.5 | 6.5 |
| t_{PHL} | | | | 6 | 4.5 |

UNIT: ns

265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

$$\bullet Y = \overline{A}, W = A$$

$$\bullet Y = AB, W = AB$$

Logic Diagram

ELEMENTS 1 and 4



ELEMENTS 2 and 3



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 34 | mA |
| I_{OH} | MAX | -0.8 | mA |
| I_{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|------------------------------|--------|------------------|------------|---------|
| $t_{PLH}(W)$ | A or B | W | MAX | 18 |
| $t_{PHL}(Y)$ | A or B | Y | MAX | 18 |
| $t_{PLH}(W)$ | A or B | W | MAX | 18 |
| $t_{PHL}(Y)$ | A or B | Y | MAX | 18 |
| $t_{PLH}(W)$ $t_{PHL}(Y)$ | A or B | W with respect Y | MAX | ± 3 |
| $t_{PHL}(W)$ $t_{PLH}(Y)$ | A or B | W with respect Y | MAX | ± 3 |

UNIT: ns

QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-DRAIN OUTPUTS



$$Y = \overline{A \oplus B}$$

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | SN74 HC | UNIT |
|-----------------|------------|-----|-----------------|------|
| I _{cc} | MAX | 13 | 0.02 | mA |
| V _{OH} | MAX | 5.5 | V _{cc} | V |
| I _{OL} | MAX | 8 | 4 | mA |

SWITCHING CHARACTERISTICS

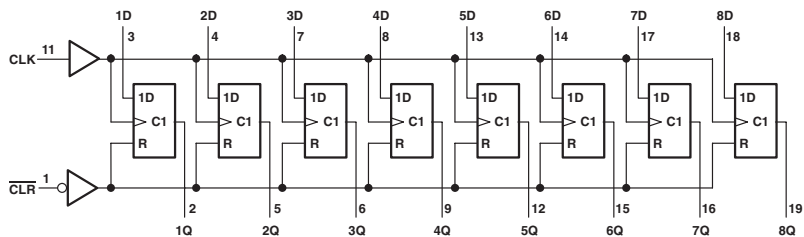
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC |
|------------------|-------------------------------|--------|------------|----|---------|
| t _{PLH} | A or B Other INPUT Low | Y | MAX | 30 | 31 |
| t _{PHL} | A or B Other INPUT Low | Y | MAX | 30 | 25 |
| t _{PLH} | A or B Other INPUT High | Y | MAX | 30 | 31 |
| t _{PHL} | A or B Other INPUT High | Y | MAX | 30 | 25 |

UNIT: ns

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT |
|--------|-------|---|----------------|
| CLEAR | CLOCK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q ₀ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | LVTH 3V | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------|------|------|------|---------|---------|----------|----------|-----|---------|---------|----------|------|
| I _{CC} | MAX | 94 | 27 | 29 | 0.08 | 0.16 | 0.08 | 0.16 | 30 | 5 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -2.6 | -4 | -4 | -4 | -4 | -32 | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 16 | 8 | 24 | 4 | 4 | 4 | 4 | 64 | 64 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|-------|-------|------|
| I _{CC} | MAX | 0.04 | 0.04 | - | 0.02 | mA |
| I _{OH} | MAX | -8 | -8 | -6 | -12 | mA |
| I _{OL} | MAX | 8 | 8 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT |
|------------------|--------------|--------|------------|------|----|-----|---------|---------|----------|----------|-----|
| f _{max} | | | MIN | 30 | 30 | 35 | 21 | 20 | 16 | 16 | 150 |
| t _w | | | MIN | 16.5 | 20 | 14 | 20 | 24 | 25 | 30 | 3.3 |
| t _{SU} | DATA INPUT | | MIN | 20 | 20 | 10 | 25 | 18 | 25 | 18 | 2.5 |
| | CLR INACTIVE | | MIN | 25 | 25 | 15 | 25 | - | 25 | - | 2 |
| t _H | | | MIN | 5 | 5 | 0 | 0 | 3 | 0 | 3 | 1.2 |
| t _{PHL} | CLEAR | ANY Q | MAX | 27 | 27 | 18 | 40 | 45 | 42 | 48 | 7.4 |
| t _{PLH} | | | MAX | 27 | 27 | 12 | 40 | 45 | 42 | 45 | 6.5 |
| t _{PHL} | CLOCK | ANY Q | MAX | 27 | 27 | 15 | 40 | 45 | 42 | 45 | 7.3 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V |
|------------------|--------------|--------|------------|---------|---------|----------|------|------|-------|-------|
| f _{max} | | | MIN | 150 | 100 | 85 | 70 | 45 | 45 | 70 |
| t _w | | | MIN | 3.3 | 5 | 6 | 5 | 6.5 | 6.5 | 5 |
| t _{SU} | DATA INPUT | | MIN | 2.3 | 2 | 2 | 4.5 | 5 | 6.5 | 4.5 |
| | CLR INACTIVE | | MIN | 2.3 | - | - | 2 | 2.5 | 2.5 | 2 |
| t _H | | | MIN | 0 | 2 | 2 | 1 | 0 | 1 | 1 |
| t _{PHL} | CLEAR | ANY Q | MAX | 4.3 | 13.5 | 13.5 | 12 | 12.6 | 19.5 | 12 |
| t _{PLH} | | | MAX | 4.9 | 13.5 | 13.5 | 12.5 | 9.8 | 19.5 | 12.5 |
| t _{PHL} | CLOCK | ANY Q | MAX | 4.8 | 13.5 | 13.5 | 12.5 | 11 | 19.5 | 12.5 |

UNIT f_{max} : MHz, other : ns

QUADRUPLE J-K FLIP-FLORS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

FUNCTION TABLE

| COMMON INPUTS | | INPUTS | | | OUTPUT |
|---------------|-------|--------|---|-----------|----------------|
| PRESET | CLEAR | CLOCK | J | \bar{K} | Q |
| L | H | X | X | X | H |
| H | L | X | X | X | L |
| L | L | X | X | X | H† |
| H | H | ↓ | L | H | Q ₀ |
| H | H | ↓ | H | H | H |
| H | H | ↓ | L | L | L |
| H | H | ↓ | H | L | TOGGLE |
| H | H | H | X | X | Q ₀ |

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

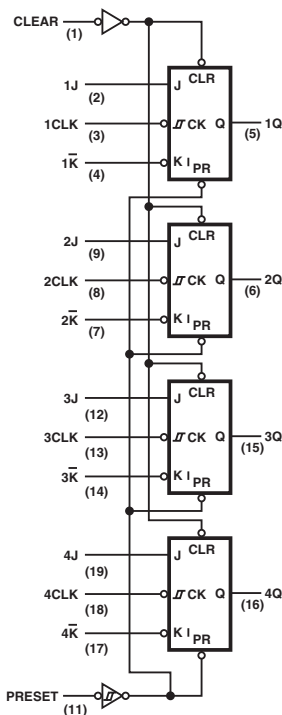
| PARAMETER | MAX or MIN | TTL | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 81 | mA |
| I_{OH} | MAX | -0.8 | mA |
| I_{OL} | MAX | 16 | mA |

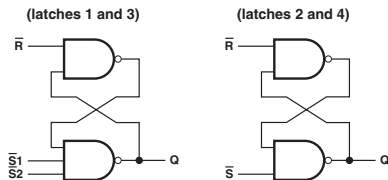
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL |
|-----------|----------------------------|--------|------------|------|
| f_{max} | | | MIN | 35 |
| t_w | CLOCK high | | MIN | 13.5 |
| | CLOCK low | | MIN | 15 |
| t_{SU} | J, K | | MIN | 3 |
| | CLR, PRE | | MIN | 10 |
| | | | MIN | 10 |
| t_h | | | MIN | 10 |
| t_{PLH} | $\overline{\text{PRESET}}$ | Q | MAX | 25 |
| t_{PHL} | $\overline{\text{CLEAR}}$ | Q | MAX | 30 |
| t_{PLH} | CLOCK | Q | MAX | 30 |
| t_{PHL} | | | | 30 |

UNIT f_{max} : MHz, other : ns

Logic Diagram



QUADRUPLE \overline{S} - \overline{R} LATCHES

FUNCTION TABLE
(each latch)

| INPUTS | | OUTPUT |
|------------------|----------------|----------------|
| \overline{S} † | \overline{R} | Q |
| H | H | Q ₀ |
| L | H | H |
| H | L | L |
| L | L | H† |

H = high level L = low level

†For latches with double S inputs:

Q₀ = the level of Q before the indicated input conditions were established.

†This configuration is nonstable; that is, it may not persist when the \overline{S} and \overline{R} inputs return to their inactive (high) level.

H = both \overline{S} inputs high

L = one or both \overline{S} inputs low

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 30 | 7 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

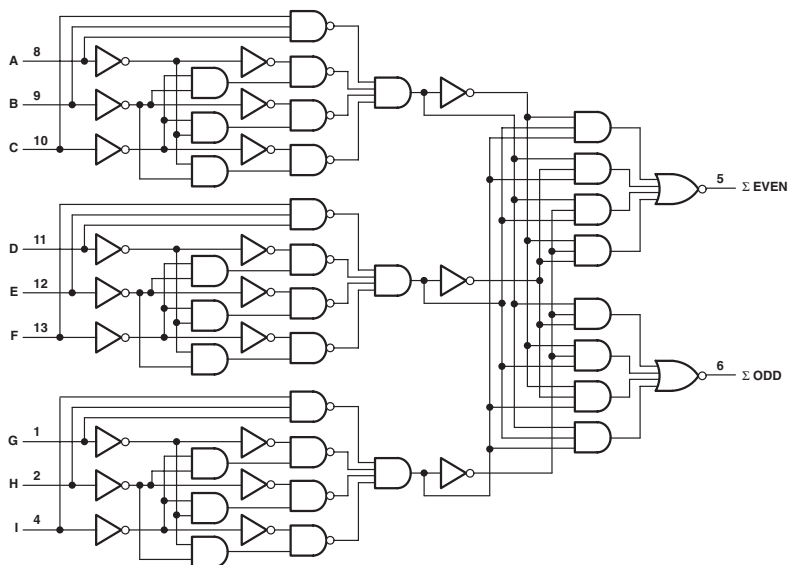
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|----------------|--------|------------|-----|----|
| t _W | | | MIN | 20 | 20 |
| t _{PLH} | \overline{S} | Q | MAX | 22 | 22 |
| t _{PHL} | | | | 15 | 21 |
| t _{PHL} | \overline{R} | | MAX | 27 | 27 |

UNIT: ns

9-BIT PARITY GENERATORS/CHECKERS

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| NO. OF INPUTS A-1 THAT ARE HIGH | OUTPUTS | |
|---------------------------------------|---------------|--------------|
| | Σ EVEN | Σ ODD |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------|------------|------|-----|------|----|----|------------|------------|-------------|------------|-------------|------|
| I_{CC} | MAX | 27 | 105 | 16 | 35 | 35 | 0.08 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -0.4 | -1 | -2.6 | -2 | -1 | -4 | -4 | -4 | -24 | -24 | mA |
| I_{OL} | MAX | 8 | 20 | 24 | 20 | 20 | 4 | 4 | 4 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

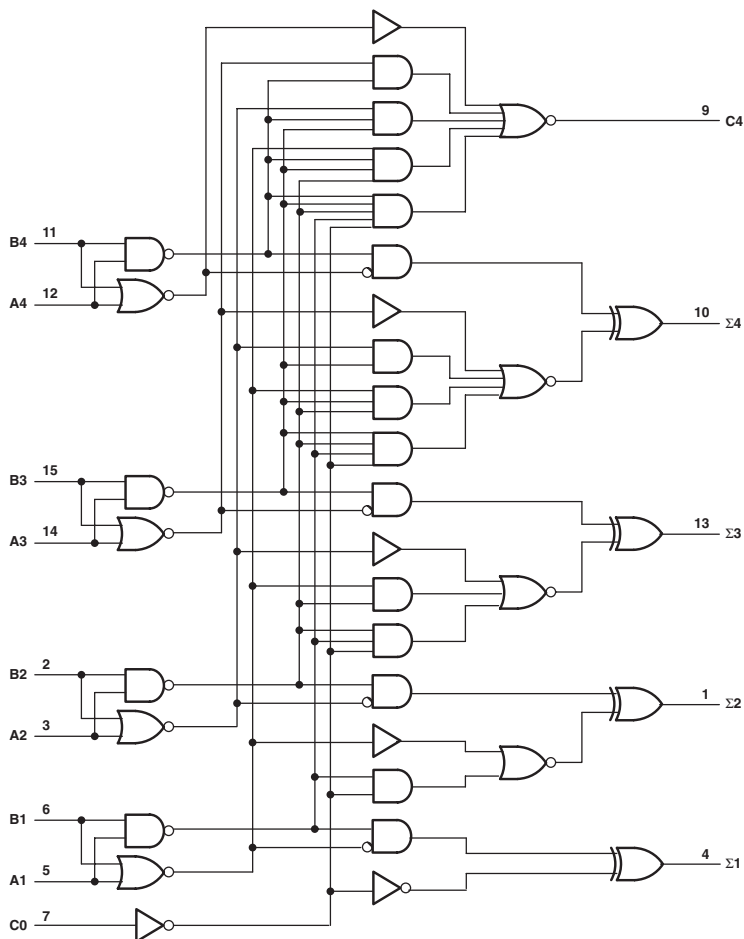
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|-----------|-------|--------------------------------------|------------|----|----|-----|------|----|------------|------------|-------------|------------|-------------|
| t_{PLH} | DATA | Σ EVEN (CD74: ΣE) | MAX | 50 | 21 | 20 | 12 | 10 | 52 | 60 | 63 | 20 | 21.6 |
| | | | | 45 | 18 | 20 | 11 | 11 | 52 | 60 | 63 | 20 | 21.6 |
| t_{PHL} | DATA | Σ ODD (CD74: ΣD) | MAX | 35 | 21 | 20 | 12 | 10 | 52 | 60 | 68 | 21 | 21.6 |
| | | | | 50 | 18 | 22 | 11.5 | 11 | 52 | 60 | 68 | 21 | 21.6 |

UNIT: ns

4-BIT BINARY FULL ADDERS WITH FAST CARRY

- Full-Carry Look-Ahead Across the Four Bits

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | | | | | | | |
|--------|----|----|----|-------------|------------|----|------------|-------------|----|--|--|
| | | | | WHEN C0 = L | | | | WHEN C0 = H | | | |
| | | | | WHEN C2 = L | | | | WHEN C2 = H | | | |
| A1 | B1 | A2 | B2 | $\Sigma 1$ | $\Sigma 2$ | C2 | $\Sigma 1$ | $\Sigma 2$ | C2 | | |
| A3 | B3 | A4 | B4 | $\Sigma 3$ | $\Sigma 4$ | C4 | $\Sigma 3$ | $\Sigma 4$ | C4 | | |
| L | L | L | L | L | L | L | H | L | L | | |
| H | L | L | L | L | L | L | L | H | L | | |
| L | H | L | L | L | H | L | L | H | L | | |
| H | H | L | L | L | L | H | L | H | L | | |
| L | L | H | L | L | L | H | L | H | L | | |
| H | L | H | L | L | H | L | L | L | H | | |
| L | H | H | L | L | H | L | L | L | H | | |
| H | H | H | L | L | L | L | H | L | H | | |
| L | L | L | H | L | L | H | L | H | L | | |
| H | L | L | H | L | H | L | H | L | H | | |
| L | L | L | H | H | H | L | L | L | H | | |
| L | L | L | H | H | H | L | L | L | H | | |
| L | H | L | H | H | H | L | L | L | H | | |
| L | H | L | H | L | L | H | H | L | H | | |
| L | L | H | H | L | L | H | H | L | H | | |
| H | L | H | H | H | L | H | L | H | H | | |
| L | H | H | H | H | L | H | L | H | H | | |
| H | H | H | H | L | H | H | H | H | H | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | TTL | LS | S | F | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|----------------------|------------|------|------|-----|----|---------|----------|---------|----------|------|
| I _{CC} | | MAX | 110 | 39 | 160 | 55 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | Any OUTPUT except C4 | MAX | -0.8 | -0.4 | -1 | -1 | -4 | -4 | -24 | -24 | mA |
| | C4 | MAX | -0.4 | | | | | | | | |
| I _{OL} | Any OUTPUT except C4 | MAX | 16 | 8 | 20 | 4 | 4 | 24 | 24 | mA | |
| | C4 | MAX | 8 | | | | | | | | |

SWITCHING CHARACTERISTICS

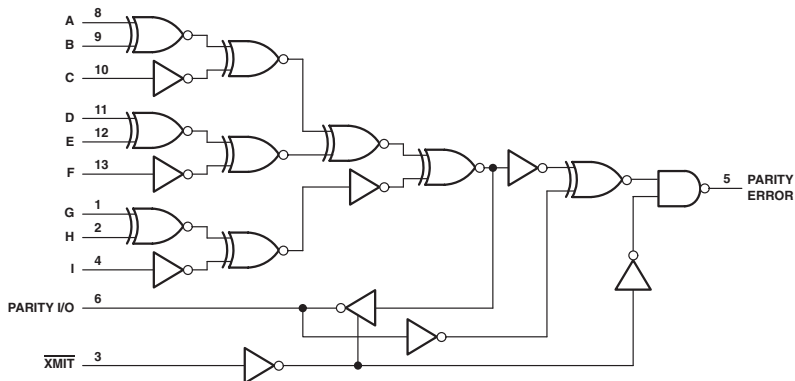
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | S | F | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|------------------|----------------------------|-------------------------------------|------------|-----|----|----|------|---------|----------|---------|----------|
| t _{PLH} | C0 (CD74:C _{in}) | Any Σ (CD74:S _j) | MAX | 21 | 24 | 18 | 10.5 | 69 | 80 | 17.6 | 17.6 |
| t _{PHL} | | | MAX | 21 | 24 | 18 | 10.5 | 69 | 80 | 17.6 | 17.6 |
| t _{PLH} | An or Bn | Σn (CD74:S _n) | MAX | 24 | 24 | 18 | 10.5 | 63 | 74 | 18.2 | 18.2 |
| t _{PHL} | | | MAX | 24 | 24 | 18 | 10.5 | 63 | 74 | 18.2 | 18.2 |
| t _{PLH} | C0 (CD74:C _{in}) | C4 (CD74:C _{out}) | MAX | 14 | 17 | 11 | 8.5 | 59 | 69 | 17.6 | 17.6 |
| t _{PHL} | | | MAX | 16 | 22 | 11 | 8 | 59 | 69 | 17.6 | 17.6 |
| t _{PLH} | An or Bn | | MAX | 14 | 17 | 12 | 8.5 | 59 | 72 | 17.6 | 17.6 |
| t _{PHL} | | | MAX | 16 | 17 | 12 | 8 | 59 | 72 | 17.6 | 17.6 |

UNIT: ns

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74AS)



FUNCTION TABLE (SN74AS)

| NUMBER OF INPUTS (A-I) THAT ARE HIGH | $\overline{\text{XMIT}}$ | PARITY I/O | PARITY ERROR |
|--------------------------------------|--------------------------|------------|--------------|
| 0, 2, 4, 6, 8 | l | H | H |
| 1, 3, 5, 7, 9 | l | L | H |
| 0, 2, 4, 6, 8 | h | h | H |
| | h | l | L |
| 1, 3, 5, 7, 9 | h | h | L |
| | h | l | H |

h = high input level l = low input level
 H = high output level L = low output level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | AS | AC 11 | ACT 11 | UNIT |
|-----------------|--------------|------------|-----|-------|--------|------|
| I _{CC} | | MAX | 50 | 0.08 | 0.08 | mA |
| I _{OH} | Parity error | MAX | -2 | -24 | -24 | mA |
| | Parity I/O | MAX | -15 | -24 | -24 | mA |
| I _{OL} | Parity error | MAX | 20 | 24 | 24 | mA |
| | Parity I/O | MAX | 48 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS | AC 11 | ACT 11 |
|------------------|--------------------------|--------------|------------|------|-------|--------|
| t _{PLH} | A to I | Parity I/O | MAX | 15 | 9 | 10.4 |
| | | | | 14 | 107 | 12 |
| t _{PLH} | A to I | Parity error | MAX | 16.5 | 10 | 11.3 |
| | | | | 16.5 | 12 | 12.9 |
| t _{PHL} | Parity I/O | Parity error | MAX | 9 | 6.2 | 7.7 |
| | | | | 9 | 7.9 | 9.1 |
| t _{PZH} | $\overline{\text{XMIT}}$ | Parity I/O | MAX | 13 | 5.3 | 7.3 |
| | | | | 16 | 8.9 | 11.4 |
| t _{PZL} | $\overline{\text{XMIT}}$ | Parity I/O | MAX | 11.5 | 6.5 | 8.5 |
| | | | | 10 | 6.3 | 7.8 |

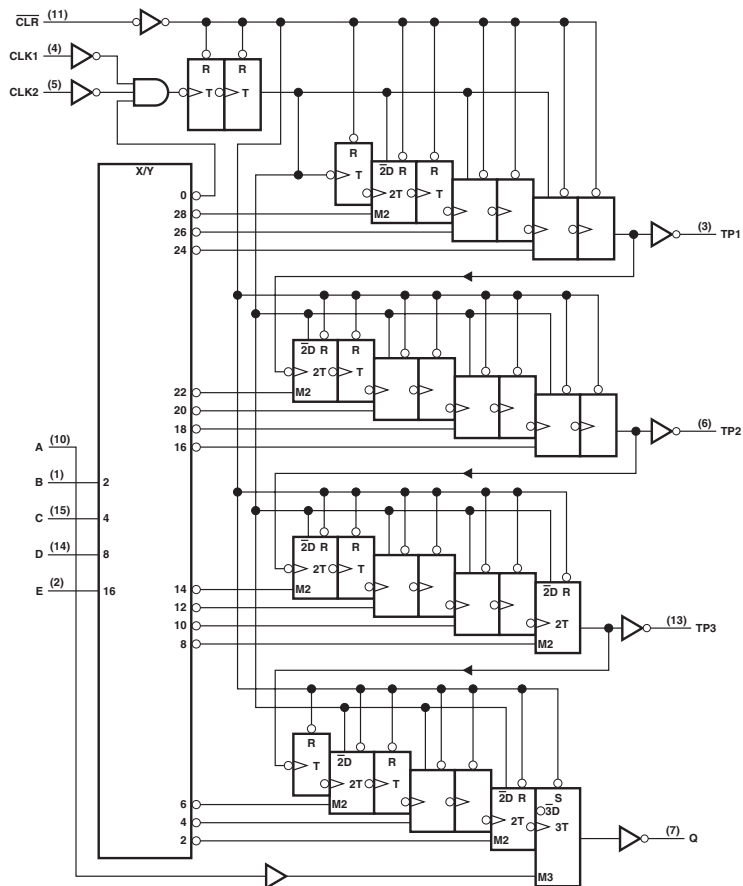
UNIT: ns

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from 2^2 to 2^{31}
- Easily Expandable
- Applications:

Frequency Division
Digital Timing

Logic Diagram



FUNCTION TABLE

| CLEAR | CLK 1 | CLK 2 | Q OUTPUT MODE |
|-------|-------|-------|---------------|
| L | X | X | Cleared to L |
| H | ≠ | L | Count |
| H | L | ≠ | Count |
| H | H | X | Inhibit |
| H | X | H | Inhibit |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

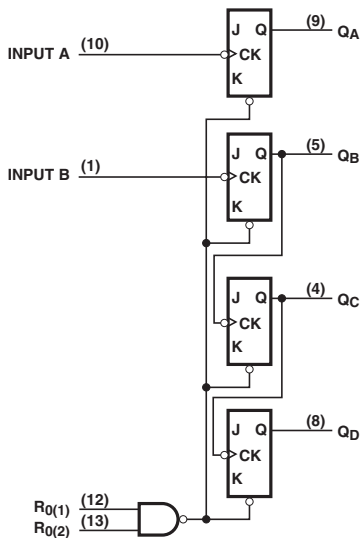
| PARAMETER | MAX or MIN | LS | UNIT |
|--------------------------|------------|------|------|
| I _{CC} | MAX | 75 | mA |
| I _{OH} (Q only) | MAX | -1.2 | V |
| I _{OL} (Q only) | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|-------|--------|------------|-----|
| f _{max} | CLK | | MIN | 30 |
| t _{PLH} | CLK | Q | MAX | 90 |
| t _{PHL} | CLK | Q | MAX | 120 |
| t _{PHL} | CLR | Q | MAX | 65 |

UNIT f_{max}: MHz, other: ns

Logic Diagram



COUNT SEQUENCE

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

NOTE: Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

| RESET INPUTS | | OUTPUTS | | | |
|--------------------|--------------------|----------------|----------------|----------------|----------------|
| P ₀ (1) | P ₀ (2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | L | L | L |
| L | X | | | | COUNT |
| X | L | | | | COUNT |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 39 | 15 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | mA |
| I _{OL} | MAX | 16 | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS |
|------------------|-------|----------------|------------|-----|----|
| f _{max} | A | Q _A | MIN | 32 | 32 |
| | B | Q _B | MIN | 16 | 16 |
| t _w | A | A, B | MIN | 15 | 15 |
| | B | | | 30 | 30 |
| | Reset | | | 15 | 15 |
| t _{SU} | | | MIN | 25 | 25 |
| t _{PLH} | A | Q _A | MAX | 16 | 16 |
| t _{PHL} | | | | 18 | 18 |
| t _{PLH} | A | Q _B | MAX | 70 | 70 |
| t _{PHL} | | | | 70 | 70 |
| t _{PLH} | B | Q _B | MAX | 16 | 16 |
| t _{PHL} | | | | 21 | 21 |
| t _{PLH} | B | Q _C | MAX | 32 | 32 |
| t _{PHL} | | | | 35 | 35 |
| t _{PLH} | B | Q _D | MAX | 51 | 51 |
| t _{PHL} | | | | 51 | 51 |

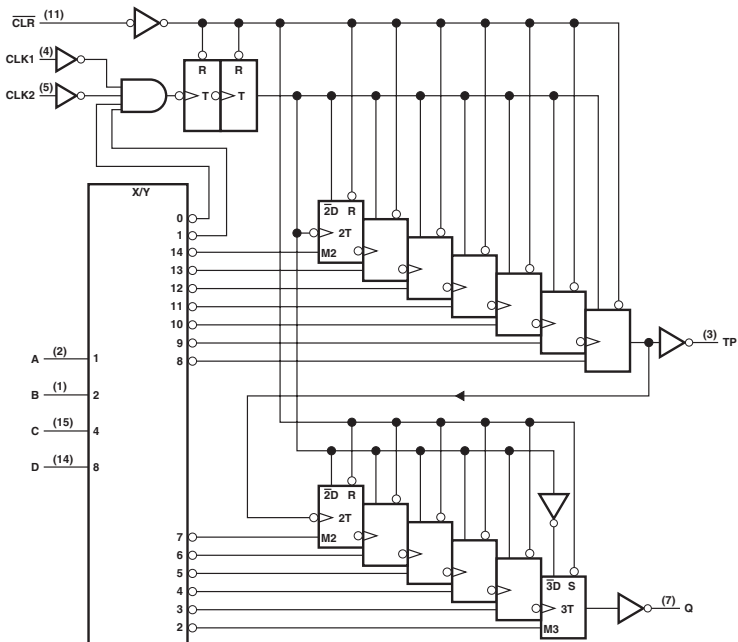
UNIT f_{max}: MHz, other: ns

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from 2^2 to 2^{15}
- Easily Expandable
- Applications

Frequency Division
Digital Timing

Logic Diagram



FUNCTION TABLE

| PROGRAMMING INPUTS | | | | FREQUENCY DIVISION | | | |
|--------------------|---|---|---|--------------------|---------|----------------|---------|
| | | | | Q | | TP | |
| D | C | B | A | BINARY | DECIMAL | BINARY | DECIMAL |
| L | L | L | L | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | L | H | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | H | L | 2 ² | 4 | 2 ⁹ | 512 |
| L | L | H | H | 2 ³ | 8 | 2 ⁹ | 512 |
| L | H | L | L | 2 ⁴ | 16 | 2 ⁹ | 512 |
| L | H | L | H | 2 ⁵ | 32 | 2 ⁹ | 512 |
| L | H | H | L | 2 ⁶ | 64 | 2 ⁹ | 512 |
| L | H | H | H | 2 ⁷ | 128 | Disabled | Low |
| H | L | L | L | 2 ⁸ | 256 | 2 ² | 4 |
| H | L | L | H | 2 ⁹ | 512 | 2 ³ | 8 |
| H | L | H | L | 2 ¹⁰ | 1024 | 2 ⁴ | 16 |
| H | L | H | H | 2 ¹¹ | 2048 | 2 ⁵ | 32 |
| H | H | L | L | 2 ¹² | 4096 | 2 ⁶ | 64 |
| H | H | L | H | 2 ¹³ | 8192 | 2 ⁷ | 128 |
| H | H | H | L | 2 ¹⁴ | 16384 | 2 ⁸ | 256 |
| H | H | H | H | 2 ¹⁵ | 32768 | 2 ⁹ | 512 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

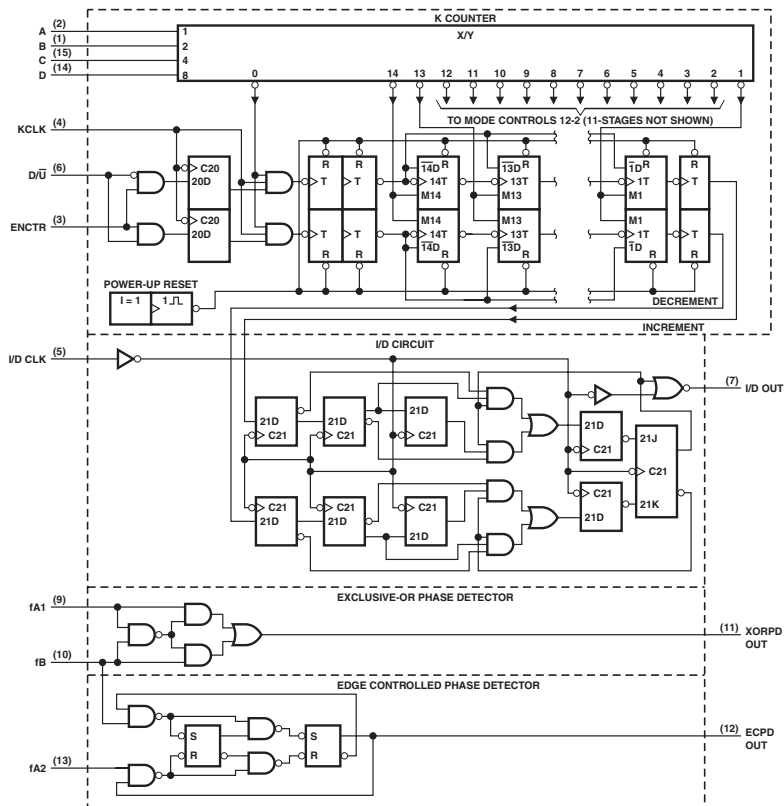
| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 50 | mA |
| I _{OH} | MAX | -1.2 | V |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|-------------------------|-----------------------|------------|-----|
| f _{max} | CLK | | MIN | 30 |
| t _w | CLK 1 or 2 | | MIN | 16 |
| | CLR | | MIN | 35 |
| t _{PLH} | CLK 1 or 2 | Q | MAX | 90 |
| t _{PHL} | | | | 120 |
| t _{PLH} | $\overline{\text{CLR}}$ | $\overline{\text{Q}}$ | MAX | 65 |

 UNIT f_{max}: MHz, other: ns

Logic Diagram (SN74LS)



FUNCTION TABLES (SN74LS)

**K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)**

| D | C | B | A | MODULO (K) |
|---|---|---|---|-----------------|
| L | L | L | L | Inhibited |
| L | L | L | H | 2 ² |
| L | L | H | L | 2 ⁴ |
| L | L | H | H | 2 ⁵ |
| L | H | L | L | 2 ⁶ |
| L | H | L | H | 2 ⁷ |
| L | H | H | L | 2 ⁸ |
| L | H | H | H | 2 ⁹ |
| H | L | L | L | 2 ¹⁰ |
| H | L | L | H | 2 ¹¹ |
| H | L | H | L | 2 ¹² |
| H | L | H | H | 2 ¹³ |
| H | H | L | L | 2 ¹⁴ |
| H | H | L | H | 2 ¹⁵ |
| H | H | H | L | 2 ¹⁶ |
| H | H | H | H | 2 ¹⁷ |

EXCLUSIVE OR PHASE DETECTOR

| $\phi A1$ | ϕB | XORPD OUT |
|-----------|----------|-----------|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

EDGE-CONTROLLED PHASE DETECTOR

| $\phi A2$ | ϕB | ECPD OUT |
|-----------|----------|-----------|
| H or L | ↓ | H |
| ↓ | H or L | L |
| H or L | ↑ | No change |
| ↑ | H or L | No change |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | CD74 HC | CD74 HCT | CD74 ACT | UNIT |
|-----------|------------|-----|---------|----------|----------|------|
| I_{CC} | MAX | 120 | 0.16 | 0.16 | 0.08 | mA |
| I_{OH} | I/D OUT | MAX | -1 | -6 | -4 | -24 |
| | XDR, ECPD | MAX | -0.4 | | | |
| I_{OL} | I/D OUT | MAX | 24 | 4 | 4 | 24 |
| | XDR, ECPD | MAX | 8 | | | |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

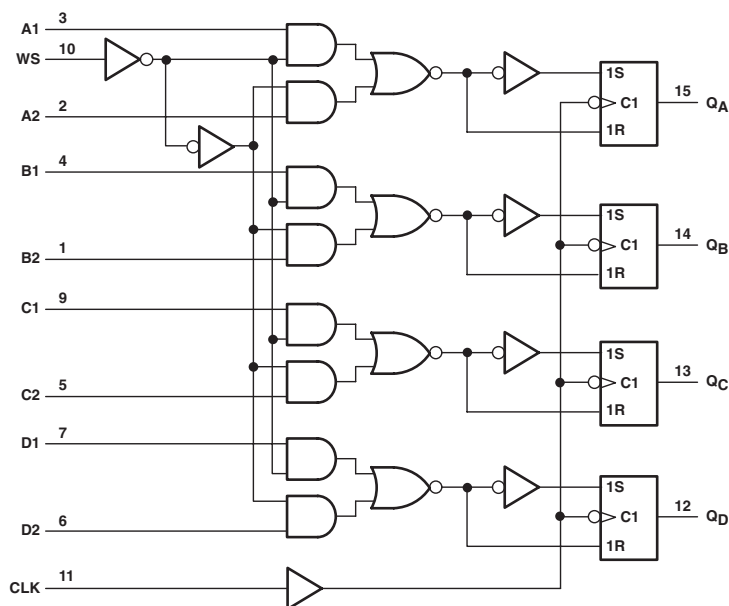
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | CD74 HC | CD74 HCT | CD74 ACT |
|-----------|------------------------|------------------|------------|-----|---------|----------|----------|
| f_{max} | K CLK (K_{CP}) | I/D OUT | MIN | 32 | 20 | 20 | 45 |
| | I/D CLK (I/D_{CP}) | I/D OUT | | 16 | 13 | 13 | 35 |
| t_w | K CLK (K_{CP}) | | MIN | 16 | 24 | 24 | 8 |
| | I/D CLK (I/D_{CP}) | | | 33 | 38 | 38 | 9 |
| t_{SU} | \bar{D}/U | | MIN | 30 | 30 | 30 | 17 |
| | ENCLR (EN_{CTR}) | | | 31 | 30 | 30 | 16 |
| t_h | \bar{D}/U | | MIN | 0 | 0 | 0 | 7 |
| | ENCLR (EN_{CTR}) | | | 0 | 0 | 0 | 6 |
| t_{PLH} | I/D CLK ↑ | I/D OUT | MAX | 25 | 53 | 53 | 24 |
| t_{PHL} | | | | 35 | 53 | 53 | 24 |
| t_{PLH} | $\phi A1$ or ϕB | other INPUT low | XORPD OUT | MAX | 15 | 45 | 45 |
| | | other INPUT high | | | 25 | 45 | 45 |
| t_{PHL} | $\phi A1$ or ϕB | other INPUT low | XORPD OUT | MAX | 25 | 45 | 45 |
| | | other INPUT high | | | 25 | 45 | 45 |
| t_{PLH} | ϕB ↓ | ECPD OUT | MAX | 30 | 60 | 60 | |
| t_{PHL} | $\phi A2$ ↓ | ECPD OUT | | 30 | 60 | 60 | |

 UNIT f_{max} : MHz, other : ns

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Outputs Storage Register

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|-------------|-------|-----------------|-----------------|-----------------|-----------------|
| WORD SELECT | CLOCK | Q _A | Q _B | Q _C | Q _D |
| L | ↓ | A1 | B1 | C1 | D1 |
| H | ↓ | A2 | B2 | C2 | D2 |
| X | H | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |

† a1, a2, etc. = the level of steady-state input at A1, A2, etc.
 Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent O transition of CLK

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | AS | SN74 HC | UNIT |
|-----------------|------------|------|------|----|---------|------|
| I _{CC} | MAX | 65 | 21 | 36 | 0.08 | mA |
| I _{OL} | MAX | 16 | 8 | 20 | 4 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -2 | -4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

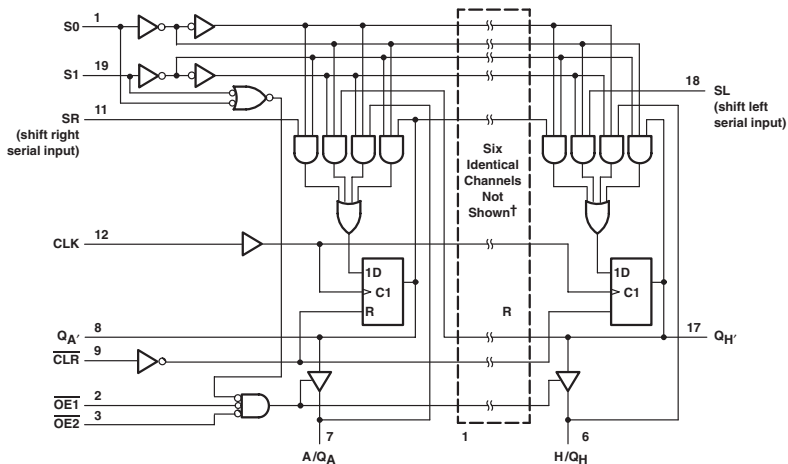
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | AS | SN74 HC | |
|------------------|-------|--------|-------------|----------|-----|----|---------|----|
| t _w | | | MIN | 20 | 20 | 8 | 27 | |
| t _{su} | | | Data | MIN | 15 | 15 | 4.5 | 21 |
| | | | Word Select | MIN | 25 | 25 | 13 | 21 |
| t _h | | | Data | MIN | 5 | 5 | 3.5 | 0 |
| | | | Word Select | MIN | 0 | 0 | 1 | 0 |
| t _{PLH} | | | CLK | GA to GD | MAX | 27 | 27 | 9 |
| t _{PHL} | MAX | 32 | | | 32 | 11 | 31 | |

UNIT: ns

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

FUNCTION TABLE (SN74)

| MODE | INPUTS | | | | | | | | I/O PORTS | | | | | | | | OUTPUTS | |
|-------------|--------|----|----|------|------|-----|----|----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|
| | CLR | S1 | S0 | OE1† | OE2† | CLK | SL | SR | A/Q _A | B/Q _B | C/Q _C | D/Q _D | E/Q _E | F/Q _F | G/Q _G | H/Q _H | Q _A | Q _H |
| Clear | L | X | L | L | L | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X |
| Hold | H | L | L | L | L | X | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} | Q _{E0} | Q _{F0} | Q _{G0} | Q _{H0} | Q _{A0} | Q _{H0} |
| | H | X | X | L | L | L | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} | Q _{E0} | Q _{F0} | Q _{G0} | Q _{H0} | Q _{A0} | Q _{H0} |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | Q _{An} | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | H | Q _{Gn} |
| | H | L | H | L | L | ↑ | X | L | L | Q _{An} | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | L | Q _{Gn} |
| Shift Left | H | H | L | L | L | ↑ | L | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | Q _{Hn} | H | Q _{Bn} | H |
| | H | H | L | L | L | ↑ | L | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | Q _{Hn} | L | Q _{Bn} | L |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a | h |

NOTE: a...h—the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.
 † When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation/clearing of the register is not affected.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | S | ALS | F | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT | UNIT |
|-----------------|------------------------------------|------------|------|------|------|----|---------|----------|---------|----------|------|
| I _{CC} | | MAX | 53 | 225 | 40 | 95 | 0.16 | 0.16 | 0.16 | 0.16 | mA |
| I _{OH} | Q _A thru Q _H | MAX | -2.6 | -6.5 | -2.6 | -3 | -6 | -4 | -24 | -24 | mA |
| | Q _A or Q _H † | | | | | | | | | | |
| I _{OL} | Q _A thru Q _H | MAX | 24 | 20 | 24 | 24 | 6 | 4 | 24 | 24 | mA |
| | Q _A or Q _H † | | | | | | | | | | |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

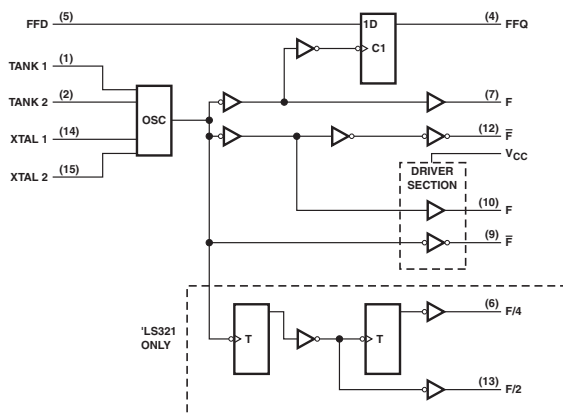
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | F | CD74 HC | CD74 HCT | CD74 AC | CD74 ACT |
|------------------|-------------------|--|--------|------------|----|----|------|------|---------|----------|---------|----------|
| f _{max} | | | | MIN | 20 | 50 | 30 | 70 | 20 | 16 | 95 | 90 |
| t _w | CLK (CP) high | | | MIN | 30 | 10 | 16.5 | 7 | 24 | 30 | 5.2 | 5.5 |
| | CLK (CP) low | | | | 10 | 10 | 16.5 | 7 | 24 | 30 | 5.2 | 5.5 |
| | CLR (MR) | | | | 20 | 10 | 10 | 7 | 15 | 22 | 5 | 5 |
| t _{su} | DATA "H" | | | MIN | 20 | 7 | 16 | 5.5 | 36 | 30 | 4.5 | 4.5 |
| | DATA "L" | | | | 20 | 5 | 6 | 5.5 | 36 | 30 | 4.5 | 4.5 |
| | SELECT | | | | 35 | 15 | 20 | 8.5 | 36 | 41 | 9 | 9 |
| | CLR (MR) INACTIVE | | | | 20 | 10 | 15 | 7 | - | - | - | - |
| t _h | DATA | | | MIN | 0 | 5 | 0 | 2 | 0 | 0 | 0 | 0 |
| | SELECT | | | | 10 | 5 | 0 | 0 | 0 | 0 | 0 | 0 |
| †P _{LH} | CLK (CD74: CP) | Q _A or Q _H (CD74: Q ₀ or Q ₇) | | MAX | 33 | 20 | 15 | 10 | 60 | 68 | 12.9 | 12.9 |
| †P _{HL} | | | | | 39 | 20 | 18 | 9.5 | 60 | 68 | 12.9 | 12.9 |
| †P _{LH} | CLK (CD74: CP) | Q _A thru Q _H (CD74: I/O ₀ thru I/O ₇) | | MAX | 25 | 21 | 13 | 10 | 60 | 68 | 13.5 | 14.5 |
| †P _{HL} | | | | | 39 | 21 | 19 | 12 | 60 | 68 | 13.5 | 14.5 |
| †P _{HL} | CLR | Q _A or Q _H (CD74: Q ₀ or Q ₇) | | MAX | 40 | 21 | 22 | 10.5 | 60 | 69 | 11.2 | 12.2 |
| †P _{HL} | CLR | Q _A thru Q _H (CD74: I/O ₀ thru I/O ₇) | | | 40 | 24 | 22 | 15 | 60 | 69 | 13.9 | 18.6 |
| †P _{ZH} | OE1, OE2 | Q _A thru Q _H | | MAX | 21 | 18 | 16 | 9 | 47 | 48 | 14.9 | 14.9 |
| †P _{ZL} | | | | | 30 | 18 | 22 | 11 | 39 | 45 | 14.9 | 14.9 |
| †P _{HZ} | OE1, OE2 | Q _A thru Q _H | | MAX | 20 | 12 | 8 | 7 | 56 | 56 | 14.9 | 14.9 |
| †P _{ZL} | | | | | 15 | 12 | 15 | 6.5 | 47 | 48 | 14.9 | 14.9 |

UNIT f_{max}: MHz, other: ns

CRYSTAL-CONTROLLED OSCILLATORS

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|----------------------------------|------------|------|------|
| I _{CC} | | MAX | 75 | mA |
| I _{OH} | F ⁻ or F ⁻ | MAX | -24 | mA |
| | F, F ⁻ , F/2, F/4 | MAX | -0.4 | mA |
| I _{OL} | F ⁻ or F ⁻ | MAX | 24 | mA |
| | F, F ⁻ , F/2, F/4 | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

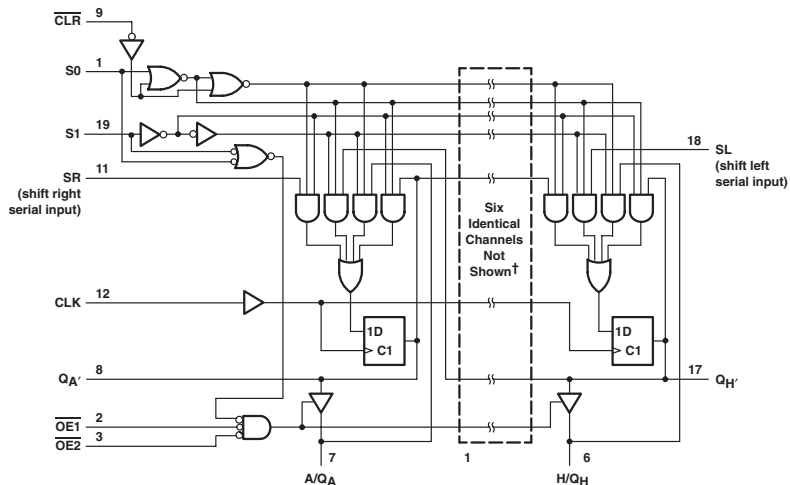
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|-------|---------------------------------|------------|----|
| f _{max} | | F/2 | MIN | 10 |
| | | F/4 | MAX | 5 |
| | | ANY | MIN | 20 |
| t _r | | F ⁻ , F ⁻ | MAX | 14 |
| | | ANY | MAX | 40 |
| t _f | | F ⁻ , F ⁻ | MAX | 10 |
| | ANY | MAX | 20 | |

UNIT f_{max} : MHz, other : ns

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74ALS)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

FUNCTION TABLE (SN74)

| MODE | INPUTS | | | | | | | | I/O BOND | | | | | | | | OUTPUTS | |
|----------------|--------|--------|--------|----------------|--------|--------|--------|--------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| | CLR | SELECT | | OUTPUT CONTROL | | CLK | SREAL | | A/QA | B/QB | C/QC | C/QD | C/QE | C/QF | C/QG | H/QH | QA' | QH' |
| | | S1 | S0 | OE1† | OE2† | | SL | SR | | | | | | | | | | |
| Clear | L L | X L | L X | L L | L L | ↑ ↑ | X X | X X | L L | L L | L L | L L | L L | L L | L L | L L | L L | L L |
| Hold | H H | L X | L X | L L | L L | X L | X X | X X | QA0 QA0 | QB0 QB0 | QC0 QC0 | QD0 QD0 | QE0 QE0 | QF0 QF0 | QG0 QG0 | QH0 QH0 | QA0 QA0 | QH0 QH0 |
| Shift Right | H H | L L | H H | L L | L L | ↑ ↑ | X X | H L | H L | QA QA | QB QB | QC QC | QD QD | QE QE | QF QF | QG QG | H L | QA QA |
| Shift Left | H H | H H | L L | L L | L L | ↑ ↑ | H L | X X | QB QB | QC QC | QD QD | QE QE | QF QF | QG QG | QH QH | L L | QB QB | H L |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a | h |

† a ...t he level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | CD74 AC | CD74 ACT | UNIT |
|-----------|------------|------|------|------------|-------------|------|
| | | | | | | |
| Icc | MAX | 225 | 40 | 0.16 | 0.16 | mA |
| Ioh | QA' or QH' | -0.5 | -0.4 | -24 | -24 | mA |
| | | -6.5 | -2.6 | -24 | -24 | mA |
| Iol | QA' or QH' | 6 | 8 | 24 | 24 | mA |
| | | 20 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

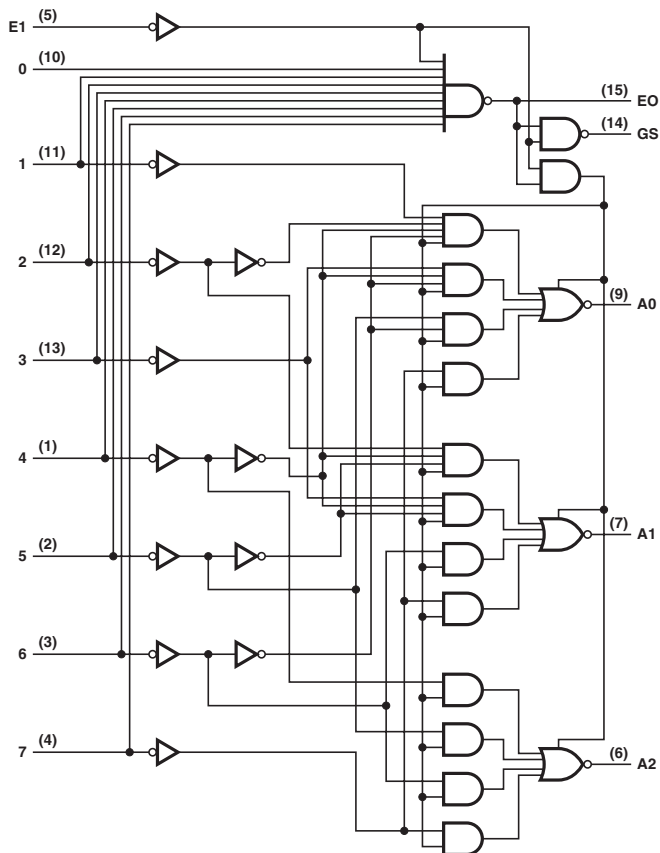
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | CD74 AC | CD74 ACT | |
|-----------|--------|--------|------------|-----|------|------------|-------------|------|
| | | | | | | | | |
| fmax | | | MIN | 25 | 17 | 95 | 90 | |
| tw | CLK | | MIN | 30 | 16.5 | 5.2 | 5.5 | |
| | CLR | | MIN | 20 | - | 5 | 5 | |
| tsu | DATA H | | MIN | 20 | 16 | 4.5 | 4.5 | |
| | DATA L | | | 20 | 6 | 4.5 | 4.5 | |
| | SELECT | | | - | 20 | 9 | 9 | |
| | CLR | | | - | 20 | 5.5 | 5.5 | |
| th | SELECT | | MIN | - | 0 | 0 | 0 | |
| | DATA | | MIN | 0 | 0 | 0 | 0 | |
| TPHL | | CLK | QA' or QB' | MAX | 33 | 15 | 12.9 | 12.9 |
| TPHL | | CLK | QA thru QH | MAX | 39 | 18 | 12.9 | 12.9 |
| TPHL | | CLK | QA thru QH | MAX | 25 | 13 | 13.5 | 14.5 |
| TPHL | | CLK | QA thru QH | MAX | 39 | 19 | 13.5 | 14.5 |
| TPZH | | OE1 | QA thru QH | MAX | 21 | 16 | 14.9 | 14.9 |
| TPZL | | OE1 | QA thru QH | MAX | 30 | 22 | 14.9 | 14.9 |
| TPZH | | OE1 | QA thru QH | MAX | 20 | 8 | 14.9 | 14.9 |
| TPHZ | | OE1 | QA thru QH | MAX | 15 | 15 | 14.9 | 14.9 |
| TPZH | | OE2 | QA thru QH | MAX | 21 | 16 | 14.9 | 14.9 |
| TPZL | | OE2 | QA thru QH | MAX | 30 | 22 | 14.9 | 14.9 |
| TPHZ | | OE2 | QA thru QH | MAX | 20 | 8 | 14.9 | 14.9 |
| TPHZ | | OE2 | QA thru QH | MAX | 15 | 15 | 14.9 | 14.9 |

UNIT fmax : MHz, other : ns

8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)

Logic Diagram



FUNCTION TABLE

| E1 | INPUTS | | | | | | | OUTPUTS | | | | | |
|----|--------|---|---|---|---|---|---|---------|----|----|----|----|----|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | E0 |
| H | X | X | X | X | X | X | X | X | Z | Z | Z | H | H |
| L | H | H | H | H | H | H | H | H | Z | Z | Z | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|------------|------------|------|------|
| Icc | | MAX | 25 | mA |
| I _{OH} | A0, A1, A2 | MAX | -2.6 | mA |
| | E0, ES | MAX | -0.4 | mA |
| I _{OL} | A0, A1, A2 | MAX | 24 | mA |
| | E0, ES | MAX | 8 | mA |

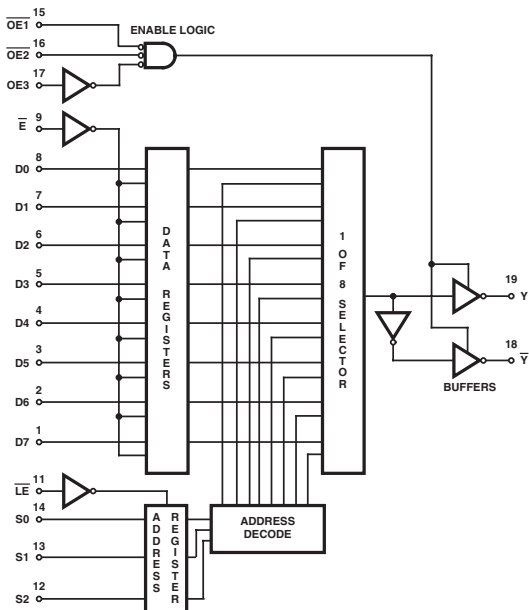
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|--------|------------|------------|----|
| t _{PLH} | 1 to 7 | A0, A1, A2 | MAX | 35 |
| | | | MAX | 35 |
| t _{PHL} | 0 to 7 | E0 | MAX | 18 |
| | | | MAX | 40 |
| t _{PLH} | 0 to 7 | GS | MAX | 55 |
| | | | MAX | 21 |

UNIT: ns

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT/REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram
(CD74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT ENABLES | | | OUTPUTS | | |
|---------|----|---|----------------|----|----|---------|-----|-----|
| SELECT† | DC | | G1 | G2 | G3 | W | Y | |
| X | X | X | X | H | X | X | Z | Z |
| X | X | X | X | X | H | X | Z | Z |
| X | X | X | X | X | X | L | Z | Z |
| L | L | L | L | L | L | H | D0 | D0 |
| L | L | L | H | L | L | H | D0n | D0n |
| L | L | H | L | L | L | H | D1 | D1 |
| L | L | H | H | L | L | H | D1n | D1n |
| L | H | L | L | L | L | H | D2 | D2 |
| L | H | L | H | L | L | H | D2n | D2n |
| L | H | H | L | L | L | H | D3 | D3 |
| L | H | H | H | L | L | H | D3n | D3n |
| H | L | L | L | L | L | H | D4 | D4 |
| H | L | L | H | L | L | H | D4n | D4n |
| H | L | H | L | L | L | H | D5 | D5 |
| H | L | H | H | L | L | H | D5n | D5n |
| H | H | L | L | L | L | H | D6 | D6 |
| H | H | L | H | L | L | H | D6n | D6n |
| H | H | H | L | L | L | H | D7 | D7 |
| H | H | H | H | L | L | H | D7n | D7n |

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), X = Don't Care, Z = High Impedance State (Off State), D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with \overline{LE} low.

TRUTH TABLE (CD74)

| INPUTS | | | | | | | OUTPUTS | |
|-----------------|----|----|----------------|------------------|------------------|------------------|----------------|-----|
| SELECT (NOTE 3) | | | ENABLE DATA | OUTPUT ENABLES | | | | |
| S2 | S1 | S0 | \overline{E} | $\overline{OE1}$ | $\overline{OE2}$ | $\overline{OE3}$ | \overline{Y} | Y |
| X | X | X | X | H | X | X | Z | Z |
| X | X | X | X | X | H | X | Z | Z |
| X | X | X | X | X | X | L | Z | Z |
| L | L | L | L | L | L | H | D0 | D0 |
| L | L | L | H | L | L | H | D0n | D0n |
| L | L | H | L | L | L | H | D1 | D1 |
| L | L | H | H | L | L | H | D1n | D1n |
| L | H | L | L | L | L | H | D2 | D2 |
| L | H | L | H | L | L | H | D2n | D2n |
| L | H | H | L | L | L | H | D3 | D3 |
| L | H | H | H | L | L | H | D3n | D3n |
| H | L | L | L | L | L | H | D4 | D4 |
| H | L | L | H | L | L | H | D4n | D4n |
| H | L | H | L | L | L | H | D5 | D5 |
| H | L | H | H | L | L | H | D5n | D5n |
| H | H | L | L | L | L | H | D6 | D6 |
| H | H | L | H | L | L | H | D6n | D6n |
| H | H | H | L | L | L | H | D7 | D7 |
| H | H | H | H | L | L | H | D7n | D7n |

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

NOTE:

- This column shows the input address setup with \overline{CE} low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

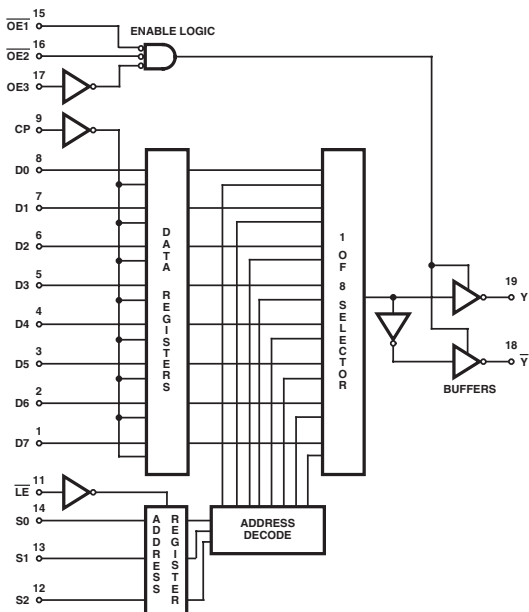
| PARAMETER | MAX or MIN | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|---------|---------|----------|------|
| I _{CC} | MAX | 46 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -6 | -6 | -4 | mA |
| I _{OL} | MAX | 24 | 6 | 6 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|-------------------------|-------------------------|------------|----|---------|---------|----------|
| t _{su} | | | MAX | 15 | 19 | 15 | 15 |
| t _h | | | MAX | 15 | 5 | 14 | 14 |
| t _{PLH} | D0 thru D7 | Y | MAX | 36 | 59 | 63 | 71 |
| t _{PHL} | | | MAX | 35 | 59 | 63 | 71 |
| t _{PLH} | D0 thru D7 | W | MAX | 27 | 59 | 63 | 71 |
| t _{PHL} | | (CD74: \overline{Y}) | MAX | 44 | 59 | 63 | 71 |
| t _{PLH} | \overline{DC} | Y | MAX | 42 | 68 | 75 | 81 |
| t _{PHL} | (CD74: \overline{E}) | | MAX | 39 | 68 | 75 | 81 |
| t _{PLH} | \overline{DC} | W | MAX | 33 | 68 | 75 | 81 |
| t _{PHL} | (CD74: \overline{E}) | (CD74: \overline{Y}) | MAX | 50 | 68 | 75 | 81 |

UNIT:ns

Logic Diagram
(CD74)



FUNCTION TABLE (SN74)

| INPUTS | | | | OUTPUTS | | | | |
|---------|----|----|------|----------------|----|----|-----|-----|
| SELECT† | | | CLK | OUTPUT ENABLES | | | | |
| C2 | C1 | C0 | | G1 | G2 | G3 | W | Y |
| X | X | X | X | H | X | X | Z | Z |
| X | X | X | X | X | H | X | Z | Z |
| X | X | X | X | X | X | L | Z | Z |
| L | L | L | ↑ | L | L | H | D0 | D0 |
| L | L | L | HorL | L | L | H | D0n | D0n |
| L | L | H | ↑ | L | L | H | D1 | D1 |
| L | L | H | HorL | L | L | H | D1n | D1n |
| L | H | L | ↑ | L | L | H | D2 | D2 |
| L | H | L | HorL | L | L | H | D2n | D2n |
| L | H | H | ↑ | L | L | H | D3 | D3 |
| L | H | H | HorL | L | L | H | D3n | D3n |
| H | L | L | ↑ | L | L | H | D4 | D4 |
| H | L | L | HorL | L | L | H | D4n | D4n |
| H | L | H | ↑ | L | L | H | D5 | D5 |
| H | L | H | HorL | L | L | H | D5n | D5n |
| H | H | L | ↑ | L | L | H | D6 | D6 |
| H | H | L | HorL | L | L | H | D6n | D6n |
| H | H | H | ↑ | L | L | H | D7 | D7 |
| H | H | H | HorL | L | L | H | D7n | D7n |

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), ↑ = Transition from Low to High Level, X = Don't Care, Z = High Impedance State (Off State), D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with \overline{LE} low.

TRUTH TABLE (CD74)

| INPUTS | | | | | | | OUTPUTS | |
|-----------------|----|----|-------|----------------|-----|-----|----------------|-----|
| SELECT (NOTE 3) | | | CLOCK | OUTPUT ENABLES | | | \overline{Y} | Y |
| S2 | S1 | S0 | CP | OE1 | OE2 | OE3 | \overline{Y} | Y |
| X | X | X | X | H | X | X | Z | Z |
| X | X | X | X | X | X | H | Z | Z |
| X | X | X | X | X | X | L | Z | Z |
| L | L | L | ↑ | L | L | H | D0 | D0 |
| L | L | L | HorL | L | L | H | D0n | D0n |
| L | L | L | ↑ | L | L | H | D1 | D1 |
| L | L | L | HorL | L | L | H | D1n | D1n |
| L | L | L | ↑ | L | L | H | D2 | D2 |
| L | L | L | HorL | L | L | H | D2n | D2n |
| L | L | L | ↑ | L | L | H | D3 | D3 |
| L | L | L | HorL | L | L | H | D3n | D3n |
| L | L | L | ↑ | L | L | H | D4 | D4 |
| L | L | L | HorL | L | L | H | D4n | D4n |
| L | L | L | ↑ | L | L | H | D5 | D5 |
| L | L | L | HorL | L | L | H | D5n | D5n |
| L | L | L | ↑ | L | L | H | D6 | D6 |
| L | L | L | HorL | L | L | H | D6n | D6n |
| L | L | L | ↑ | L | L | H | D7 | D7 |
| L | L | L | HorL | L | L | H | D7n | D7n |
| H | L | L | ↑ | L | L | H | D4 | D4 |
| H | L | L | HorL | L | L | H | D4n | D4n |
| H | L | L | ↑ | L | L | H | D5 | D5 |
| H | L | L | HorL | L | L | H | D5n | D5n |
| H | L | L | ↑ | L | L | H | D6 | D6 |
| H | L | L | HorL | L | L | H | D6n | D6n |
| H | L | L | ↑ | L | L | H | D7 | D7 |
| H | L | L | HorL | L | L | H | D7n | D7n |
| H | L | L | ↑ | L | L | H | D4 | D4 |
| H | L | L | HorL | L | L | H | D4n | D4n |
| H | L | L | ↑ | L | L | H | D5 | D5 |
| H | L | L | HorL | L | L | H | D5n | D5n |
| H | L | L | ↑ | L | L | H | D6 | D6 |
| H | L | L | HorL | L | L | H | D6n | D6n |
| H | L | L | ↑ | L | L | H | D7 | D7 |
| H | L | L | HorL | L | L | H | D7n | D7n |

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level; X = Don't Care; Z = High-Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

NOTE:

- This column shows the input address setup with \overline{LE} low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | SN74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|---------|----------|------|
| I _{CC} | MAX | 46 | 0.08 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -6 | -4 | mA |
| I _{OL} | MAX | 24 | 6 | 4 | mA |

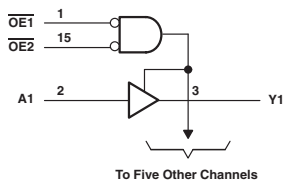
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC | CD74 HCT |
|------------------|------------|-----------------|------------|----|---------|----------|
| t _{su} | D0 thru D7 | | MIN | 15 | 19 | 11 |
| t _h | D0 thru D7 | | MIN | 0 | 5 | 14 |
| t _{PLH} | CLK | Y | MAX | 27 | 64 | 77 |
| t _{PHL} | | | | 50 | 64 | 77 |
| t _{PLH} | CLK | W (CD74 : Y) | MAX | 36 | 64 | 77 |
| t _{PHL} | | | | 27 | 64 | 77 |
| t _{PLH} | S0, S1, S2 | Y | MAX | 45 | 71 | 89 |
| t _{PHL} | | | | 48 | 71 | 89 |
| t _{PLH} | S0, S1, S2 | W (CD74 : Y) | MAX | 54 | 71 | 89 |
| t _{PHL} | | | | 45 | 71 | 89 |

UNIT: ns

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)



FUNCTION TABLE (SN74) (each buffer/driver)

| INPUTS | | | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------|------|---------|---------|----------|------|
| I_{CC} | MAX | 85 | 24 | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -5.2 | -2.6 | -6 | -6 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 6 | 6 | 4 | mA |

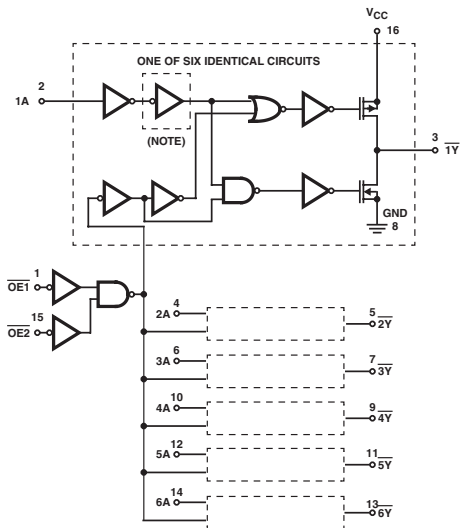
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|-----------|--|--------|------------|-----|----|---------|---------|----------|
| t_{PLH} | A | Y | MAX | 16 | 15 | 24 | 32 | 38 |
| t_{PHL} | | | MAX | 22 | 18 | 24 | 32 | 38 |
| t_{PZH} | \overline{G} (CD74: \overline{OE}) | Y | MAX | 35 | 35 | 48 | 45 | 53 |
| t_{PZL} | | | MAX | 37 | 45 | 48 | 45 | 53 |
| t_{PHZ} | \overline{G} (CD74: \overline{OE}) | Y | MAX | 11 | 32 | 48 | 45 | 53 |
| t_{PLZ} | | | MAX | 27 | 35 | 48 | 45 | 53 |

UNIT: ns

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram
(CD74HC)



NOTE: Inverter not included in HC/HCT365.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (OUTPUTS FOR HC/HCT365 ARE COMPLEMENTS OF THOSE SHOWN, I.E., 1Y, 2Y, ETC.)

FUNCTION TABLE (CD74)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | H |
| L | L | H | L |
| X | H | X | Z |
| H | X | X | Z |

NOTES:

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance (OFF) State

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | UNIT |
|-----------|------------|------|------|---------|---------|------|
| I_{CC} | MAX | 77 | 21 | 0.08 | 160 | mA |
| I_{OH} | MAX | -5.2 | -2.6 | -6 | -6 | mA |
| I_{OL} | MAX | 32 | 24 | 6 | 6 | mA |

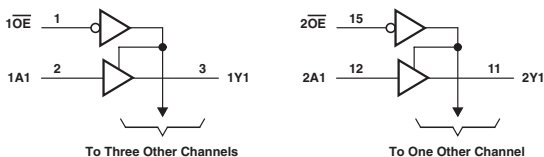
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC |
|-----------|--------------------------|--------------------------|------------|-----|----|---------|---------|
| t_{PLH} | A | Y (CD74 : \bar{Y}) | MAX | 17 | 15 | 24 | 33 |
| t_{PHL} | | | MAX | 16 | 18 | 24 | 33 |
| t_{PZH} | \bar{G} (CD74 : OE) | Y (CD74 : \bar{Y}) | MAX | 35 | 35 | 48 | 45 |
| t_{PZL} | | | MAX | 37 | 45 | 48 | 45 |
| t_{PHZ} | \bar{G} (CD74 : OE) | Y (CD74 : \bar{Y}) | MAX | 11 | 32 | 48 | 45 |
| t_{PLZ} | | | MAX | 27 | 35 | 48 | 45 |

UNIT:ns

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)

FUNCTION TABLE (SN74)
(each buffer/driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------|------------|------|------|---------|---------|----------|------|------|-------|-------|------|
| I_{CC} | MAX | 85 | 24 | 0.08 | 0.16 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I_{OH} | MAX | -5.2 | -2.6 | -6 | -6 | -4 | -8 | -8 | -8 | -16 | mA |
| I_{OL} | MAX | 32 | 24 | 6 | 6 | 4 | 8 | 8 | 8 | 16 | mA |

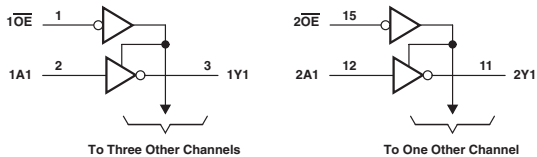
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | AHC | AHCT | LV 3V | LV 5V |
|-----------|-----------------|--------|------------|-----|----|---------|---------|----------|------|------|-------|-------|
| t_{PLH} | A | Y | MAX | 16 | 16 | 24 | 32 | 38 | 9 | 6.5 | 13.5 | 9 |
| t_{PHL} | | | MAX | 22 | 22 | 24 | 32 | 38 | 9 | 6.5 | 13.5 | 9 |
| t_{PZH} | \overline{OE} | Y | MAX | 35 | 35 | 48 | 45 | 53 | 10.5 | 9.5 | 16 | 10.5 |
| t_{PZL} | | | MAX | 47 | 40 | 48 | 45 | 53 | 10.5 | 8.5 | 16 | 10.5 |
| t_{PHZ} | \overline{OE} | Y | MAX | 11 | 30 | 48 | 45 | 53 | 10.5 | 9.5 | 15.5 | 10.5 |
| t_{PLZ} | | | MAX | 27 | 35 | 48 | 45 | 53 | 10.5 | 8.5 | 15.5 | 10.5 |

UNIT: ns

HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)

FUNCTION TABLE (SN74)
(each buffer/driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------|------|---------|---------|----------|------|
| I_{CC} | MAX | 77 | 21 | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -5.2 | -2.6 | -6 | -6 | -4 | mA |
| I_{OL} | MAX | 32 | 24 | 6 | 6 | 4 | mA |

SWITCHING CHARACTERISTICS

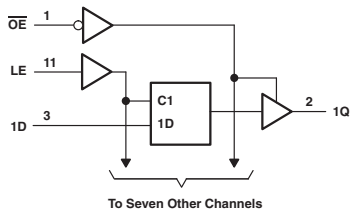
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|-----------|-------|--------|------------|-----|----|---------|---------|----------|
| t_{PLH} | A | Y | MAX | 17 | 15 | 24 | 32 | 45 |
| t_{PHL} | | | MAX | 16 | 18 | 24 | 32 | 45 |
| t_{PZH} | OE | Y | MAX | 35 | 35 | 48 | 45 | 53 |
| t_{PZL} | | | MAX | 37 | 45 | 48 | 45 | 53 |
| t_{PHZ} | OE | Y | MAX | 11 | 32 | 48 | 45 | 53 |
| t_{PLZ} | | | MAX | 27 | 35 | 48 | 45 | 53 |

UNIT: ns

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving True Outputs
- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| OUTPUT CONTROL | INPUTS | | OUTPUT Q |
|----------------|--------|---|----------|
| | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q0 |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVTH 3V | UNIT |
|-----------|------------|------|------|------|-----|----|---------|---------|----------|----------|----------|-----|---------|------|
| I_{CC} | MAX | 40 | 190 | 27 | 100 | 55 | 0.08 | 0.16 | 0.08 | 0.16 | 60 | 30 | 5 | mA |
| I_{OH} | MAX | -2.6 | -6.5 | -2.6 | -15 | -3 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | mA |
| I_{OL} | MAX | 24 | 20 | 24 | 48 | 24 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | ALVCH 3V | UNIT |
|-----------|------------|-------|---------|---------|--------|----------|----------|------|------|-------|-------|-------|--------|----------|------|
| I_{CC} | MAX | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | 0.02 | 0.01 | 0.02 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | -16 | -16 | -24 | -24 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | 16 | 16 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT |
|-----------|-----------------|--------|------------|----|-----|-----|------|-----|---------|---------|----------|----------|----------|-----|
| tw | High | | MIN | 15 | 6 | 10 | 4.5 | 6 | 20 | 24 | 25 | 24 | 7.5 | 3.3 |
| | Low | | MIN | 15 | 7.3 | - | - | - | - | - | - | - | - | - |
| tsu | | | MIN | 5 | 0 | 10 | 2 | 2 | 13 | 15 | 13 | 20 | 2 | 1.9 |
| th | | | MIN | 20 | 10 | 7 | 3 | 3 | 12 | 5 | 10 | 15 | 5.5 | 1 |
| tpLH | D | Q | MAX | 18 | 12 | 12 | 6 | 8 | 38 | 45 | 44 | 48 | 9.3 | 5.9 |
| tpHL | | | MAX | 18 | 12 | 16 | 6 | 6 | 38 | 45 | 44 | 48 | 9.5 | 6.2 |
| tpLH | LE | Q | MAX | 30 | 14 | 22 | 11.5 | 13 | 44 | 53 | 44 | 53 | 9.3 | 6.6 |
| tpHL | | | MAX | 30 | 18 | 23 | 7.5 | 8 | 44 | 53 | 44 | 53 | 8.8 | 7.2 |
| tpZH | \overline{DE} | Q | MAX | 28 | 15 | 18 | 6.5 | 12 | 38 | 45 | 44 | 53 | 11.8 | 5.2 |
| tpZL | | | MAX | 36 | 18 | 20 | 9.5 | 8.5 | 38 | 45 | 44 | 53 | 12 | 6.7 |
| tpHZ | \overline{DE} | Q | MAX | 25 | 9 | 10 | 6.5 | 7.5 | 38 | 45 | 44 | 53 | 7 | 6.9 |
| tpLZ | | | MAX | 20 | 12 | 12 | 7 | 6 | 38 | 45 | 44 | 53 | 7.4 | 6.5 |

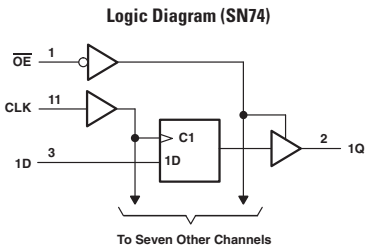
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V |
|-----------|-----------------|--------|------------|---------|-------|---------|---------|--------|----------|----------|------|------|-------|-------|
| tw | High | | MIN | 3 | 4 | 4.5 | 4 | 5 | 8 | 4 | 5 | 6.5 | 5 | 5 |
| | Low | | MIN | - | - | - | 4 | - | - | 4 | - | - | - | - |
| tsu | | | MIN | 1.1 | 3.5 | 4.5 | 2 | 3.5 | 8 | 2 | 4 | 1.5 | 4 | 4 |
| th | | | MIN | 1.4 | 2 | 1 | 3 | 3.5 | 1 | 3 | 1 | 3.5 | 1 | 1 |
| tpLH | D | Q | MAX | 3.9 | 10.3 | 10.5 | 8.5 | 11.8 | 11.5 | 10.4 | 10.5 | 10.5 | 17 | 10.5 |
| tpHL | | | MAX | 3.9 | 8.4 | 10.5 | 8.5 | 10 | 11.5 | 10.4 | 10.5 | 10.5 | 17 | 10.5 |
| tpLH | LE | Q | MAX | 4.2 | 11.3 | 10.5 | 12 | 13 | 11.5 | 12.5 | 10.5 | 14.5 | 16.5 | 10.5 |
| tpHL | | | MAX | 4.2 | 10.2 | 10.5 | 12 | 12.2 | 11.5 | 12.5 | 10.5 | 14.5 | 16.5 | 10.5 |
| tpZH | \overline{DE} | Q | MAX | 4.8 | 10.8 | 9.5 | 10.5 | 12.5 | 10.5 | 13.5 | 11.5 | 13.5 | 17 | 11.5 |
| tpZL | | | MAX | 4.8 | 9.7 | 9.5 | 10.5 | 12 | 10.5 | 13.5 | 11.5 | 13.5 | 17 | 11.5 |
| tpHZ | \overline{DE} | Q | MAX | 4.6 | 11.1 | 12.5 | 11.5 | 12.2 | 12.5 | 12.5 | 10.5 | 12 | 15 | 10.5 |
| tpLZ | | | MAX | 4.5 | 8.7 | 10 | 11.5 | 10.1 | 10 | 12.5 | 10.5 | 12 | 15 | 10.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LV-AT | LVC 3V | ALVCH 3V |
|-----------|-----------------|--------|------------|-------|--------|----------|
| tw | High | | MIN | 8.5 | 3.3 | 3.3 |
| | Low | | MIN | - | - | - |
| tsu | | | MIN | 1.5 | 2 | 0.5 |
| th | | | MIN | 3.5 | 1.5 | 1.2 |
| tpLH | D | Q | MAX | 11 | 6.8 | 3.6 |
| tpHL | | | MAX | 11 | 6.8 | 3.6 |
| tpLH | LE | Q | MAX | 15 | 7.6 | 3.3 |
| tpHL | | | MAX | 15 | 7.6 | 3.3 |
| tpZH | \overline{DE} | Q | MAX | 14 | 7.7 | 4.8 |
| tpZL | | | MAX | 14 | 7.7 | 4.8 |
| tpHZ | \overline{DE} | Q | MAX | 12.5 | 7 | 4.4 |
| tpLZ | | | MAX | 12.5 | 7 | 4.4 |

UNIT fmax : MHz, other : ns

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE (SN74)

| OUTPUT CONTROL | INPUTS | | OUTPUT Q |
|----------------|--------|---|----------------|
| | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVTH 3V | UNIT |
|-----------|------------|------|------|------|-----|----|---------|---------|----------|----------|----------|-----|---------|------|
| I_{CC} | MAX | 40 | 160 | 31 | 128 | 86 | 0.08 | 0.16 | 0.08 | 0.16 | 60 | 30 | 5 | mA |
| I_{OH} | MAX | -2.6 | -6.5 | -2.6 | -15 | -3 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | mA |
| I_{OL} | MAX | 24 | 20 | 24 | 48 | 24 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | ALVCH 3V | UNIT |
|-----------|------------|-------|---------|---------|--------|----------|----------|------|------|-------|-------|--------|----------|------|
| I_{CC} | MAX | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | 0.01 | 0.01 | mA |
| I_{OH} | MAX | -24 | -24 | -24 | -24 | -24 | -24 | -8 | -8 | -8 | -16 | -24 | -24 | mA |
| I_{OL} | MAX | 24 | 24 | 24 | 24 | 24 | 24 | 8 | 8 | 8 | 16 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | S | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT |
|------------------|-------------------|--------|------------|----|-----|-----|-----|------|---------|---------|----------|----------|----------|-----|
| f _{max} | | | MIN | 35 | 75 | 35 | 125 | 70 | 24 | 20 | 25 | 20 | 70 | 150 |
| t _w | High Low | | MIN | 15 | 6 | 14 | 4 | 7 | 20 | 24 | 20 | 24 | 7 | 3.3 |
| | | | MIN | 15 | 7.3 | 14 | 3 | 6 | 20 | 24 | 20 | 24 | - | 3.3 |
| t _{su} | | | MIN | 20 | 5 | 10 | 2 | 2 | 25 | 18 | 25 | 18 | 6.5 | 1.9 |
| t _h | | | MIN | 0 | 2 | 0 | 2 | 2 | 5 | 5 | 10 | 5 | 0 | 2.1 |
| t _{PLH} | CLK (CD74: CP) | Q | MAX | 28 | 15 | 12 | 8 | 10 | 45 | 50 | 45 | 50 | 10.6 | 6.2 |
| t _{PHL} | | | MAX | 28 | 17 | 16 | 9 | 10 | 45 | 50 | 45 | 50 | 10 | 7.1 |
| t _{PZH} | OE | Q | MAX | 26 | 15 | 17 | 6 | 12.5 | 38 | 45 | 38 | 45 | 12.3 | 5.2 |
| t _{PZL} | | | MAX | 28 | 18 | 18 | 10 | 8.5 | 38 | 45 | 38 | 45 | 12.7 | 6.7 |
| t _{PHZ} | OE | Q | MAX | 28 | 9 | 10 | 6 | 8 | 38 | 41 | 38 | 42 | 6.8 | 6.7 |
| t _{PLZ} | | | MAX | 20 | 12 | 18 | 6 | 6.5 | 38 | 41 | 38 | 42 | 6.8 | 6.5 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V |
|------------------|-------------------|--------|------------|---------|-------|---------|---------|--------|----------|----------|------|------|-------|-------|
| f _{max} | | | MIN | 150 | 95 | 100 | 12.5 | 55 | 90 | 110 | 75 | 75 | 50 | 75 |
| t _w | High Low | | MIN | 3.3 | 5 | 4.5 | 4 | 9 | 5 | 4.5 | 5 | 6.5 | 5.5 | 5 |
| | | | MIN | 3.3 | 5 | 4.5 | 4 | 9 | 5 | 4.5 | 5 | 6.5 | 5.5 | 5 |
| t _{su} | | | MIN | 1.5 | 2.5 | 4.5 | 2 | 3 | 5.5 | 2 | 3 | 2.5 | 4.5 | 3 |
| t _h | | | MIN | 0.8 | 3.5 | 1.5 | 2 | 5.5 | 1.5 | 3 | 2 | 2.5 | 2 | 2 |
| t _{PLH} | CLK (CD74: CP) | Q | MAX | 4.5 | 10.2 | 10.5 | 10.8 | 12.4 | 11.5 | 11.2 | 11.5 | 11.5 | 18.5 | 11.5 |
| t _{PHL} | | | MAX | 4.2 | 10.1 | 10 | 10.8 | 13 | 11 | 11.2 | 11.5 | 11.5 | 18.5 | 11.5 |
| t _{PZH} | OE | Q | MAX | 4.7 | 9.1 | 9.5 | 14.5 | 12.3 | 10.5 | 14.5 | 11 | 12.5 | 16.5 | 11 |
| t _{PZL} | | | MAX | 4.7 | 9.4 | 9.5 | 14.5 | 12.3 | 10.5 | 14.5 | 11 | 12.5 | 16.5 | 11 |
| t _{PHZ} | OE | Q | MAX | 4.6 | 11.2 | 12.5 | 14.5 | 13.2 | 12.5 | 14.5 | 10 | 12 | 16 | 10 |
| t _{PLZ} | | | MAX | 4.5 | 9.2 | 10 | 14.5 | 10.8 | 10 | 14.5 | 10 | 12 | 16 | 10 |

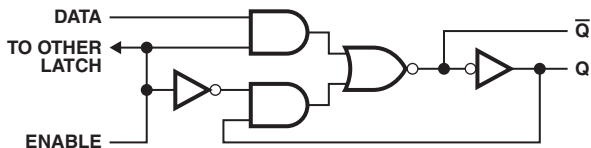
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 3V | ALVCH 3V |
|------------------|-------------|--------|------------|--------|----------|
| f _{max} | | | MIN | 100 | 150 |
| t _w | High Low | | MIN | 3.3 | 3.3 |
| | | | MIN | 3.3 | 3.3 |
| t _{su} | | | MIN | 2 | 1.8 |
| t _h | | | MIN | 1.5 | 0.5 |
| t _{PLH} | CLK | Q | MAX | 7 | 3.6 |
| t _{PHL} | | | MAX | 7 | 3.6 |
| t _{PZH} | OE | Q | MAX | 7.5 | 5.2 |
| t _{PZL} | | | MAX | 7.5 | 5.2 |
| t _{PHZ} | OE | Q | MAX | 6.5 | 4.5 |
| t _{PLZ} | | | MAX | 6.5 | 4.5 |

UNIT f_{max} : MHz, other : ns

4-BIT BISTABLE LATCHES

- Complementary Outputs (Q , \bar{Q})

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUTS Q | |
|--------|---|--------------|-------------|
| D | C | L | H |
| L | H | L | H |
| H | H | H | L |
| X | L | Q_0 | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | SN74 HC | UNIT |
|-----------|------------|------|------------|------|
| I_{CC} | MAX | 12 | 0.04 | mA |
| I_{OH} | MAX | -0.4 | -4 | mA |
| I_{OL} | MAX | 8 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

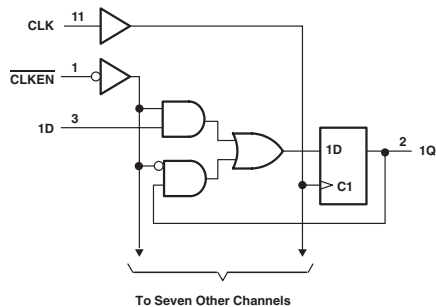
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC |
|-----------|-------|-----------|------------|----|------------|
| t_W | | | MIN | 20 | 20 |
| t_{SU} | | | MIN | 20 | 25 |
| t_H | | | MIN | 0 | 5 |
| t_{PLH} | | | MAX | 27 | 30 |
| t_{PHL} | D | Q | MAX | 17 | 30 |
| t_{PLH} | | | MAX | 20 | 30 |
| t_{PHL} | D | \bar{Q} | MAX | 15 | 30 |
| t_{PLH} | | | MAX | 27 | 33 |
| t_{PHL} | | | MAX | 25 | 33 |
| t_{PLH} | C | Q | MAX | 30 | 33 |
| t_{PHL} | | | MAX | 30 | 33 |
| t_{PLH} | C | \bar{Q} | MAX | 15 | 33 |
| t_{PHL} | | | MAX | 15 | 33 |

UNIT: ns

OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

- Individual Data Input to Each Flip-Flop
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

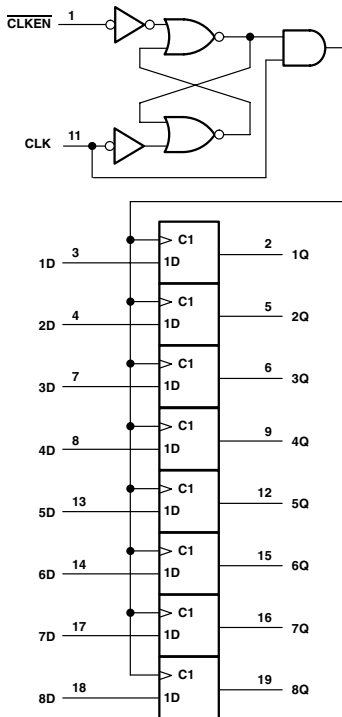
Logic Diagram (SN74ABT)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUTS | |
|--------|-------|------|----------------|-------------|
| CLKEN | CLOCK | DATA | Q | \bar{Q} |
| H | X | X | Q ₀ | \bar{Q}_0 |
| L | ↑ | H | H | L |
| L | ↑ | L | L | H |
| X | L | X | Q ₀ | \bar{Q}_0 |

Logic Diagram (SN74HC)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 | UNIT |
|-----------------|------------|------|----|---------|---------|----------|----------|-----|-------|------|
| I _{CC} | MAX | 28 | 90 | 0.08 | 0.16 | 0.08 | 0.16 | 30 | 0.08 | mA |
| I _{OH} | MAX | -0.4 | -1 | -4 | -4 | -4 | -4 | -32 | -24 | mA |
| I _{OL} | MAX | 8 | 20 | 4 | 4 | 4 | 4 | 64 | 24 | mA |

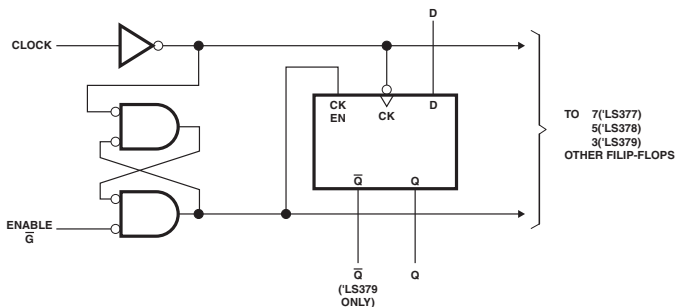
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 |
|------------------|-----------------|--------|------------|----|------|---------|---------|----------|----------|-----|-------|
| f _{max} | | | MIN | 30 | 110 | 20 | 20 | 17 | 16 | 150 | 100 |
| t _w | | | MIN | 20 | 5 | 25 | 24 | 25 | 30 | 3.3 | 5 |
| t _{su} | DATA | | MIN | 20 | 2 | 25 | 18 | 15 | 18 | 2.5 | 4 |
| | *CLKEN ACTIVE | | MIN | 25 | 2.5 | 25 | - | 15 | - | 3 | 6 |
| | *CLKEN INACTIVE | | MIN | 10 | 4.5 | 25 | 18 | 15 | 18 | 3 | 6 |
| t _h | | | MIN | 5 | 1 | 5 | 5 | 5 | 5 | 1.8 | 0 |
| t _{PLH} | CLK (CD74: CP) | Q | MAX | 27 | 10 | 40 | 53 | 45 | 57 | 6.5 | 11.3 |
| t _{PHL} | | | MAX | 27 | 10.5 | 40 | 53 | 45 | 57 | 7.3 | 12.9 |

UNIT f_{max} : MHz, other : ns
 *CD74: E

HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|-----------|-------|------|---------|-------------|
| \bar{G} | CLOCK | DATA | Q | \bar{Q} |
| H | X | X | Q_0 | \bar{Q}_0 |
| L | ↑ | H | H | L |
| L | ↑ | L | L | H |
| X | L | X | Q_0 | \bar{Q}_0 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | F | SN74 HC | UNIT |
|-----------|------------|------|----|---------|------|
| I_{CC} | MAX | 22 | 45 | 0.08 | mA |
| I_{DH} | MAX | -0.4 | -1 | -4 | mA |
| I_{OL} | MAX | 8 | 20 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

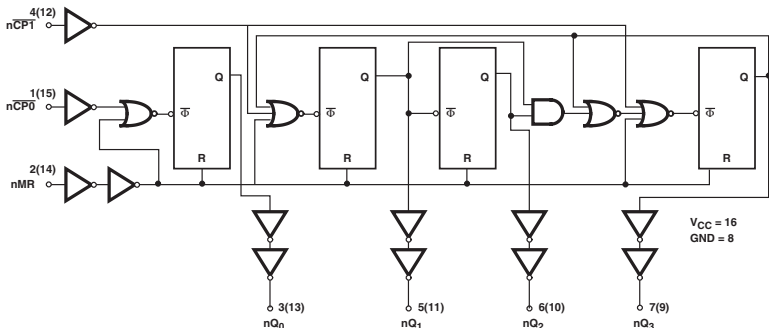
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | F | SN74 HC |
|-----------|--------------------|--------|------------|----|-----|---------|
| f_{max} | | | MIN | 30 | 110 | 20 |
| t_w | CLK H | | MIN | 20 | 4 | 25 |
| | CLK L | | MIN | 20 | 6 | 25 |
| | DATA | | MIN | 20 | 5 | 25 |
| t_{su} | \bar{G} ACTIVE | | MIN | 25 | 3.5 | 25 |
| | \bar{G} INACTIVE | | MIN | 10 | 5 | 25 |
| | | | MIN | 5 | 0 | 5 |
| t_h | | | MIN | 5 | 0 | 5 |
| t_{PH} | CLK | Q | MAX | 27 | 6.7 | 40 |
| t_{PHL} | | | MAX | 27 | 6.1 | 40 |

UNIT f_{max} : MHz, other : ns

DUAL 4-BIT DECADE COUNTERS

- Individual Clock for A and B Flip-Flops Provide Dual + 2 and + 5 Counters
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

Logic Diagram (CD74)



FUNCTION TABLE (CD74)

BCD COUNT SEQUENCE FOR 1/2

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

BI-QUINARY COUNT SEQUENCE FOR 1/2

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 69 | 26 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--|-------------------------------|------------|-----|------|---------|---------|----------|
| f _{max} | nCKA (CD74: nCP ₀) | nQA (CD74: nQP ₀) | MIN | 25 | 25 | 25 | 20 | 18 |
| | nCKB (CD74: nCP ₁) | nQB (CD74: nQP ₁) | MIN | 20 | 12.5 | 25 | 20 | 18 |
| t _w | nCKA (CD74: nCP ₀) nCKB (CD74: nCP ₁) *CLR H | | MIN | 20 | 20 | 20 | 24 | 29 |
| | | | MIN | 25 | 40 | 20 | 24 | 29 |
| | | | MIN | 20 | 20 | 20 | 15 | 20 |
| t _{su} | | | MIN | 25 | 25 | 5 | - | - |
| t _{PLH} | nCKA (CD74: nCP ₀) | nQA (CD74: nQ ₀) | MAX | 20 | 20 | 30 | 53 | 60 |
| t _{PHL} | | | MAX | 20 | 20 | 30 | 53 | 60 |
| t _{PLH} | nCKA (CD74: nCP ₀) | nQC (CD74: nQ ₂) | MAX | 60 | 60 | 72 | - | 126 |
| t _{PHL} | | | MAX | 60 | 60 | 72 | - | 126 |
| t _{PLH} | nCKB (CD74: nCP ₁) | nQB (CD74: nQ ₁) | MAX | 21 | 21 | 33 | 56 | 65 |
| t _{PHL} | | | MAX | 21 | 21 | 33 | 56 | 65 |
| t _{PLH} | nCKB (CD74: nCP ₁) | nQC (CD74: nQ ₂) | MAX | 39 | 39 | 46 | 74 | 83 |
| t _{PHL} | | | MAX | 39 | 39 | 46 | 74 | 83 |
| t _{PLH} | nCKB (CD74: nCP ₁) | nQD (CD74: nQ ₃) | MAX | 21 | 21 | 33 | 54 | 63 |
| t _{PHL} | | | MAX | 21 | 21 | 33 | 54 | 63 |
| t _{PHL} | *CLR | Q | MAX | 39 | 39 | 41 | 57 | 63 |

UNIT f_{max}: MHz, other: ns

*CD74: MR

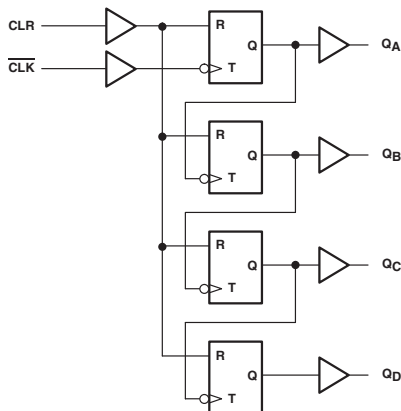
DUAL 4-BIT BINARY COUNTERS

- Dual 4-Bit Binary Counter with Individual Clock
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

FUNCTION TABLE (SN74)

| COUNT | INPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|------|------|---------|---------|----------|-------|-------|------|
| I _{CC} | MAX | 64 | 26 | 0.08 | 0.16 | 0.16 | - | 0.02 | mA |
| I _{OH} | MAX | -0.8 | -0.4 | -4 | -4 | -4 | -6 | -12 | mA |
| I _{OL} | MAX | 16 | 8 | 4 | 4 | 4 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

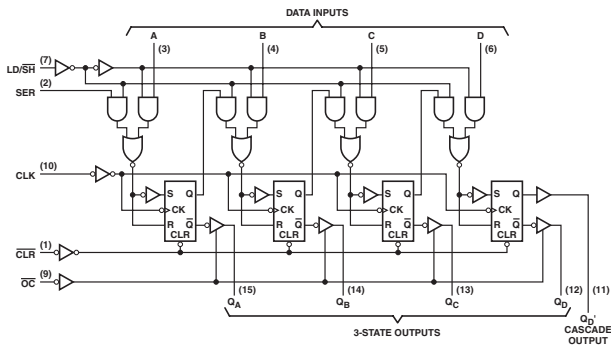
| PARAMETER | INPUT | OUTPUT | MAX or MIN | TTL | LS | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|------------------|--------------------|--------|------------|-----|----|---------|---------|----------|-------|-------|
| f _{max} | | | MIN | 25 | 25 | 25 | 20 | 18 | 35 | 75 |
| t _w | CLK | A | MIN | 20 | 20 | 20 | 24 | 29 | 5 | 5 |
| | | B | MIN | 25 | 40 | 20 | 24 | 29 | 5 | 5 |
| | CLR H | | MIN | 20 | 20 | 20 | 24 | 24 | 5 | 5 |
| t _{su} | | | MIN | 25 | 25 | 5 | - | - | 5 | 4 |
| t _{PLH} | CLKA (CD74:nCP) | QA | MAX | 20 | 20 | 30 | 59 | 48 | 19 | 12 |
| t _{PHL} | | | MAX | 20 | 20 | 30 | 59 | 48 | 19 | 12 |
| t _{PLH} | CLKB (CD74:nCP) | QD | MAX | 60 | 60 | 72 | 86 | 93 | 26.5 | 16.5 |
| t _{PHL} | | | MAX | 60 | 60 | 72 | 86 | 93 | 26.5 | 16.5 |
| t _{PHL} | CLR | Q | MAX | 39 | 39 | 41 | 41 | 48 | 18 | 11.5 |

UNIT f_{max}: MHz, other: ns

CASCADABLE SHIFT REGISTERS

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)

Logic Diagram



FUNCTION TABLE

| CLEAR | INPUTS | | | | 3-STATE OUTPUTS | | | | CASCADE OUTPUT QD |
|-------|--------------------|-------|--------|------------------|-----------------|------|------|------|-------------------|
| | LOAD/SHIFT CONTROL | CLOCK | SERIAL | PARALLEL A B C D | QA | QB | QC | QD | |
| L | X | X | X | X X X X | L | L | L | L | L |
| H | H | H | X | X X X X | QA0 | QB0 | QC0 | QD0 | L |
| H | H | ↓ | X | a b c d | a | b | c | d | d |
| H | L | H | X | X X X X | QA0 | QBn | QCn | QDn | QDn |
| H | L | ↓ | H | X X X X | H | QA n | QB n | QC n | QC n |
| H | L | ↓ | L | X X X X | L | QA n | QB n | QC n | QC n |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|----------------|-----|---------|
| Icc | MAX | 34 | mA |
| Ioh | QA, QB, QC, QD | MAX | -2.6 mA |
| | QD' | MAX | -0.4 mA |
| Iol | QA, QB, QC, QD | MAX | 24 mA |
| | QD' | MAX | 8 mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

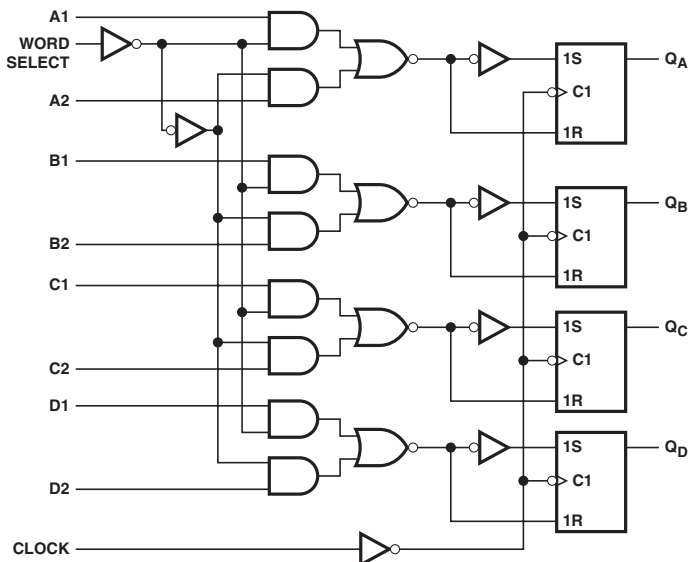
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-----------|-------|--------|------------|----|
| fmax | | | MIN | 30 |
| tw | | | MIN | 16 |
| tsu | LD/SR | | MIN | 40 |
| | OTHER | | MIN | 20 |
| th | | | MIN | 10 |
| TPLH | CLK | Q | MAX | 30 |
| TPHL | | | MAX | 30 |

UNIT fmax : MHz, other : ns

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Single-Rail Outputs (Q , \bar{Q})
- Select One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|-------------|-------|----------|----------|----------|----------|
| WORD SELECT | CLOCK | Q_A | Q_B | Q_C | Q_D |
| L | ↑ | A1 | B1 | C1 | D1 |
| H | ↑ | A2 | B2 | C2 | D2 |
| X | L | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 13 | mA |
| I_{OH} | MAX | -0.4 | mA |
| I_{OL} | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

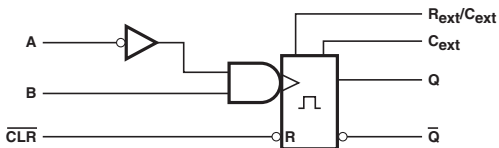
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-----------|-------------|--------|------------|----|
| t_w | | | MIN | 20 |
| t_{su} | DATA | | MIN | 25 |
| | WORD SELECT | | MIN | 45 |
| t_h | DATA | | MIN | 0 |
| | WORD SELECT | | MIN | 0 |
| t_{PLH} | CLK | Q | MAX | 27 |
| t_{PHL} | | | MAX | 32 |

UNIT: ns

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Will Not Trigger from Clear

Logic Diagram (SN74LS)



FUNCTION TABLE (SN74LS)

| CLR | INPUTS | | OUTPUTS | |
|-----|--------|---|---------|-----------|
| | A | B | Q | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | | |
| H | ↓ | H | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------|---------|----------|------|
| I_{CC} | MAX | 20 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -0.4 | -4 | -4 | mA |
| I_{OL} | MAX | 8 | 4 | 4 | mA |

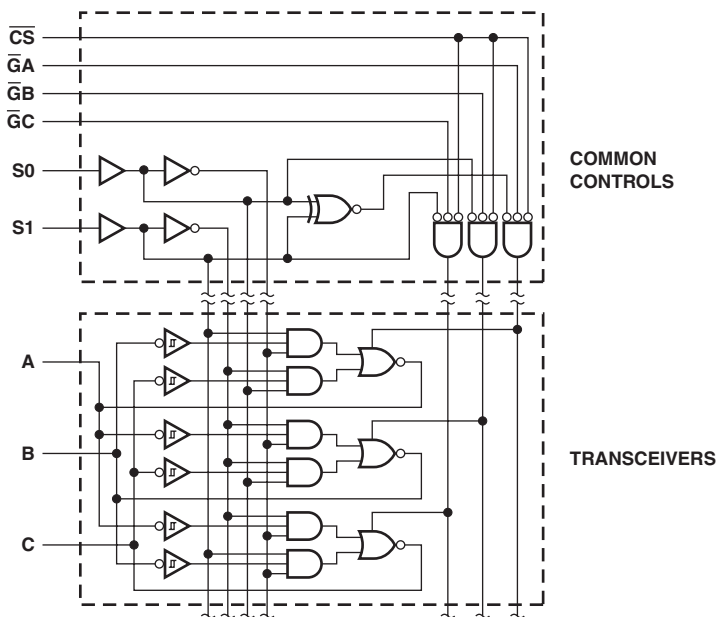
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | CD74 HC | CD74 HCT |
|-----------|--------------------------------|-----------|------------|----|---------|----------|
| t_W | | | MIN | 40 | 30 | 30 |
| t_{PLH} | A (CD74: \bar{A}) | Q | MAX | 33 | 90 | 90 |
| | B | | | 44 | 90 | 90 |
| t_{PHL} | A (CD74: \bar{A}) | \bar{Q} | MAX | 45 | 96 | 102 |
| | B | | | 56 | 96 | 102 |
| t_{PLH} | \bar{CLR} (CD74: \bar{R}) | Q | MAX | 27 | 65 | 72 |
| | | \bar{Q} | MAX | 45 | 65 | 72 |

UNIT: ns

QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | TRANSFERS BUSES |
|-----------------|----|----|-----------------|-----------------|-----------------|--------------------|
| \overline{CS} | S1 | S0 | \overline{GA} | \overline{GB} | \overline{GC} | |
| H | X | X | X | X | X | None |
| X | H | H | X | X | X | None |
| X | X | X | H | H | H | None |
| X | L | L | H | X | H | None |
| X | H | L | H | H | X | None |
| L | L | L | X | L | L | A → B, A → C |
| L | L | H | L | X | L | B → C, B → A |
| L | H | L | L | L | X | C → A, C → B |
| L | L | L | X | L | H | A → B |
| L | L | H | H | X | L | B → C |
| L | H | L | L | H | X | C → A |
| L | L | L | X | H | L | A → C |
| L | L | H | L | X | H | B → A |
| L | H | L | H | L | X | C → B |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 95 | mA |
| I_{OH} | MAX | -15 | mA |
| I_{OL} | MAX | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-----------|-------------------------------------|---------|------------|----|
| t_{PLH} | A | B or C | MAX | 14 |
| | B | A or C | | |
| | C | A or B | | |
| t_{PHL} | A | B or C | MAX | 20 |
| | B | A or C | | |
| | C | A or B | | |
| t_{PZL} | Any \overline{G} | A, B, C | MAX | 33 |
| | S0, S1 | | | 42 |
| | \overline{CS} | | | 36 |
| t_{PZH} | \overline{G} , S, \overline{CS} | A, B, C | MAX | 32 |
| t_{PLZ} | \overline{G} , S, \overline{CS} | A, B, C | MAX | 35 |
| t_{PHZ} | \overline{G} , S, \overline{CS} | A, B, C | MAX | 25 |

UNIT:ns

OCTAL BUFFERS WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

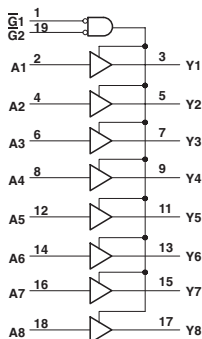
| PARAMETER | MAX or MIN | LS | ALS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 37 | 33 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS |
|------------------|-----------|--------|------------|----|-----|
| t _{PLH} | A | Y | MAX | 15 | 13 |
| | | | | 18 | 12 |
| t _{PZH} | \bar{G} | Y | MAX | 40 | 23 |
| t _{PZL} | | | | 45 | 25 |
| t _{PHZ} | \bar{G} | | MAX | 40 | 10 |
| t _{PLZ} | | | | 45 | 18 |

UNIT:ns

Logic Diagram



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

518

OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- Open-Collector Outputs
- 20-k Ω Pullup Resistors on Q Inputs

FUNCTION TABLE

| INPUTS | | OUTPUT |
|-----------|----------|--------|
| DATA P, Q | ENABLE G | P = Q |
| P = Q | L | H |
| P > Q | L | L |
| P < Q | L | L |
| X | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

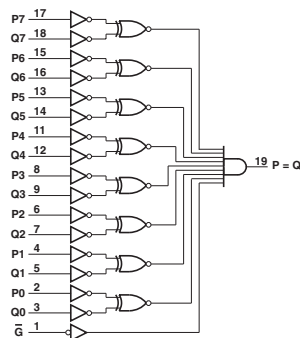
| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 17 | mA |
| I _{OL} | MAX | 24 | mA |
| V _{OH} | MAX | 5.5 | V |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-----------|--------|------------|-----|
| t _{PLH} | P or Q | P = Q | MAX | 33 |
| | | | | 15 |
| t _{PHL} | \bar{G} | P = Q | MAX | 33 |
| | | | | 15 |

UNIT: ns

Logic Diagram



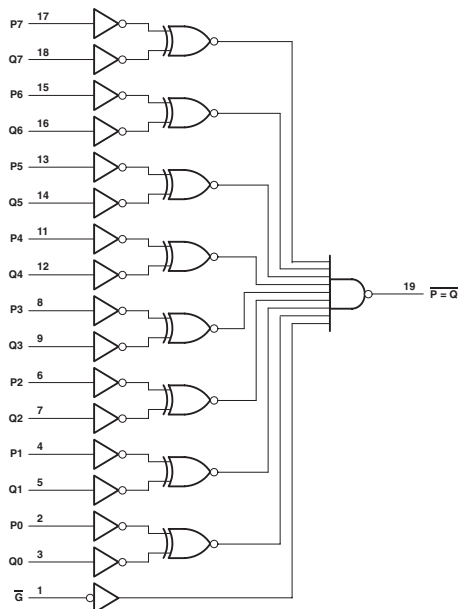
OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- 20-k Ω Pullup Resistors on Q Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------------|--------------------------|--------------------|
| DATA P, Q | ENABLE \overline{G} | $\overline{P = Q}$ |
| P = Q | L | L |
| P > Q | L | H |
| P < Q | L | H |
| X | H | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | F | AC 11 | UNIT |
|-----------|------------|------|----|----------|------|
| I_{CC} | MAX | 19 | 32 | 8 | mA |
| I_{OH} | MAX | -2.6 | -1 | -24 | mA |
| I_{OL} | MAX | 24 | 20 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | F | AC 11 |
|-----------|-----------------|--------------------|------------|-----|------|----------|
| t_{PLH} | P or Q | $\overline{P = Q}$ | MAX | 12 | 8.7 | 12.6 |
| t_{PHL} | | | | 20 | 10.3 | 11.3 |
| t_{PLH} | \overline{OE} | $\overline{P = Q}$ | MAX | 12 | 6.4 | 7.4 |
| t_{PHL} | | | | 22 | 10.4 | 7.8 |

UNIT: ns

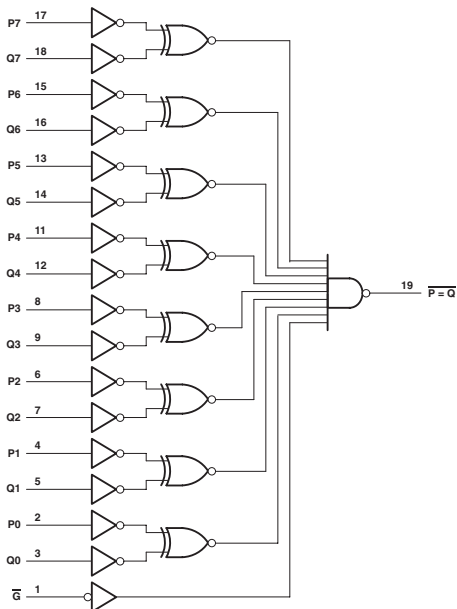
8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

● 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------------|---------------------|--------------------|
| DATA P, Q | ENABLE \bar{G} | $\overline{P = Q}$ |
| P = Q | L | L |
| P > Q | L | H |
| P < Q | L | H |
| X | H | H |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | F | AC 11 | UNIT |
|-----------------|------------|------|----|----------|------|
| I _{CC} | MAX | 19 | 32 | 0.08 | mA |
| I _{OH} | MAX | -2.6 | -1 | -24 | mA |
| I _{OL} | MAX | 24 | 20 | 24 | mA |

SWITCHING CHARACTERISTICS

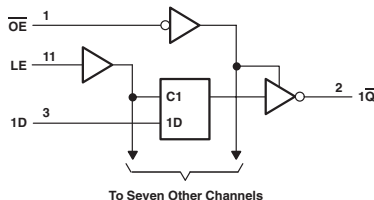
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | F | AC 11 |
|------------------|-----------|--------------------|------------|-----|-----|----------|
| t _{PLH} | P or Q | $\overline{P = Q}$ | MAX | 12 | 11 | 13 |
| t _{PHL} | | | | 20 | 11 | 11.4 |
| t _{PLH} | \bar{G} | $\overline{P = Q}$ | MAX | 12 | 7.5 | 7.9 |
| t _{PHL} | | | | 22 | 10 | 8.1 |

UNIT: ns

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- Functionally Equivalent to '373, Except for Having Inverted Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT |
|-----------------|--------------|---|------------------|
| \overline{OE} | ENABLE LE | D | |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q_0}$ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 | SN74 AC | ACT 11 | SN74 ACT | UNIT |
|-----------|------------|------|-----|------------|------------|-------------|-------------|-----|----------|------------|-----------|-------------|------|
| I_{CC} | MAX | 28 | 110 | 0.08 | 0.16 | 0.08 | 0.16 | 30 | 0.08 | 0.04 | 0.08 | 0.04 | mA |
| I_{OH} | MAX | -2.6 | -15 | -6 | -6 | -6 | -6 | -32 | -24 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 24 | 48 | 6 | 6 | 6 | 6 | 64 | 24 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

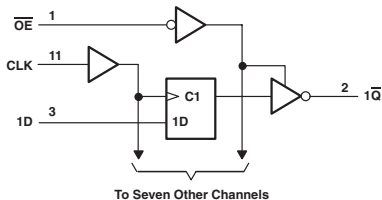
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 | SN74 AC | ACT 11 | SN74 ACT |
|-----------|--------------------------------|----------------|------------|-----|-----|------------|------------|-------------|-------------|-----|----------|------------|-----------|-------------|
| t_w | | | MIN | 15 | 2 | 20 | 24 | 25 | 24 | 3.3 | 4 | 5 | 5 | 6 |
| t_{SU} | | | MIN | 15 | 2 | 13 | 15 | 13 | 15 | 2.1 | 3.5 | 4.5 | 3.5 | 4 |
| t_h | | | MIN | 7 | 3 | 5 | 11 | 5 | 12 | 2.1 | 2 | 1 | 3.5 | 2.5 |
| t_{PLH} | D | \overline{Q} | MAX | 19 | 7.5 | 38 | 50 | 44 | 51 | 6.4 | 9.8 | 11 | 11.3 | 11.5 |
| t_{PHL} | | | | 13 | 7 | 38 | 50 | 44 | 51 | 6.6 | 8 | 10.5 | 9.5 | 11 |
| t_{PLH} | LE (CD74: \overline{LE}) | \overline{Q} | MAX | 23 | 9 | 44 | 53 | 44 | 57 | 7.3 | 11.3 | 11.5 | 13 | 11.5 |
| t_{PHL} | | | | 18 | 8 | 44 | 53 | 44 | 57 | 7.3 | 10.3 | 11 | 12.2 | 11.5 |
| t_{PZH} | \overline{OE} | \overline{Q} | MAX | 17 | 6.5 | 38 | 45 | 44 | 53 | 5.7 | 10.8 | 10.5 | 12.5 | 11 |
| t_{PZL} | | | | 18 | 9.5 | 38 | 45 | 44 | 53 | 6.7 | 9.7 | 10.5 | 12 | 11 |
| t_{PHZ} | \overline{OE} | \overline{Q} | MAX | 10 | 6.5 | 38 | 45 | 44 | 45 | 6.9 | 11.4 | 11 | 12.8 | 11 |
| t_{PLZ} | | | | 16 | 7 | 38 | 45 | 44 | 45 | 6.5 | 8.9 | 11 | 10.3 | 11 |

UNIT: ns

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- '534 Have Inverted Outputs, But Otherwise Are Functionally Equivalent to '374
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | OUTPUT | |
|--------|--------|--------|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 | SN74 AC | CD74 AC | ACT 11 | SN74 ACT | UNIT |
|-----------------|------------|------|-----|---------|---------|----------|----------|-----|-------|---------|---------|--------|----------|------|
| I _{CC} | MAX | 31 | 128 | 0.08 | 0.16 | 0.08 | 0.16 | 30 | 0.08 | 0.04 | 0.16 | 0.08 | 0.04 | mA |
| I _{OH} | MAX | -2.6 | -15 | -6 | -6 | -6 | -6 | -32 | -24 | -24 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 48 | 6 | 6 | 6 | 6 | 64 | 24 | 24 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | ABT | AC 11 | SN74 AC | CD74 AC |
|------------------|----------------|--------|------------|-----|-----|---------|---------|----------|----------|-----|-------|---------|---------|
| f _{max} | | | MIN | 35 | 125 | 25 | 20 | 25 | 16 | 125 | 75 | 140 | 125 |
| t _w | CLK "H" | | MIN | 14 | 4 | 20 | 24 | 20 | 30 | 3.5 | 6.5 | 4 | 4 |
| | CLK "L" | | MIN | 14 | 3 | 20 | 24 | 20 | 30 | 3.5 | 6.5 | 4 | 4 |
| t _{su} | | | MIN | 10 | 2 | 25 | 18 | 25 | 30 | 1.6 | 3.5 | 4 | 2 |
| | | | MIN | 0 | 2 | 5 | 5 | 5 | 5 | 2 | 4.5 | 1.5 | 2 |
| t _h | | | | | | | | | | | | | |
| EP _{LH} | CLK (CD74: CP) | Q | MAX | 12 | 8 | 45 | 50 | 45 | 53 | 6.7 | 11.7 | 12 | 11.3 |
| EP _{HL} | | | | 16 | 9 | 45 | 50 | 45 | 53 | 7.6 | 12.1 | 11 | 11.3 |
| EP _{ZH} | OE | Q | MAX | 17 | 6 | 38 | 45 | 37 | 53 | 5 | 10.4 | 11.5 | 14.5 |
| EP _{ZL} | | | | 18 | 10 | 38 | 45 | 37 | 53 | 6.8 | 10.4 | 11.5 | 14.5 |
| EP _{HZ} | OE | Q | MAX | 10 | 6 | 38 | 45 | 37 | 45 | 7.3 | 11.6 | 12.5 | 14.5 |
| EP _{LZ} | | | | 14 | 6 | 38 | 45 | 37 | 45 | 6.5 | 9.2 | 11 | 14.5 |

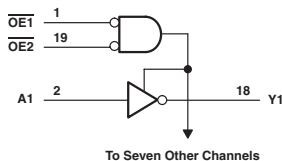
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT 11 | SN74 ACT |
|------------------|----------------|--------|------------|--------|----------|
| f _{max} | | | MIN | 55 | 120 |
| t _w | CLK "H" | | MIN | 9 | 3.5 |
| | CLK "L" | | MIN | 9 | 3.5 |
| t _{su} | | | MIN | 3 | 4 |
| | | | MIN | 5.5 | 1.5 |
| t _h | | | | | |
| EP _{LH} | CLK (CD74: CP) | Q | MAX | 14.5 | 12.5 |
| EP _{HL} | | | | 15 | 12 |
| EP _{ZH} | OE | Q | MAX | 13.3 | 12.5 |
| EP _{ZL} | | | | 13.5 | 11.5 |
| EP _{HZ} | OE | Q | MAX | 13.5 | 13.5 |
| EP _{LZ} | | | | 12 | 10.5 |

UNIT f_{max}: MHz, other: ns

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS540)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS-1 | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVTH 3V | CD74 AC | CD74 ACT | AHC | UNIT |
|-----------------|------------|-----|-----|-------|---------|---------|----------|----------|----------|-----|---------|---------|----------|------|------|
| I _{CC} | MAX | 52 | 22 | 22 | 0.08 | 0.16 | 0.08 | 0.16 | 71 | 30 | 5 | 0.16 | 0.16 | 0.04 | mA |
| I _{DH} | MAX | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | -24 | -24 | -8 | mA |
| I _{OL} | MAX | 24 | 24 | 48 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | 24 | 24 | 8 | mA |

| PARAMETER | MAX or MIN | AHCT | LV 3V | LV 5V | LVC 3V | UNIT |
|-----------------|------------|------|-------|-------|--------|------|
| I _{CC} | MAX | 0.04 | - | 0.02 | 0.01 | mA |
| I _{DH} | MAX | -8 | -8 | -16 | -24 | mA |
| I _{OL} | MAX | 8 | 8 | 16 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS-1 | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT |
|------------------|-----------------|-------------------------|------------|----|-----|-------|---------|---------|----------|----------|----------|-----|
| t _{PLH} | A | Y (CD74: \bar{Y}) | MAX | 15 | 12 | 12 | 25 | 33 | 25 | 36 | 6.9 | 4.8 |
| t _{PHL} | | | | 15 | 9 | 9 | 25 | 33 | 25 | 36 | 4 | 4.8 |
| t _{PZH} | \overline{OE} | Y (CD74: \bar{Y}) | MAX | 25 | 15 | 15 | 38 | - | 38 | - | 10.1 | 5.9 |
| t _{PZL} | | | | 38 | 20 | 20 | 38 | - | 38 | - | 11.3 | 6.4 |
| t _{PHZ} | \overline{OE} | Y (CD74: \bar{Y}) | MAX | 25 | 10 | 10 | 38 | 48 | 38 | 53 | 9 | 7.3 |
| t _{PLZ} | | | | 18 | 12 | 12 | 38 | 48 | 38 | 53 | 8.5 | 6.2 |

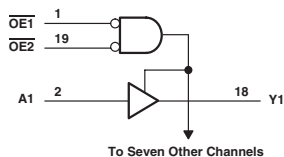
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V |
|------------------|-----------------|-------------------------|------------|---------|---------|----------|------|------|-------|-------|--------|
| t _{PLH} | A | Y (CD74: \bar{Y}) | MAX | 3.8 | 68 | 7.2 | 8 | 10 | 12 | 8 | 5.3 |
| t _{PHL} | | | | 3.8 | 68 | 7.2 | 8 | 10 | 12 | 8 | 5.3 |
| t _{PZH} | \overline{OE} | Y (CD74: \bar{Y}) | MAX | 5.2 | 12 | 13.4 | 10.5 | 12 | 16 | 10.5 | 6.6 |
| t _{PZL} | | | | 5.3 | 12 | 13.4 | 10.5 | 12 | 16 | 10.5 | 6.6 |
| t _{PHZ} | \overline{OE} | Y (CD74: \bar{Y}) | MAX | 5.6 | 12 | 13.4 | 10 | 12 | 17.5 | 10 | 7.4 |
| t _{PLZ} | | | | 5 | 12 | 13.4 | 10 | 12 | 17.5 | 10 | 7.4 |

UNIT: ns

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS541)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS-1 | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVTH 3V | CD74 AC | UNIT |
|-----------------|------------|-----|-----|-------|-----|---------|---------|----------|----------|----------|-----|---------|---------|------|
| I _{CC} | MAX | 55 | 25 | 25 | 75 | 0.08 | 0.16 | 0.08 | 0.16 | 72 | 30 | 5 | 0.16 | mA |
| I _{OH} | MAX | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 48 | 64 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LV 3V | UNIT |
|-----------------|------------|----------|------|------|-------|-------|-------|-------|------|
| I _{CC} | MAX | 0.16 | 0.04 | 0.04 | - | 0.02 | 0.02 | 0.01 | mA |
| I _{OH} | MAX | -24 | -8 | -8 | -8 | -16 | -16 | -24 | mA |
| I _{OL} | MAX | 24 | 8 | 8 | 8 | 16 | 16 | 24 | mA |

SWITCHING CHARACTERISTICS

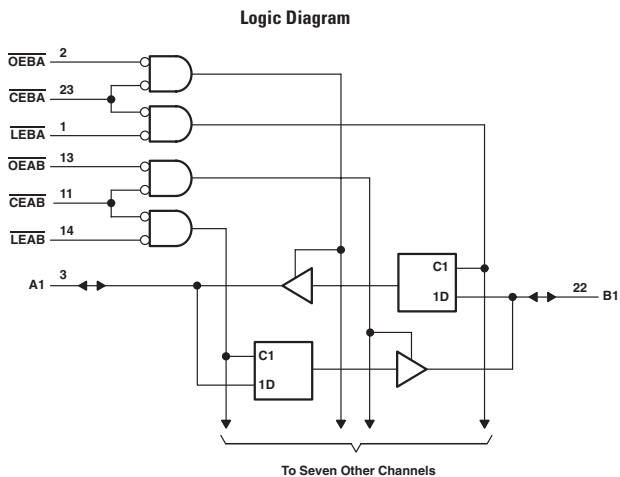
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS-1 | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|------------------|-----------------|--------|------------|----|-----|-------|-----|---------|---------|----------|----------|----------|
| t _{PLH} | A | Y | MAX | 15 | 14 | 14 | 6 | 29 | 35 | 29 | 42 | 6 |
| t _{PHL} | | | | 18 | 10 | 10 | 6 | 29 | 35 | 29 | 42 | 8.2 |
| t _{PZH} | \overline{OE} | Y | MAX | 32 | 15 | 15 | 9.5 | 38 | - | 38 | - | 10.7 |
| t _{PZL} | | | | 38 | 20 | 20 | 9.5 | 38 | - | 38 | - | 11.5 |
| t _{PHZ} | \overline{OE} | Y | MAX | 29 | 10 | 10 | 6.5 | 38 | 48 | 38 | 53 | 8.6 |
| t _{PLZ} | | | | 18 | 12 | 12 | 6 | 38 | 48 | 38 | 53 | 8.6 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | CD74 AC | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V |
|------------------|-----------------|--------|------------|-----|---------|---------|----------|------|------|-------|-------|-------|--------|
| t _{PLH} | A | Y | MAX | 3.6 | 3.5 | 7.8 | 8.2 | 8 | 9.5 | 12 | 8 | 9 | 5.1 |
| t _{PHL} | | | | 3.9 | 3.5 | 7.8 | 8.2 | 8 | 9.5 | 12 | 8 | 9 | 5.1 |
| t _{PZH} | \overline{OE} | Y | MAX | 4 | 5.2 | 12 | 13.4 | 10.5 | 12 | 16 | 10.5 | 14 | 7 |
| t _{PZL} | | | | 5.9 | 5.3 | 12 | 13.4 | 10.5 | 12 | 16 | 10.5 | 14 | 7 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.8 | 5.6 | 12 | 13.4 | 10 | 12 | 17.5 | 10 | 13.5 | 7 |
| t _{PLZ} | | | | 4.4 | 5 | 12 | 13.4 | 10 | 12 | 17.5 | 10 | 13.5 | 7 |

UNIT: ns

OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

- Back-to-Back Registers for Storage
- 3-State True Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE†

| INPUTS | | | | OUTPUT B |
|--------|------|------|---|------------------|
| CEAB | LEAB | OEAB | A | |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B ₀ † |
| L | L | L | L | L |
| L | L | L | H | H |

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.
 † Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | F | SN74 BCT | ABT | LVT 3V | LVTH 3V | ACT 11 | LVC 3V | UNIT |
|------------------|---|------------|-----|-------------|------|-----------|------------|-----------|-----------|------|
| I _{CCH} | | MAX | 100 | 8 | 0.25 | 0.19 | 0.19 | 0.08 | 0.01 | mA |
| I _{CCL} | | MAX | 125 | 71 | 30 | 12 | 5 | 0.08 | 0.01 | mA |
| I _{CCZ} | | MAX | 125 | 15 | 0.25 | 0.19 | 0.19 | 0.08 | 0.01 | mA |
| I _{OH} | A | MAX | -3 | -15 | -32 | -32 | -32 | -24 | -24 | mA |
| | B | MAX | -15 | -15 | -32 | -32 | -32 | -24 | -24 | mA |
| I _{OL} | A | MAX | 24 | 64 | 64 | 64 | 64 | 24 | 24 | mA |
| | B | MAX | 64 | 64 | 64 | 64 | 64 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

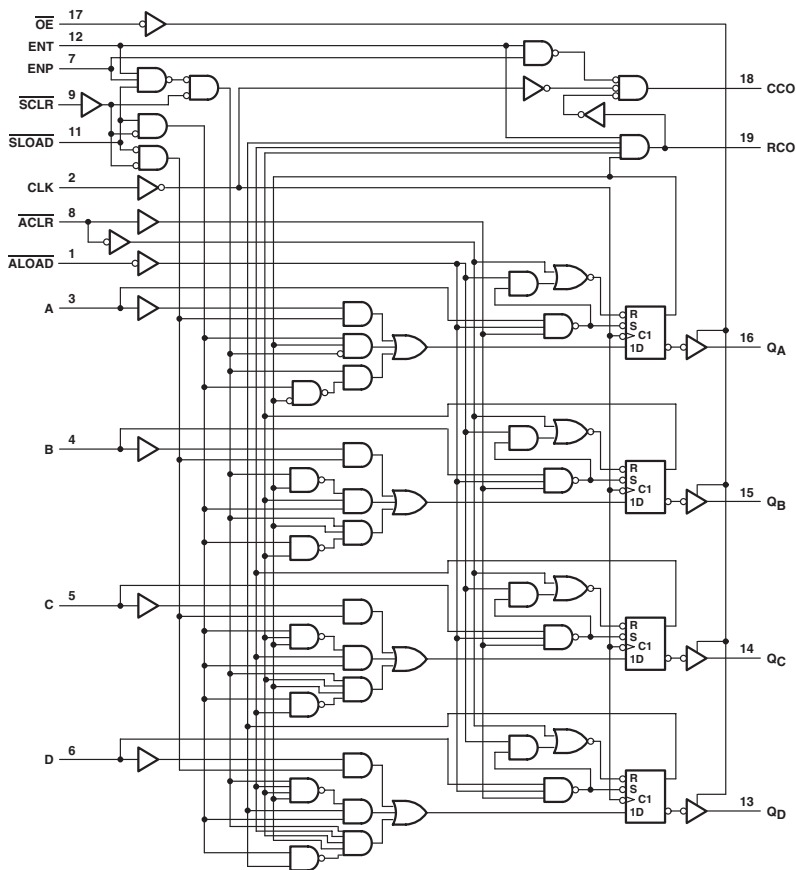
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | F | SN74 BCT | ABT | LVT 3V | LVTH 3V | ACT 11 | LVC 3V |
|------------------|-------------|--------|--------|------------|------|-------------|-----|-----------|------------|-----------|-----------|
| t _w | | | | MIN | 5 | 7 | 3.5 | 3.3 | 3.3 | 4 | 3.3 |
| t _{su} | LE ↑ before | "H" | | MIN | 3.5 | 4.5 | 3.5 | 0 | 0.4 | 2.5 | 1.6 |
| | LE ↑ before | "L" | | | 3.5 | 4.5 | 3 | 0.8 | 1 | 2.5 | 1.6 |
| | CE ↑ before | "H" | | | - | - | 3.5 | 0 | 0.2 | 3 | 1.6 |
| | CE ↑ before | "L" | | | - | - | 3 | 0.9 | 0.7 | 3 | 1.6 |
| t _{th} | LE ↑ after | "H" | | MIN | 3.5 | 1.5 | 0.5 | 1.7 | 1.5 | 2 | 2.1 |
| | LE ↑ after | "L" | | | 3.5 | 1.5 | 0.5 | 1.7 | 1.3 | 2 | 2.1 |
| | CE ↑ after | "H" | | | - | - | 0.5 | 1.8 | 1.6 | 1.5 | 2.1 |
| | CE ↑ after | "L" | | | - | - | 0.5 | 1.8 | 1.4 | 1.5 | 2.1 |
| t _{PLH} | A or B | B or A | MAX | 8.5 | 8.8 | 6.9 | 4.7 | 3.7 | 10.2 | 7 | |
| t _{PHL} | | | | 7.5 | 9.6 | 6.9 | 4.6 | 3.7 | 12.1 | 7 | |
| t _{PLH} | LEBA | A | MAX | 12.5 | 12.9 | 6.6 | 5.9 | 4.7 | 11.2 | 8.5 | |
| t _{PHL} | | | | 12.5 | 12.7 | 7.1 | 5.7 | 4.7 | 13.2 | 8.5 | |
| t _{PLH} | LEAB | B | MAX | 12.5 | 12.9 | 6.6 | 5.9 | 4.7 | 11.2 | 8.5 | |
| t _{PHL} | | | | 12.5 | 12.7 | 7.1 | 5.7 | 4.7 | 13.2 | 8.5 | |
| t _{PZH} | OE | A or B | MAX | 10 | 10.7 | 6.4 | 5.8 | 4.9 | 11.5 | 7.7 | |
| t _{PZL} | | | | 12 | 12.3 | 7.5 | 6.4 | 4.9 | 15.3 | 7.7 | |
| t _{PHZ} | OE | A or B | MAX | 9 | 8.1 | 8.4 | 6.5 | 5.3 | 10.4 | 7 | |
| t _{PLZ} | | | | 8.5 | 7.2 | 8 | 5.8 | 5.3 | 10.5 | 7 | |
| t _{PZH} | CE | A or B | MAX | 10 | 12 | 6.4 | 6 | 5.3 | 12.2 | 8 | |
| t _{PZL} | | | | 12 | 13.5 | 7.5 | 6.7 | 5.3 | 16 | 8 | |
| t _{PHZ} | CE | A or B | MAX | 9 | 8.5 | 8.4 | 6.4 | 5.4 | 11 | 7 | |
| t _{PLZ} | | | | 8.5 | 7.6 | 8 | 5.4 | 5.4 | 11.1 | 7 | |

UNIT: ns

SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | | | OPERATION |
|--------|-----|-------|------|-------|-----|-----|-----|--------------------|
| OE | ACL | ALOAD | SCLR | SLOAD | ENT | ENP | CLK | |
| H | X | X | X | X | X | X | X | Q outputs disabled |
| L | L | X | X | X | X | X | X | Asynchronous clear |
| L | H | L | X | X | X | X | X | Asynchronous load |
| L | H | H | L | X | X | X | ↑ | Synchronous clear |
| L | H | H | H | L | X | X | ↑ | Synchronous load |
| L | H | H | H | H | H | H | ↑ | Count |
| L | H | H | H | H | L | X | X | Inhibit counting |
| L | H | H | H | H | X | L | X | Inhibit counting |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------------|-----------|------------|------|------|
| I _{CC} | | MAX | 36 | mA |
| I _{OH} | OUTPUT Q | MAX | -2.6 | mA |
| | CCO & RCO | MAX | -0.4 | mA |
| I _{OL} | OUTPUT Q | MAX | 24 | mA |
| | CCO & RCO | MAX | 8 | mA |

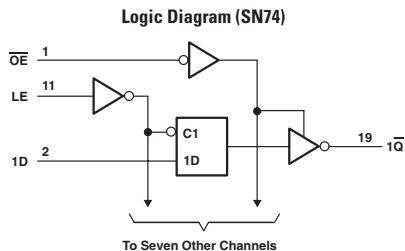
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|------------|---------------------------|--------|------------|------|
| f _{max} | | | | MIN | 30 |
| t _w | CLK "H" | | | MIN | 16.5 |
| | CLK "L" | | | MIN | 16.5 |
| t _{su} | ENP or ENT | H | | MIN | 20 |
| | | L | | | 20 |
| | A, B, C, D | | | | 20 |
| | SCLR | L | | | 15 |
| | | H | | | 30 |
| | SLOAD | L | | | 15 |
| | | H | | | 30 |
| t _h | | | MIN | 0 | |
| t _{PLH} | | CLK | Q | MAX | 12 |
| t _{PHL} | | | | | 18 |
| t _{PLH} | | CLK | RCO | MAX | 29 |
| t _{PHL} | | | | | 24 |
| t _{PLH} | | $\overline{\text{ALOAD}}$ | Q | MAX | 35 |
| t _{PHL} | | | | | 23 |
| t _{PLH} | | $\overline{\text{ALOAD}}$ | CCO | MAX | 55 |
| t _{PHL} | | | | | 33 |
| t _{PLH} | | ENT | RCO | MAX | 16 |
| t _{PHL} | | | | | 14 |
| t _{PHL} | | $\overline{\text{ACL}}$ | Q | MAX | 22 |

 UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT \bar{Q} |
|-----------------|--------------|---|---------------------|
| \overline{OE} | ENABLE LE | D | |
| L | H | H | L |
| L | H | L | H |
| L | L | X | O_D |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | CD74 AC | SN74 ACT | UNIT |
|-----------|------------|------|------------|------------|-------------|-------------|------------|------------|-------------|------|
| I_{CC} | MAX | 29 | 0.08 | 0.16 | 0.08 | 0.16 | 0.08 | 0.16 | 0.04 | mA |
| I_{OH} | MAX | -2.6 | -6 | -6 | -6 | -6 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 24 | 6 | 6 | 6 | 6 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

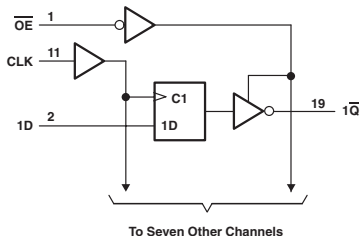
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | CD74 AC | SN74 ACT |
|-----------|--------------------------------|-----------|------------|-----|------------|------------|-------------|-------------|------------|------------|-------------|
| t_W | | | MIN | 15 | 20 | 24 | 25 | 24 | 5 | 4 | 3 |
| t_{SU} | | | | 10 | 13 | 15 | 13 | 15 | 2.5 | 2 | 4.5 |
| t_H | | | | 10 | 5 | 4 | 10 | 5 | 2 | 3 | 0 |
| t_{PLH} | D | \bar{Q} | MAX | 18 | 44 | 45 | 44 | 45 | 11.5 | 10.5 | 12.5 |
| t_{PHL} | | | | 14 | 44 | 45 | 44 | 45 | 11 | 10.5 | 11 |
| t_{PLH} | LE (CD74: \overline{LE}) | \bar{Q} | MAX | 22 | 44 | 50 | 44 | 53 | 11 | 12 | 11.5 |
| t_{PHL} | | | | 21 | 44 | 50 | 44 | 53 | 9.5 | 12 | 10.5 |
| t_{PZH} | \overline{OE} | \bar{Q} | MAX | 18 | 38 | 45 | 44 | 53 | 10 | 10.5 | 10 |
| t_{PZL} | | | | 18 | 38 | 45 | 44 | 53 | 9.5 | 10.5 | 9.5 |
| t_{PHZ} | \overline{OE} | \bar{Q} | MAX | 10 | 38 | 45 | 44 | 53 | 12 | 11.5 | 11.5 |
| t_{PLZ} | | | | 15 | 38 | 45 | 44 | 53 | 9 | 11.5 | 8.5 |

UNIT: ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT |
|--------|-----|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | SN74 ACT | UNIT |
|-----------------|------------|------|---------|---------|----------|----------|---------|----------|------|
| I _{CC} | MAX | 30 | 0.08 | 0.16 | 0.08 | 0.16 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -2.6 | -6 | -6 | -6 | -6 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 6 | 6 | 6 | 6 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

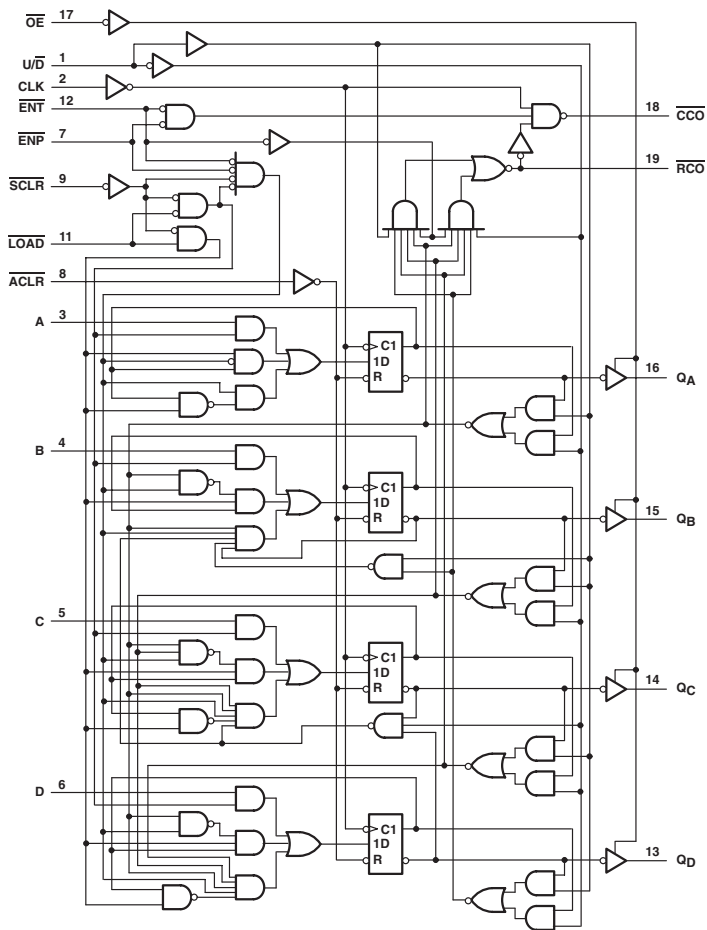
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 AC | SN74 ACT |
|------------------|---------|--------|------------|-----|---------|---------|----------|----------|---------|----------|
| f _{max} | | | MIN | 30 | 25 | 20 | 25 | 16 | 85 | 75 |
| t _w | CLK "H" | | MIN | 14 | 20 | 24 | 20 | 30 | 5 | 3.5 |
| | | | | 14 | 20 | 24 | 20 | 30 | 5 | 3.5 |
| t _{su} | CLK ↑ | | MIN | 15 | 25 | 18 | 25 | 30 | 2.5 | 3 |
| t _h | CLK ↑ | | | 0 | 5 | 5 | 5 | 3 | 2 | 1 |
| t _{PLH} | CLK | Q̄ | MAX | 14 | 45 | 50 | 45 | 53 | 11.5 | 11.5 |
| t _{PHL} | | | | 14 | 45 | 50 | 45 | 53 | 10.5 | 10.5 |
| t _{PZH} | OE | Q̄ | MAX | 18 | 38 | 45 | 38 | 53 | 9.5 | 9.5 |
| t _{PZL} | | | | 18 | 38 | 45 | 38 | 53 | 9.5 | 9.5 |
| t _{PHZ} | OE | Q̄ | MAX | 10 | 38 | 41 | 38 | 45 | 11.5 | 11.5 |
| t _{PLZ} | | | | 15 | 38 | 41 | 38 | 45 | 9 | 8.5 |

UNIT f_{max} : MHz, other : ns

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS

- 3-State Q Outputs Drive Bus Lines Directly
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | | | OPERATION |
|--------|------|------|------|-----|-----|-----|-----|--------------------|
| OE | ACLR | SCLR | LOAD | ENT | ENP | U/D | CLK | |
| H | X | X | X | X | X | X | X | Q outputs disabled |
| L | L | X | X | X | X | X | X | Asynchronous clear |
| L | H | L | X | X | X | X | ↑ | Synchronous clear |
| L | H | H | L | X | X | X | ↑ | Load |
| L | H | H | H | L | L | H | ↑ | Count up |
| L | H | H | H | L | L | L | ↑ | Count down |
| L | H | H | H | H | X | X | X | Inhibit count |
| L | H | H | H | X | H | X | X | Inhibit count |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------------|-----------|------------|------|------|
| I _{CC} | | MAX | 32 | mA |
| I _{OH} | OUTPUT Q | MAX | -2.6 | mA |
| | CCO & RCO | | -0.4 | mA |
| I _{OL} | OUTPUT Q | MAX | 24 | mA |
| | CCO & RCO | | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|--------------------|-------|--------|------------|------|
| f _{max} | | | | MIN | 30 |
| t _w | ACLR, LOAD | | | MIN | 15 |
| | CLK "H" | | | | 16.5 |
| | CLK "L" | | | | 16.5 |
| t _{su} | Data at A, B, C, D | | | MIN | 20 |
| | ENP, ENT | High | | | 30 |
| | | Low | | | 20 |
| | SCLR | High | | | 15 |
| | | Low | | | 30 |
| | LOAD | High | | | 15 |
| | | Low | | | 30 |
| | U/D | | | | 30 |
| | ACLR | | | | 10 |
| | t _h | | | | |
| t _{PLH} | | CLK | ANY Q | MAX | 13 |
| t _{PHL} | | | | | 16 |
| t _{PLH} | | CLK | RCO | MAX | 28 |
| t _{PHL} | | | | | 19 |
| t _{PLH} | | ENT | RCO | MAX | 15 |
| t _{PHL} | | | | | 13 |
| t _{PHL} | | ACLR | Q | MAX | 20 |
| t _{PZH} | | OE | Q | MAX | 18 |
| t _{PZL} | | | | | 24 |
| t _{PHZ} | | OE | Q | MAX | 10 |
| t _{PLZ} | | | | | 13 |

 UNIT f_{max} : MHz, other : ns

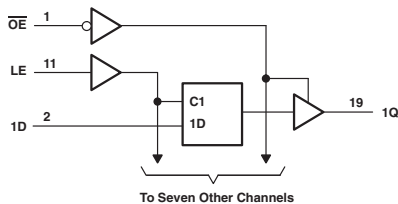
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT Q |
|--------|-----------|---|----------------|
| OE | ENABLE LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVT 3V | LVTH 3V | SN74 AC | CD74 AC | UNIT |
|-----------------|------------|------|-----|----|---------|---------|----------|----------|----------|-----|--------|---------|---------|---------|------|
| I _{CC} | MAX | 27 | 106 | 55 | 0.08 | 0.16 | 0.08 | 0.16 | 62 | 30 | 12 | 5 | 0.04 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -15 | -3 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 48 | 24 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | 64 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V | UNIT |
|-----------------|------------|----------|----------|------|------|-------|-------|-------|--------|------|
| I _{CC} | MAX | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | 0.02 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -8 | -8 | -8 | -16 | -16 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 8 | 8 | 8 | 16 | 16 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|------------------|------|-----------------|--------|------------|-----|-----|-----|---------|---------|----------|----------|----------|
| t _w | LE | | | MIN | 10 | 4.5 | 6 | 20 | 24 | 25 | 24 | 4 |
| t _{su} | LE ↓ | | | | 10 | 2 | 2 | 13 | 15 | 13 | 20 | 1 |
| t _h | LE ↓ | | | | 7 | 3 | 3 | 5 | 12 | 5 | 15 | 4 |
| t _{PLH} | | D | Q | MAX | 14 | 8 | 8 | 44 | 53 | 44 | 53 | 8.4 |
| t _{PHL} | | | | | 14 | 7 | 6 | 44 | 53 | 44 | 53 | 9.6 |
| t _{PLH} | | LE | Q | MAX | 20 | 13 | 13 | 44 | 53 | 44 | 53 | 8.1 |
| t _{PHL} | | | | | 19 | 7.5 | 8 | 44 | 53 | 44 | 53 | 7.8 |
| t _{PZH} | | \overline{OE} | Q | MAX | 18 | 6.5 | 12 | 38 | 45 | 44 | 53 | 10.4 |
| t _{PZL} | | | | | 18 | 9.5 | 8.5 | 38 | 45 | 44 | 53 | 11 |
| t _{PHZ} | | \overline{OE} | Q | MAX | 10 | 6.5 | 7.5 | 38 | 45 | 44 | 53 | 6 |
| t _{PLZ} | | | | | 15 | 7 | 6 | 38 | 45 | 44 | 53 | 6 |

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | SN74 AC | CD74 AC | SN74 ACT | CD74 ACT | AHC |
|------------------|------|------------------------|--------|------------|-----|--------|---------|---------|---------|----------|----------|-----|
| t _w | LE | | | MIN | 3.3 | 3.3 | 3 | 5 | 4 | 4 | 4 | 5 |
| t _{su} | LE ↓ | | | | 1.9 | 0.7 | 0.7 | 3.5 | 2 | 3.5 | 2 | 3.5 |
| t _h | LE ↓ | | | | 1.8 | 1.6 | 1.5 | 2 | 3 | 0 | 3 | 1.5 |
| t _{PLH} | | D | Q | MAX | 5.9 | 4.2 | 3.9 | 11.5 | 8.5 | 12 | 10.4 | 10 |
| t _{PHL} | | | | | 6.2 | 4.3 | 3.9 | 11 | 8.5 | 12 | 10.4 | 10 |
| t _{PLH} | | LE (CD74AC/ACT: LE) | Q | MAX | 6.6 | 5.6 | 4.2 | 11 | 12 | 12 | 12.5 | 11 |
| t _{PHL} | | | | | 7.2 | 6.5 | 4.2 | 10 | 12 | 10.5 | 12.5 | 11 |
| t _{PZH} | | \overline{OE} | Q | MAX | 5.2 | 5.1 | 5.1 | 10 | 10.5 | 11 | 13.5 | 11 |
| t _{PZL} | | | | | 6.7 | 5.5 | 5.1 | 9.5 | 10.5 | 10.5 | 13.5 | 11 |
| t _{PHZ} | | \overline{OE} | Q | MAX | 7.1 | 5.7 | 4.9 | 12 | 11.5 | 12.5 | 12.5 | 11 |
| t _{PLZ} | | | | | 6.5 | 4.6 | 4.6 | 9 | 11.5 | 9.5 | 12.5 | 11 |

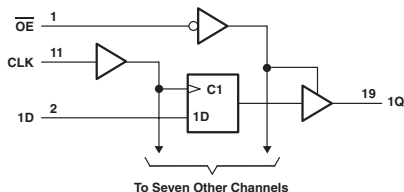
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | AHCT | LV 3V | LV 5V | LV-AT | LVC 3V |
|------------------|------|------------------------|--------|------------|------|-------|-------|-------|--------|
| t _w | LE | | | MIN | 5 | 5 | 5 | 8.5 | 3.3 |
| t _{su} | LE ↓ | | | | 3.5 | 3.5 | 3.5 | 1.5 | 2 |
| t _h | LE ↓ | | | | 1.5 | 1.5 | 1.5 | 3.5 | 1.5 |
| t _{PLH} | | D | Q | MAX | 7.5 | 16.5 | 10 | 10.5 | 6.9 |
| t _{PHL} | | | | | 10 | 16.5 | 10 | 10.5 | 6.9 |
| t _{PLH} | | LE (CD74AC/ACT: LE) | Q | MAX | 8.5 | 17.5 | 11 | 14.5 | 7.7 |
| t _{PHL} | | | | | 10 | 17.5 | 11 | 14.5 | 7.7 |
| t _{PZH} | | \overline{OE} | Q | MAX | 8 | 17 | 11 | 13.5 | 7.5 |
| t _{PZL} | | | | | 11 | 17 | 11 | 13.5 | 7.5 |
| t _{PHZ} | | \overline{OE} | Q | MAX | 12 | 16.5 | 11 | 12 | 6.5 |
| t _{PLZ} | | | | | 10.5 | 16.5 | 11 | 12 | 6.5 |

UNIT: ns

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | OUTPUT |
|--------|-----|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | LVT 3V | LVTH 3V | SN74 AC | UNIT |
|-----------------|------------|------|-----|----|---------|---------|----------|----------|----------|-----|--------|---------|---------|------|
| I _{CC} | MAX | 28 | 134 | 86 | 0.08 | 0.16 | 0.08 | 0.16 | 62 | 30 | 12 | 5 | 0.04 | mA |
| I _{OH} | MAX | -2.6 | -15 | -3 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | -32 | -24 | mA |
| I _{OL} | MAX | 24 | 48 | 24 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | 64 | 24 | mA |

| PARAMETER | MAX or MIN | CD74 AC | SN74 ACT | CD74 ACT | AHC | AHCT | LV 3V | LV 5V | LVC 3V | UNIT |
|-----------------|------------|---------|----------|----------|------|------|-------|-------|--------|------|
| I _{CC} | MAX | 0.16 | 0.04 | 0.16 | 0.04 | 0.04 | - | 0.02 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -8 | -8 | -8 | -16 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 8 | 8 | 8 | 16 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | F | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|-----------|-----------------|--------|------------|-----|-----|------|---------|---------|----------|----------|----------|
| fmax | | | MIN | 35 | 125 | 100 | 24 | 20 | 24 | 20 | 77 |
| tw | | | MIN | 14 | 5.5 | 7 | 20 | 24 | 20 | 24 | 6.5 |
| tsu | | | MIN | 15 | 5.5 | 2 | 25 | 18 | 25 | 18 | 6 |
| th | | | MIN | 0 | 0 | 2 | 5 | 5 | 5 | 5 | 0 |
| ↑PLH | CLK (CD74: CP) | Q | MAX | 14 | 8 | 10 | 45 | 50 | 45 | 50 | 10 |
| ↑PHL | | | | 14 | 9 | 10 | 45 | 50 | 45 | 50 | 8.9 |
| ↑PZH | \overline{OE} | Q | MAX | 18 | 6 | 12.5 | 38 | 45 | 38 | 45 | 10.4 |
| ↑PZL | | | | 18 | 10 | 8.5 | 38 | 45 | 38 | 45 | 10.9 |
| ↑PHZ | \overline{OE} | Q | MAX | 10 | 6 | 8 | 38 | 41 | 38 | 42 | 7.5 |
| ↑PLZ | | | | 12 | 6 | 6.5 | 38 | 41 | 38 | 42 | 6.4 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | SN74 AC | CD74 AC | SN74 ACT | CD74 ACT | AHC |
|-----------|-----------------|--------|------------|-----|--------|---------|---------|---------|----------|----------|------|
| fmax | | | MIN | 150 | 150 | 150 | 85 | 125 | 85 | 110 | 75 |
| tw | | | MIN | 3.3 | 3.3 | 3.3 | 5 | 4 | 4 | 4.5 | 5 |
| tsu | | | MIN | 1.5 | 2 | 2 | 2 | 2 | 2.5 | 2 | 3 |
| th | | | MIN | 1.8 | 0.3 | 0.3 | 1.5 | 2 | 1 | 3 | 1.5 |
| ↑PLH | CLK (CD74: CP) | Q | MAX | 6.8 | 5.4 | 4.5 | 11 | 10.8 | 12 | 11.2 | 12 |
| ↑PHL | | | | 7.1 | 5.9 | 4.5 | 9.5 | 10.8 | 11 | 11.2 | 12 |
| ↑PZH | \overline{OE} | Q | MAX | 5.1 | 4.8 | 4.8 | 9 | 14.5 | 10 | 14.5 | 12.5 |
| ↑PZL | | | | 6.7 | 5.1 | 4.8 | 9 | 14.5 | 10 | 14.5 | 12.5 |
| ↑PHZ | \overline{OE} | Q | MAX | 7 | 5.5 | 4.8 | 10.5 | 14.5 | 11.5 | 14.5 | 11.5 |
| ↑PLZ | | | | 6.5 | 4.5 | 4.4 | 8.5 | 14.5 | 9 | 14.5 | 11.5 |

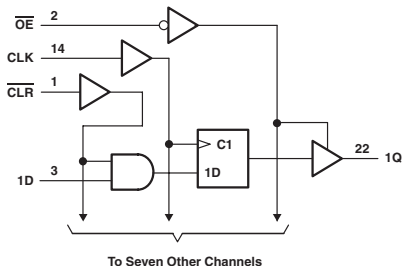
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHCT | LV 3V | LV 5V | LVC 3V |
|-----------|-----------------|--------|------------|------|-------|-------|--------|
| fmax | | | MIN | 75 | 45 | 75 | 150 |
| tw | | | MIN | 5.5 | 5 | 5 | 3.3 |
| tsu | | | MIN | 3.5 | 3.5 | 3.5 | 2 |
| th | | | MIN | 1.5 | 1.5 | 1.5 | 1.5 |
| ↑PLH | CLK (CD74: CP) | Q | MAX | 12 | 19 | 12 | 7 |
| ↑PHL | | | | 12 | 19 | 12 | 7 |
| ↑PZH | \overline{OE} | Q | MAX | 12.5 | 18.5 | 12.5 | 7.5 |
| ↑PZL | | | | 12.5 | 18.5 | 12.5 | 7.5 |
| ↑PHZ | \overline{OE} | Q | MAX | 11.5 | 17 | 11.5 | 6.4 |
| ↑PLZ | | | | 11.5 | 17 | 11.5 | 6.4 |

UNIT fmax : MHz, other : ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|-----|-----|---|----------------|
| OE | CLR | CLK | D | Q |
| L | L | ↑ | X | L |
| L | H | ↑ | H | H |
| L | H | ↑ | L | L |
| L | H | L | X | Q ₀ |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 30 | 142 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

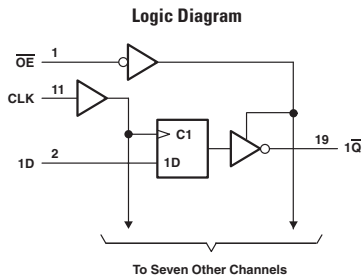
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | |
|------------------|-------|--------|------------|------|-----|-----|
| f _{max} | | | MIN | 30 | 90 | |
| t _w | CLK | H | MIN | 16.5 | 5.5 | |
| | CLK | L | | | 5.5 | |
| t _{su} | DATA | | | 15 | 15 | 5.5 |
| | CLR | L | | | | 6.5 |
| t _h | DATA | | 0 | 0 | 3 | |
| | CLR | | | | 0 | |
| t _{PLH} | CLK | Q | MAX | 14 | 8 | |
| t _{PHL} | | | | | 9 | |
| t _{PZH} | OC | Q | MAX | 18 | 6 | |
| t _{PZL} | | | | | 10 | |
| t _{PHZ} | OC | Q | MAX | 10 | 6 | |
| t _{PLZ} | | | | | 6 | |

UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Functionally Equivalent to '576, Except for Having Inverted Outputs



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 30 | 135 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

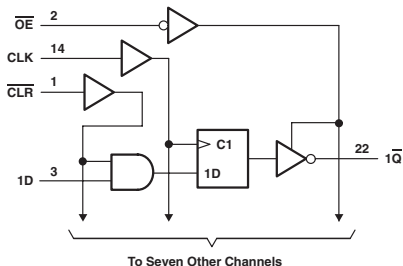
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|-------|--------|------------|------|-----|
| f _{max} | | | MIN | 30 | 125 |
| t _w | H | | MIN | 16.5 | 4 |
| | L | | | 2 | |
| t _{su} | DATA | | | 15 | 2 |
| t _h | DATA | | | 0 | 2 |
| t _{PLH} | CLK | Q̄ | MAX | 14 | 8 |
| t _{PHL} | | | | 14 | 9 |
| t _{PZH} | OE | Q̄ | MAX | 18 | 6 |
| t _{PZL} | | | | 18 | 10 |
| t _{PHZ} | OE | Q̄ | MAX | 10 | 6 |
| t _{PLZ} | | | | 15 | 6 |

UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|-----------------|------------------|------------|---|------------------|
| \overline{OE} | \overline{CLR} | CLK | D | \overline{Q} |
| L | L | \uparrow | X | H |
| L | H | \uparrow | H | L |
| L | H | \uparrow | L | H |
| L | H | L | X | $\overline{Q_0}$ |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------|------------|------|-----|------|
| I_{CC} | MAX | 30 | 142 | mA |
| I_{OH} | MAX | -2.6 | -15 | mA |
| I_{OL} | MAX | 24 | 48 | mA |

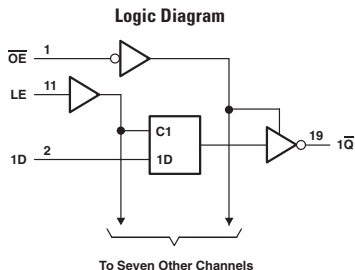
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-----------|-----------------|----------------|------------|------|-----|
| f_{max} | | | MIN | 30 | 125 |
| t_w | | | MIN | 16.5 | 4 |
| t_{su} | DATA | | MIN | 15 | 2 |
| t_h | CLR | | | 0 | 2 |
| t_{PLH} | | | | 14 | 8 |
| t_{PHL} | CLK | \overline{Q} | MAX | 14 | 9 |
| t_{PZH} | | | | 18 | 6 |
| t_{PZL} | \overline{OE} | \overline{Q} | MAX | 18 | 10 |
| t_{PHZ} | | | | 10 | 6 |
| t_{PLZ} | \overline{OE} | \overline{Q} | MAX | 15 | 6 |

UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Inverting-Logic Outputs
- Bus-Structured Pinout



FUNCTION TABLE

| INPUTS | | | OUTPUT Q |
|--------|--------------|---|-------------|
| OE | ENABLE LE | D | |
| L | H | H | L |
| L | H | L | H |
| L | L | X | \bar{Q}_0 |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 29 | 115 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

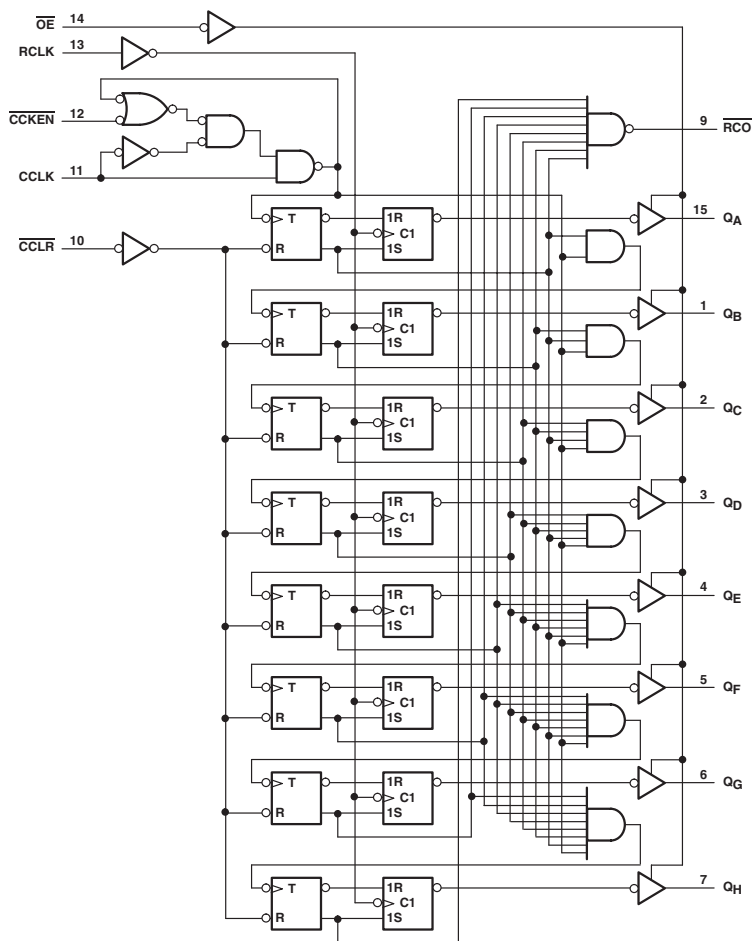
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|------------|-----------|------------|-----|-----|
| t _w | C | | | 15 | 2 |
| t _{su} | C ↓ | | MIN | 10 | 2 |
| t _h | C ↓ | | | 10 | 3 |
| t _{PLH} | D | \bar{Q} | MAX | 18 | 7.5 |
| t _{PHL} | | | | 14 | 7 |
| t _{PLH} | LE | \bar{Q} | MAX | 22 | 9 |
| t _{PHL} | | | | 21 | 8 |
| t _{PZH} | \bar{OE} | \bar{Q} | MAX | 18 | 6.5 |
| t _{PZL} | | | | 18 | 9.5 |
| t _{PHZ} | \bar{OE} | \bar{Q} | MAX | 10 | 6.5 |
| t _{PLZ} | | | | 15 | 7 |

UNIT: ns

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

- Parallel Register Outputs
- Counter Has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency: DC to 20MHz

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | SN74 HC | UNIT |
|-----------------|------------------|------------|------|---------|------|
| I _{CC} | | MAX | 65 | 0.08 | mA |
| I _{OH} | \overline{RCO} | MAX | -1 | -4 | mA |
| | Q | MAX | -2.6 | -6 | mA |
| I _{OL} | \overline{RCO} | MAX | 16 | 4 | mA |
| | Q | MAX | 24 | 6 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

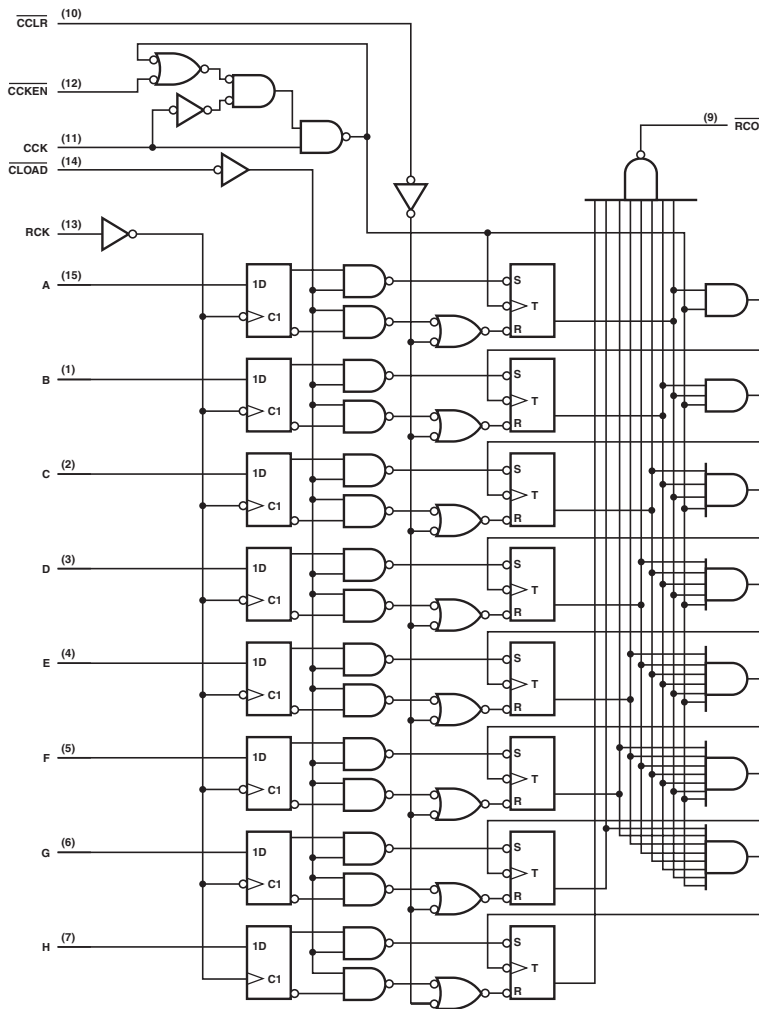
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC |
|------------------|---|------------------------------|------------------|------------|----|---------|
| f _{max} | | CCK | \overline{RCO} | MIN | 20 | 13 |
| t _w | CCK | | | MIN | 25 | 31 |
| | CCLR | | | | 20 | 25 |
| | RCK | | | | 20 | 31 |
| t _{su} | $\overline{CCLR} \uparrow$ before CCK \uparrow | | | MIN | 20 | 25 |
| | CCK \uparrow before RCK \uparrow | | | | 40 | 25 |
| t _{PLH} | | CCK \uparrow | \overline{RCO} | MAX | 22 | 45 |
| t _{PHL} | | | | | 30 | 45 |
| t _{PLH} | | $\overline{CCLR} \downarrow$ | \overline{RCO} | MAX | 45 | 39 |
| t _{PLH} | | RCK \uparrow | Q | MAX | 18 | 42 |
| t _{PHL} | | | | | 33 | 42 |
| t _{PZH} | | $\overline{OE} \downarrow$ | Q | MAX | 38 | 37 |
| t _{PZL} | | | | | 45 | 37 |
| t _{PHZ} | | $\overline{OE} \downarrow$ | Q | MAX | 30 | 37 |
| t _{PLZ} | | | | | 38 | 37 |

UNIT f_{max} : MHz, other : ns

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel Register Inputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|----|------|
| I _{CC} | MAX | 60 | mA |
| I _{OH} | MAX | -1 | mA |
| I _{OL} | MAX | 16 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

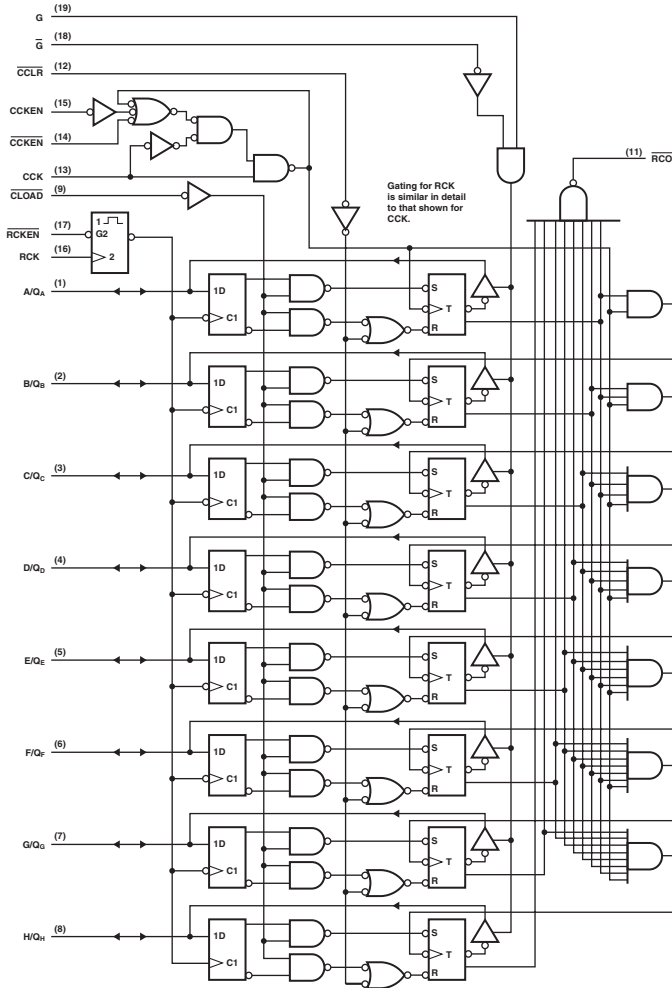
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|--|-----------------------------|------------------|------------|----|
| f _{max} | | CCK | \overline{RCO} | MIN | 20 |
| t _w | CCK | | | MIN | 25 |
| | \overline{CCLR} | | | | 20 |
| | RCK | | | | 20 |
| | \overline{CLOAD} | | | | 40 |
| t _{su} | $\overline{CCLR} \uparrow$ before CCK \uparrow | | | MIN | 20 |
| | $\overline{CLOAD} \uparrow$ before CCK \uparrow | | | | 20 |
| | RCK \uparrow | | | | 30 |
| | $\overline{CLOAD} \uparrow$ A to H before RCK | | | | 20 |
| | | | | | |
| t _h | | | | MIN | 0 |
| t _{PLH} | CCK \uparrow | \overline{RCO} | MAX | 23 | |
| t _{PHL} | | | | 30 | |
| t _{PLH} | $\overline{CLOAD} \downarrow$ | \overline{RCO} | MAX | 47 | |
| t _{PHL} | | | | 17 | |
| t _{PLH} | $\overline{CCLR} \downarrow$ | \overline{RCO} | MAX | 45 | |
| t _{PLH} | RCK \uparrow | $\overline{RCO} \downarrow$ | MAX | 53 | |
| t _{PHL} | | | | 45 | |

UNIT f_{max} : MHz, other : ns

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel 3-State I/O: Register Inputs/Counter Outputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | ACT 11 | UNIT |
|-----------------|------------------|------------|------|--------|------|
| I _{CC} | | MAX | 85 | 0.08 | mA |
| I _{OH} | \overline{RCO} | MAX | -1 | -24 | mA |
| | Q | MAX | -2.6 | -24 | mA |
| I _{OL} | \overline{RCO} | MAX | 16 | 24 | mA |
| | Q | MAX | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

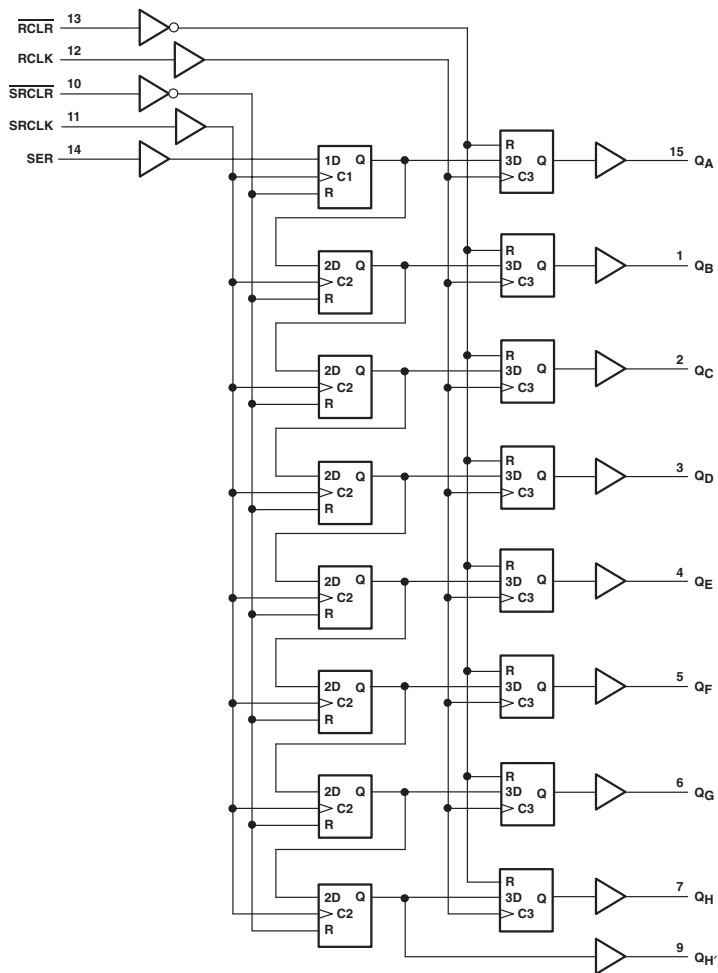
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | ACT 11 |
|------------------|-------------------------------------|-------|------------------|------------|------|--------|
| f _{max} | | CCK | \overline{RCO} | MIN | 20 | 52 |
| t _w | CCK | | | MIN | 25 | 9.6 |
| | \overline{CCLR} | | | | 20 | 7.6 |
| | RCK | | | | 20 | 5.8 |
| | CLOAD | | | | 40 | 6.2 |
| t _{su} | \overline{CCLR} ↑ before CCK ↑ | | | MIN | 20 | 1.2 |
| | CLOAD ↑ before CCK ↑ | | | | 20 | 5.1 |
| | RCK ↑ before CLOAD ↑ | | | | 30 | 7.4 |
| | A to H before RCK | | | | 20 | 2.4 |
| t _h | | | | MIN | 0 | 0.8 |
| t _{PLH} | CCK ↑ | Q | MAX | 21 | 15.1 | |
| t _{PHL} | | | | 39 | 15 | |
| t _{PLH} | \overline{CLOAD} ↓ | Q | MAX | 51 | 19.1 | |
| t _{PHL} | | | | 42 | 21.7 | |
| t _{PHL} | \overline{CCLR} ↓ | Q | MAX | 38 | 16 | |

UNIT f_{max} : MHz, other : ns

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | FUNCTION |
|--------|-------|-------|------|------|--|
| SER | SRCLK | SRCLR | RCLK | RCLR | |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of shift register goes high. Other stages store the data of previous stage, respectively. |
| L | ↓ | H | X | X | Shift register state is not changed. |
| X | X | X | X | L | Storage register is cleared. |
| X | X | X | ↑ | H | Shift register data is stored in the storage register. |
| X | X | X | ↓ | H | Storage register state is not changed. |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | SN74 HC | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------------|----------|------------|------|---------|------|------|-------|-------|------|
| I _{CC} | | MAX | 65 | 0.08 | 0.04 | 0.02 | - | 0.02 | mA |
| I _{OH} | QH' | MAX | -1 | -4 | -4 | -4 | -6 | -12 | mA |
| | Q | MAX | -2.6 | -6 | -8 | -8 | -6 | -12 | mA |
| I _{OL} | QH' | MAX | 16 | 4 | 4 | 4 | 6 | 12 | mA |
| | QA to QH | MAX | 24 | 6 | 8 | 8 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

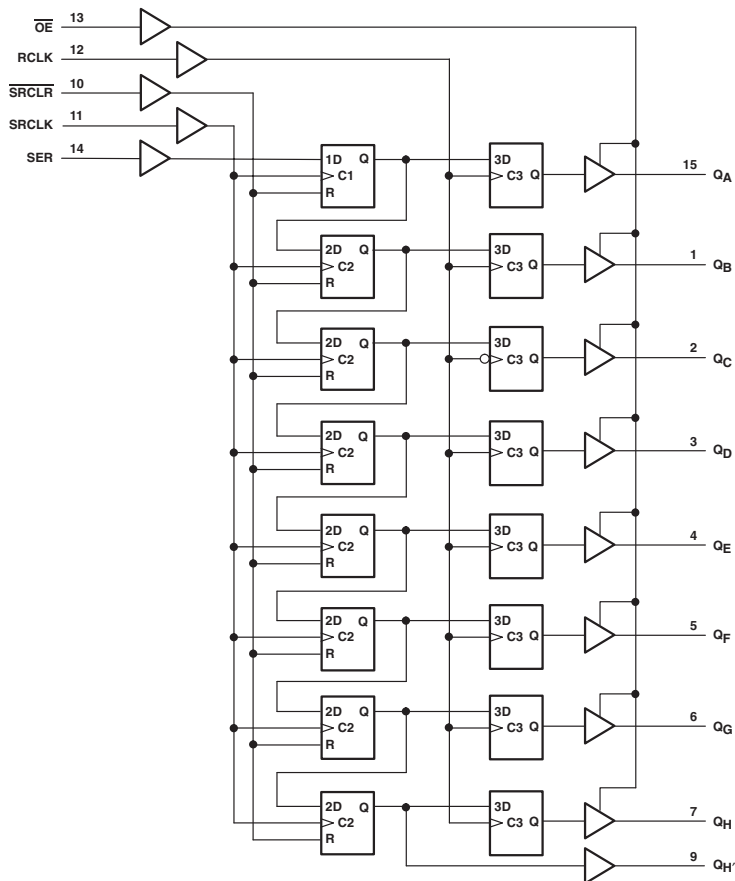
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC | AHC | AHCT | LV 3V | LV 5V |
|------------------|-------------------|----------|--------|------------|-----|---------|------|------|-------|-------|
| t _w | SRCK | | | MIN | 25 | 20 | 5 | 5.5 | 5.5 | 5 |
| | RCK | | | | 20 | 20 | 5 | 5.5 | 5.5 | 5 |
| t _{su} | SRCLR ↑ to SRCK ↑ | | | MIN | 20 | 10 | 3.3 | 3.3 | 4.8 | 3.3 |
| | SER to SRCK ↑ | | | | 20 | 22 | 3 | 3 | 3.5 | 3 |
| | SRCK ↑ to RCK ↑ | | | | 40 | 22 | 5 | 5 | 8.5 | 5 |
| | SRCLR ↓ to RCK ↑ | | | | 40 | 13 | 5 | 5 | 9 | 5 |
| | RCLR ↑ to RCK ↑ | 20 | 5 | 3.7 | 3.8 | 5.3 | 3.7 | | | |
| t _h | | | | MIN | 0 | 5 | 2 | 2 | 1.5 | 2 |
| t _{PLH} | SRCK ↑ | QH' | MAX | 18 | 37 | 9.1 | 9.1 | 12.4 | 9.1 | |
| t _{PHL} | | | | 23 | 37 | 10.1 | 10.1 | 13.9 | 10.1 | |
| t _{PLH} | RCK ↑ | QA to QH | MAX | 18 | 37 | 8.3 | 8.3 | 11.1 | 8.3 | |
| t _{PHL} | | | | 30 | 37 | 9.7 | 9.7 | 13.1 | 9.7 | |
| t _{PLH} | SRCLR ↓ | QH' | MAX | 33 | 37 | 10.1 | 10.1 | 14 | 10.1 | |
| t _{PHL} | RCLR ↓ | QA to QH | | 57 | 31 | 10.7 | 10.7 | 14.4 | 10.7 | |

UNIT: ns

8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- 3-State Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | FUNCTION |
|--------|-------|-------|------|----|--|
| SER | SRCLK | SRCLR | RCLK | OE | |
| X | X | X | X | H | Outputs Q _A -Q _H are disabled. |
| X | X | X | X | L | Outputs Q _A -Q _H are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | ↓ | H | X | X | Shift-register state is not changed. |
| X | X | X | ↑ | X | Shift-register data is stored in the storage register. |
| X | X | X | ↓ | X | Storage-register state is not changed. |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | SN74 HC | CD74 HC | AHC | AHCT | LV 3V | LV 5V | UNIT |
|-----------------|----------|------------|-----|---------|---------|------|------|-------|-------|------|
| I _{CC} | | MAX | 65 | 0.08 | 0.16 | 0.04 | 0.04 | - | 0.02 | mA |
| I _{OH} | QH' | MAX | -1 | -4 | -4 | -8 | -8 | -8 | -16 | mA |
| | QA to QH | MAX | -26 | -6 | -6 | -8 | -8 | -8 | -16 | mA |
| I _{OL} | QH' | MAX | 16 | 4 | 4 | 8 | 8 | 8 | 16 | mA |
| | QA to QH | MAX | 24 | 6 | 6 | 8 | 8 | 8 | 16 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

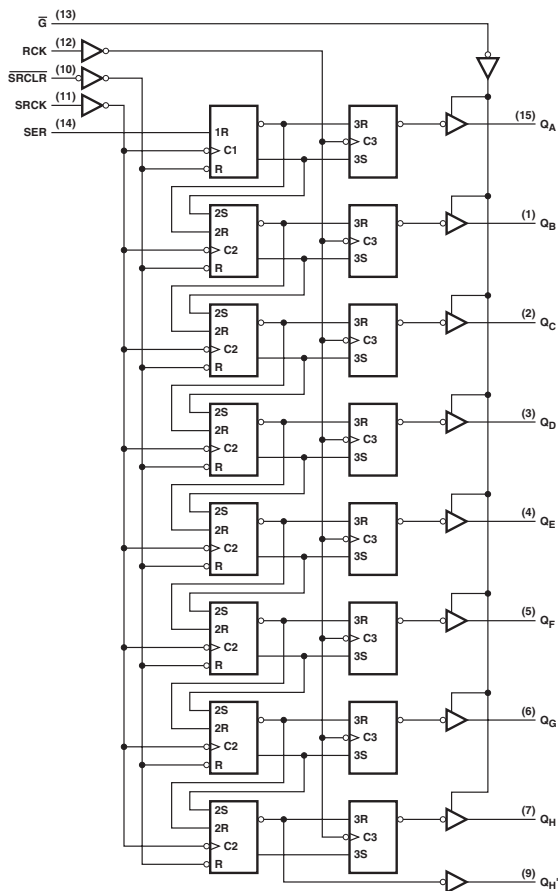
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC | CD74 HC | AHC | AHCT | LV 3V | LV 5V |
|------------------|-------------------|---------|----------|------------|----|---------|---------|------|------|-------|-------|
| t _w | SRCK | | | MIN | 25 | 20 | 20 | 5 | 5.5 | 5.5 | 5 |
| | RCK | | | | 20 | 20 | 20 | 5 | 5.5 | 5.5 | 5 |
| t _{su} | SRCLR ↑ to SRCK ↑ | | | MIN | 20 | 12 | 12 | 2.5 | 3.8 | 3 | 2.5 |
| | SER to SRCK ↑ | | | | 20 | 25 | 25 | 3 | 3 | 3.5 | 3 |
| | SRCK ↑ to RCK ↑ | | | | 40 | 19 | 19 | 5 | 5 | 8.5 | 5 |
| | SRCLR ↓ to RCK ↑ | | | | 40 | 13 | 13 | 5 | 5 | 9 | 5 |
| t _h | | | | MIN | 0 | 0 | 0 | 2 | 2 | 1.5 | 2 |
| t _{PLH} | | SRCK ↑ | QH' | MAX | 18 | 40 | 48 | 11.4 | 11.4 | 18.5 | 11.4 |
| t _{PHL} | | | | | 25 | 40 | 48 | 11.4 | 11.4 | 18.5 | 11.4 |
| t _{PLH} | | RCK ↑ | QA to QH | MAX | 18 | 37 | 45 | 10.5 | 10.5 | 17 | 10.5 |
| t _{PHL} | | | | | 35 | 37 | 45 | 10.5 | 10.5 | 17 | 10.5 |
| t _{PHL} | | SRCLR ↓ | QH' | MAX | 35 | 44 | 44 | 11.1 | 11.1 | 17.2 | 11.1 |

UNIT: ns

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Open-Collector Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|----------|------------|-----|------|
| I _{CC} | | MAX | 55 | mA |
| I _{OH} | QH' | MAX | 16 | mA |
| | Q | MAX | 24 | mA |
| I _{OL} | QH' | MAX | -1 | mA |
| V _{OH} | QA to QH | MAX | 5.5 | V |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

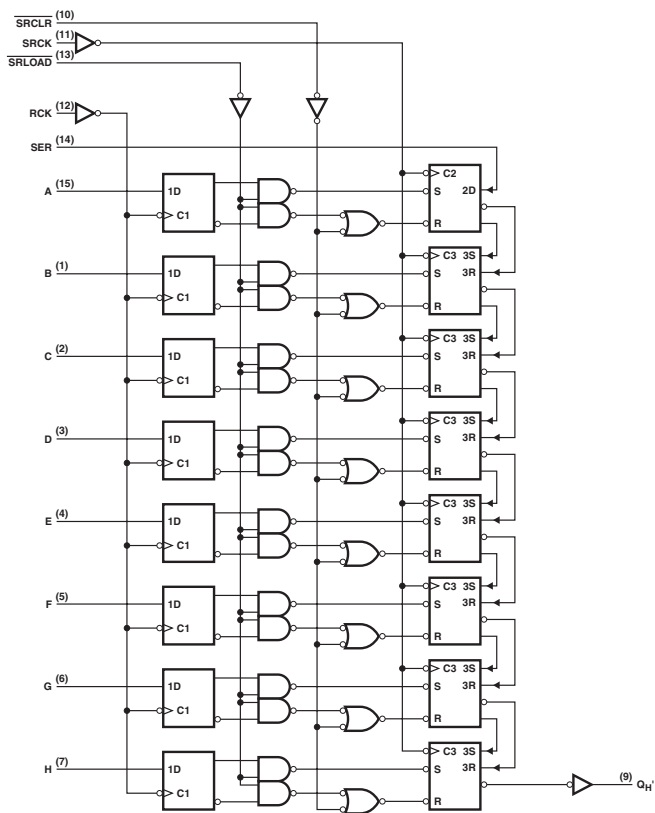
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|----------------------|---------|----------|------------|----|
| t _w | SRCK | | | MIN | 25 |
| | RCK | | | | 20 |
| t _{su} | SRCLR ↑ to SRCK ↑ | | | MIN | 20 |
| | SER to SRCK ↑ | | | | 20 |
| | SRCK ↑ to RCK ↑ | | | | 40 |
| | SRCLR ↓ to RCK ↑ | | | | 40 |
| t _h | | | MIN | 0 | |
| t _{PLH} | | SRCK ↑ | QH' | MAX | 21 |
| t _{PHL} | | | | | 30 |
| t _{PLH} | | RCK ↑ | QA to QH | MAX | 42 |
| t _{PHL} | | | | | 35 |
| t _{PHL} | | SRCLR ↓ | QH' | MAX | 35 |

UNIT: ns

SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram (SN74LS)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|----|---------|----------|------|
| I _{CC} | MAX | 53 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -1 | -4 | -4 | mA |
| I _{OL} | MAX | 16 | 4 | 4 | mA |

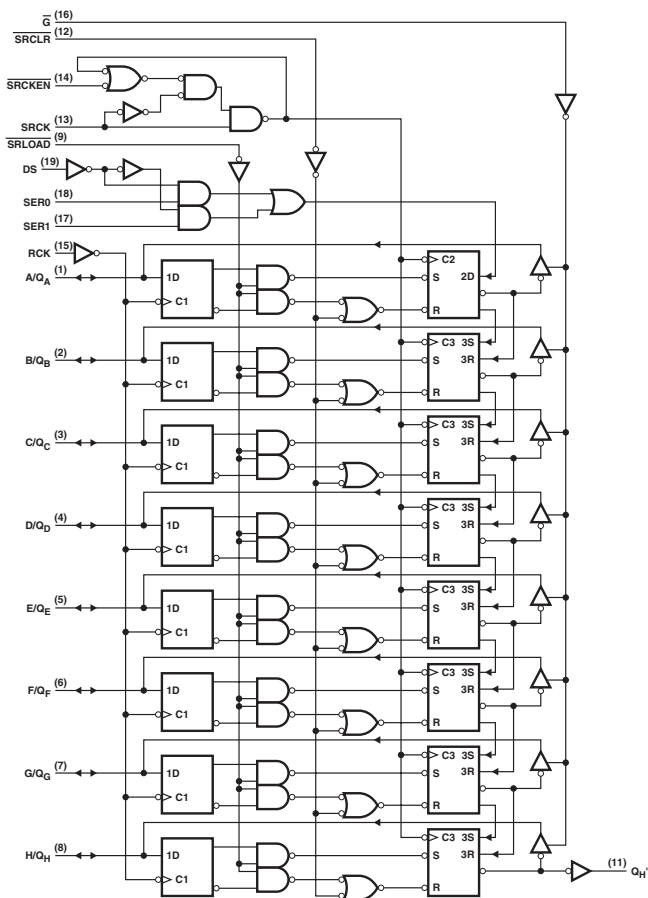
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | CD74 HC | CD74 HCT |
|------------------|--------------------------------------|--------|------------|----|---------|----------|
| f _{max} | SRCK | Q | MIN | 20 | - | - |
| | SRCK | QH' | MIN | 20 | - | - |
| | SH _{CP} | | MIN | - | 20 | 16 |
| t _w | SRCK high | | MIN | 15 | - | - |
| | SRCK low | | MIN | 35 | - | - |
| | RCK | | MIN | 20 | - | - |
| | SRCLR | | MIN | 20 | - | - |
| | SRLOAD | | MIN | 40 | - | - |
| | SH _{CP} | | MIN | - | 20 | 30 |
| | ST _{CP} | | MIN | - | 15 | 20 |
| | MR | | MIN | - | 20 | 27 |
| | PL | | MIN | - | 18 | 24 |
| t _{su} | Data before RCK ↑ | | MIN | 20 | - | - |
| | SRCLR inactive before SRCK ↑ | | MIN | 25 | - | - |
| | SRLOAD inactive before SRCK ↑ | | MIN | 30 | - | - |
| | RCK ↑ before SRLOAD ↑ | | MIN | 40 | - | - |
| | SER before SRCK ↑ | | MIN | 20 | - | - |
| | ST _{CP} to SH _{CP} | | MIN | - | 30 | 36 |
| | D _s to SH _{CP} | | MIN | - | 15 | 15 |
| t _h | D _n to ST _{CP} | | MIN | - | 15 | 15 |
| | LS597 only | | MIN | 0 | - | - |
| | ST _{CP} to SH _{CP} | | | - | 0 | 0 |
| | D _s to SH _{CP} | | | - | 3 | 3 |
| | D _n to ST _{CP} | | | - | 3 | 3 |
| | | - | | | | |
| t _{PLH} | SRCK ↑ | QH' | MAX | 23 | - | - |
| t _{PHL} | | | | 23 | - | - |
| t _{PLH} | SRLOAD ↓ | QH' | MAX | 57 | - | - |
| t _{PHL} | | | | 44 | - | - |
| t _{PLH} | SRCLR ↓ | QH' | MAX | 36 | - | - |
| t _{PHL} | | | | 60 | - | - |
| t _{PLH} | RCK ↑ | QH' | MAX | 48 | - | - |
| t _{PHL} | | | | - | 53 | 57 |
| t _{PLH} | SH _{CP} | Q7 | MAX | - | 53 | 57 |
| t _{PHL} | | | | - | 60 | 72 |
| t _{PLH} | PL | Q7 | MAX | - | 60 | 72 |
| t _{PHL} | | | | - | 72 | 84 |
| t _{PLH} | ST _{CP} | Q7 | MAX | - | 72 | 84 |
| t _{PHL} | | | | - | 53 | 66 |
| t _{PLH} | MR | Q7 | MAX | - | 53 | 66 |
| t _{PHL} | | | | - | 53 | 66 |

UNIT f_{max} : MHz, other : ns

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 85 | mA |
| I _{OH} | MAX | -2.6 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

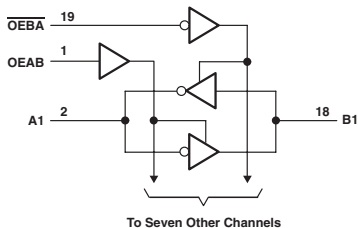
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|-------------------|-------------------------------|--------|------------|----|
| f _{max} | SRCK | Q | MIN | 20 |
| | SRCK | QHB | MIN | 20 |
| t _w | SRCK high | | MIN | 15 |
| | SRCK low | | MIN | 35 |
| | RCK | | MIN | 20 |
| | SRCLR | | MIN | 20 |
| | SRLOAD | | MIN | 40 |
| t _{su} | Data before RCK ↑ | | MIN | 20 |
| | DS before RCK ↑ | | MIN | 30 |
| | SRCKEN low before SRCK ↑ | | MIN | 20 |
| | SRCLR inactive before SRCK ↑ | | MIN | 25 |
| | SRLOAD inactive before SRCK ↑ | | MIN | 30 |
| | RCK ↑ before SRLOAD ↑ | | MIN | 40 |
| SER before SRCK ↑ | | MIN | 20 | |
| t _h | | | MIN | 0 |
| t _{PLH} | SRCK ↑ | QHB | MAX | 17 |
| t _{PHL} | | | | 23 |
| t _{PLH} | SRLOAD ↓ | QHB | MAX | 42 |
| t _{PHL} | | | | 39 |
| t _{PHL} | SRCLR ↓ | QHB | MAX | 27 |
| t _{PLH} | | | | 48 |
| t _{PHL} | RCK ↑ | QHB | MAX | 36 |
| t _{PLH} | | | | 18 |
| t _{PHL} | SHCP | Q7 | MAX | 28 |

UNIT f_{max} : MHz, other : ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State Inverting Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

| ENABLE INPUTS | | OPERATION |
|---------------|------|-----------------------------------|
| OEBA | OEAB | |
| L | L | B data to Abus |
| H | H | A data to B bus |
| H | L | Isolation |
| L | H | B data to Abus A data to B bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS-1 | AS | SN74 HC | SN74 BCT | ABT | AC 11 | ACT 11 | UNIT |
|--------------------------|------------|-----|-----|-------|-----|---------|----------|------|-------|--------|------|
| I _{CCZ} | MAX | 95 | 47 | 47 | 77 | 0.08 | 10 | 0.25 | 0.08 | 0.008 | mA |
| I _{CCL} | MAX | 90 | 44 | 44 | 122 | 0.08 | 84 | 30 | 0.08 | 0.008 | mA |
| I _{OH} (A port) | MAX | -15 | -15 | -15 | -15 | -6 | -3 | -32 | -24 | -24 | mA |
| I _{OH} (B port) | MAX | -15 | -15 | -15 | -15 | -6 | -15 | -32 | -24 | -24 | mA |
| I _{OL} (A port) | MAX | 24 | 24 | 48 | 64 | 6 | 24 | 64 | 24 | 24 | mA |
| I _{OL} (B port) | MAX | 24 | 24 | 48 | 64 | 6 | 64 | 64 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS-1 | AS | SN74 HC | SN74 BCT | ABT | AC 11 | ACT 11 |
|------------------|-------|--------|------------|----|-----|-------|----|---------|----------|-----|-------|--------|
| t _{PLH} | A | B | MAX | 10 | 10 | 10 | 7 | 26 | 5.8 | 4.8 | 7.4 | 9.4 |
| | | | | 15 | 10 | 10 | 6 | 26 | 3.6 | 4.8 | 7.1 | 8.6 |
| t _{PHL} | B | A | MAX | 10 | 10 | 10 | 7 | 26 | 6.9 | 4.8 | 7.4 | 9.4 |
| | | | | 15 | 10 | 10 | 6 | 26 | 3.9 | 4.8 | 7.1 | 8.6 |
| t _{PHZ} | OEBA | A | MAX | 40 | 17 | 17 | 8 | 53 | 10.6 | 5.5 | 8.9 | 10.3 |
| | | | | 40 | 25 | 25 | 9 | 53 | 11.1 | 7.1 | 8.5 | 10.1 |
| t _{PZL} | OEBA | A | MAX | 25 | 12 | 12 | 6 | 38 | 10 | 7 | 8.1 | 10.4 |
| | | | | 25 | 18 | 18 | 12 | 38 | 7.8 | 5.8 | 8.7 | 10.9 |
| t _{PZH} | OEAB | B | MAX | 40 | 18 | 18 | 8 | 53 | 7.4 | 6.8 | 8.8 | 11.3 |
| | | | | 40 | 25 | 25 | 9 | 53 | 9 | 6.4 | 8.8 | 11 |
| t _{PHZ} | OEAB | B | MAX | 25 | 12 | 12 | 6 | 38 | 8.1 | 6.5 | 8.2 | 9.4 |
| | | | | 25 | 18 | 18 | 13 | 38 | 5.9 | 5.6 | 8.6 | 9.6 |

UNIT: ns

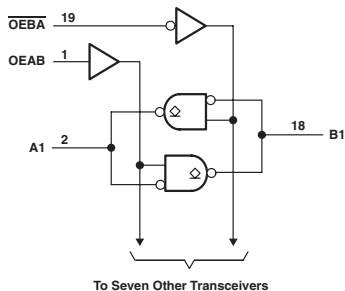
OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- Open-Collector True Outputs
- Schmitt-Triggered Inputs (SN74LS621)

FUNCTION TABLE

| ENABLE INPUTS | | OPERATION |
|---------------|------|-----------------------------------|
| OEBA | OEAB | |
| L | L | B data to Abus |
| H | H | A data to B bus |
| H | L | Isolation |
| L | H | B data to Abus A data to B bus |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | UNIT |
|-----------------|------------|-----|-----|---------|-----|------|
| I _{CC} | MAX | 90 | 48 | 48 | 189 | mA |
| V _{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I _{OL} | MAX | 24 | 24 | 48 | 64 | mA |

SWITCHING CHARACTERISTICS

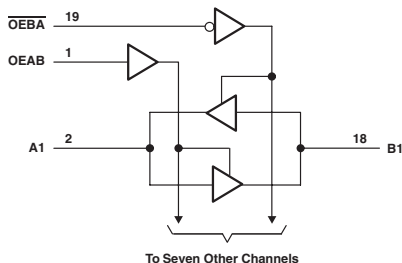
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS |
|------------------|-------|--------|------------|----|-----|---------|-----|
| t _{PLH} | A | B | MAX | 25 | 33 | 33 | 24 |
| | | | | 25 | 20 | 20 | 21 |
| t _{PHL} | B | A | MAX | 25 | 33 | 33 | 7.5 |
| | | | | 25 | 20 | 20 | 7.5 |
| t _{PLH} | OEBA | A | MAX | 40 | 39 | 39 | 21 |
| | | | | 50 | 35 | 35 | 9 |
| t _{PHL} | OEAB | B | MAX | 40 | 39 | 39 | 22 |
| | | | | 50 | 35 | 35 | 10 |

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State True Outputs
- Schmitt-Triggered Inputs (SN74LS623)
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| ENABLE INPUTS | | OPERATION |
|---------------|------|-----------------------------------|
| OEBA | OEAB | |
| L | L | B data to Abus |
| H | H | A data to B bus |
| H | L | Isolation |
| L | H | B data to Abus A data to B bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | F | SN74 HC | SN74 HCT | SN74 BCT | ABT | AC 11 | ACT 11 | CD74 AC | CD74 ACT | UNIT |
|--------------------------|------------|-----|-----|-----|-----|---------|----------|----------|------|-------|--------|---------|----------|------|
| I _{CCZ} | MAX | 95 | 55 | 116 | 130 | 0.08 | 0.08 | 11 | 0.25 | 0.08 | 0.04 | 0.16 | 0.16 | mA |
| I _{CCL} | MAX | 90 | 50 | 189 | 140 | 0.08 | 0.08 | 92 | 30 | 0.08 | 0.04 | 0.16 | 0.16 | mA |
| I _{OH} (A port) | MAX | -15 | -15 | -15 | -3 | -6 | -6 | -3 | -32 | -24 | -24 | -24 | -24 | mA |
| I _{OH} (B port) | MAX | -15 | -15 | -15 | -15 | -6 | -6 | -15 | -32 | -24 | -24 | -24 | -24 | mA |
| I _{OL} (A port) | MAX | 24 | 24 | 64 | 24 | 6 | 6 | 24 | 64 | 24 | 24 | 24 | 24 | mA |
| I _{OL} (B port) | MAX | 24 | 24 | 64 | 64 | 6 | 6 | 64 | 64 | 24 | 24 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

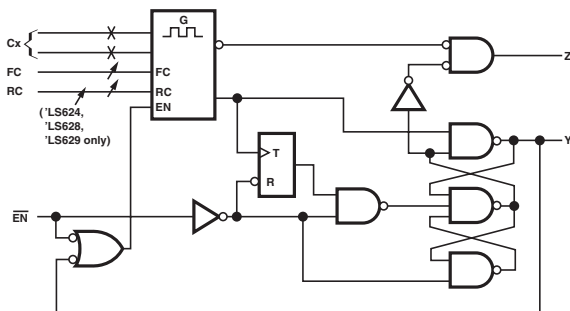
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | F | SN74 HC | SN74 HCT | SN74 BCT | ABT | AC 11 | ACT 11 | CD74 AC | CD74 ACT |
|------------------|-------|--------|------------|----|-----|------|------|---------|----------|----------|-----|-------|--------|---------|----------|
| t _{PLH} | A | B | MAX | 15 | 13 | 9 | 6.5 | 26 | 28 | 5.2 | 4.6 | 7.8 | 8.5 | 9.6 | 10.6 |
| | | | | 15 | 11 | 8 | 7.5 | 26 | 28 | 7.4 | 4.6 | 7.1 | 7.9 | 9.6 | 10.6 |
| t _{PHL} | B | A | MAX | 15 | 13 | 9 | 6.5 | 26 | 28 | 6.7 | 4.6 | 7.8 | 8.5 | 9.6 | 10.6 |
| | | | | 15 | 11 | 8.5 | 7.5 | 26 | 28 | 8 | 4.6 | 7.1 | 7.9 | 9.6 | 10.6 |
| t _{PZH} | OEBA | A | MAX | 40 | 22 | 11 | 12 | 53 | 53 | 10.6 | 7.5 | 9 | 9.7 | 13.4 | 14.4 |
| | | | | 40 | 22 | 10 | 10 | 53 | 53 | 10.7 | 7.5 | 9.1 | 10 | 13.4 | 14.4 |
| t _{PZH} | OEBA | A | MAX | 25 | 16 | 7.5 | 7.5 | 38 | 38 | 9.8 | 7.5 | 8.3 | 10.9 | 13.4 | 14.4 |
| | | | | 25 | 19 | 11.5 | 7 | 38 | 38 | 7.8 | 7.5 | 8.8 | 11.5 | 13.4 | 14.4 |
| t _{PLZ} | OEAB | B | MAX | 40 | 22 | 11.5 | 11.5 | 53 | 53 | 7.6 | 7.5 | 9.2 | 10.7 | 13.4 | 14.4 |
| | | | | 40 | 22 | 11 | 9.5 | 53 | 53 | 8.9 | 7.5 | 9.4 | 10.9 | 13.4 | 14.4 |
| t _{PHZ} | OEAB | B | MAX | 25 | 16 | 7 | 10 | 38 | 38 | 7.7 | 7.5 | 8.3 | 9.5 | 13.4 | 14.4 |
| | | | | 25 | 19 | 9 | 10 | 38 | 38 | 7.1 | 7.5 | 8.8 | 10 | 13.4 | 14.4 |

UNIT: ns

VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 35 | mA |
| I_{OL} | MAX | 24 | mA |
| I_{OH} | MAX | -1.2 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

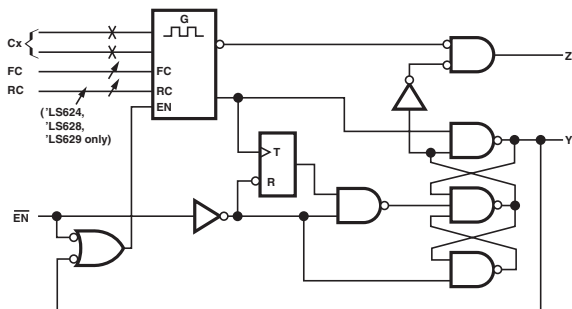
| PARAMETER | MAX or MIN | LS |
|-----------|------------|----|
| f_o | MAX | 25 |

UNIT: MHz

VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges
- Two Rexternal Pins Can Offer More Precise Temperature Compensation

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPER

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 35 | mA |
| I_{OH} | MAX | -1.2 | mA |
| I_{OL} | MAX | 24 | mA |

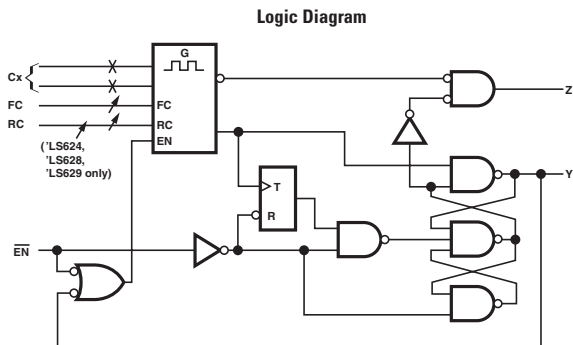
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTIC

| PARAMETER | MAX or MIN | LS |
|-----------|------------|----|
| f_o | MAX | 25 |

UNIT: MHz

DUAL VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 55 | mA |
| I_{OH} | MAX | -1.2 | mA |
| I_{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

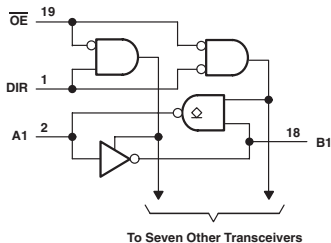
| PARAMETER | MAX or MIN | LS |
|-----------|------------|----|
| f_o | MAX | 25 |

UNIT: MHz

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- Inverting Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | UNIT |
|---------------------|------------|-----|-----|---------|-----|------|
| I _{CCZ} | MAX | 95 | 30 | 30 | 61 | mA |
| I _{CCL} | MAX | 90 | 41 | 41 | 122 | mA |
| I _{OH} (B) | MAX | -15 | -15 | -15 | -15 | mA |
| V _{OH} (A) | MAX | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I _{OL} | MAX | 24 | 24 | 48 | 64 | mA |

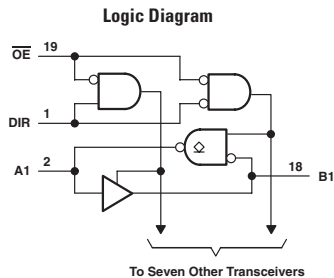
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS |
|------------------|-------|--------|------------|----|-----|---------|-----|
| | | | | ns | ns | ns | ns |
| t _{PLH} | A | B | MAX | 10 | 12 | 12 | 7 |
| | | | | 15 | 12 | 12 | 6.5 |
| t _{PHL} | B | A | MAX | 25 | 25 | 25 | 20 |
| | | | | 25 | 30 | 30 | 7 |
| t _{PLH} | OE | A | MAX | 40 | 25 | 25 | 19 |
| | | | | 60 | 45 | 45 | 9 |
| t _{PHL} | OE | B | MAX | 40 | 20 | 20 | 8 |
| | | | | 40 | 22 | 22 | 10 |
| t _{PHZ} | OE | B | MAX | 25 | 10 | 10 | 7 |
| | | | | 25 | 15 | 15 | 10 |

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS A-1 | | | | UNIT |
|---------------------|------------|---------|-----|-----|-----|------|
| | | LS | ALS | AS | | |
| I _{CCZ} | MAX | 95 | 54 | 54 | 100 | mA |
| I _{CCL} | MAX | 90 | 50 | 50 | 154 | mA |
| I _{OH} (B) | MAX | -15 | -15 | -15 | -15 | mA |
| V _{OH} (A) | MAX | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I _{OL} | MAX | 24 | 24 | 48 | 64 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS A-1 | | | |
|------------------|-------|--------|------------|---------|-----|----|------|
| | | | | LS | ALS | AS | |
| t _{PLH} | A | B | MAX | 15 | 12 | 12 | 9.5 |
| | | | | 15 | 12 | 12 | 9 |
| t _{PHL} | B | A | MAX | 25 | 30 | 30 | 22 |
| | | | | 25 | 22 | 22 | 9 |
| t _{PLH} | OE | A | MAX | 40 | 30 | 30 | 21.5 |
| | | | | 50 | 35 | 35 | 11.5 |
| t _{PZH} | OE | B | MAX | 40 | 21 | 21 | 10.5 |
| | | | | 40 | 25 | 25 | 10.5 |
| t _{PHZ} | OE | B | MAX | 25 | 10 | 10 | 7 |
| | | | | 25 | 16 | 16 | 10.5 |

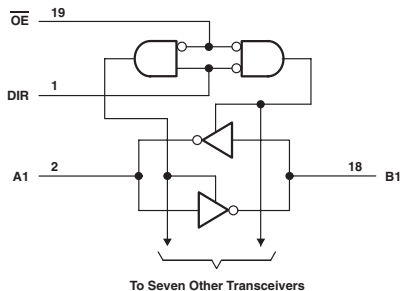
UNIT: ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Transceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS640, 640-1)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE (SN74)

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

Logic Diagram (SN74)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | LS-1 | ALS | ALS B-1 | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | ACT 11 | UNIT |
|--------------------------|------------|-----|------|-----|---------|-----|---------|---------|----------|----------|----------|------|--------|------|
| I _{CCZ} | MAX | 95 | 95 | 50 | 50 | 80 | 0.08 | 0.16 | 0.08 | 0.16 | 11 | 0.25 | 0.08 | mA |
| I _{CCL} | MAX | 90 | 90 | 55 | 55 | 123 | 0.08 | 0.16 | 0.08 | 0.16 | 94 | 30 | 0.08 | mA |
| I _{OH} (A port) | MAX | -15 | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -3 | -32 | -24 | mA |
| I _{OH} (B port) | MAX | -15 | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | -24 | mA |
| I _{OL} (A port) | MAX | 24 | 48 | 24 | 48 | 64 | 6 | 6 | 6 | 6 | 24 | 64 | 24 | mA |
| I _{OL} (B port) | MAX | 24 | 48 | 24 | 48 | 64 | 6 | 6 | 6 | 6 | 64 | 64 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | LS-1 | ALS | ALS B-1 | AS | SN74 HC | CD74 HC | SN74 HCT |
|------------------|-------|--------|------------|----|------|-----|---------|----|---------|---------|----------|
| t _{PLH} | A | B | MAX | 10 | 10 | 11 | 11 | 7 | 26 | 27 | 28 |
| | | | | 15 | 15 | 10 | 10 | 6 | 26 | 27 | 28 |
| t _{PHL} | B | A | MAX | 10 | 10 | 11 | 11 | 7 | 26 | 27 | 28 |
| | | | | 15 | 15 | 10 | 10 | 6 | 26 | 27 | 28 |
| t _{PZH} | OE | A | MAX | 40 | 40 | 21 | 21 | 8 | 58 | 45 | 58 |
| | | | | 40 | 40 | 24 | 24 | 10 | 58 | 45 | 58 |
| t _{PHZ} | OE | A | MAX | 25 | 25 | 10 | 10 | 8 | 38 | 45 | 50 |
| | | | | 25 | 25 | 15 | 15 | 13 | 38 | 45 | 50 |
| t _{PZH} | OE | B | MAX | 40 | 40 | 21 | 21 | 8 | 58 | 45 | 58 |
| | | | | 40 | 40 | 24 | 24 | 10 | 58 | 45 | 58 |
| t _{PHZ} | OE | B | MAX | 25 | 25 | 10 | 10 | 8 | 38 | 45 | 50 |
| | | | | 25 | 25 | 15 | 15 | 13 | 38 | 45 | 50 |

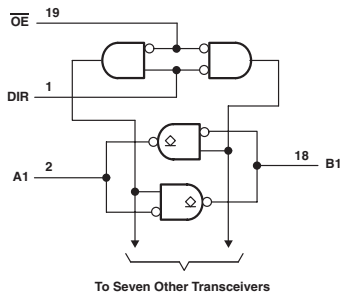
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HCT | SN74 BCT | ABT | ACT 11 |
|------------------|-------|--------|------------|----------|----------|-----|--------|
| t _{PLH} | A | B | MAX | 33 | 6.5 | 4.9 | 10.5 |
| | | | | 33 | 3.7 | 4.9 | 9.5 |
| t _{PHL} | B | A | MAX | 33 | 6.5 | 4.9 | 10.5 |
| | | | | 33 | 3.7 | 4.9 | 9.5 |
| t _{PZH} | OE | A | MAX | 45 | 10.2 | 5.8 | 13.4 |
| | | | | 45 | 10.7 | 7.3 | 13.6 |
| t _{PHZ} | OE | A | MAX | 45 | 10.2 | 6.8 | 13.9 |
| | | | | 45 | 7.8 | 5.5 | 14.2 |
| t _{PZH} | OE | B | MAX | 45 | 10.2 | 5.8 | 13.4 |
| | | | | 45 | 10.7 | 7.3 | 13.6 |
| t _{PHZ} | OE | B | MAX | 45 | 10.2 | 6.8 | 13.9 |
| | | | | 45 | 7.8 | 5.5 | 14.2 |

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS641)

Logic Diagram



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-----------------|
| \overline{G} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS | UNIT |
|-----------|------------|-----|------|-----|---------|-----|------|
| I_{CCZ} | MAX | 95 | 95 | - | - | - | mA |
| I_{CCL} | MAX | 90 | 90 | 47 | 47 | 136 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I_{OL} | MAX | 24 | 48 | 24 | 48 | 64 | mA |

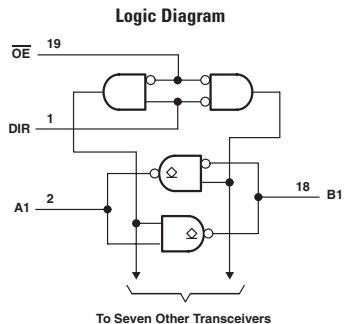
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS |
|-----------|-----------------|--------|------------|----|------|-----|---------|-----|
| t_{PLH} | A | B | MAX | 25 | 25 | 25 | 25 | 21 |
| t_{PHL} | | | | 25 | 25 | 18 | 18 | 7.5 |
| t_{PLH} | B | A | MAX | 25 | 25 | 25 | 25 | 21 |
| t_{PHL} | | | | 25 | 25 | 18 | 18 | 7.5 |
| t_{PLH} | \overline{OE} | A, B | MAX | 40 | 40 | 30 | 30 | 21 |
| t_{PHL} | | | | 50 | 50 | 30 | 30 | 9 |
| t_{PLH} | DIR | A, B | MAX | 40 | 40 | 32 | 32 | 22 |
| t_{PHL} | | | | 50 | 50 | 32 | 32 | 10 |

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

- Bidirectional Bus Transceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS642)



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-------------------------|
| OE | DIR | |
| L | L | \bar{B} data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS | UNIT |
|-----------|------------|-----|------|-----|---------|-----|------|
| I_{CCZ} | MAX | 95 | 95 | - | - | - | mA |
| I_{CCL} | MAX | 90 | 90 | 28 | 28 | 104 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | V |
| I_{OL} | MAX | 24 | 48 | 24 | 48 | 64 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS |
|-----------|------------------|--------|------------|----|------|-----|---------|------|
| t_{PLH} | A | B | MAX | 25 | 25 | 30 | 30 | 24 |
| t_{PHL} | | | | 25 | 25 | 22 | 22 | 7.5 |
| t_{PLH} | B | A | MAX | 25 | 25 | 30 | 30 | 24 |
| t_{PHL} | | | | 25 | 25 | 22 | 22 | 7.5 |
| t_{PLH} | \bar{OE} , DIR | A | MAX | 40 | 40 | 30 | 30 | 23.5 |
| t_{PHL} | | | | 60 | 60 | 38 | 38 | 11.5 |
| t_{PLH} | \bar{OE} , DIR | B | MAX | 40 | 40 | 30 | 30 | 23.5 |
| t_{PHL} | | | | 60 | 60 | 38 | 38 | 11.5 |

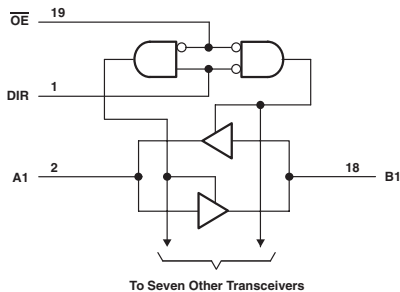
UNIT: ns

645

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Transceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS645, 645-1)

Logic Diagram



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS | SN74 HC | SN74 HCT | UNIT |
|-----------|------------|-----|------|-----|---------|-----|---------|----------|------|
| I_{CCZ} | MAX | 95 | 95 | 58 | 58 | 123 | 0.08 | 0.08 | mA |
| I_{CCL} | MAX | 90 | 90 | 55 | 55 | 149 | 0.08 | 0.08 | mA |
| I_{OH} | MAX | -15 | -15 | -15 | -15 | -15 | -6 | -6 | mA |
| I_{OL} | MAX | 24 | 48 | 24 | 48 | 64 | 6 | 6 | mA |

SWITCHING CHARACTERISTICS

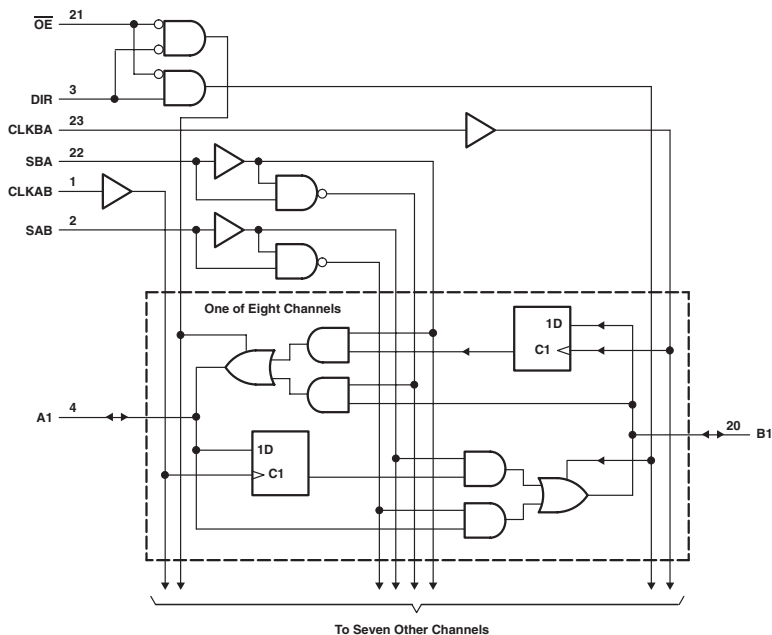
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | LS-1 | ALS | ALS A-1 | AS | SN74 HC | SN74 HCT |
|-----------|-----------------|--------|------------|----|------|-----|---------|-----|---------|----------|
| t_{PLH} | A | B | MAX | 15 | 15 | 10 | 10 | 9.5 | 26 | 28 |
| t_{PHL} | | | | 15 | 15 | 10 | 10 | 9 | 26 | 28 |
| t_{PLH} | B | A | MAX | 15 | 15 | 10 | 10 | 9.5 | 26 | 28 |
| t_{PHL} | | | | 15 | 15 | 10 | 10 | 9 | 26 | 28 |
| t_{PZH} | \overline{OE} | A | MAX | 40 | 40 | 20 | 20 | 11 | 58 | 58 |
| t_{PZL} | | | | 40 | 40 | 20 | 20 | 10 | 58 | 58 |
| t_{PHZ} | \overline{OE} | A | MAX | 25 | 25 | 10 | 10 | 7 | 50 | 50 |
| t_{PLZ} | | | | 25 | 25 | 15 | 15 | 12 | 50 | 50 |
| t_{PZH} | \overline{OE} | B | MAX | 40 | 40 | 20 | 20 | 11 | 58 | 58 |
| t_{PZL} | | | | 40 | 40 | 20 | 20 | 10 | 58 | 58 |
| t_{PHZ} | \overline{OE} | B | MAX | 25 | 25 | 10 | 10 | 7 | 50 | 50 |
| t_{PLZ} | | | | 25 | 25 | 15 | 15 | 12 | 50 | 50 |

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Transceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | ABT Ver.A | UNIT |
|-----------|------------|-----|-----|---------|-----|---------|---------|----------|----------|----------|-----|-----------|------|
| I_{CC} | MAX | 165 | 88 | 88 | 211 | 0.08 | 0.16 | 0.08 | 0.16 | 67 | 30 | 30 | mA |
| I_{OH} | MAX | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | -32 | mA |
| I_{OL} | MAX | 24 | 24 | 48 | 48 | 6 | 6 | 6 | 6 | 64 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | LVTH 3V | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LVC 3V | UNIT |
|-----------|------------|---------|-------|---------|--------|----------|--------|------|
| I_{CC} | MAX | 5 | 0.08 | 0.08 | 0.08 | 0.08 | 0.01 | mA |
| I_{OH} | MAX | -32 | -24 | -24 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 64 | 24 | 24 | 24 | 24 | 24 | mA |

FUNCTION TABLE (SN74)

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION | | | |
|--------|-----|--------|--------|-----|-----|-----------|--------|---------------------------|--|--|--|
| OE | DIR | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 | | | | |
| H | X | H to L | H to L | X | X | Input | Input | Isolation | | | |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data | | | |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus | | | |
| L | L | X | H to L | X | H | Output | Input | Stored B data to A bus | | | |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus | | | |
| L | H | H to L | X | H | X | Input | Output | Stored A data to B bus | | | |

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|------------------|------------------------------|--------|------------|----|------|---------|-----|---------|---------|----------|----------|----------|
| f _{max} | | | MIN | - | 40 | 40 | 90 | 27 | 20 | 27 | 17 | 83 |
| t _w | CLKBA,CLKAB "H" | | MIN | 15 | 12.5 | 12.5 | 5 | 19 | 24 | 19 | 38 | 6 |
| | CLKBA,CLKAB "L" | | | 30 | 12.5 | 12.5 | 6 | 19 | 24 | 19 | 38 | 6 |
| | DATA | | | 30 | - | - | - | - | - | - | - | - |
| t _{su} | CLKBA,CLKAB "H" | | MIN | 15 | 10 | 10 | 6 | 25 | - | 25 | 18 | 6 |
| | CLKBA,CLKAB "L" | | | 15 | 10 | 10 | 6 | 25 | - | 25 | 18 | 6 |
| t _h | CLKBA,CLKAB | | MIN | 0 | 0 | 0 | 5 | 11 | 5 | 5 | 0.5 | |
| ↑P _{LH} | CLOCK | A,B | MAX | 25 | 30 | 30 | 8.5 | 45 | 66 | 45 | 66 | 11.2 |
| ↑P _{HL} | | | | 35 | 17 | 17 | 9 | 45 | 66 | 45 | 66 | 10.6 |
| ↑P _{LH} | A,B | B,A | MAX | 18 | 20 | 20 | 9 | 34 | 41 | 34 | 56 | 9.5 |
| ↑P _{HL} | | | | 20 | 12 | 12 | 7 | 34 | 41 | 34 | 56 | 10.5 |
| ↑P _{LH} | SAB,SBA (sored data high) | A,B | MAX | 40 | 25 | 25 | 11 | 48 | 51 | 48 | 69 | 13.8 |
| ↑P _{HL} | | | | 35 | 20 | 20 | 9 | 48 | 51 | 48 | 69 | 9.1 |
| ↑P _{LH} | SAB,SBA (sored data low) | A,B | MAX | 50 | 35 | 35 | 11 | 48 | 51 | 48 | 69 | 12 |
| ↑P _{HL} | | | | 25 | 20 | 20 | 9 | 48 | 51 | 48 | 69 | 12.9 |
| ↑P _{ZH} | OE | A,B | MAX | 55 | 17 | 17 | 9 | 61 | 53 | 61 | 68 | 13.2 |
| ↑P _{ZL} | | | | 65 | 20 | 20 | 14 | 61 | 53 | 61 | 68 | 14.4 |
| ↑P _{HZ} | OE | A,B | MAX | 35 | 10 | 10 | 9 | 61 | 53 | 61 | 53 | 10.9 |
| ↑P _{LZ} | | | | 35 | 16 | 16 | 9 | 61 | 53 | 61 | 53 | 10.5 |
| ↑P _{ZH} | DIR | A,B | MAX | 45 | 30 | 30 | 16 | 61 | 53 | 61 | - | 13.1 |
| ↑P _{ZL} | | | | 60 | 25 | 25 | 18 | 61 | 53 | 61 | - | 14.6 |
| ↑P _{HZ} | DIR | A,B | MAX | 30 | 10 | 10 | 10 | 61 | 53 | 61 | - | 12.6 |
| ↑P _{LZ} | | | | 30 | 16 | 16 | 10 | 61 | 53 | 61 | - | 11.8 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABT Ver.A | LVTH 3V | AC 11 | CD74 AC | AC 11 | CD74 ACT | LVC 3V |
|------------------|------------------------------|--------|------------|-----|-----------|---------|-------|---------|-------|----------|--------|
| f _{max} | | | MIN | 125 | 125 | 150 | 100 | 125 | 105 | 110 | 150 |
| t _w | CLKBA,CLKAB "H" | | MIN | 4 | 4 | 3.3 | 5 | 4 | 4.8 | 4.5 | 3.3 |
| | CLKBA,CLKAB "L" | | | 4 | 4 | 3.3 | 5 | 4 | 4.8 | 4.5 | 3.3 |
| | DATA | | | - | - | - | - | - | - | - | - |
| t _{su} | CLKBA,CLKAB "H" | | MIN | 3.5 | 3 | 1.2 | 4.5 | 2.5 | 4.5 | 2.5 | 1.5 |
| | CLKBA,CLKAB "L" | | | 3 | 3 | 1.6 | 4.5 | 2.5 | 4.5 | 2.5 | 1.5 |
| t _h | CLKBA,CLKAB | | MIN | 0 | 0 | 0.8 | 1 | 2 | 2.5 | 2 | 1.7 |
| ↑P _{LH} | CLOCK | A,B | MAX | 7.8 | 5.6 | 4.7 | 11 | 13.5 | 13.5 | 15.5 | 8.4 |
| ↑P _{HL} | | | | 8.4 | 5.6 | 4.7 | 12.2 | 13.5 | 14.9 | 15.5 | 8.4 |
| ↑P _{LH} | A,B | B,A | MAX | 6.9 | 4.8 | 3.5 | 8.8 | 11 | 11.5 | 12.5 | 7.4 |
| ↑P _{HL} | | | | 6.9 | 5.4 | 3.5 | 9.8 | 11 | 12 | 12.5 | 7.4 |
| ↑P _{LH} | SAB,SBA (sored data high) | A,B | MAX | 7.1 | 6.5 | 4.9 | 9.4 | 12 | 11.5 | 14.5 | 8.6 |
| ↑P _{HL} | | | | 7.9 | 5.9 | 4.9 | 10.7 | 12 | 13.5 | 14.5 | 8.6 |
| ↑P _{LH} | SAB,SBA (sored data low) | A,B | MAX | 7.1 | 6.5 | 4.9 | 9.9 | 12 | 12.4 | 14.5 | 8.6 |
| ↑P _{HL} | | | | 7.9 | 5.9 | 4.9 | 11 | 12 | 13.1 | 14.5 | 8.6 |
| ↑P _{ZH} | OE | A,B | MAX | 6.3 | 6.3 | 5.2 | 12 | 13.5 | 14.4 | 15.5 | 8.2 |
| ↑P _{ZL} | | | | 8.8 | 8.8 | 5.2 | 13.1 | 13.5 | 15.3 | 15.5 | 8.2 |
| ↑P _{HZ} | OE | A,B | MAX | 8.3 | 5 | 5.5 | 8.9 | 13.5 | 11.6 | 15.5 | 7.5 |
| ↑P _{LZ} | | | | 7.5 | 4.5 | 5.5 | 8.3 | 13.5 | 10.6 | 15.5 | 7.5 |
| ↑P _{ZH} | DIR | A,B | MAX | 6.7 | 6.7 | 5.2 | 12.6 | 13.5 | 15.3 | 15.5 | 8.3 |
| ↑P _{ZL} | | | | 9.5 | 9.5 | 5.2 | 13.7 | 13.5 | 16.5 | 15.5 | 8.3 |
| ↑P _{HZ} | DIR | A,B | MAX | 7.7 | 5.7 | 5.6 | 8.7 | 13.5 | 11.3 | 15.5 | 7.9 |
| ↑P _{LZ} | | | | 8.2 | 6 | 5.6 | 8.1 | 13.5 | 10.3 | 15.5 | 7.9 |

UNIT f_{max}: MHz other: ns

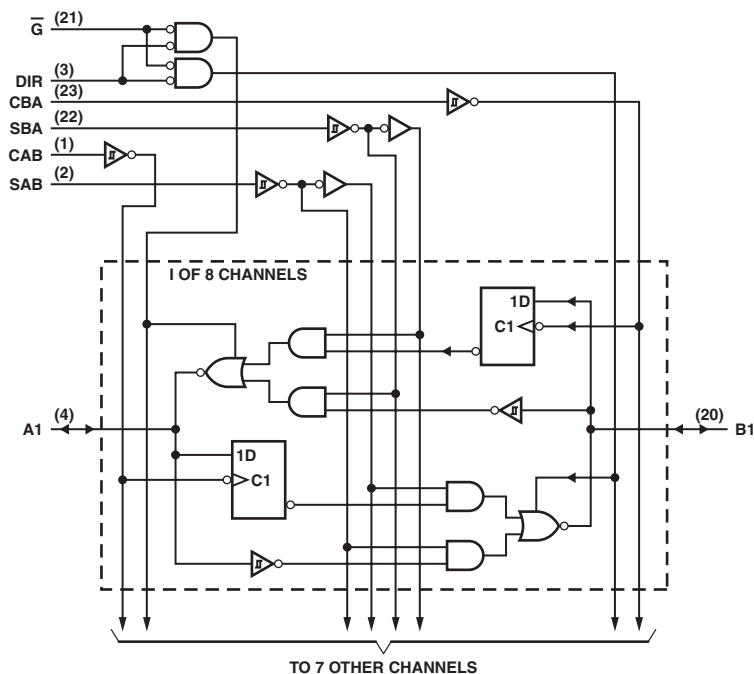
CD74HC: NOT RECOMMENDED FOR NEW DESIGNS

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See www.ti.com/sc/logic for the most current data sheets.

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Transceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Open-Collector Outputs

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|-----------|-----|--------|--------|-----|-----|-----------|--------|---|
| \bar{G} | DIR | CAB | CBA | SAB | SBA | A1–A8 | B1–B8 | |
| H | X | H to L | H to L | X | X | Input | Input | Isolation Store A and B data |
| H | X | ↑ | ↑ | X | X | Input | Input | |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus Stored B data to A bus |
| L | L | X | H to L | X | H | Output | Output | |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus Stored A data to B bus |
| L | H | H to L | X | H | X | Input | Output | |

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 150 | mA |
| V _{OH} | MAX | 5.5 | V |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

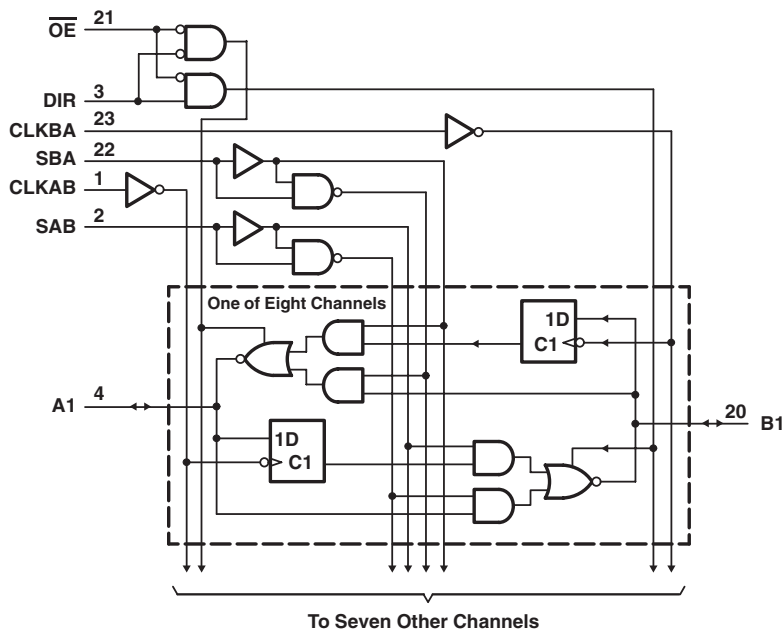
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|-----------------------------------|--------|------------|----|
| t _w | | | MIN | 30 |
| t _{su} | | A, B | MIN | 15 |
| t _h | | A, B | MIN | 0 |
| t _{PLH} | CLOCK | A, B | MAX | 35 |
| t _{PHL} | | | | 45 |
| t _{PLH} | A, B | B, A | MAX | 26 |
| t _{PHL} | | | | 27 |
| t _{PLH} | SAB, SBA (With Bus Input High) | A, B | MAX | 50 |
| t _{PHL} | | | | 45 |
| t _{PLH} | SAB, SBA (With Bus Input Low) | A, B | MAX | 60 |
| t _{PHL} | | | | 30 |
| t _{PLH} | \bar{G} | A, B | MAX | 40 |
| t _{PHL} | | | | 50 |
| t _{PLH} | DIR | A, B | MAX | 35 |
| t _{PHL} | | | | 40 |

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Trceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|--------|-----|--------|------------------|-----|-----|-----------|--------|---|
| OE | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| H | X | H to L | CLKAB, CLKBA "H" | X | X | Input | Input | Isolation Store A and B data |
| H | X | ↑ | ↑ | X | X | Input | Input | |
| L | L | X | CLKAB, CLKBA "L" | X | L | Output | Input | Real-time B data to A bus Stored B data to A bus |
| L | L | X | H to L | X | H | Output | Output | |
| L | H | X | CLKAB, CLKBA | L | X | Input | Output | Real-time A data to B bus Stored A data to B bus |
| L | H | H to L | X | H | X | Input | Output | |

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | AS | SN74 HC | SN74 HCT | UNIT |
|-----------------|------------|-----|-----|-----|---------|----------|------|
| I _{CC} | MAX | 180 | 88 | 195 | 0.08 | 0.08 | mA |
| I _{OH} | MAX | -15 | -15 | -15 | -6 | -6 | mA |
| I _{OL} | MAX | 24 | 24 | 48 | 6 | 6 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

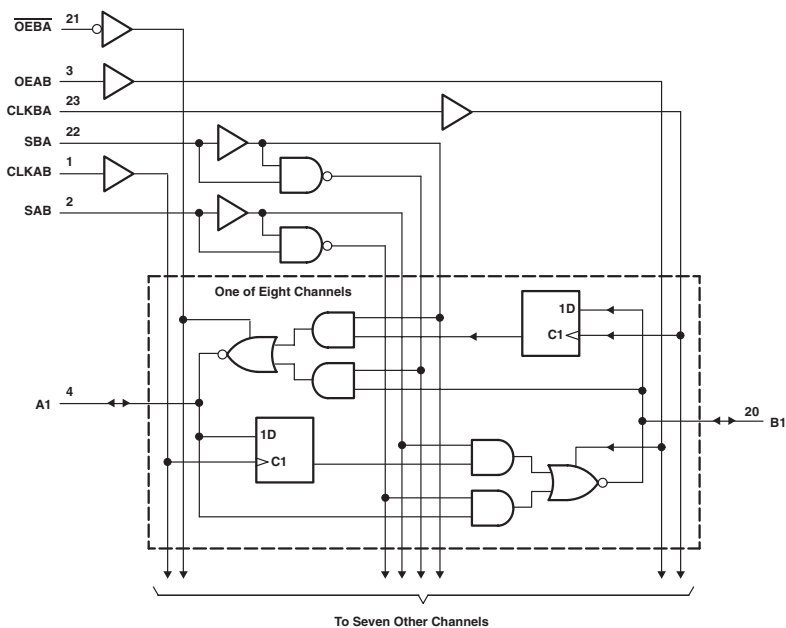
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | AS | SN74 HC | SN74 HCT |
|------------------|-----------------------------------|--------|------------|----|------|-----|---------|----------|
| f _{max} | | | MIN | - | 40 | 90 | 27 | 27 |
| t _w | CLKAB, CLKBA "H" | | MIN | 15 | 12.5 | 5 | 19 | 19 |
| | CLKAB, CLKBA "L" | | MIN | 30 | 12.5 | 6 | 19 | 19 |
| | DATA | | MIN | 30 | - | - | - | - |
| t _{su} | CLKAB, CLKBA | | MIN | 15 | 10 | 6 | 25 | 25 |
| t _h | CLKAB, CLKBA | | MIN | 0 | 0 | 0 | 5 | 5 |
| t _{PLH} | CLOCK | A, B | MAX | 25 | 33 | 8.5 | 45 | 45 |
| t _{PHL} | | | | 40 | 20 | 9 | 45 | 45 |
| t _{PLH} | A, B | B, A | MAX | 18 | 17 | 8 | 34 | 34 |
| t _{PHL} | | | | 25 | 10 | 7 | 34 | 34 |
| t _{PLH} | SAB, SBA (With Bus Input High) | A, B | MAX | 55 | 25 | 11 | 48 | 48 |
| t _{PHL} | | | | 40 | 21 | 9 | 48 | 48 |
| t _{PLH} | SAB, SBA (With Bus Input Low) | A, B | MAX | 40 | 39 | 11 | 48 | 48 |
| t _{PHL} | | | | 40 | 22 | 9 | 48 | 48 |
| t _{PZH} | OE | A, B | MAX | 50 | 22 | 9 | 61 | 61 |
| t _{PZL} | | | | 55 | 22 | 15 | 61 | 61 |
| t _{PHZ} | OE | A, B | MAX | 45 | 10 | 9 | 61 | 61 |
| t _{PLZ} | | | | 35 | 15 | 9 | 61 | 61 |
| t _{PZH} | DIR | A, B | MAX | 40 | 27 | 16 | 61 | 61 |
| t _{PZL} | | | | 45 | 19 | 18 | 61 | 61 |
| t _{PHZ} | DIR | A, B | MAX | 35 | 14 | 10 | 61 | 61 |
| t _{PLZ} | | | | 30 | 15 | 10 | 61 | 61 |

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| INPUTS | | | | | | DATA I/O | | | | OPERATION OR FUNCTION |
|--------|------|--------|--------|-----|-----|-------------|-------------|--|--|--|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 | | | |
| L | H | H to L | H to L | X | X | Input | Input | | | Isolation Store A and B data |
| L | H | ↑ | ↑ | X | X | Input | Input | | | |
| X | H | ↑ | H to L | X | X | Input | Unspecified | | | Store A, hold B Store A in both registers |
| H | H | ↑ | ↑ | X | X | Input | Output | | | |
| L | X | H to L | ↑ | X | X | Unspecified | Input | | | Hold A, store B Store B in both registers |
| L | L | ↑ | ↑ | X | X | | Input | | | |
| L | L | X | X | X | L | Output | Input | | | Real-time \bar{B} data to A bus Stored \bar{B} data to A bus |
| L | L | X | H to L | X | H | | Input | | | |
| H | H | X | X | L | X | Input | Output | | | Real-time \bar{A} data to B bus Stored \bar{A} data to B bus |
| H | H | H to L | X | H | X | | Output | | | |
| H | L | H to L | H to L | H | H | Output | Output | | | Stored \bar{A} data to B bus and stored \bar{B} data to A bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | SN74 HCT | SN74 BCT | ABT | CD74 ACT | UNIT |
|-----------------|------------|-----|-----|---------|-----|---------|----------|----------|-----|----------|------|
| I _{cc} | MAX | 165 | 82 | 82 | 195 | 0.08 | 0.08 | 62 | 30 | 160 | mA |
| I _{oh} | MAX | -15 | -15 | -15 | -15 | -6 | -6 | -15 | -32 | -24 | mA |
| I _{ol} | MAX | 24 | 24 | 48 | 48 | 6 | 6 | 64 | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

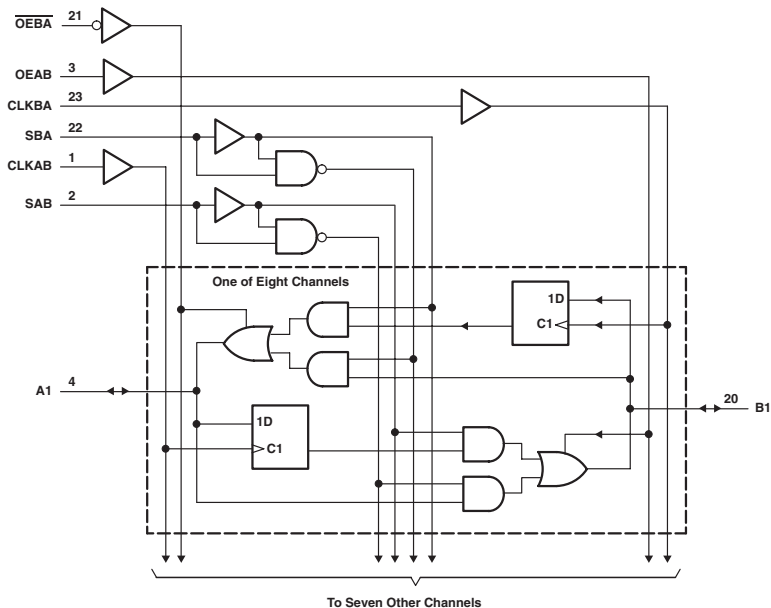
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | SN74 HCT | SN74 BCT | ABT | CD74 ACT |
|------------------|----------------------------------|--------|------------|----|------|---------|-----|---------|----------|----------|-----|----------|
| t _{max} | | | MIN | - | 40 | 40 | 90 | 27 | 20 | 85 | 125 | 110 |
| t _w | CLKBA, CLKAB "H" | | MIN | 15 | 12.5 | 12.5 | 5 | 19 | 25 | 4.8 | 4 | 4.5 |
| | CLKBA, CLKAB "L" | | MIN | 15 | 12.5 | 12.5 | 6 | 19 | 25 | 7 | 4 | 4.5 |
| | DATA | | MIN | 15 | - | - | - | - | - | - | - | - |
| t _{su} | A,B | | MIN | 15 | 10 | 10 | 6 | 25 | 19 | 6 | 3 | 2.5 |
| t _h | A,B | | MIN | 0 | 0 | 0 | 0 | 5 | 5 | 1 | 0 | 2 |
| t _{PLH} | CLOCK | A,B | MAX | 24 | 32 | 32 | 8.5 | 45 | 45 | 11.7 | 5.6 | 15.5 |
| t _{PHL} | | | | 35 | 17 | 17 | 9 | 45 | 45 | 11.8 | 5.6 | 15.5 |
| t _{PLH} | A,B | B,A | MAX | 18 | 18 | 18 | 9 | 34 | 34 | 12.6 | 6.2 | 12.5 |
| t _{PHL} | | | | 30 | 10 | 10 | 7 | 34 | 34 | 9.8 | 5.4 | 12.5 |
| t _{PLH} | SAB,SBA (With Bus Input High) | A,B | MAX | 47 | 38 | 38 | 11 | 48 | 48 | 9.8 | 6.5 | 15.5 |
| t _{PHL} | | | | 33 | 21 | 21 | 9 | 48 | 48 | 15.5 | 5.9 | 15.5 |
| t _{PLH} | SAB,SBA (With Bus Input Low) | A,B | MAX | 35 | 25 | 25 | 11 | 48 | 48 | 14.6 | 6.5 | 15.5 |
| t _{PHL} | | | | 30 | 21 | 21 | 9 | 48 | 48 | 12.8 | 5.9 | 15.5 |
| t _{PZH} | \overline{OEBA} | A | MAX | 44 | 20 | 20 | 10 | 61 | 61 | 12 | 5.8 | 15.5 |
| t _{PZL} | | | | 60 | 18 | 18 | 16 | 61 | 61 | 13.1 | 8.5 | 15.5 |
| t _{PHZ} | \overline{OEBA} | A | MAX | 38 | 9 | 9 | 9 | 61 | 61 | 10.2 | 5 | 15.5 |
| t _{PLZ} | | | | 30 | 12 | 12 | 9 | 61 | 61 | 9.6 | 4.1 | 15.5 |
| t _{PZH} | OEAB | B | MAX | 29 | 22 | 22 | 11 | 61 | 61 | 8.3 | 6.5 | 15.5 |
| t _{PZL} | | | | 40 | 21 | 21 | 16 | 61 | 61 | 9.7 | 7.4 | 15.5 |
| t _{PHZ} | OEAB | B | MAX | 38 | 12 | 12 | 10 | 61 | 61 | 15 | 5.5 | 15.5 |
| t _{PLZ} | | | | 30 | 14 | 14 | 11 | 61 | 61 | 12.3 | 5.1 | 15.5 |

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Transceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

| OEAB | | OEB A | | INPUTS | | DATA I/O | | OPERATION OR FUNCTION |
|------|-------|--------|--------|--------|-----|-------------|-------------|---|
| OEAB | OEB A | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 | |
| L | H | H to L | H to L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H to L | X | X | Input | Unspecified | Store A, hold B |
| H | H | ↑ | ↑ | X | X | Input | Output | Store A in both registers |
| L | X | H to L | ↑ | X | X | Unspecified | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H to L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | H to L | X | H | X | Input | Output | Stored A data to B bus |
| H | L | H to L | H to L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT | ABT | UNIT |
|-----------------|------------|-----|-----|---------|-----|---------|---------|----------|----------|----------|-----|------|
| I _{CC} | MAX | 180 | 88 | 88 | 211 | 0.08 | 0.16 | 0.08 | 0.16 | 69 | 30 | mA |
| I _{OH} | MAX | -15 | -15 | -15 | -15 | -6 | -6 | -6 | -6 | -15 | -32 | mA |
| I _{OL} | MAX | 24 | 24 | 48 | 48 | 6 | 6 | 6 | 6 | 64 | 64 | mA |

| PARAMETER | MAX or MIN | ABT Ver.A | LVTH 3V | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LVC 3V | UNIT |
|-----------------|------------|-----------|---------|-------|---------|--------|----------|--------|------|
| I _{CC} | MAX | 30 | 5 | 0.08 | 0.16 | 0.08 | 0.16 | 0.01 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -24 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 24 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | ALS A-1 | AS | SN74 HC | CD74 HC | SN74 HCT | CD74 HCT | SN74 BCT |
|------------------|----------------------------------|--------|------------|----|------|---------|-----|---------|---------|----------|----------|----------|
| f _{max} | | | MIN | - | 40 | 40 | 90 | 27 | 20 | 20 | 17 | 77 |
| t _w | CLKBA, CLKAB "H" | | MIN | 15 | 12.5 | 12.5 | 5 | 19 | 24 | 25 | 38 | 6.5 |
| | CLKBA, CLKAB "L" | | MIN | 15 | 12.5 | 12.5 | 6 | 19 | 24 | 25 | 38 | 6.5 |
| | DATA | | MIN | 15 | - | - | - | - | - | - | - | - |
| t _{su} | A,B High | | MIN | 15 | 10 | 10 | 6 | 25 | 18 | 19 | 18 | 5 |
| | A,B Low | | MIN | 15 | 10 | 10 | 6 | 25 | 18 | 19 | 18 | 5 |
| t _h | A,B | | MIN | 0 | 0 | 0 | 5 | 11 | 5 | 5 | 1 | |
| t _{PLH} | CLOCK | A,B | MAX | 25 | 30 | 30 | 8.5 | 45 | 66 | 45 | 66 | 10.5 |
| | | | | 36 | 17 | 17 | 9 | 45 | 66 | 45 | 66 | 9.9 |
| t _{PHL} | A,B | B,A | MAX | 18 | 18 | 18 | 9 | 34 | 41 | 34 | 56 | 8.9 |
| | | | | 20 | 12 | 12 | 7 | 34 | 41 | 34 | 56 | 9.8 |
| t _{PLH} | SAB,SBA (With Bus Input High) | A,B | MAX | 35 | 35 | 35 | 11 | 48 | 51 | 48 | 69 | 13.1 |
| | | | | 32 | 20 | 20 | 9 | 48 | 51 | 48 | 69 | 8.5 |
| t _{PHL} | SAB,SBA (With Bus Input Low) | A,B | MAX | 50 | 25 | 25 | 11 | 48 | 51 | 48 | 69 | 11.3 |
| | | | | 23 | 20 | 20 | 9 | 48 | 51 | 48 | 69 | 12.5 |
| t _{PZH} | OEBA | A | MAX | 45 | 17 | 17 | 10 | 61 | 53 | 61 | 68 | 10.6 |
| | | | | 54 | 18 | 18 | 16 | 61 | 53 | 61 | 68 | 12 |
| t _{PHZ} | OEBA | A | MAX | 38 | 10 | 10 | 9 | 61 | 53 | 61 | 53 | 10 |
| | | | | 30 | 16 | 16 | 9 | 61 | 53 | 61 | 53 | 9.5 |
| t _{PZH} | OEAB | B | MAX | 30 | 22 | 22 | 11 | 61 | 53 | 61 | 68 | 8.1 |
| | | | | 38 | 18 | 18 | 16 | 61 | 53 | 61 | 68 | 9.3 |
| t _{PHZ} | OEAB | B | MAX | 38 | 10 | 10 | 10 | 61 | 53 | 61 | 53 | 11.6 |
| | | | | 30 | 16 | 16 | 11 | 61 | 53 | 61 | 53 | 11.3 |

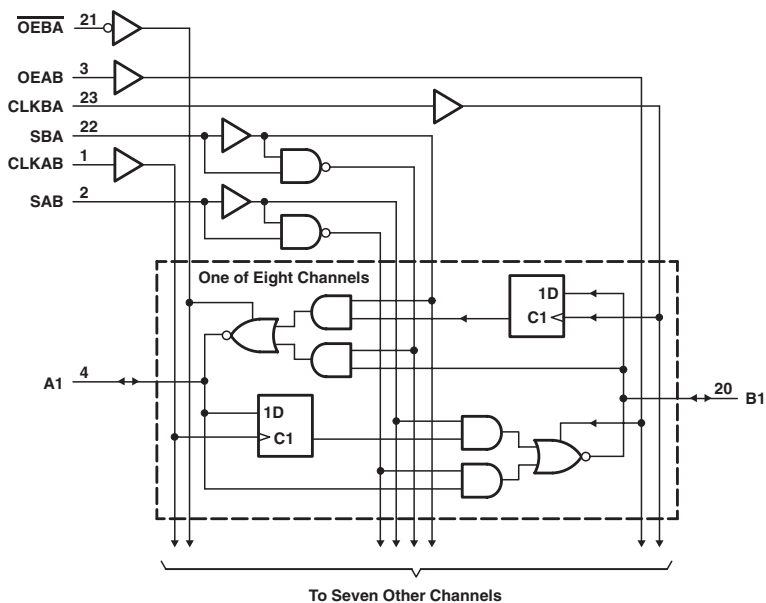
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABT Ver.A | LVTH 3V | AC 11 | CD74 AC | ACT 11 | CD74 ACT | LVC 3V |
|------------------|----------------------------------|--------|------------|-----|-----------|---------|-------|---------|--------|----------|--------|
| f _{max} | | | MIN | 125 | 125 | 150 | 105 | 125 | 105 | 110 | 100 |
| t _w | CLKBA, CLKAB "H" | | MIN | 4 | 4 | 3.3 | 4.8 | 4 | 4.8 | 4.5 | 3.3 |
| | CLKBA, CLKAB "L" | | MIN | 4 | 4 | 3.3 | 4.8 | 4 | 4.8 | 4.5 | 3.3 |
| | DATA | | MIN | - | - | - | - | - | - | - | - |
| t _{su} | A,B High | | MIN | 3.5 | 3 | 1.2 | 4.5 | 2.5 | 4 | 2.5 | 1.9 |
| | A,B Low | | MIN | 3.5 | 3 | 1.6 | 4.5 | 2.5 | 4 | 2.5 | 1.9 |
| t _h | A,B | | MIN | 0 | 0 | 0.8 | 1 | 2 | 2.5 | 2 | 1.7 |
| t _{PLH} | CLOCK | A,B | MAX | 7.8 | 5.6 | 4.7 | 10.7 | 13.5 | 13.1 | 15.5 | 8 |
| | | | | 8.4 | 5.6 | 4.7 | 12 | 13.5 | 14.4 | 15.5 | 8 |
| t _{PHL} | A,B | B,A | MAX | 6.7 | 4.8 | 3.5 | 8.6 | 11 | 11.1 | 12.5 | 7.4 |
| | | | | 6.7 | 5.4 | 3.5 | 9.6 | 11 | 11.6 | 12.5 | 7.4 |
| t _{PLH} | SAB,SBA (With Bus Input High) | A,B | MAX | 6.9 | 6.5 | 4.9 | 9.1 | 12 | 11 | 14.5 | 8.7 |
| | | | | 7.7 | 5.9 | 4.9 | 10.7 | 12 | 13.3 | 14.5 | 8.7 |
| t _{PHL} | SAB,SBA (With Bus Input Low) | A,B | MAX | 6.9 | 6.5 | 4.9 | 9.9 | 12 | 12.2 | 14.5 | 8.7 |
| | | | | 7.7 | 5.9 | 4.9 | 10.9 | 12 | 12.6 | 14.5 | 8.7 |
| t _{PZH} | OEBA | A | MAX | 5.8 | 5.8 | 5.2 | 10.9 | 13.5 | 12.6 | 15.5 | 7.4 |
| | | | | 8.5 | 8.5 | 5.2 | 12.2 | 13.5 | 13.8 | 15.5 | 7.4 |
| t _{PHZ} | OEBA | A | MAX | 8.2 | 5 | 5.5 | 7.6 | 13.5 | 9.9 | 15.5 | 7.5 |
| | | | | 6.8 | 4.1 | 5.5 | 7.1 | 13.5 | 9.3 | 15.5 | 7.5 |
| t _{PZH} | OEAB | B | MAX | 6.5 | 6.5 | 4.7 | 11.3 | 13.5 | 15.2 | 15.5 | 7.1 |
| | | | | 7.4 | 7.4 | 4.7 | 12.3 | 13.5 | 16.1 | 15.5 | 7.1 |
| t _{PHZ} | OEAB | B | MAX | 6.9 | 5.5 | 5.6 | 7.6 | 13.5 | 10.3 | 15.5 | 7.4 |
| | | | | 6.2 | 5.1 | 5.6 | 7.2 | 13.5 | 9.3 | 15.5 | 7.4 |

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Outputs
 - A Bus: Open-Collector
 - B Bus: 3-State

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|--------|------|--------|--------|-----|-----|--------------|--------------|--|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified‡ | Store A, hold B Store A in both registers |
| H | H | ↑ | ↑ | X† | X | Input | Output | |
| L | X | H or L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B Store B in both registers |
| L | L | ↑ | ↑ | X | X† | Output | Input | |
| L | L | X | X | X | L | Output | Input | Real-time \overline{B} data to A bus Stored \overline{B} data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time \overline{A} data to B bus Stored \overline{A} data to B bus |
| H | H | H or L | X | H | X | | | |
| H | L | H or L | H or L | H | H | Output | Output | Stored \overline{A} data to B bus and stored \overline{B} data to A bus |

NOTES:

† The data output functions can be enabled or disabled by a variety of level combinations at GAB or \overline{GBA} . Data input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

§ Select control = H: clock must be staggered to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | UNIT |
|-----------------|------------|-----|-----|------|
| I _{CC} | MAX | 165 | 88 | mA |
| I _{OH} | MAX | -15 | -15 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

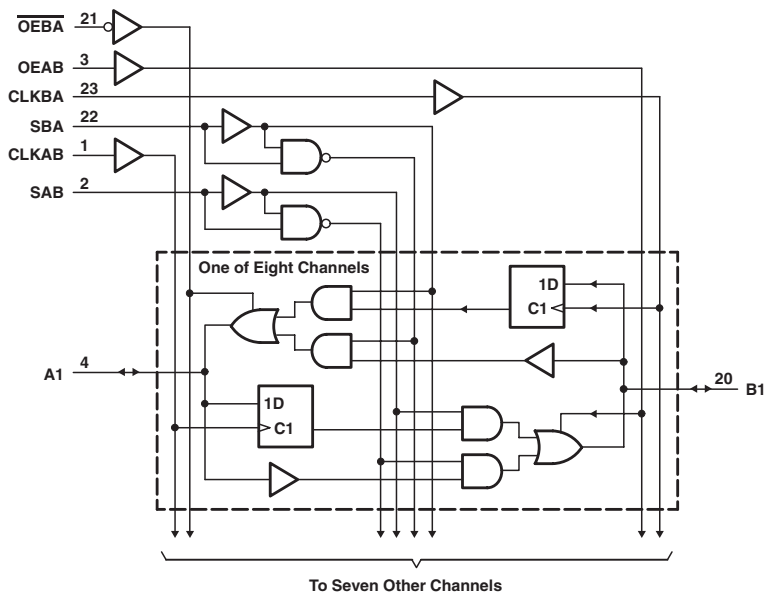
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS |
|------------------|-------------------|--------|------------|----|------|
| t _w | CLK "H" | | MIN | 15 | 14.5 |
| | CLK "L" | | MIN | 30 | 14.5 |
| | DATA | | MIN | 30 | - |
| t _{su} | A, B | | MIN | 15 | 10 |
| | A, B | | MIN | 0 | 0 |
| t _{PLH} | CLKBA | A | MAX | 38 | 64 |
| t _{PHL} | | | | 39 | 22 |
| t _{PLH} | CLKAB | B | MAX | 23 | 30 |
| t _{PHL} | | | | 36 | 17 |
| t _{PLH} | | | | 18 | 18 |
| t _{PHL} | A | B | MAX | 30 | 15 |
| t _{PLH} | B | A | MAX | 32 | 56 |
| t _{PHL} | | | | 24 | 15 |
| t _{PLH} | SBA (B "H") | A | MAX | 57 | 62 |
| t _{PHL} | | | | 39 | 25 |
| t _{PLH} | SBA (B "L") | A | MAX | 51 | 62 |
| t _{PHL} | | | | 35 | 25 |
| t _{PLH} | SAB (A "H") | B | MAX | 48 | 35 |
| t _{PHL} | | | | 33 | 22 |
| t _{PLH} | SAB (A "L") | B | MAX | 36 | 25 |
| t _{PHL} | | | | 30 | 22 |
| t _{PLH} | \overline{OEBA} | A | MAX | 35 | 30 |
| t _{PHL} | | | | 55 | 24 |
| t _{PZH} | OEAB | B | MAX | 29 | 22 |
| t _{PZL} | | | | 38 | 22 |
| t _{PHZ} | OEAB | B | MAX | 39 | 14 |
| t _{PLZ} | | | | 29 | 16 |

UNIT:ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Outputs
 - A Bus: Open-Collector
 - B Bus: 3-State

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|--------|------|--------|--------|-----|-----|-------------|-------------|--|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 | |
| L | H | H to L | H to L | X | X | Input | Input | Isolation Store A and B data |
| L | H | ↑ | ↑ | X | X | Input | Input | |
| X | H | ↑ | H to L | X | X | Input | Unspecified | Store A, hold B Store A in both registers |
| H | H | ↑ | ↑ | X | X | Input | Output | |
| L | X | H to L | ↑ | X | X | Unspecified | Input | Hold A, store B Store B in both registers |
| L | L | ↑ | ↑ | X | X | | Input | |
| L | L | X | X | X | L | Output | Input | Real-time \bar{B} data to A bus Stored \bar{B} data to A bus |
| L | L | X | H to L | X | H | Output | Input | |
| H | H | X | X | L | X | Input | Output | Real-time \bar{A} data to B bus Stored \bar{A} data to B bus |
| H | H | H to L | X | H | X | Input | Output | |
| H | L | H to L | H to L | H | H | Output | Output | Stored \bar{A} data to B bus and stored \bar{B} data to A bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | UNIT |
|-----------------|------------|-----|-----|------|
| I _{CC} | MAX | 180 | 88 | mA |
| I _{OH} | MAX | -15 | -15 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

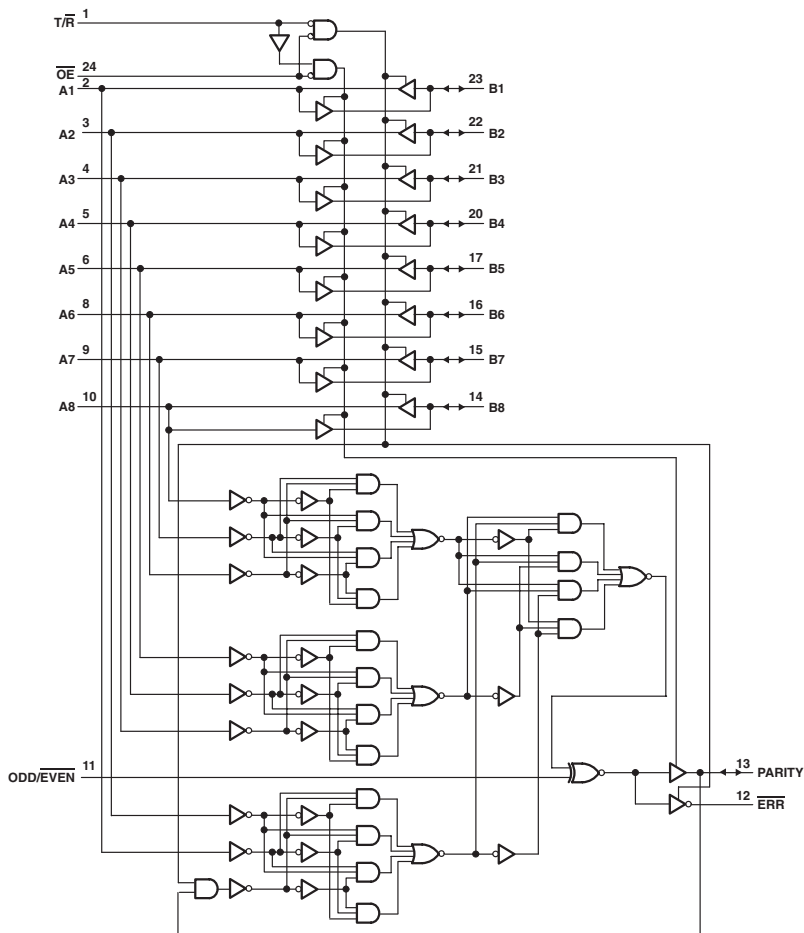
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS |
|------------------|-------------------|--------|------------|----|------|
| t _w | CLKBA, CLKAB "H" | | MIN | 15 | 14.5 |
| | CLKBA, CLKAB "L" | | MIN | 30 | 14.5 |
| | DATA | | MIN | 30 | - |
| t _{su} | A, B | | MIN | 15 | 10 |
| t _h | A, B | | MIN | 0 | 0 |
| t _{PLH} | CLKBA | A | MAX | 33 | 64 |
| t _{PHL} | | | | 36 | 22 |
| t _{PLH} | CLKAB | B | MAX | 21 | 30 |
| t _{PHL} | | | | 33 | 17 |
| t _{PLH} | A | B | MAX | 18 | 18 |
| t _{PHL} | | | | 30 | 15 |
| t _{PLH} | B | A | MAX | 27 | 56 |
| t _{PHL} | | | | 21 | 21 |
| t _{PLH} | SBA (B "H") | A | MAX | 48 | 62 |
| t _{PHL} | | | | 32 | 25 |
| t _{PLH} | SBA (B "L") | A | MAX | 54 | 62 |
| t _{PHL} | | | | 29 | 25 |
| t _{PLH} | SAB (A "H") | B | MAX | 35 | 25 |
| t _{PHL} | | | | 27 | 22 |
| t _{PLH} | SAB (A "L") | B | MAX | 45 | 35 |
| t _{PHL} | | | | 21 | 22 |
| t _{PLH} | \overline{OEBA} | A | MAX | 35 | 30 |
| t _{PHL} | | | | 53 | 24 |
| t _{PZH} | OEAB | B | MAX | 29 | 22 |
| t _{PZL} | | | | 33 | 22 |
| t _{PHZ} | OEAB | B | MAX | 39 | 14 |
| t _{PLZ} | | | | 29 | 16 |

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

- Combines SN74F245 and SN74F280B Functions in One Package
- 3-State Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | F | SN74 BCT | ABT | ACT 11 | UNIT |
|---------------------------------------|------------|-----|-------------|------|-----------|------|
| ICCH | MAX | 125 | 2 | 0.25 | 0.08 | mA |
| ICCL | MAX | 150 | 90 | 40 | 0.08 | mA |
| ICcz | MAX | 145 | 1 | 0.25 | 0.08 | mA |
| I _{OH} A1-A9 | MAX | -3 | -3 | -32 | -24 | mA |
| I _{OH} B1-B9, PARITY, ERR | MAX | -12 | -15 | -32 | -24 | mA |
| I _{OL} A1-A8 | MAX | 24 | 24 | 64 | 24 | mA |
| I _{OL} B1-B8, PARITY, ERR | MAX | 64 | 64 | 64 | 24 | mA |

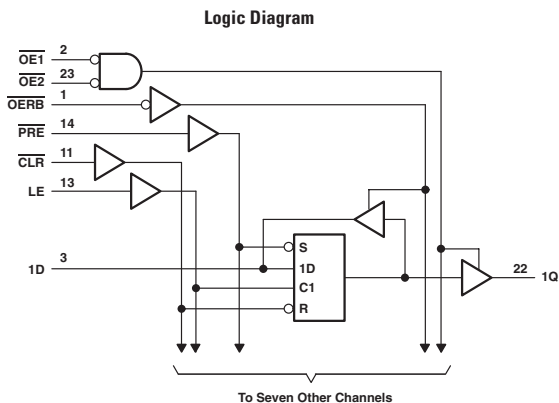
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | F | SN74 BCT | ABT | ACT 11 |
|-----------|-------------------------------|---------------------------------|------------|------|-------------|-----|-----------|
| t_{PLH} | A, B | B, A | MAX | 8 | 6.6 | 4.6 | 9.4 |
| t_{PHL} | | | MAX | 8 | 9 | 4.3 | 9.4 |
| t_{PLH} | A | PARITY | MAX | 16 | 15.4 | 8.1 | 14.4 |
| t_{PHL} | | | MAX | 16 | 15.9 | 7.7 | 15 |
| t_{PLH} | ODD/ $\overline{\text{EVEN}}$ | PARITY, $\overline{\text{ERR}}$ | MAX | 12 | 7.1 | 4.9 | 10.7 |
| t_{PHL} | | | MAX | 12.5 | 9 | 4.9 | 11.3 |
| t_{PLH} | B | $\overline{\text{ERR}}$ | MAX | 22.5 | 15.3 | 7.9 | 23.6 |
| t_{PHL} | | | MAX | 22.5 | 15.5 | 7.8 | 24.6 |
| t_{PLH} | PARITY | $\overline{\text{ERR}}$ | MAX | 16.5 | 13.2 | 7.7 | 14.6 |
| t_{PHL} | | | MAX | 17 | 13.9 | 7.5 | 14.7 |
| t_{PZH} | $\overline{\text{OE}}$ | A, B, PARITY | MAX | 9 | 9.1 | 6.5 | 12.1 |
| t_{PZL} | | | MAX | 11 | 16.3 | 6.5 | 13.8 |
| t_{PZH} | $\overline{\text{OE}}$ | $\overline{\text{ERR}}$ | MAX | 9 | 9.1 | 6.6 | 12.1 |
| t_{PZL} | | | MAX | 11 | 16.3 | 9.2 | 13.8 |
| t_{PHZ} | $\overline{\text{OE}}$ | A, B, PARITY, ERR | MAX | 8 | 9.1 | 6.2 | 12.1 |
| t_{PLZ} | | | MAX | 6.5 | 8 | 7.8 | 11.6 |

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Outputs
- Bus-Structured Pinout



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------|---|------------|------|------|
| I_{CC} | | MAX | 73 | mA |
| I_{OH} | Q | MAX | -2.6 | mA |
| | D | MAX | -0.4 | mA |
| I_{OL} | Q | MAX | 24 | mA |
| | D | MAX | 8 | mA |

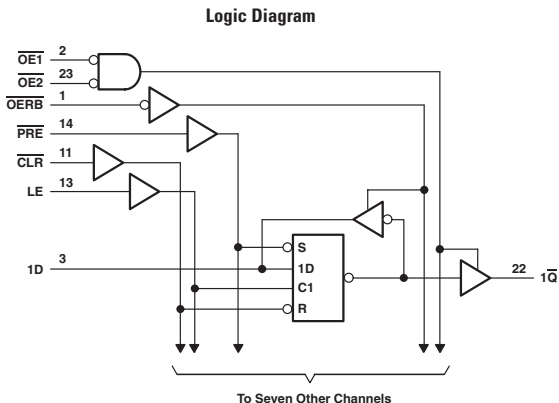
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|-----------|----------------------------------|--------|------------|-----|
| t_{LW} | LE "H" | | MIN | 10 |
| | \overline{CLR} "L" | | MIN | 10 |
| | \overline{PRE} "L" | | MIN | 10 |
| t_{SU} | DATA (LE) | | MIN | 10 |
| | DATA (\overline{OERB}) | | MIN | 10 |
| t_H | DATA (LE) | | MIN | 5 |
| t_{PLH} | D | Q | MAX | 14 |
| t_{PHL} | | | | 18 |
| t_{PLH} | LE | Q | MAX | 21 |
| t_{PHL} | | | | 27 |
| t_{PHL} | \overline{CLR} | Q | MAX | 29 |
| t_{PLH} | | | | 32 |
| t_{PHL} | \overline{PRE} | Q | MAX | 22 |
| t_{PLH} | | | | 28 |
| t_{en} | \overline{OERB} | D | MAX | 21 |
| t_{dis} | | | | 14 |
| t_{en} | $\overline{OE1}, \overline{OE2}$ | Q | MAX | 21 |
| t_{dis} | | | | 14 |

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- Inverted Outputs
- Bus-Structured Pinout



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------------|---|------------|------|------|
| I _{CC} | | MAX | 79 | mA |
| I _{OH} | Q | MAX | -2.6 | mA |
| | D | MAX | -0.4 | mA |
| I _{OL} | Q | MAX | 24 | mA |
| | D | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

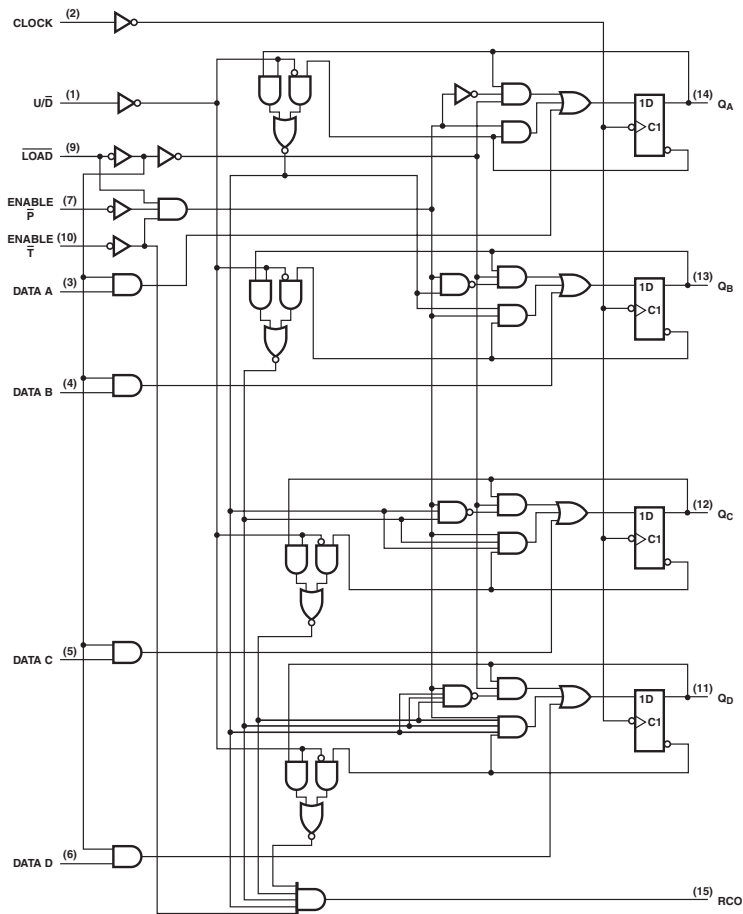
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-------------|-------|--------|------------|-----|
| t _{lv} | LE "H" | | | MIN | 10 |
| | CLR "L" | | | MIN | 10 |
| | PRE "L" | | | MIN | 10 |
| | DATA (LE) | | | MIN | 10 |
| t _{bu} | DATA (OERB) | | | MIN | 10 |
| | DATA (LE) | | | MIN | 5 |
| t _{PH} | | D | Q | MAX | 20 |
| t _{PHL} | | | | | 15 |
| t _{PLH} | | LE | Q | MAX | 28 |
| t _{PLH} | | | | | 22 |
| t _{PHL} | CLR | D | Q | MAX | 24 |
| | | | D | | 26 |
| t _{PLH} | PRE | D | Q | MAX | 25 |
| | | | D | | 28 |
| t _{en} | OERB | D | | MAX | 21 |
| t _{dis} | | | | | 14 |
| t _{en} | OE1, OE2 | | Q | MAX | 21 |
| t _{dis} | | | | | 14 |

UNIT: ns

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 34 | mA |
| I _{OH} | MAX | -0.4 | mA |
| I _{OL} | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

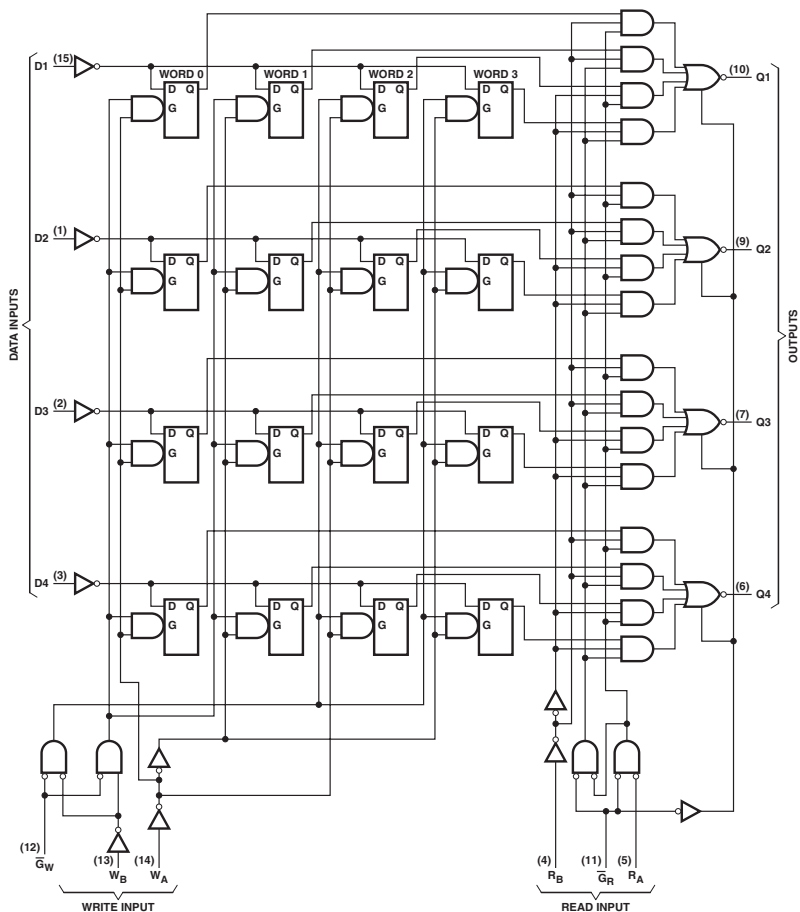
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|--|-------------------------|------------|----|
| f _{max} | | | MIN | 25 |
| t _w | | | MIN | 20 |
| t _{su} | A, B, C, D | | MIN | 25 |
| | $\overline{\text{ENP}}, \overline{\text{ENT}}$ | | MIN | 40 |
| | LOAD | | MIN | 30 |
| | U/ $\overline{\text{D}}$ | | MIN | 45 |
| t _h | | | MIN | 0 |
| t _{PLH} | CLOCK | $\overline{\text{RCO}}$ | MAX | 40 |
| t _{PHL} | | | | 60 |
| t _{PLH} | CLOCK | Q | MAX | 27 |
| t _{PHL} | | | | 27 |
| t _{PLH} | $\overline{\text{ENT}}$ | $\overline{\text{RCO}}$ | MAX | 17 |
| t _{PHL} | | | | 45 |
| t _{PLH} | U/ $\overline{\text{D}}$ | $\overline{\text{RCO}}$ | MAX | 35 |
| t _{PHL} | | | | 40 |

UNIT f_{max} : MHz other : ns

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

- Separate Read / Write Addressing Permits Simultaneous Reading and Writing
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- 3-State Outputs

Logic Diagram (SN74LS)



FUNCTION TABLE (SN74)

| WRITE INPUTS | | | WORD | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| W _B | W _A | W _V | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | Q ₀ | Q ₀ | Q ₀ |
| L | H | L | Q ₀ | Q = D | Q ₀ | Q ₀ |
| H | L | L | Q ₀ | Q ₀ | Q = D | Q ₀ |
| H | H | L | Q ₀ | Q ₀ | Q ₀ | Q = D |
| X | X | H | Q ₀ | Q ₀ | Q ₀ | Q ₀ |

| READ INPUTS | | | OUTPUTS | | | |
|----------------|----------------|----------------|---------|------|------|------|
| R _B | R _A | R _V | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | Z | Z | Z | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|---------|----------|------|
| I _{CC} | MAX | 50 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -2.6 | -6 | -6 | mA |
| I _{OL} | MAX | 8 | 6 | 6 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

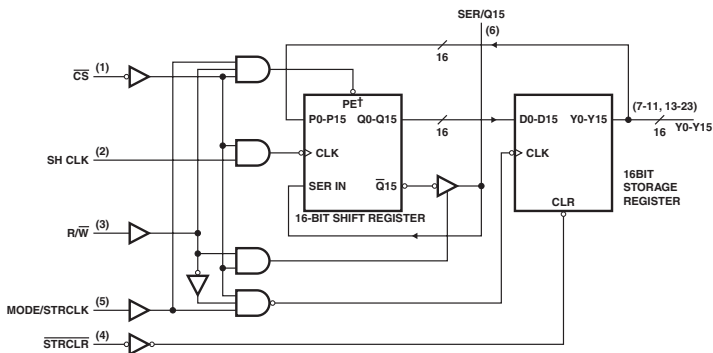
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | CD74 HC | CD74 HCT |
|--------------------|--|--------|------------|----|---------|----------|
| t _w | Width of write-enable or read-enable pulse | | MIN | 25 | 24 | 30 |
| t _{su} | Data input with respect to write enable | | MIN | 10 | 18 | 18 |
| | Write select with respect to write enable | | | 15 | 18 | 27 |
| t _h | Data input with respect to write enable | | MIN | 15 | 5 | 5 |
| | Write select with respect to write enable | | | 5 | 5 | 5 |
| t _{latch} | | | MIN | 25 | 30 | 38 |
| t _{PLH} | Read Select | Q | MAX | 40 | 59 | 53 |
| t _{PHL} | | | | 45 | 59 | 53 |
| t _{PLH} | Write Enable | Q | MAX | 45 | 75 | 75 |
| t _{PHL} | | | | 50 | 75 | 75 |
| t _{PLH} | Data | Q | MAX | 45 | 75 | 75 |
| t _{PHL} | | | | 40 | 75 | 75 |
| t _{PZH} | Read Enable | Q | MAX | 35 | 45 | 57 |
| t _{PZL} | | | | 40 | 45 | 57 |
| t _{PHZ} | Read Disable | Q | MAX | 50 | 45 | 53 |
| t _{PLZ} | | | | 35 | 45 | 53 |

UNIT : ns

16-BIT SHIFT REGISTERS

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

FUNCTION TABLE

| INPUTS | | | | | SER/ Q15 | SHIFT REGISTER FUNCTIONS | | | | STORAGE REGISTER FUNCTIONS | |
|--------|-----|--------|--------|-----------------|-------------|--------------------------|---------------------------|----------------------------|------------------|-------------------------------|------|
| CS | R/W | SH CLK | STRCLR | MODE/ STRCLK | | SHIFT | READ FROM SERIAL INPUT | WRITE INTO SERIAL INPUT | PARALLEL LOAD | CLEAR | LOAD |
| H | X | X | X | X | Z | NO | NO | NO | NO | | NO |
| X | X | X | L | X | | | | | | YES | |
| L | L | ↓ | X | X | Z | YES | NO | YES | NO | | |
| L | H | X | X | X | Q15 | | YES | NO | | | NO |
| L | H | ↓ | X | L | Q14n | YES | YES | NO | NO | | NO |
| L | H | ↓ | L | X | L | NO | YES | | YES | YES; | NO |
| L | H | ↓ | H | X | Y15n | NO | YES | | YES | NO | NO |
| L | L | X | H | ↑ | Z | | NO | | | NO | YES |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|---------|------------|------|------|
| I _{CC} | | MAX | 80 | mA |
| I _{OH} | SER/Q15 | MAX | -2.6 | mA |
| | Y0-Y15 | MAX | -0.4 | mA |
| I _{OL} | SER/Q15 | MAX | 24 | mA |
| | Y0-Y15 | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

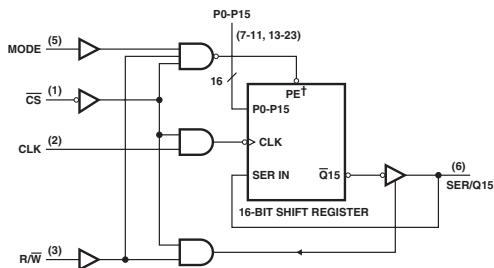
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|---------|-----------------|---------|------------|----|
| f _{max} | | | | MIN | 20 |
| t _v | CLK | | | MIN | 20 |
| | CLR | | | MIN | 20 |
| t _{su} | SER/Q15 | | | MIN | 20 |
| | Y0-Y15 | | | MIN | 20 |
| | Mode | | | MIN | 35 |
| | R/W/CS | | | MIN | 35 |
| t _h | SER/Q15 | | | MIN | 0 |
| | Y0-Y15 | | | MIN | 0 |
| | Mode | | | MIN | 0 |
| t _{PLH} | | STRCLR | Y0-Y15 | MAX | 40 |
| t _{PLH} | | MODE/ STRCLK | Y0-Y15 | MAX | 45 |
| t _{PHL} | | | | MAX | 45 |
| t _{PLH} | | SH CLK | SER/Q15 | MAX | 33 |
| t _{PHL} | | | | MAX | 40 |

 UNIT f_{max} : MHz other : ns

16-BIT SHIFT REGISTERS

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.

FUNCTION TABLE

| INPUTS | | | | SER/ Q15 | OPERATION |
|--------|-----|------|-----|-------------|----------------------------------|
| CS | R/W | MODE | CLK | | |
| H | X | X | X | Z | Do nothing |
| L | L | X | ↓ | Z | Shift and write (serial load) |
| L | H | L | ↓ | Q14n | Shift and read |
| L | H | H | ↓ | P15 | parallel load |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|---------|------------|------|------|
| I _{CC} | | MAX | 40 | mA |
| I _{OH} | SER/Q15 | MAX | -2.6 | mA |
| | P0-P15 | MAX | -0.4 | mA |
| I _{OL} | SER/Q15 | MAX | 24 | mA |
| | P0-P15 | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

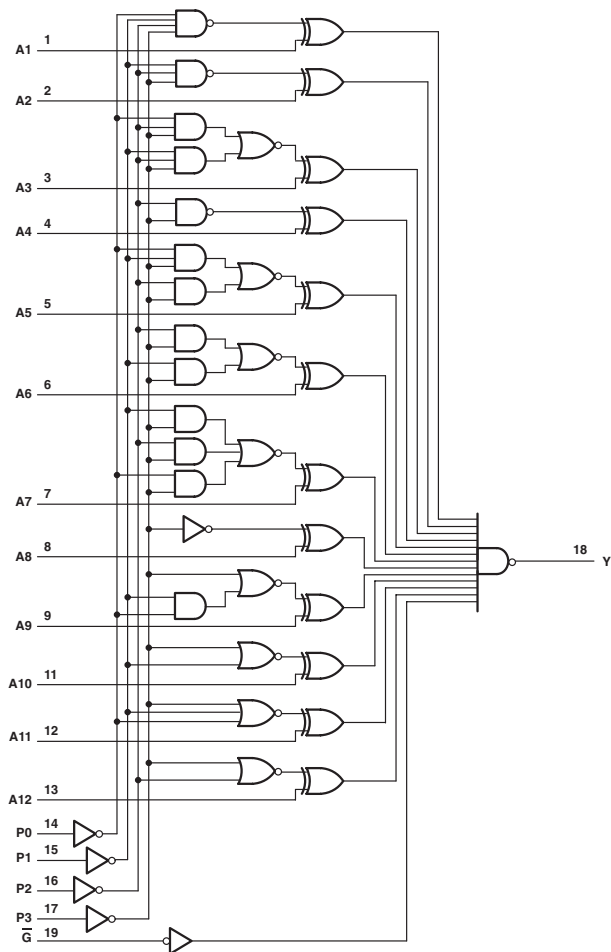
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|---------|---------|---------|------------|----|
| t _{max} | | | | MIN | 20 |
| t _w | CLK | | | MIN | 20 |
| | CLR | | | | 20 |
| t _{su} | SER/Q15 | | | MIN | 20 |
| | P0-P15 | | | | 20 |
| | Mode | | | | 35 |
| | R/W, CS | | | | 35 |
| t _h | SER/Q15 | | | MIN | 0 |
| | P0-P15 | | | | 0 |
| | Mode | | | | 0 |
| t _{PLH} | | CLK | SER/Q15 | MAX | 33 |
| t _{FHL} | | | | | 40 |
| t _{PZH} | | CS, R/W | SER/Q15 | MAX | 45 |
| t _{PZL} | | | | | 45 |
| t _{PHZ} | | CS, R/W | SER/Q15 | MAX | 40 |
| t _{PLZ} | | | | | 40 |

 UNIT f_{max} : MHz other : ns

12-BIT ADDRESS COMPARATOR

- 12-Bit Address Comparator with Enable

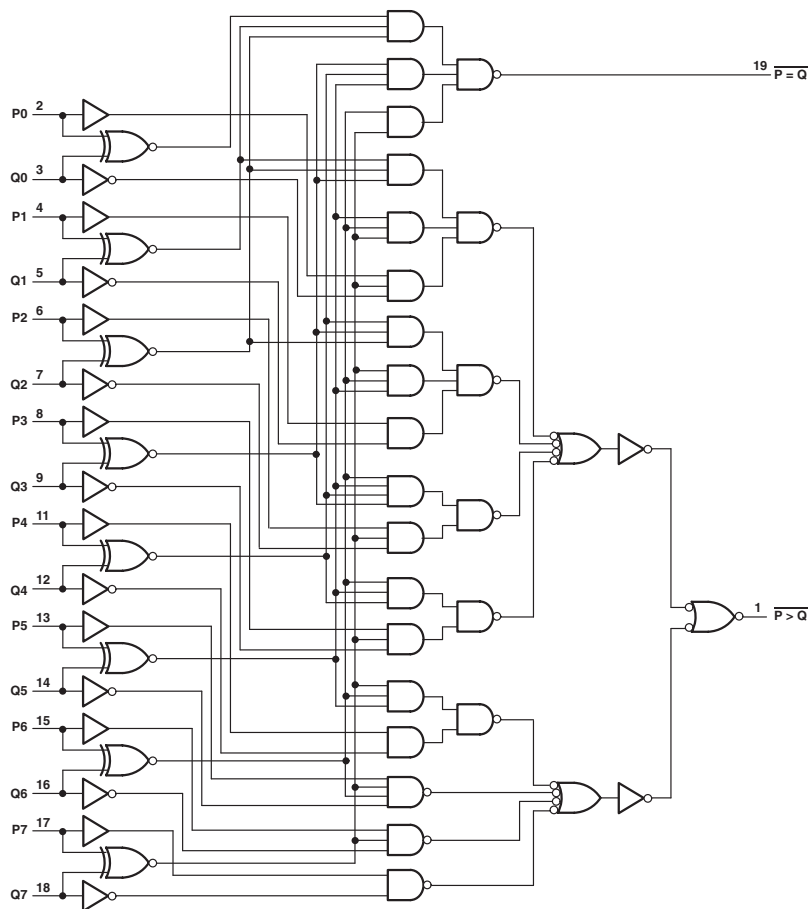
Logic Diagram



8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs
- 20k Ω Pullup Resistors on the Q Inputs

Logic Diagram



FUNCTION TABLE

| DATA INPUT P, Q | OUTPUTS | |
|-----------------------|------------------|------------------|
| | $\overline{P=Q}$ | $\overline{P>Q}$ |
| P=Q | L | H |
| P>Q | H | L |
| P<Q | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | SN74 HC | UNIT |
|-----------------|------------|------|------------|------|
| I _{CC} | MAX | 70 | 0.11 | mA |
| I _{OH} | MAX | -0.4 | -4 | mA |
| I _{OL} | MAX | 24 | 4 | mA |

SWITCHING CHARACTERISTICS

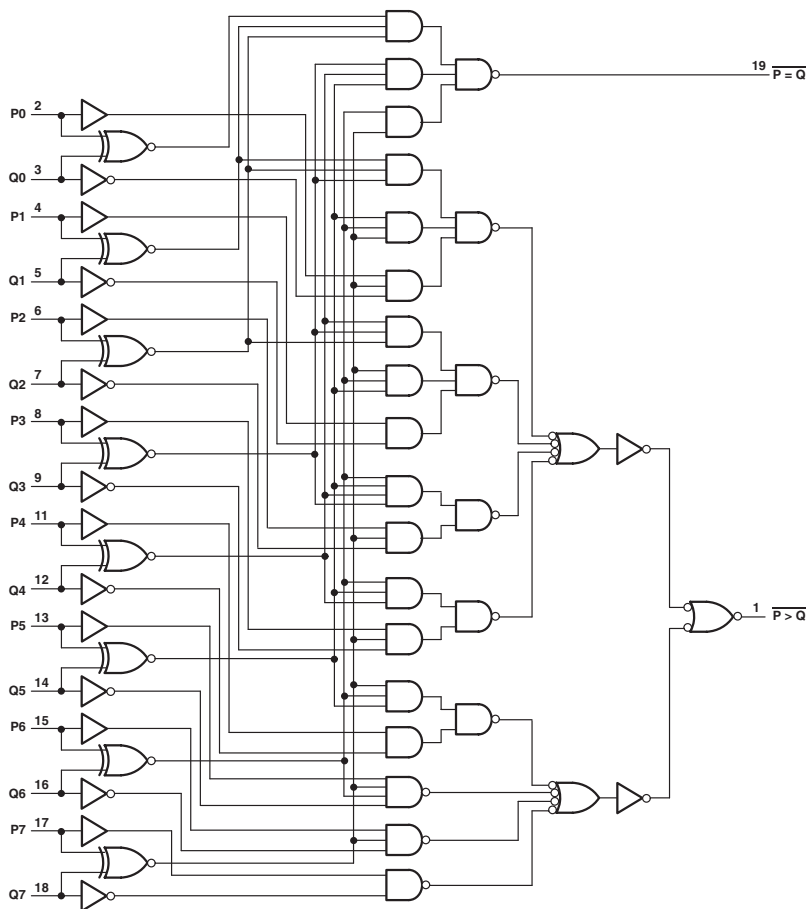
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC |
|------------------|-------|------------------|------------|----|------------|
| t _{PLH} | P | $\overline{P=Q}$ | MAX | 25 | 69 |
| | | | | 25 | 69 |
| t _{PHL} | Q | $\overline{P=Q}$ | MAX | 25 | 69 |
| | | | | 25 | 69 |
| t _{PLH} | P | $\overline{P>Q}$ | MAX | 30 | 69 |
| | | | | 30 | 69 |
| t _{PHL} | Q | $\overline{P>Q}$ | MAX | 30 | 69 |
| | | | | 30 | 69 |

UNIT: ns

8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

| DATA INPUT P, Q | OUTPUTS | |
|------------------------|------------------------|--------------------|
| | $\overline{P \cdot Q}$ | $\overline{P > Q}$ |
| $\overline{P \cdot Q}$ | L | H |
| $\overline{P > Q}$ | H | L |
| $\overline{P < Q}$ | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | SN74 HC | UNIT |
|-----------|------------|------|------------|------|
| I_{CC} | MAX | 65 | 0.08 | mA |
| I_{OH} | MAX | -0.4 | -4 | mA |
| I_{OL} | MAX | 24 | 4 | mA |

SWITCHING CHARACTERISTICS

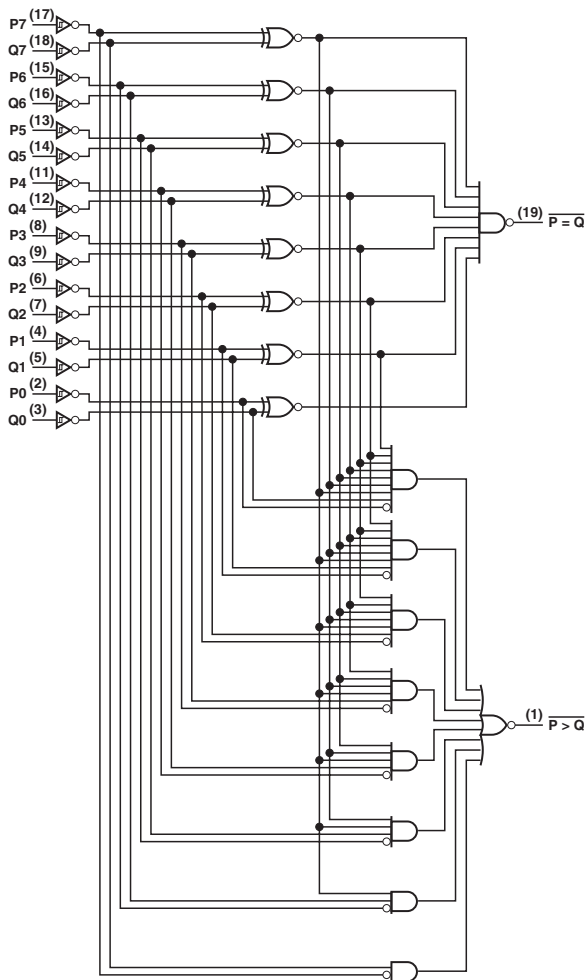
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | SN74 HC |
|-----------|-------|--------------------|------------|----|------------|
| t_{PLH} | P | $\overline{P = Q}$ | MAX | 25 | 69 |
| t_{PHL} | | | | 25 | 69 |
| t_{PLH} | Q | $\overline{P = Q}$ | MAX | 25 | 69 |
| t_{PHL} | | | | 25 | 69 |
| t_{PLH} | P | $\overline{P > Q}$ | MAX | 30 | 69 |
| t_{PHL} | | | | 30 | 69 |
| t_{PLH} | Q | $\overline{P > Q}$ | MAX | 30 | 69 |
| t_{PHL} | | | | 30 | 69 |

UNIT: ns

8-BIT MAGNITUDE/IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

| DATA | INPUTS | | OUTPUTS | |
|------|-----------------|-----------------|------------------|-------|
| | ENABLE | | $\overline{P-Q}$ | $P-Q$ |
| P, Q | $\overline{G1}$ | $\overline{G2}$ | | |
| P=Q | L | L | L | H |
| P>Q | L | L | H | L |
| P<Q | L | L | H | H |
| X | H | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 75 | mA |
| I _{OH} | MAX | -0.4 | mA |
| I _{OL} | MAX | 24 | mA |

SWITCHING CHARACTERISTICS

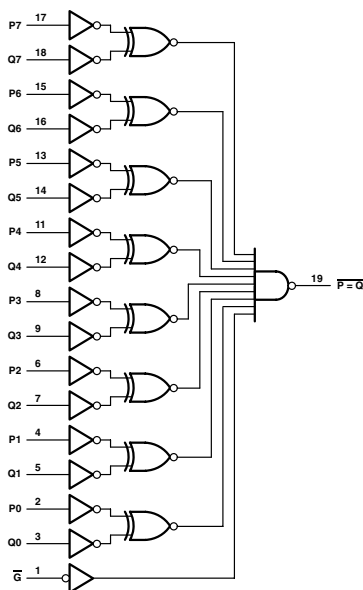
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS |
|------------------|-----------------|------------------|------------|----|
| t _{PLH} | P | $\overline{P=Q}$ | MAX | 25 |
| | | | | 30 |
| t _{PHL} | Q | $\overline{P=Q}$ | MAX | 25 |
| | | | | 30 |
| t _{PLH} | $\overline{G1}$ | $\overline{P=Q}$ | MAX | 20 |
| | | | | 30 |
| t _{PHL} | P | $\overline{P>Q}$ | MAX | 30 |
| | | | | 30 |
| t _{PLH} | Q | $\overline{P>Q}$ | MAX | 30 |
| | | | | 30 |
| t _{PHL} | $\overline{G2}$ | $\overline{P>Q}$ | MAX | 30 |
| | | | | 25 |

UNIT: ns

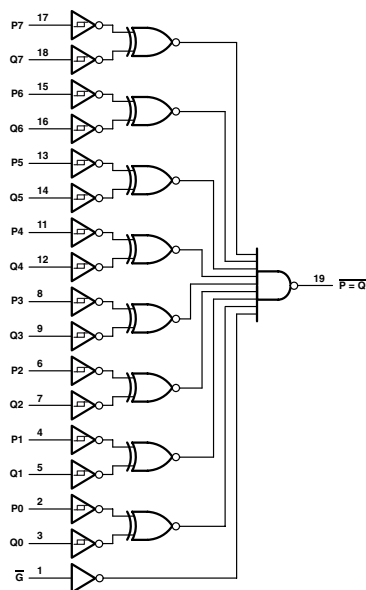
8-BIT IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram
(SN74ALS)



(SN74LS)



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|----------------|------------------|
| DATA | ENABLE | $\overline{P=Q}$ |
| P, Q | \overline{G} | |
| P=Q | L | L |
| P>Q | L | H |
| P<Q | L | H |
| X | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LS | ALS | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------|------|---------|---------|----------|------|
| I _{CC} | MAX | 65 | 19 | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -0.4 | -2.6 | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 24 | 24 | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

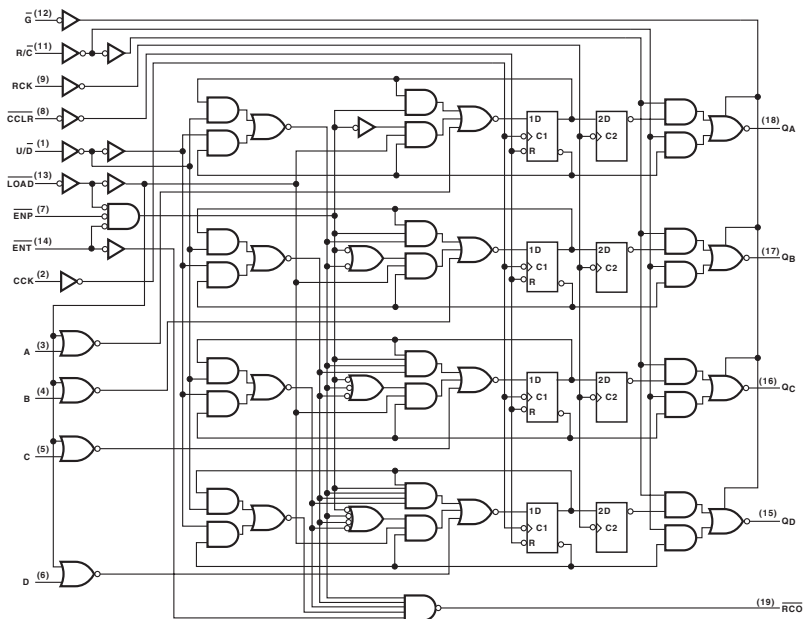
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LS | ALS | SN74 HC | CD74 HC | CD74 HCT |
|------------------|-----------------------------|-------------------------------|------------|----|-----|---------|---------|----------|
| t _{PLH} | P (CD74: A) | $\overline{P=Q}$ (CD74: Y) | MAX | 18 | 12 | 53 | 51 | 51 |
| | | | | 23 | 20 | 53 | 51 | 51 |
| t _{PLH} | Q (CD74: B) | $\overline{P=Q}$ (CD74: Y) | MAX | 18 | 12 | 53 | 51 | 51 |
| | | | | 23 | 20 | 53 | 51 | 51 |
| t _{PHL} | \overline{G} (CD74: E) | $\overline{P=Q}$ (CD74: Y) | MAX | 18 | 12 | 30 | 36 | 36 |
| | | | | 20 | 22 | 30 | 36 | 36 |

UNIT: ns

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Direct Clear

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|------------------|------------|------|------|
| I _{CC} | | MAX | 70 | mA |
| I _{OH} | Q | MAX | -2.6 | mA |
| | \overline{RCO} | | -0.4 | mA |
| I _{OL} | Q | MAX | 24 | mA |
| | \overline{RCO} | | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

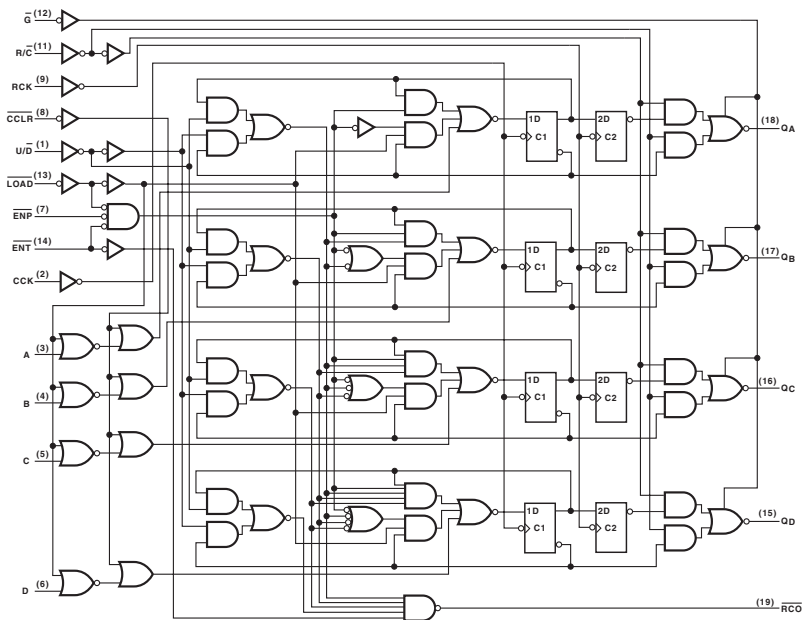
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | |
|------------------|-------------------------------------|-------|--------|------------------|-----|----|
| t _w | CCK | | | MIN | 25 | |
| | RCK | | | | 25 | |
| t _{su} | A thru D | | | MIN | 30 | |
| | \overline{ENT} , \overline{ENP} | | | | 30 | |
| | U/D | | | | 35 | |
| t _h | | | | MIN | 0 | |
| t _{PLH} | CCK ↑ | | | \overline{RCO} | MAX | 40 |
| t _{PHL} | | | | | | 40 |
| t _{PLH} | \overline{ENT} | | | \overline{RCO} | MAX | 20 |
| t _{PHL} | | | | | | 20 |
| t _{PLH} | CCK ↓ | Q | MAX | 20 | | |
| t _{PHL} | | | | 25 | | |
| t _{PLH} | RCK ↓ | Q | MAX | 20 | | |
| t _{PHL} | | | | 25 | | |
| t _{PHL} | \overline{CCLR} ↓ | Q | MAX | 40 | | |
| t _{PLH} | R / \overline{C} | Q | MAX | 25 | | |
| t _{PHL} | | | | 25 | | |

UNIT: ns

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Synchronous Clear

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | LS | UNIT |
|-----------------|------------------|------------|------|------|
| I _{CC} | | MAX | 70 | mA |
| I _{OH} | Q | MAX | -2.6 | mA |
| | \overline{RCO} | MAX | -0.4 | mA |
| I _{OL} | Q | MAX | 24 | mA |
| | \overline{RCO} | MAX | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

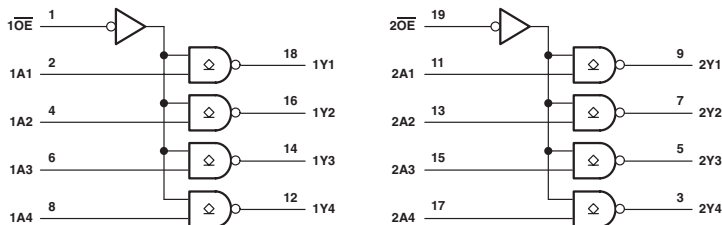
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | LS | |
|------------------|-------------------------------------|-------|--------|------------------|-----|----|
| t _{vr} | CCK | | | MIN | 25 | |
| | RCK | | | | 25 | |
| t _{su} | A thru D | | | MIN | 30 | |
| | \overline{ENT} , \overline{ENP} | | | | 30 | |
| | U/D | | | | 35 | |
| | CCLR | | | | 30 | |
| t _h | | | | MIN | 0 | |
| t _{PLH} | CCK ↑ | | | \overline{RCO} | MAX | 40 |
| t _{PHL} | | | | | | 40 |
| t _{PLH} | \overline{ENT} | | | \overline{RCO} | MAX | 20 |
| t _{PHL} | | 20 | | | | |
| t _{PLH} | CCK ↑ | Q | MAX | 20 | | |
| t _{PHL} | | | | 25 | | |
| t _{PLH} | RCK ↑ | Q | MAX | 20 | | |
| t _{PHL} | | | | 25 | | |
| t _{PLH} | R/ \overline{C} | Q | MAX | 25 | | |
| t _{PHL} | | | | 25 | | |

UNIT: ns

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS240A

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | SN74 BCT | UNIT |
|-----------|------------|-----|----------|------|
| I_{CC} | MAX | 80 | 86 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | V |
| I_{OL} | MAX | 64 | 64 | mA |

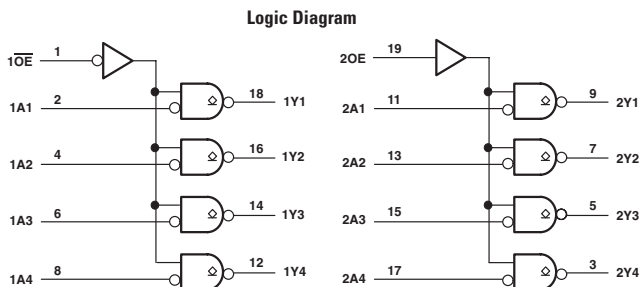
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS | SN74 BCT |
|-----------|-----------------|--------|------------|------|----------|
| t_{PLH} | A | Y | MAX | 19 | 11.3 |
| t_{PHL} | | | | 6 | 4.2 |
| t_{PLH} | \overline{OE} | Y | MAX | 19.5 | 16.5 |
| t_{PHL} | | | | 7.5 | 10.3 |

UNIT:ns

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS241



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | SN74 BCT | SN64 BCT | UNIT |
|-----------------|------------|-----|-------------|-------------|------|
| I _{CC} | MAX | 95 | 77 | 77 | mA |
| V _{OH} | MAX | 5.5 | 5.5 | 5.5 | V |
| I _{OL} | MAX | 64 | 64 | 64 | mA |

SWITCHING CHARACTERISTICS

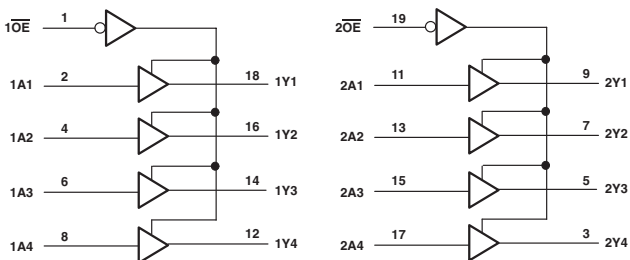
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS | SN74 BCT | SN64 BCT |
|------------------|-------|--------|------------|------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 18.5 | 10.1 | 10.1 |
| | | | | 6 | 6.6 | 6.6 |
| t _{PHL} | 10E | 1Y | MAX | 20 | 19.7 | 19.7 |
| | | | | 7 | 6.9 | 6.9 |
| t _{PLH} | 20E | 2Y | MAX | 21 | 18 | 18 |
| | | | | 7.5 | 8.5 | 8.5 |

UNIT:ns

OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS

- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74ALS244 and SN74AS244

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | SN74 BCT | UNIT |
|-----------|------------|-----|-----|----------|------|
| I_{CC} | MAX | 19 | 94 | 76 | mA |
| V_{OH} | MAX | 5.5 | 5.5 | 5.5 | V |
| I_{OL} | MAX | 24 | 64 | 64 | mA |

SWITCHING CHARACTERISTICS

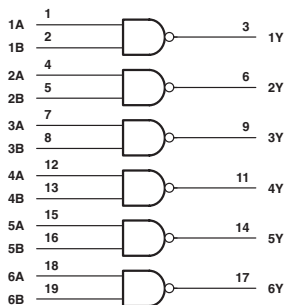
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 BCT |
|-----------|-----------------|--------|------------|-----|------|----------|
| t_{PLH} | A | Y | MAX | 15 | 18.5 | 10 |
| t_{PHL} | | | | 12 | 6 | 7.2 |
| t_{PLH} | \overline{OE} | Y | MAX | 16 | 18.5 | 17.5 |
| t_{PHL} | | | | 13 | 7 | 9.9 |

UNIT:ns

HEX 2-INPUT NAND DRIVERS

- $Y = \overline{A \cdot B}$
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | SN74 HC | UNIT |
|-----------|------------|-----|-----|---------|------|
| I_{CC} | MAX | 12 | 27 | 0.08 | mA |
| I_{OH} | MAX | -15 | -48 | -6 | mA |
| I_{OL} | MAX | 24 | 48 | 6 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 HC |
|-----------|-------|--------|------------|-----|----|---------|
| t_{PLH} | A, B | Y | MAX | 7 | 4 | 25 |
| t_{PHL} | | | MAX | 8 | 4 | 25 |

UNIT:ns

805

HEX 2-INPUT NOR DRIVERS

- $Y = \overline{A + B}$
- High Capacitive-Drive Capability

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION¹⁾

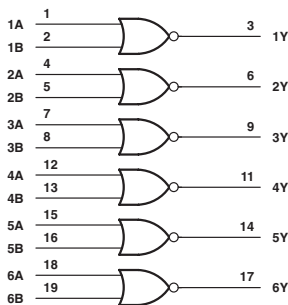
| PARAMETER | MAX or MIN | ALS | AS | SN74 HC | UNIT |
|-----------|------------|-----|-----|---------|------|
| I_{CC} | MAX | 14 | 32 | 0.08 | mA |
| I_{OH} | MAX | -15 | -48 | -6 | mA |
| I_{OL} | MAX | 24 | 48 | 6 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 HC |
|-----------|-------|--------|------------|-----|-----|---------|
| t_{PLH} | A, B | Y | MAX | 7 | 4.3 | 24 |
| t_{PHL} | | | MAX | 8 | 4.3 | 24 |

UNIT:ns

Logic Diagram



808

HEX 2-INPUT AND DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION¹⁾

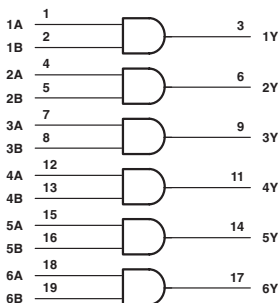
| PARAMETER | MAX or MIN | AS | SN74 HC | UNIT |
|-----------|------------|-----|---------|------|
| I_{CC} | MAX | 33 | 0.08 | mA |
| I_{OH} | MAX | -48 | -6 | mA |
| I_{OL} | MAX | 48 | 6 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS | SN74 HC |
|-----------|-------|--------|------------|----|---------|
| t_{PLH} | A, B | Y | MAX | 6 | 25 |
| t_{PHL} | | | MAX | 6 | 25 |

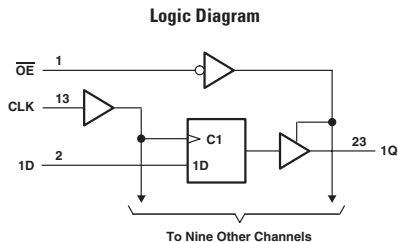
UNIT:ns

Logic Diagram



10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS

- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | ABT | LVC 3V | UNIT |
|-----------------|------------|-----|-----|--------|------|
| I _{CC} | MAX | 113 | 38 | 0.01 | mA |
| I _{OH} | MAX | -24 | -32 | -24 | mA |
| I _{OL} | MAX | 48 | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

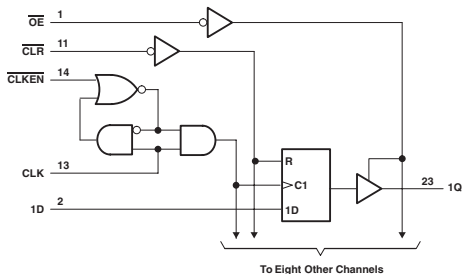
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS | ABT | LVC 3V |
|------------------|-------|--------|------------|-----|-----|--------|
| t _w | High | | MIN | 8 | 2.9 | 3.3 |
| | Low | | MIN | 8 | 3.8 | 3.3 |
| t _{su} | | | MIN | 6 | 2.1 | 1.9 |
| | | | MIN | 0 | 1.3 | 1.5 |
| t _{PLH} | CLK | Q | MAX | 7.5 | 6.2 | 7.3 |
| t _{PHL} | | | | 13 | 6.7 | 7.3 |
| t _{PZH} | OE | Q | MAX | 11 | 5.8 | 7.6 |
| t _{PZL} | | | | 12 | 6.3 | 7.6 |
| t _{PHZ} | OE | Q | MAX | 8 | 6.7 | 6.2 |
| t _{PLZ} | | | | 8 | 6.5 | 6.2 |

UNIT: ns

9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Functionally Equivalent to AMD's AM29823 and AM29824
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|--------|-----|-------|-----|---|----------------|
| OE | CLR | CLKEN | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | Q ₀ |
| H | X | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | ABT | LVC 3V | UNIT |
|-----------------|------------|-----|-----|--------|------|
| I _{CC} | MAX | 103 | 38 | 0.01 | mA |
| I _{OH} | MAX | -24 | -32 | -24 | mA |
| I _{OL} | MAX | 48 | 64 | 24 | mA |

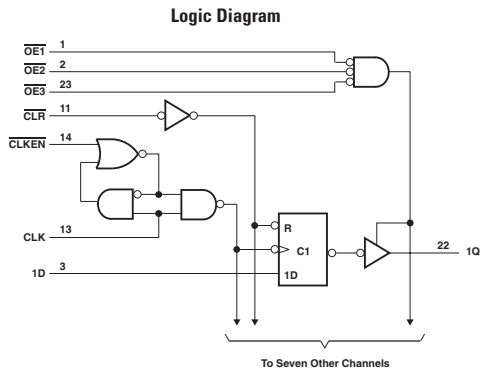
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | AS | ABT | LVC 3V |
|------------------|--------------|-------|--------|------------|------|-----|--------|
| t _w | CLR "L" | | | MIN | 6.5 | 5.5 | 3.3 |
| | CLK "H" | | | | 8 | 2.9 | 3.3 |
| | CLK "L" | | | | 8 | 3.8 | 3.3 |
| t _{su} | CLR inactive | | | MIN | 8 | 2.5 | 1 |
| | DATA | | | | 6 | 2.1 | 1.3 |
| | CLKEN "H" | | | | 7.5 | 2 | - |
| | CLKEN "L" | | | | 7.5 | 3.3 | 1.8 |
| | DATA | | | | - | 1.3 | 2 |
| t _h | DATA | | | MIN | - | 1 | - |
| | CLKEN "H" | | | | 0 | 2 | 1.3 |
| | CLKEN "L" | | | | | | |
| t _{PLH} | | CLK | Q | MAX | 7.5 | 6.8 | 8 |
| t _{PHL} | | CLK | Q | MAX | 13 | 6.7 | 8 |
| t _{PHL} | | CLR | Q | MAX | 15.5 | 7.1 | 7.9 |
| t _{PZH} | | OE | Q | MAX | 11 | 6 | 7.2 |
| t _{PZL} | | OE | Q | MAX | 12 | 6.5 | 7.2 |
| t _{PHZ} | | OE | Q | MAX | 8 | 7.5 | 6 |
| t _{PLZ} | | OE | Q | MAX | 8 | 6.9 | 6 |

UNIT: ns

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Improved I_{OH} Specifications (Max: -24mA)
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|--------|-----|-------|-----|---|----------------|
| OE | CLR | CLKEN | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | Q ₀ |
| H | X | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 95 | mA |
| I_{OH} | MAX | -24 | mA |
| I_{OL} | MAX | 48 | mA |

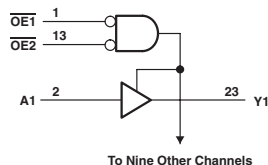
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | AS |
|-----------|-----------------------------|-------|--------|------------|------|
| t_w | $\overline{\text{CLR}}$ "L" | | | MIN | 4 |
| | CLK "H" | | | | 8 |
| | CLK "L" | | | | 8 |
| t_{su} | CLR | | | MIN | 8 |
| | DATA | | | | 6 |
| | CLKEN | | | | 6 |
| t_h | | | | MIN | 0 |
| t_{PLH} | | CLK | Q | MAX | 7.5 |
| t_{PHL} | | CLK | Q | MAX | 13 |
| t_{PHL} | | CLR | Q | MAX | 15.5 |
| t_{PZH} | | OE | Q | MAX | 11 |
| t_{PZL} | | OE | Q | MAX | 12 |
| t_{PHZ} | | OE | Q | MAX | 8 |
| t_{PLZ} | | OE | Q | | 8 |

UNIT: ns

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | H | H |
| L | L | L | L |
| X | H | X | Z |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | AC 11 | ACT 11 | LVC 3V | UNIT |
|-----------------|------------|-----|-------|--------|--------|------|
| I _{CC} | MAX | 40 | 0.08 | 0.08 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 24 | 24 | mA |

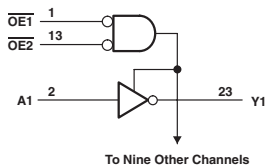
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | AC 11 | ACT 11 | LVC 3V | |
|------------------|-------|--------|------------|-----|-------|--------|--------|-----|
| t _{PLH} | A | Y | MAX | 4.8 | 8.7 | 9.2 | 6.7 | |
| t _{PHL} | | | | 4.7 | 9.7 | 11.2 | 6.7 | |
| t _{PZH} | OE | | MAX | 5.9 | 9.7 | 11.3 | 7.3 | |
| t _{PZL} | | | | 6.9 | 13 | 14 | 7.3 | |
| t _{PHZ} | OE | | MAX | MAX | 6.8 | 9.1 | 12 | 6.7 |
| t _{PLZ} | | | | | 6.9 | 8.8 | 11.6 | 6.7 |

UNIT: ns

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | H | L |
| L | L | L | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AC 11 | ACT 11 | LVC 3V | UNIT |
|-----------------|------------|-------|--------|--------|------|
| I _{CC} | MAX | 0.08 | 0.08 | 0.01 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC 11 | ACT 11 | LVC 3V | |
|------------------|-------|--------|------------|-------|--------|--------|-----|
| t _{PLH} | A | Y | MAX | 9.5 | 10.2 | 6.7 | |
| t _{PHL} | | | | 10.4 | 11.7 | 6.7 | |
| t _{PZH} | OE | | MAX | 10.7 | 12.1 | 7.3 | |
| t _{PZL} | | | | 13.2 | 14.7 | 7.3 | |
| t _{PHZ} | OE | | MAX | MAX | 9.6 | 12.3 | 6.7 |
| t _{PLZ} | | | | | 9.2 | 11.7 | 6.7 |

UNIT: ns

HEX 2-INPUT OR DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

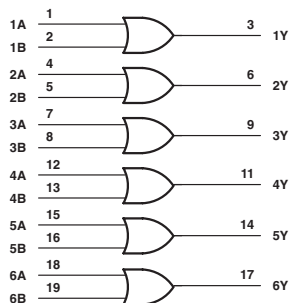
| PARAMETER | MAX or MIN | ALS | AS | SN74 HC | UNIT |
|-----------|------------|-----|-----|---------|------|
| I_{CC} | MAX | 16 | 36 | 0.08 | mA |
| I_{OH} | MAX | -15 | -48 | -6 | mA |
| I_{OL} | MAX | 24 | 48 | 6 | mA |

SWITCHING CHARACTERISTICS

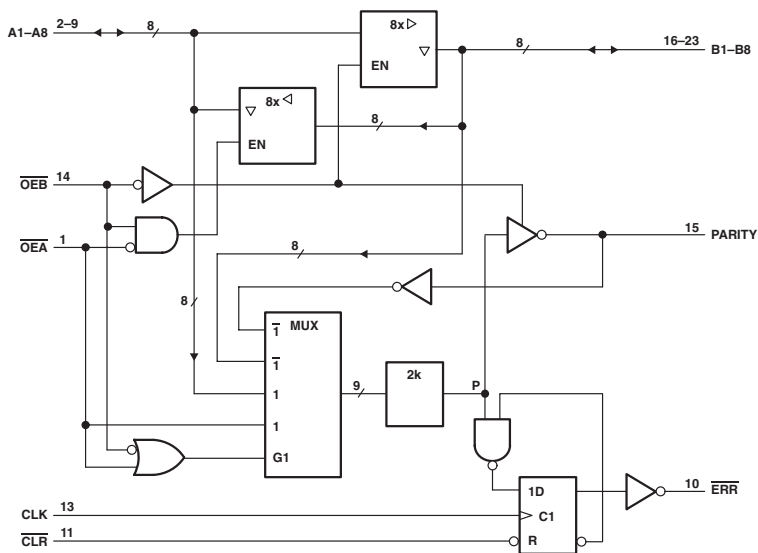
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | SN74 HC |
|-----------|-------|--------|------------|-----|-----|---------|
| t_{PLH} | A, B | Y | MAX | 9 | 6.3 | 25 |
| t_{PHL} | | | MAX | 8 | 6.3 | 25 |

UNIT:ns

Logic Diagram



Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS AND I/O | | | | FUNCTION |
|--------|-----|-----|----------------------------|-------------------------------|-------------------------------|-----------------|----|--------|-------------------|---|
| OEB | OEA | CLR | CLK | Ai Σ OF H's Odd Even | Bi Σ OF H's Odd Even | A | B | PARITY | ERR | |
| L | H | X | X | Odd Even | NA | NA | A | L H | NA | A data to B bus and generate parity |
| H | L | H | ↑ | NA | Odd Even | B | NA | NA | H L | B data to A bus and check parity |
| X | X | L | X | X | X | X | NA | NA | H | Check error flag register |
| H | H | H | No↑ L No↑ H ↑ H ↑ | X X ↑ Odd Even | X | Z | Z | Z | NC H H L | Isolation |
| L | L | X | X | Odd Even | NA | NA | A | H L | NA | A data to B bus and generate inverted parity |

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRE-STATE | OUTPUT ERR | FUNCTION |
|--------|-----|-----------------------|----------------------|---------------|----------|
| CLR | CLK | POINT P | ERR _{n-1} † | ERR | |
| H | ↑ | H | H | H | Sample |
| H | ↑ | X | L | H | |
| H | ↑ | L | X | L | |
| L | X | X | X | H | Clear |

† The state of ERR before any changes at CLR, CLK, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 38 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

SWITCHING CHARACTERISTICS

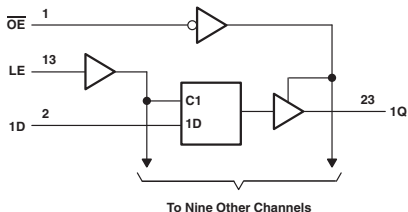
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|--------|----------------|------------|------|
| t _{PLH} | A or B | B or A | MAX | 5.3 |
| | | | | 5.3 |
| t _{PLH} | A | PARITY | MAX | 11.2 |
| | | | | 11 |
| t _{PZH} | OE | PARITY | MAX | 10.5 |
| | | | | 10 |
| t _{PLH} | CLR | ERR | MAX | 5.2 |
| | | | | 6.2 |
| t _{PZH} | OE | A,B, or PARITY | MAX | 6.5 |
| | | | | 6.5 |
| t _{PHZ} | OE | A,B, or PARITY | MAX | 7.9 |
| | | | | 8.1 |

UNIT: ns

10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | L |
| L | H | L | H |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | ABT | LVC 3V | UNIT |
|------------------|------------|------|-----|-----|--------|------|
| I _{CC} | MAX | 62 | 94 | 38 | 0.01 | mA |
| I _{OIH} | MAX | -2.6 | -24 | -32 | -24 | mA |
| I _{OL} | MAX | 24 | 48 | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS | ABT | LVC 3V |
|------------------|-------|--------|------------|-----|------|-----|--------|
| t _w | | | MIN | 20 | 4 | 3.3 | 3.3 |
| t _{su} | High | | | 10 | 2.5 | 2.5 | 2.1 |
| t _{su} | Low | | | 10 | 2.5 | 1.5 | 2.1 |
| t _h | | | | 5 | 2.5 | 1.5 | 1 |
| t _{PLH} | D | Q | MAX | 13 | 6.5 | 6.2 | 6.7 |
| t _{PHL} | | | | 13 | 10.5 | 6.2 | 6.7 |
| t _{PLH} | LE | Q | MAX | 21 | 12 | 6.5 | 7.6 |
| t _{PHL} | | | | 26 | 12 | 6.7 | 7.6 |
| t _{PZH} | OE | Q | MAX | 12 | 14 | 5.3 | 7.2 |
| t _{PZL} | | | | 12 | 16 | 6.3 | 7.2 |
| t _{PHZ} | OE | Q | MAX | 10 | 8 | 7.1 | 5.9 |
| t _{PLZ} | | | | 12 | 8 | 6.5 | 5.9 |

UNIT: ns

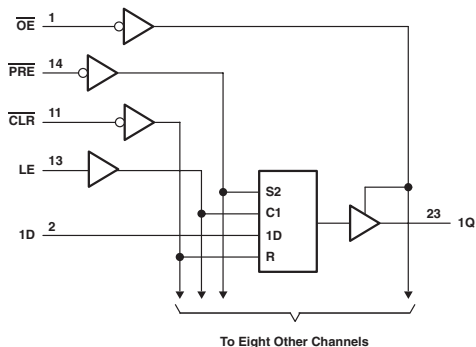
9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

FUNCTION TABLE

| | | INPUTS | | | | OUTPUT |
|-----|-----|--------|----|---|----------------|--------|
| PRE | CLR | OE | LE | D | H | |
| L | H | L | X | X | H | |
| H | L | L | X | X | L | |
| L | L | L | X | X | H | |
| H | H | L | H | L | L | |
| H | H | L | H | H | H | |
| H | H | L | L | X | Q ₀ | |
| X | X | H | X | X | Z | |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | ABT | UNIT |
|-----------------|------------|------|-----|-----|------|
| I _{CC} | MAX | 67 | 92 | 34 | mA |
| I _{OH} | MAX | -2.6 | -24 | -32 | mA |
| I _{OL} | MAX | 24 | 48 | 64 | mA |

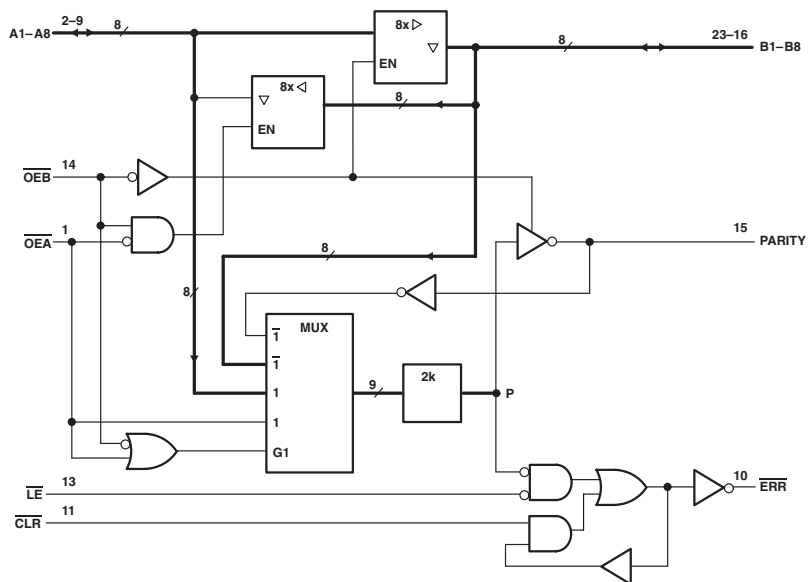
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS | AS | ABT |
|------------------|--------------|-------|--------|------------|------|-----|-----|
| t _w | CLR "L" | D | Q | MIN | 35 | 4 | 5.5 |
| | PRE "L" | | | | 35 | 4 | 4.5 |
| | LE "H" | | | | 20 | 4 | - |
| | LE "L" | | | | - | 4 | 3.4 |
| t _{su} | LE "L" | | | MIN | 10 | 2.5 | 2.5 |
| | LE "H" | | | | 10 | 2.5 | 3 |
| | PRE inactive | | | | - | 15 | 1.6 |
| | CLR inactive | | | | - | 14 | 2 |
| t _h | LE "L" | MIN | 5 | 2.5 | 1 | | |
| | LE "H" | | 5 | 2.5 | 1.5 | | |
| t _{PLH} | D | Q | MAX | 13 | 6.5 | 6.7 | |
| t _{PHL} | | | | 18 | 9 | 7.2 | |
| t _{PLH} | LE | Q | MAX | 21 | 12 | 7.2 | |
| t _{PHL} | | | | 26 | 12 | 6.9 | |
| t _{PLH} | CLR | Q | MAX | - | - | 7.1 | |
| t _{PHL} | | | | 23 | 13 | 8 | |
| t _{PLH} | PRE | Q | MAX | 22 | 10 | 7.4 | |
| t _{PHL} | | | | - | - | 7.2 | |
| t _{PZH} | OE | Q | MAX | 12 | 10.5 | 5.7 | |
| t _{PZL} | OE | Q | MAX | 14 | 13.5 | 6.5 | |
| t _{PHZ} | OE | Q | MAX | 10 | 8 | 6.8 | |
| t _{PLZ} | | | | 12 | 8 | 5.9 | |

UNIT: ns

8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | OUTPUT AND I/Os | | | | FUNCTION |
|--------|-----|-----|----|--------------------------|---------------|-----------------|----|--------|-------------------|---|
| OEB | OEA | CLR | LE | A ₁ Σ OF H | Bit Σ OF H | A | B | PARITY | ERR [‡] | |
| L | H | X | X | Odd Even | NA | NA | A | L H | NA | A data to B bus and generate parity |
| H | L | H | L | NA | Odd Even | B | NA | NA | H L | B data to A bus and check parity |
| H | L | H | H | X | X | X | NA | NA | NC | Store error flag |
| X | X | L | H | X | X | X | NA | NA | H | Clear error flag register |
| H | H | H | H | X | X | Z | Z | Z | NC H H L | Isolation [§] (parity check) |
| L | L | X | X | Odd Even | NA | NA | A | H L | NA | A data to B bus and generate inverted parity |

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRE-STATE | OUTPUT ERR | FUNCTION |
|--------|----|-----------------------|---------------------------------|---------------|----------|
| CLR | LE | POINT P | ERR _{n-1} [†] | | |
| L | L | L H | X | L H | Pass |
| H | L | L X H | X L H | L L H | Sample |
| L | H | X | X | H | Clear |
| H | H | X | L H | L H | Store |

† The state of ERR before changes at CLR, LE, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 38 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

SWITCHING CHARACTERISTICS

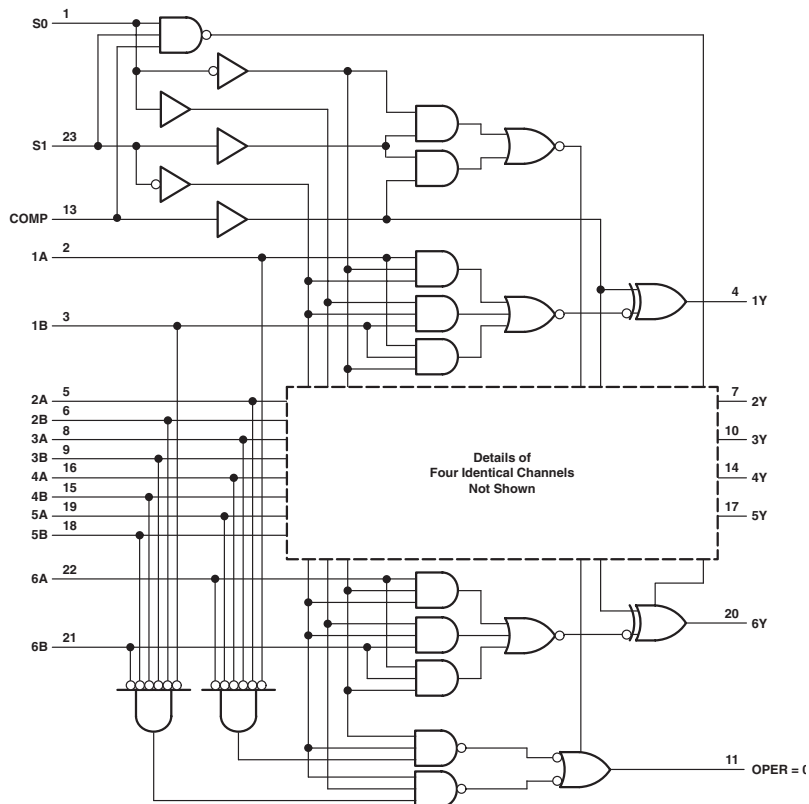
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|------------------|---------------------|------------|------|
| t _{PLH} | A or B | B or A | MAX | 5.3 |
| t _{PHL} | | | | 5.3 |
| t _{PLH} | A | PARITY | MAX | 11.2 |
| t _{PHL} | | | | 11 |
| t _{PLH} | \overline{OE} | PARITY | MAX | 10.5 |
| t _{PHL} | | | | 10 |
| t _{PLH} | \overline{CLR} | ERR | MAX | 6.2 |
| t _{PHL} | | | | 6 |
| t _{PLH} | \overline{LE} | ERR | MAX | 6 |
| t _{PHL} | | | | 6.6 |
| t _{PLH} | B or PARITY | ERR | MAX | 11.7 |
| t _{PHL} | | | | 12.8 |
| t _{PZH} | \overline{OE} | A or B or PARITY | MAX | 6.7 |
| t _{PZL} | | | | 6.7 |
| t _{PHZ} | \overline{OE} | A or B or PARITY | MAX | 7.9 |
| t _{PLZ} | | | | 8.1 |

UNIT: ns

HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------|----|----|---------|--------------------|
| COMP | S1 | S0 | Y | OPER = 0 |
| L | L | L | A | H = all A inputs L |
| L | L | H | B | H = all B inputs L |
| L | H | L | A+B | Z |
| L | H | H | L | L |
| H | L | L | A | H = all A inputs L |
| H | L | H | B | H = all B inputs L |
| H | H | L | A+B | Z |
| H | H | H | Z | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

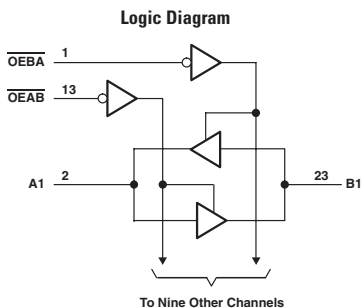
| PARAMETER | | MAX or MIN | ALS | AS | UNIT |
|-----------------|----------|------------|------|-----|------|
| IccZ | | MAX | 36 | 135 | mA |
| IcCL | | MAX | 33 | 175 | mA |
| I _{OH} | Y | MAX | -2.6 | -15 | mA |
| | OPER = 0 | MAX | -2.6 | -2 | mA |
| I _{OL} | Y | MAX | 24 | 48 | mA |
| | OPER = 0 | MAX | 24 | 20 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|------------------------|--------------------|------------|-----|----|
| t _{pd} | A or B (COMP = "H") | Y inverting | MAX | 14 | 12 |
| t _{pd} | A or B (COMP = "L") | Y non-inverting | MAX | 14 | 10 |
| t _{pd} | S0 or S1 | Y | MAX | 33 | 13 |
| t _{pd} | COMP | Y | | 18 | 13 |
| t _{pd} | A or B | OPER = 0 | | 37 | 14 |
| t _{pd} | S0 to S1 | OPER = 0 | | 23 | 18 |
| t _{en} | S0 to S1 | Y | | 35 | 12 |
| t _{dis} | COMP | Y | MAX | 23 | 11 |
| t _{en} | | | | 24 | 12 |
| t _{dis} | | | | 21 | 9 |
| t _{en} | S0 | OPER = 0 | MAX | 20 | 12 |
| t _{dis} | | | | 27 | 9 |
| t _{en} | S1 | OPER = 0 | MAX | 25 | 12 |
| t _{dis} | | | | 19 | 9 |
| t _{en} | COMP | OPER = 0 | MAX | 25 | 13 |
| t _{dis} | | | | 20 | 9 |

UNIT: ns

10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|------|-----------------------|
| OEAB | OEBA | |
| L | H | A data to B bus |
| H | L | B data to A bus |
| H | H | Isolation |
| L | L | Latch A and B (A = B) |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVC 3V | UNIT |
|-----------|------------|-----|--------|------|
| I_{CC} | MAX | 38 | 0.01 | mA |
| I_{DH} | MAX | -32 | -24 | mA |
| I_{OL} | MAX | 64 | 24 | mA |

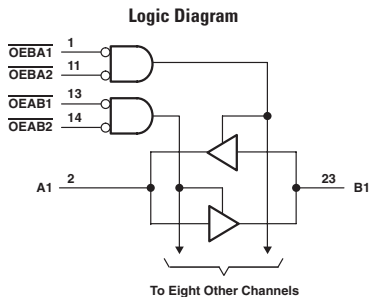
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVC 3V |
|-----------|--|--------|------------|-----|--------|
| t_{PLH} | A or B | B or A | MAX | 5.2 | 6.4 |
| t_{PHL} | | | | 4.9 | 6.4 |
| t_{PZH} | \overline{OEAB} or \overline{OEBA} | B or A | MAX | 5.9 | 7 |
| t_{PZL} | | | | 6.9 | 7 |
| t_{PHZ} | \overline{OEAB} or \overline{OEBA} | B or A | MAX | 7.5 | 5.9 |
| t_{PLZ} | | | | 7.1 | 5.9 |

UNIT: ns

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

● 3-State Outputs



FUNCTION TABLE

| INPUTS | | | | OPERATION |
|--------|-------|-------|-------|---------------|
| OEAB1 | OEAB2 | OEBA1 | OEBA2 | |
| L | L | L | L | Latch A and B |
| L | L | H | X | A to B |
| L | L | X | H | A to B |
| H | X | L | L | B to A |
| X | H | L | L | B to A |
| H | X | H | X | Isolation |
| H | X | X | H | |
| X | H | X | H | |
| X | H | H | X | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVC 3V | UNIT |
|-----------------|------------|-----|-----------|------|
| I _{CC} | MAX | 38 | 0.01 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

SWITCHING CHARACTERISTICS

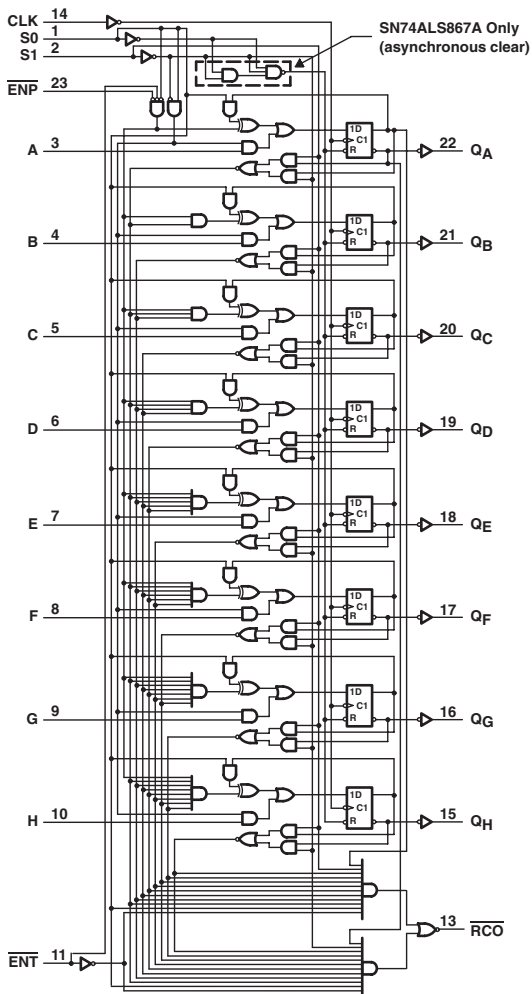
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVC 3V |
|------------------|--------|--------|------------|-----|-----------|
| t _{PLH} | A or B | B or A | MAX | 5.7 | 6.1 |
| | | | | 3.9 | 6.1 |
| t _{PZH} | OE | A or B | MAX | 5.5 | 7.2 |
| t _{PZL} | | | | 5.4 | 7.2 |
| t _{PHZ} | OE | A or B | MAX | 6.7 | 6.3 |
| | | | | 6.9 | 6.3 |

UNIT: ns

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Asynchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



FUNCTION TABLE

| S1 | S0 | FUNCTION |
|----|----|------------|
| L | L | Clear |
| L | H | Count down |
| H | L | Load |
| H | H | Count up |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 45 | 195 | mA |
| I _{OH} | MAX | -0.4 | -2 | mA |
| I _{OL} | MAX | 8 | 20 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

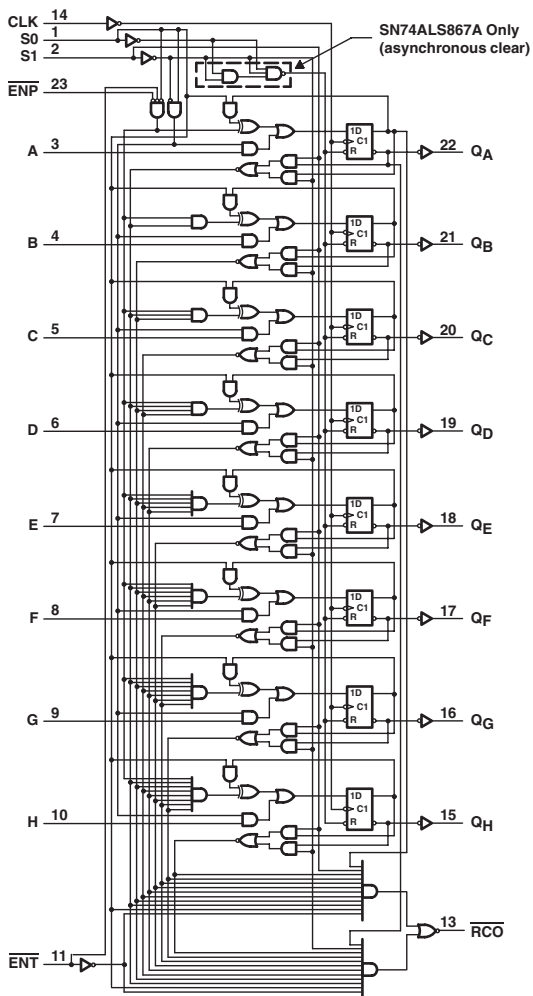
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|--|------------------|------------|-----|----|
| f _{max} | | | MIN | 35 | 50 |
| t _w | CLK (clock) | | MIN | 14 | 10 |
| | S0 and S1 (clear) | | | 10 | 10 |
| t _{su} | Data input A-H | | MIN | 10 | 4 |
| | \overline{ENP} or \overline{ENT} | | | 15 | 8 |
| | S0 low and S1 high (load) | | | 12 | 10 |
| | S0 and S1 low (clear) | | | - | 10 |
| | S0 high and S1 low (count down) | | | 12 | 40 |
| | S0 and S1 high (count up) | | | 12 | 40 |
| t _h | S0 high after S1 ↑ or S1 high after S0 ↑ | | MIN | 3 | - |
| | Data input A-H | | | 0 | 0 |
| t _{PLH} | CLK | \overline{RCO} | MAX | 14 | 22 |
| t _{PHL} | | | | 16 | 16 |
| t _{PLH} | CLK | Any Q | MAX | 16 | 11 |
| t _{PHL} | | | | 16 | 15 |
| t _{PLH} | \overline{ENT} | \overline{RCO} | MAX | 14 | 10 |
| t _{PHL} | | | | 9 | 17 |
| t _{PLH} | \overline{ENP} | \overline{RCO} | MAX | - | 14 |
| t _{PHL} | | | | - | 17 |
| t _{PHL} | S0, S1 (clear mode) | Any Q | MAX | 26 | - |
| t _{PLH} | S0 or S1 (count up/down) | \overline{RCO} | MAX | 16 | - |
| t _{PHL} | | | | 16 | - |
| t _{PHL} | S0 or S1 (clear mode) | \overline{RCO} | MAX | 16 | 21 |

 UNIT f_{max} : MHz other : ns

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Synchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



FUNCTION TABLE

| S1 | S0 | FUNCTION |
|----|----|------------|
| L | L | Clear |
| L | H | Count down |
| H | L | Load |
| H | H | Count up |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 45 | 195 | mA |
| I _{OH} | MAX | -0.4 | -2 | mA |
| I _{OL} | MAX | 8 | 20 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

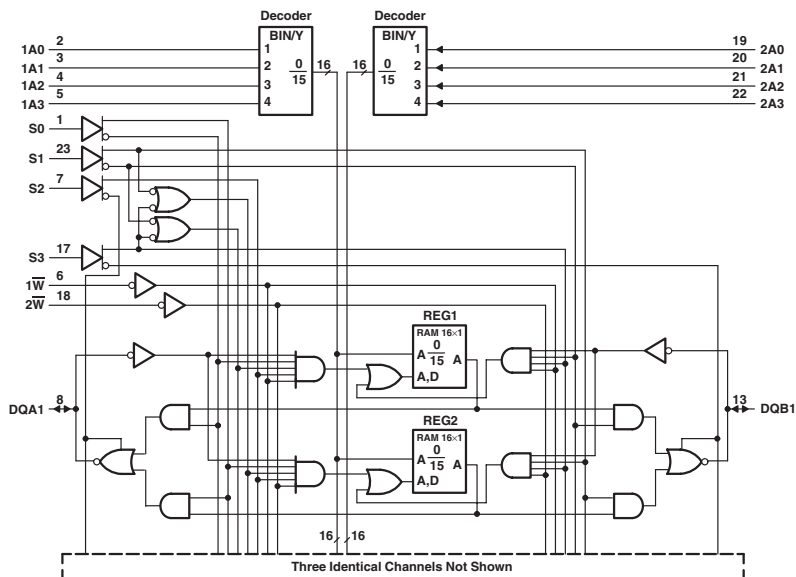
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|--|--------|------------|-----|----|
| f _{max} | | | MIN | 35 | 45 |
| t _w | CLK | | MIN | 14 | 11 |
| t _{su} | Data input A-H | | MIN | 10 | 5 |
| | ENP or ENT | | | 15 | 9 |
| | S0 low and S1 high (load) | | | 13 | 11 |
| | S0 and S1 low (clear) | | | 13 | 11 |
| | S0 high and S1 low (count down) | | | 13 | 50 |
| | S0 and S1 high (count up) | | | 13 | 50 |
| t _h | S0 high after S1 ↑ or S1 high after S0 ↑ | | MIN | 3 | - |
| | Data input A-H | | | 0 | 0 |
| t _{PLH} | CLK | RCO | MAX | 14 | 35 |
| t _{PHL} | | | | 14 | 18 |
| t _{PLH} | CLK | Any Q | MAX | 16 | 11 |
| t _{PHL} | | | | 16 | 15 |
| t _{PLH} | ENT | RCO | MAX | 14 | 15 |
| t _{PHL} | | | | 9 | 17 |
| t _{PLH} | ENP | RCO | MAX | - | 19 |
| t _{PHL} | | | | - | 18 |
| t _{PLH} | S1 (count up/down) | RCO | MAX | 15 | - |
| t _{PHL} | | | | 15 | - |
| t _{PLH} | S0 (clear/load) | RCO | MAX | 16 | - |
| t _{PHL} | | | | 12 | - |

 UNIT f_{max} : MHz other : ns

DUAL 16-BY 4-BIT REGISTER FILES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Each Register File Has Individual Write-Enable Controls and Address Lines

Logic Diagram



FUNCTION TABLE

| FILE SELECT | | | INPUT/OUTPUT | | |
|-------------|----|------------------|--------------|----|----------------------|
| S0 | S1 | FILE SEL | S2 | S3 | I/O SEL |
| L | L | 1R to A, 1R to B | L | L | A out B A out, B out |
| H | L | 2R to A, 1R to B | | | |
| L | H | 1R to A, 2R to B | | | |
| H | H | 2R to A, 2R to B | | | |
| L | L | A to 1R, 1R to B | H | L | A in B A in, B out |
| H | L | A to 2R, 1R to B | | | |
| L | H | A to 1R, 2R to B | | | |
| H | H | A to 2R, 2R to B | | | |
| L | L | 1R to A, B to 1R | L | H | A out B A out, B in |
| H | L | 2R to A, B to 1R | | | |
| L | H | 1R to A, B to 2R | | | |
| H | H | 2R to A, B to 2R | | | |
| L | L | B to 1R | H | H | A in Bin A in, B |
| H | L | A to 2R, B to 1R | | | |
| L | H | A to 1R, B to 2R | | | |
| H | H | B to 2R | | | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 110 | 190 | mA |
| I _{OL} | MAX | 24 | 48 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-------------------|------------------------|---------|------------|-----|----|
| t _w | write | | MIN | 12 | 12 |
| t _{su} | Address before write ↓ | | MIN | 5 | 5 |
| | Data before write ↑ | | | 15 | 15 |
| | Select before write ↓ | | | 12 | 12 |
| t _h | Address before write ↓ | | MIN | 0 | 0 |
| | Data before write ↑ | | | 0 | 0 |
| | Select before write ↓ | | | 12 | 12 |
| t _{a(A)} | Any A | Any DQ | MAX | 19 | 15 |
| t _{a(S)} | S0 | Any DQA | MAX | 15 | 13 |
| | S1 | Any DQB | | 15 | 13 |
| t _{dis} | S2 | Any DQA | MAX | 14 | 11 |
| | S3 | Any DQB | | 14 | 11 |
| t _{en} | S2 | Any DQA | MAX | 17 | 12 |
| | S3 | Any DQB | | 17 | 12 |
| t _{pd} | W | Any DQ | MAX | 23 | 19 |
| | DA | DQB | | 26 | 22 |
| | DQB | DQA | | 26 | 22 |
| | DQB | DQA | | 26 | 22 |

UNIT: ns

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

FUNCTION TABLE

| OE | INPUTS | | | D | OUTPUT |
|----|--------|--------------|---|---|----------------|
| | CLR | ENABLE LE | | | |
| L | L | X | X | X | L |
| L | H | H | H | L | L |
| L | H | L | X | X | Q ₀ |
| H | X | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION

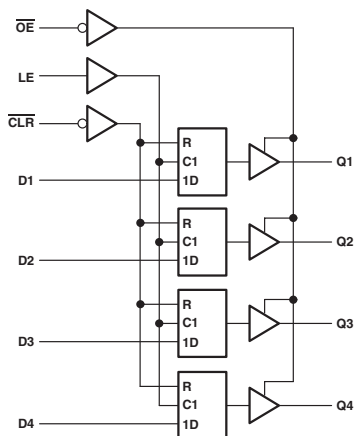
| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 31 | 129 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|---------|--------|------------|-----|------|
| t _w | CLR low | Q | MIN | 15 | 5 |
| | LE high | | | 10 | 5 |
| | | | | 10 | 2 |
| t _{su} | | | | 7 | 4.5 |
| t _h | | | | | |
| t _{PLH} | D | Q | MAX | 14 | 9.5 |
| t _{PHL} | | | | 14 | 7.5 |
| t _{PLH} | LE | Q | MAX | 22 | 13 |
| t _{PHL} | | | | 21 | 7.5 |
| t _{PHL} | CLR | Q | MAX | 20 | 9 |
| t _{PZH} | OE | Q | MAX | 18 | 6.5 |
| t _{PZL} | | | | 18 | 10.5 |
| t _{PHZ} | OE | Q | MAX | 10 | 7.5 |
| t _{PLZ} | | | | 15 | 7.5 |

UNIT: ns

Logic Diagram



DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

FUNCTION TABLE

| FUNCTION TABLE | | | | | |
|----------------|-----|-----|---|---|----------------|
| INPUTS | | | | D | OUTPUTS |
| OE | CLR | CLK | D | | |
| L | L | X | X | L | L |
| L | H | ↑ | H | L | H |
| L | H | ↑ | L | L | L |
| L | H | L | X | X | Q ₀ |
| H | X | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

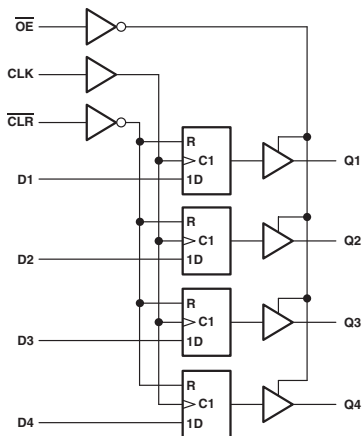
| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 32 | 160 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|---------------------|--------|------------|------|------|
| f _{max} | | | MIN | 30 | 125 |
| t _w | PRE or CLR low | | MIN | 10 | 2 |
| | CLK "H" | | | 16.5 | 3 |
| | CLK "L" | | | 16.5 | 4 |
| t _{su} | Data | | MIN | 15 | 2 |
| | PRE or CLR inactive | | | 10 | 4 |
| | | | | 0 | 1 |
| t _{PHL} | CLK | Q | MAX | 14 | 8.5 |
| t _{PLH} | | | | 14 | 10.5 |
| t _{PHL} | CLR | Q | MAX | 17 | 9.5 |
| t _{PZH} | OE | Q | MAX | 18 | 7 |
| t _{PZL} | | | | 18 | 10.5 |
| t _{PHZ} | OE | Q | MAX | 10 | 6 |
| t _{PLZ} | | | | 12 | 7.5 |

UNIT f_{max} : MHz other : ns

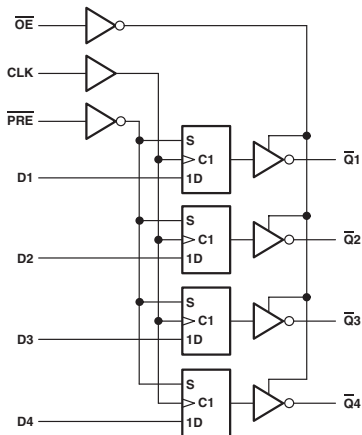
Logic Diagram



DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUT |
|--------|-----|-----|---|-------------|
| OE | PRE | CLK | D | Q |
| L | L | X | X | L |
| L | H | T | H | L |
| L | H | T | L | H |
| L | H | L | X | \bar{Q}_0 |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 31 | 160 | mA |
| I _{OH} | MAX | -2.6 | -15 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

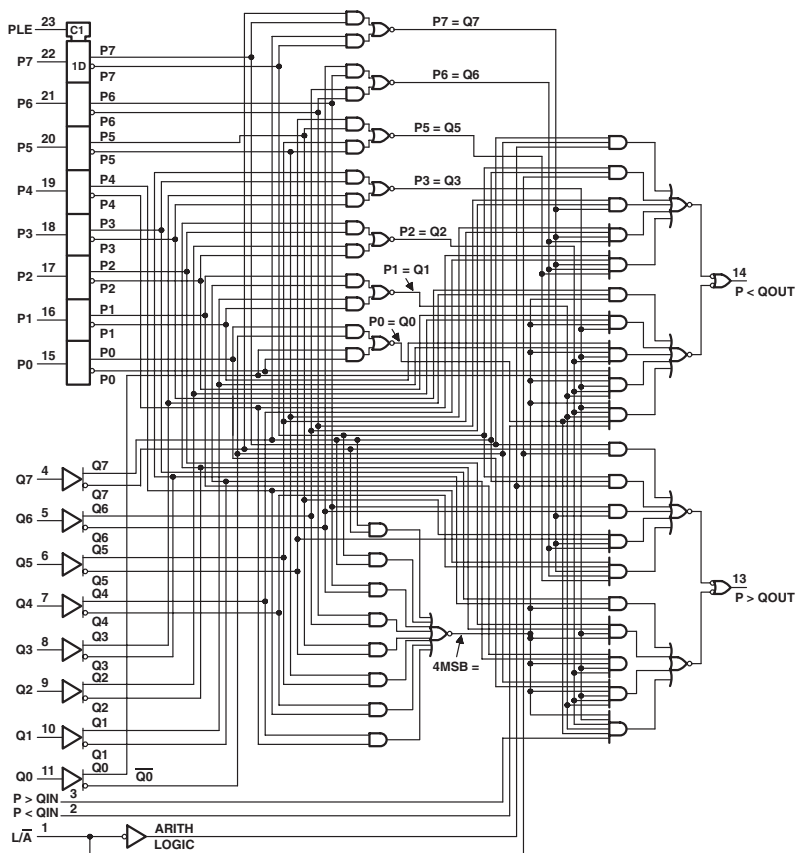
| PARAMETER | | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|--------------|-------------------------|-----------|------------|------|------|
| f _{max} | | | | MIN | 30 | 80 |
| t _w | PRE "L" | | | MIN | 10 | 4.5 |
| | CLK "H" | | | | 16.5 | 6.2 |
| | CLK "L" | | | | 16.5 | 6.2 |
| t _{su} | Data | | | MIN | 15 | 4.5 |
| | PRE inactive | | | | 10 | 5 |
| t _h | | | | MIN | 0 | 2 |
| t _{PLH} | | CLK | \bar{Q} | MAX | 14 | 8.5 |
| t _{PHL} | | | | | 14 | 10.5 |
| t _{PHL} | | $\overline{\text{PRE}}$ | \bar{Q} | MAX | 19 | 9.5 |
| t _{PZH} | | $\overline{\text{OE}}$ | \bar{Q} | MAX | 18 | 7 |
| t _{PZL} | | | | | 18 | 11 |
| t _{PHZ} | | $\overline{\text{OE}}$ | \bar{Q} | MAX | 10 | 7 |
| t _{PLZ} | | | | | 13 | 7 |

UNIT f_{max} : MHz, other : ns

8-BIT MAGNITUDE COMPARATORS

- SN54AS885 Latchable P-Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Cascadable to n Bits While Maintaining High Performance

Logic Diagram



FUNCTION TABLE

| COMPARISON | INPUTS | | | | OUTPUTS | |
|-------------|--------|-------------------------|---------|---------|----------|----------|
| | L/A | DATA P0-P7, Q0-Q7 | P > QIN | P < QIN | P > QOUT | P < QOUT |
| Logical | H | P > Q | X | X | H | L |
| Logical | H | P < Q | X | X | L | H |
| Logical† | H | P = Q | H or L | H or L | H or L | H or L |
| Arithmetic | L | P AG Q | X | X | H | L |
| Arithmetic | L | Q AG P | X | X | L | H |
| Arithmetic† | L | P = Q | H or L | H or L | H or L | H or L |

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.
AG = arithmetically greater than

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AS | UNIT |
|-----------|------------|-----|------|
| Icc | MAX | 210 | mA |
| Ioh | MAX | -2 | mA |
| Iol | MAX | 20 | mA |

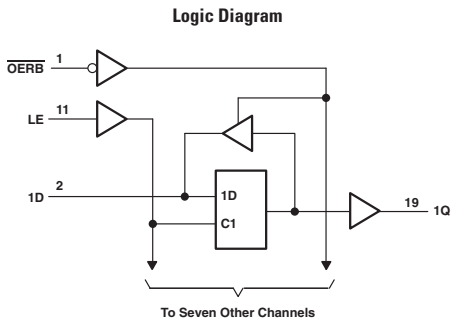
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS |
|------------------|--------------------------|-----------|------------|------|
| t _{su} | Data before PLE ↓ | | MIN | 2 |
| t _h | Data after PLE ↓ | | | 4 |
| t _{PLH} | L / \bar{A} | P < QOUT, | MAX | 13 |
| t _{PHL} | | P > QOUT | | 13 |
| t _{PLH} | P < QIN, P > QIN | P < QOUT, | MAX | 8 |
| t _{PHL} | | P > QOUT | | 8 |
| t _{PLH} | Any P or Q data input | P < QOUT, | MAX | 17.5 |
| t _{PHL} | | P > QOUT | | 15 |

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------------|---|------------|------|------|
| I _{CC} | | MAX | 70 | mA |
| I _{OH} | Q | MAX | -2.6 | mA |
| | D | | -0.4 | mA |
| I _{OL} | Q | MAX | 24 | mA |
| | D | | 8 | mA |

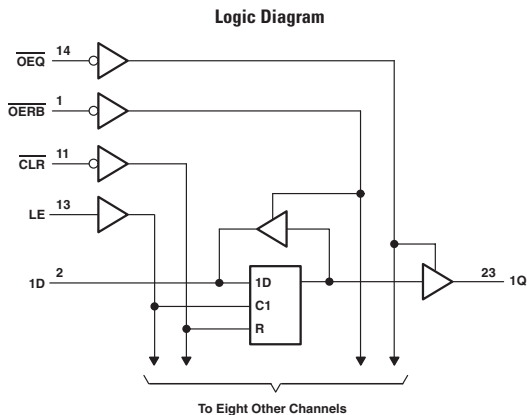
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|------------------|--------|------------|-----|
| t _w | LE high | | MIN | 10 |
| t _{su} | Data before LE ↓ | | MIN | 10 |
| | Data before OERB | | | 10 |
| t _h | Data after LE ↓ | | MIN | 5 |
| t _{PLH} | D | Q | MAX | 17 |
| | | | | 24 |
| t _{PHL} | LE | Q | MAX | 26 |
| | | | | 26 |
| t _{ten} | OERB | D | MAX | 21 |
| | | | | 19 |

UNIT: ns

9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout
- Designed with Nine Bits for Parity Applications



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------------|---|------------|------|------|
| I _{CC} | | MAX | 80 | mA |
| I _{OH} | Q | MAX | -2.6 | mA |
| | D | | -0.4 | mA |
| I _{OL} | Q | MAX | 24 | mA |
| | D | | 8 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

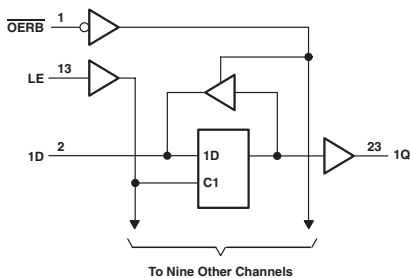
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|--------------------|--------|------------|------------------|
| t _w | C "H" | | MIN | 10 |
| | CLR "L" | | | 10 |
| t _{su} | Data before LE ↓ | | MIN | 10 |
| | Data before OERB ↓ | | | 10 |
| t _h | Data after LE ↓ | | MIN | 5 |
| | | | | 5 |
| t _{PLH} | D | Q | MAX | 14 |
| t _{PHL} | | | | 16 |
| t _{PLH} | LE | Q | MAX | 20 |
| t _{PHL} | | | | 25 |
| t _{PHL} | CLR | Q | MAX | 20 |
| | | D | | 26 |
| t _{en} | OERB | D | MAX | 21 |
| t _{dis} | | | | 14 |
| t _{en} | OEQ | Q | MAX | 18 |
| | | | | t _{dis} |

UNIT:ns

10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | UNIT |
|-----------|---|------------|------|------|
| I_{CC} | | MAX | 82 | mA |
| I_{OH} | Q | MAX | -2.6 | mA |
| | D | | -0.4 | mA |
| I_{OL} | Q | MAX | 24 | mA |
| | D | | 8 | mA |

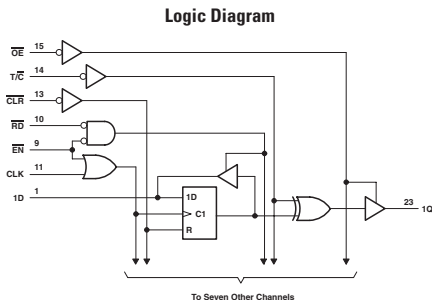
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|-----------|--------------------|--------|------------|-----|
| t_w | C "H" | | MIN | 10 |
| t_{su} | Data before LE ↓ | | MIN | 10 |
| | Data before OERB ↓ | | | 10 |
| t_h | Data after LE ↓ | | MIN | 5 |
| | | | | |
| t_{PLH} | D | Q | MAX | 14 |
| t_{PHL} | | | | 18 |
| t_{PLH} | LE | Q | MAX | 21 |
| t_{PHL} | | | | 27 |
| t_{en} | OERB | D | MAX | 21 |
| t_{dis} | | | | 16 |

UNIT:ns

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- T/C Determines True or Complementary Data at Q Outputs



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | ALS | ALS-1 | UNIT |
|-----------------|---|------------|------|-------|------|
| I _{CC} | | MAX | 85 | 85 | mA |
| I _{OL} | Q | MAX | 24 | 48 | mA |
| | D | | 8 | 8 | mA |
| I _{OH} | Q | MAX | -2.6 | -2.6 | mA |
| | D | | -0.4 | -0.4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | ALS-1 |
|--------------------|----------------------------------|--------|------------|------|-------|
| t _w | CLR low | | MIN | 10 | 10 |
| | | | | 14.5 | 14.5 |
| | | | | 14.5 | 14.5 |
| t _{su} | Data before CLK ↑ | | MIN | 15 | 15 |
| | EN low before CLK ↑ | | | 10 | 10 |
| | CLK high before EN ↑ *1 | | | 15 | 15 |
| | CLR high (inactive) before CLK ↑ | | | 10 | 10 |
| t _h | Data after CLK ↑ | | MIN | 0 | 0 |
| | EN low after CLK ↑ | | | 5 | 5 |
| | RD high after CLK ↑ *2 | | | 5 | 5 |
| t _{PLH} | CLK (T/C = H or L) | Q | MAX | 28 | 28 |
| t _{PHL} | | | | 28 | 28 |
| t _{PLH} | CLR (T/C = L) | Q | MAX | 27 | 27 |
| t _{PHL} | | | | 23 | 23 |
| t _{PLH} | T/C | Q | MAX | 23 | 23 |
| t _{PHL} | | | | 23 | 23 |
| t _{PLH} | CLR | D | MAX | 30 | 30 |
| t _{su} *3 | RD | D | MAX | 16 | 16 |
| t _{su} *4 | | | | 19 | 19 |
| t _{su} *3 | EN | D | MAX | 16 | 16 |
| t _{su} *4 | | | | 19 | 19 |
| t _{su} *3 | OE | Q | MAX | 15 | 15 |
| t _{su} *4 | | | | 10 | 10 |

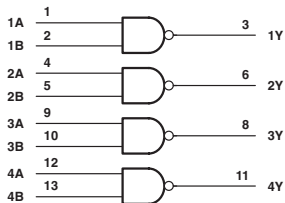
UNIT: ns

1000

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

- Buffer Version of SN74ALS00A
- Driver Version of SN74AS00
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------|------------|------|-----|------|
| I_{CC} | MAX | 7.8 | 19 | mA |
| I_{OH} | MAX | -2.6 | -48 | mA |
| I_{OL} | MAX | 24 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-----------|--------|--------|------------|-----|----|
| t_{PLH} | A or B | Y | MAX | 8 | 4 |
| t_{PHL} | | | | 7 | 4 |

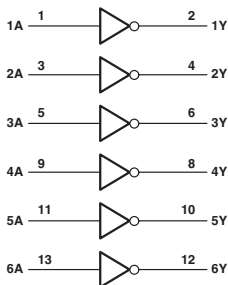
UNIT: ns

1004

HEX INVERTING DRIVERS

- Driver Version of SN74ALS04B and SN74AS04
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------|------------|-----|-----|------|
| I_{CC} | MAX | 12 | 27 | mA |
| I_{OH} | MAX | -15 | -48 | mA |
| I_{OL} | MAX | 24 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-----------|--------|--------|------------|-----|----|
| t_{PLH} | A or B | Y | MAX | 7 | 4 |
| t_{PHL} | | | | 6 | 4 |

UNIT: ns

1005

HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Buffer Version of SN74ALS05A

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

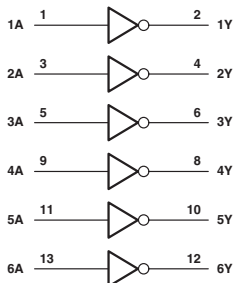
| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 12 | mA |
| V _{OH} | MAX | 5.5 | V |
| I _{OL} | MAX | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 30 |
| t _{PHL} | | | | 10 |

UNIT: ns

Logic Diagram



1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER

- Buffer Version of SN74ALS08
- Driver Version of SN74AS08

FUNCTION TABLE

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | H |
| L | X | L |
| X | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

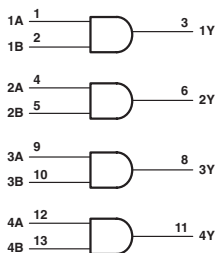
| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 9.3 | 22 | mA |
| I _{OH} | MAX | -2.6 | -48 | mA |
| I _{OL} | MAX | 24 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|--------|--------|------------|-----|----|
| t _{PLH} | A or B | Y | MAX | 9 | 6 |
| t _{PHL} | | | | 9 | 6 |

UNIT: ns

Logic Diagram

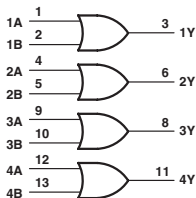


1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

- $Y = A + B$
- Driver Version of SN74AS32
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------|------------|------|-----|------|
| I_{CC} | MAX | 10.6 | 24 | mA |
| I_{OH} | MAX | -2.6 | -48 | mA |
| I_{OL} | MAX | 24 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-----------|--------|--------|------------|-----|-----|
| t_{PLH} | A or B | Y | MAX | 9 | 6.3 |
| t_{PHL} | A or B | Y | MAX | 12 | 6.3 |

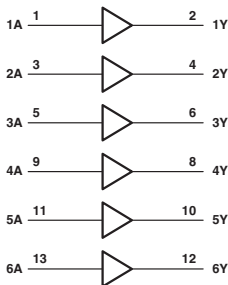
UNIT: ns

1034

HEX DRIVERS

- SN74AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers

Logic Diagram



FUNCTION TABLE

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION

| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------|------------|-----|-----|------|
| I_{CC} | MAX | 14 | 35 | mA |
| I_{OH} | MAX | -15 | -48 | mA |
| I_{OL} | MAX | 24 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|-----------|-------|--------|------------|-----|----|
| t_{PLH} | A | Y | MAX | 8 | 6 |
| t_{PHL} | | | | 8 | 6 |

UNIT: ns

1035

HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Noninverting Buffers with Open-Collector Outputs

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

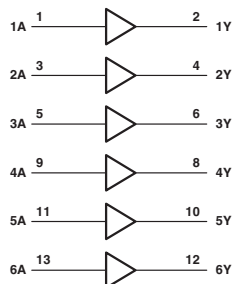
| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 14 | mA |
| V _{OH} | MAX | 5.5 | V |
| I _{OL} | MAX | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 30 |
| t _{PHL} | | | | 12 |

UNIT: ns

Logic Diagram



1240

OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

- Low-Power Versions of SN74ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

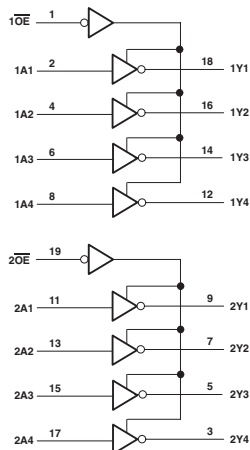
| PARAMETER | MAX or MIN | ALS | UNIT |
|------------------|------------|-----|------|
| I _{CCZ} | MAX | 13 | mA |
| I _{CCL} | MAX | 14 | mA |
| I _{OH} | MAX | -15 | mA |
| I _{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 13 |
| t _{PHL} | | | | 13 |
| t _{PZH} | \overline{OE} | Y | MAX | 20 |
| t _{PZL} | | | | 22 |
| t _{PHZ} | \overline{OE} | Y | MAX | 10 |
| t _{PLZ} | | | | 13 |

UNIT: ns

Logic Diagram



1244

OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Low-Power Versions of SN74ALS244 Series

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

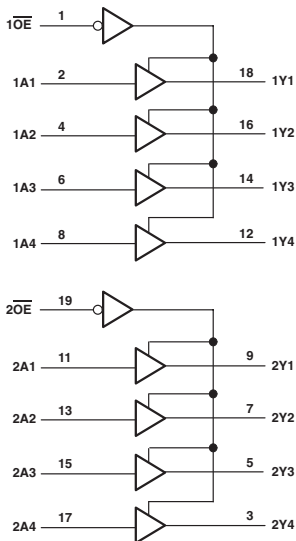
| PARAMETER | MAX or MIN | ALS | UNIT |
|------------------|------------|-----|------|
| I _{CCZ} | MAX | 20 | mA |
| I _{CCL} | MAX | 17 | mA |
| I _{OH} | MAX | -15 | mA |
| I _{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-----------------|--------|------------|-----|
| T _{PLH} | A | Y | MAX | 14 |
| | | | | 14 |
| T _{PHL} | A | Y | MAX | 14 |
| | | | | 14 |
| T _{PZH} | \overline{OE} | Y | MAX | 22 |
| T _{PZL} | | | | 22 |
| T _{PHZ} | \overline{OE} | Y | MAX | 13 |
| T _{PLZ} | | | | 16 |

UNIT: ns

Logic Diagram



1245

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Low-Power Versions of 4ALS245 Series

FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

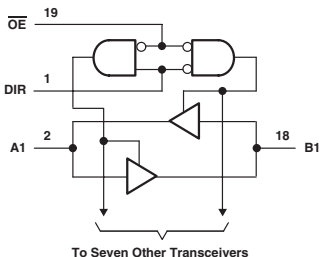
| PARAMETER | MAX or MIN | ALS | UNIT |
|------------------|------------|-----|------|
| I _{CCZ} | MAX | 36 | mA |
| I _{CCL} | MAX | 33 | mA |
| I _{OH} | MAX | -15 | mA |
| I _{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-----------------|--------|------------|-----|
| T _{PLH} | A or B | B or A | MAX | 13 |
| | | | | 13 |
| T _{PHL} | A or B | A or B | MAX | 25 |
| | | | | 25 |
| T _{PZH} | \overline{OE} | A or B | MAX | 12 |
| T _{PZL} | | | | 18 |

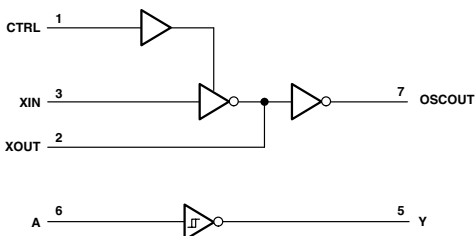
UNIT: ns

Logic Diagram



OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR

Logic Diagram



FUNCTION TABLES

| INPUTS | | OUTPUTS | |
|--------|-----|---------|--------|
| CTRL | XIN | XOUT | OSCOUT |
| H | L | H | L |
| H | H | L | H |
| L | X | L | H |

| INPUT | OUTPUT |
|-------|--------|
| A | Y |
| L | H |
| H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVC 1.8V | LVC 2.5V | LVC 3V | LVC 5V | UNIT |
|---|------------|----------|----------|--------|--------|------|
| I _{CC} | MAX | 0.01 | 0.01 | 0.01 | 0.01 | mA |
| I _{OH} (OSCOUT, XOUT, Y outputs) | MAX | -4 | -8 | -24 | -32 | mA |
| I _{OL} (OSCOUT, XOUT, Y outputs) | MAX | 4 | 8 | 24 | 32 | mA |
| I _{OL} (XOUT) | MAX | 2 | - | - | - | mA |

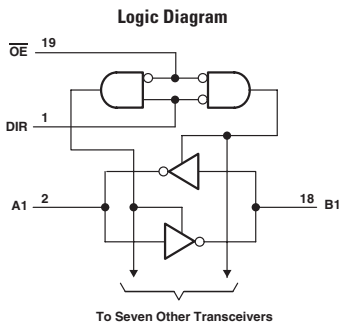
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 1.8V | LVC 2.5V | LVC 3V | LVC 5V |
|------------------|-------|--------|------------|----------|----------|--------|--------|
| t _{PLH} | A | Y | MAX | 17.3 | 7.4 | 6.4 | 5.3 |
| | | | | 17.3 | 7.4 | 6.4 | 5.3 |
| t _{PHL} | XIN | XOUT | MAX | 15.8 | 5.8 | 5.4 | 4.6 |
| | | | | 15.8 | 5.8 | 5.4 | 4.6 |
| t _{PLH} | XIN | OSCOUT | MAX | 25.7 | 7.1 | 7.8 | 6.7 |
| | | | | 25.7 | 7.1 | 7.8 | 6.7 |
| t _{PHL} | CTRL | XOUT | MAX | 24.5 | 12 | 12.7 | 11.2 |
| | | | | 24.5 | 12 | 12.7 | 11.2 |

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS640B
- Inverting Logic
- 3-State Outputs



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-------------------------|
| OE | DIR | |
| L | L | \bar{B} data to A bus |
| L | H | \bar{A} data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 32 | mA |
| I_{OH} | MAX | -15 | mA |
| I_{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

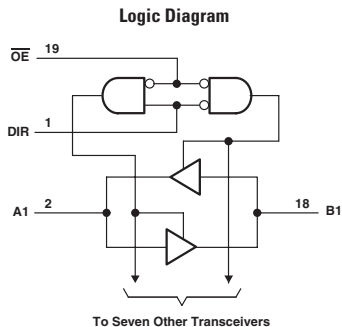
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|-----------|-----------------|--------|------------|-----|
| t_{PLH} | A or B | B or A | MAX | 15 |
| t_{PHL} | | | | 10 |
| t_{PZH} | \overline{OE} | A or B | MAX | 20 |
| t_{PZL} | | | | 22 |
| t_{PHZ} | \overline{OE} | A or B | MAX | 10 |
| t_{PLZ} | | | | 13 |

UNIT: ns

1645

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS645A
- 3-State Outputs



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|----------------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 38 | mA |
| I _{OH} | MAX | -15 | mA |
| I _{OL} | MAX | 16 | mA |

SWITCHING CHARACTERISTICS

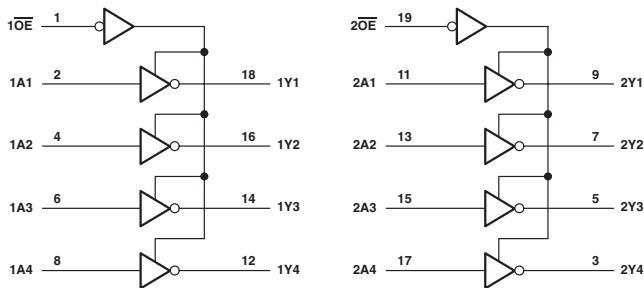
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|--------|--------|------------|-----|
| t _{PLH} | A or B | B or A | MAX | 13 |
| | | | | 13 |
| t _{PZH} | OE | A or B | MAX | 25 |
| | | | | 25 |
| t _{PHZ} | OE | A or B | MAX | 12 |
| | | | | 18 |

UNIT: ns

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required (SN74ALS2240, SN74ABT2240A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2240)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | ABT | UNIT |
|-----------|------------|-----|----------|------|------|
| I_{CCZ} | MAX | 20 | 8 | 0.25 | mA |
| I_{CCL} | MAX | 23 | 76 | 30 | mA |
| I_{OH} | MAX | -15 | -12 | -32 | mA |
| I_{OL} | MAX | 15 | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

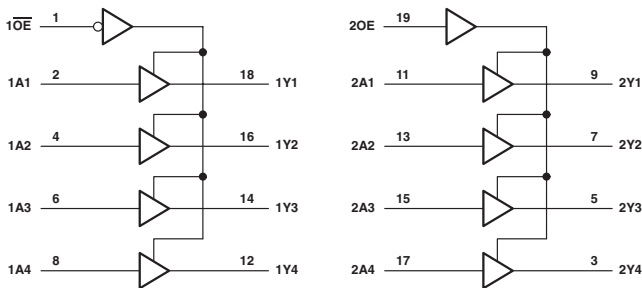
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT | ABT |
|-----------|-----------------|--------|------------|-----|----------|-----|
| t_{PLH} | A | Y | MAX | 10 | 5.7 | 4.8 |
| t_{PHL} | | | | 10 | 4.4 | 5.4 |
| t_{PZH} | \overline{OE} | Y | MAX | 17 | 9.3 | 5.2 |
| t_{PZL} | | | | 20 | 12.4 | 6.8 |
| t_{PHZ} | \overline{OE} | Y | MAX | 10 | 8.7 | 6.4 |
| t_{PLZ} | | | | 15 | 10.6 | 6.2 |

UNIT: ns

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2241A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2241)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | ABT | UNIT |
|------------------|------------|----------|------|------|
| I _{CCZ} | MAX | 9 | 0.25 | mA |
| I _{CCL} | MAX | 76 | 30 | mA |
| I _{OH} | MAX | -12 | -32 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

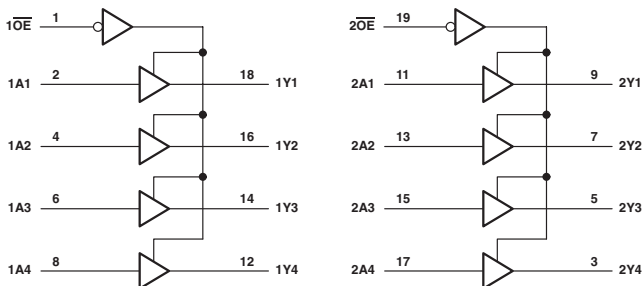
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | ABT |
|------------------|------------------|--------|------------|----------|-----|
| t _{PLH} | A | Y | MAX | 4.9 | 4.7 |
| t _{PHL} | | | | 6.9 | 5.6 |
| t _{PZH} | $\overline{1OE}$ | Y | MAX | 8.9 | 5.8 |
| t _{PZL} | | | | 10.3 | 8.4 |
| t _{PHZ} | $\overline{1OE}$ | Y | MAX | 8.7 | 6.6 |
| t _{PLZ} | | | | 11.3 | 6.4 |
| t _{PZH} | 2OE | Y | MAX | 8.9 | 5.8 |
| t _{PZL} | | | | 10.3 | 8.4 |
| t _{PHZ} | 2OE | Y | MAX | 8.7 | 6.6 |
| t _{PLZ} | | | | 11.3 | 6.4 |

UNIT: ns

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2244A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2244)
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVC2244A)

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | X | Z |
| L | L | L |
| L | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | ABT | LVC 3V | UNIT |
|-----------|------------|-----|----------|------|--------|------|
| I_{CCZ} | MAX | 23 | 10 | 0.25 | 0.01 | mA |
| I_{CCL} | MAX | 22 | 77 | 30 | 0.01 | mA |
| I_{OH} | MAX | -15 | -12 | -32 | -12 | mA |
| I_{OL} | MAX | 15 | 12 | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT | ABT | LVC 3V |
|-----------|-----------------|--------|------------|-----|----------|-----|--------|
| t_{PLH} | A | Y | MAX | 16 | 4.9 | 4.7 | 5.5 |
| t_{PHL} | | | | 17 | 6.7 | 5.6 | 5.5 |
| t_{PZH} | \overline{OE} | Y | MAX | 17 | 8.7 | 5.5 | 7.1 |
| t_{PZL} | | | | 14 | 10.4 | 8.3 | 7.1 |
| t_{PHZ} | \overline{OE} | Y | MAX | 9 | 7.8 | 6.6 | 6.8 |
| t_{PLZ} | | | | 9 | 9.8 | 5.8 | 6.8 |

UNIT: ns

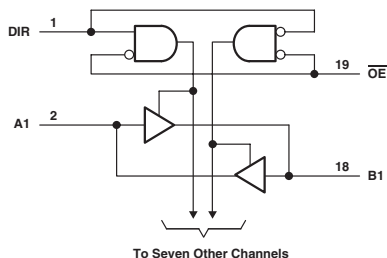
OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- B Port Has Equivalent 33- Ω Series Resistors, So No External Resistors Are Required (SN74BCT2245)
- B-Port Outputs Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required (SN74ABT2245)
- Outputs Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required (SN74ABTR2245)
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required (SN74LVCR2245)
- B-Port Outputs Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required (SN74LVTH2245)

FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | ABT | ABTR | LVTH 3V | LVCR 3V | UNIT |
|-------------------|------------|----------|------|------|---------|---------|------|
| I_{CCZ} | MAX | 15 | 0.25 | 0.25 | 0.19 | 0.01 | mA |
| I_{CCL} | MAX | 100 | 32 | 32 | 5 | 0.01 | mA |
| I_{OH} (A port) | MAX | -3 | -32 | -12 | -32 | -12 | mA |
| I_{OH} (B port) | MAX | -12 | -12 | -12 | -12 | -12 | mA |
| I_{OL} (A port) | MAX | 24 | 64 | 12 | 64 | 12 | mA |
| I_{OL} (B port) | MAX | 12 | 12 | 12 | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

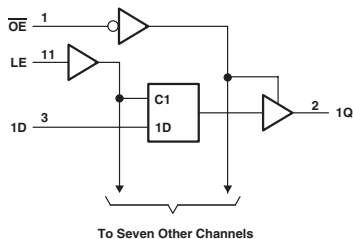
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | ABT | ABTR | LVTH 3V | LVCR 3V |
|-----------|-----------------|--------|------------|----------|-----|------|---------|---------|
| t_{PLH} | A | B | MAX | 5.8 | 3.8 | 3.8 | 4.4 | 6.3 |
| t_{PHL} | | | | 7.8 | 4.5 | 4.5 | 4.4 | 6.3 |
| t_{PLH} | B | A | MAX | 7 | 3.6 | 3.8 | 3.5 | 6.3 |
| t_{PHL} | | | | 7.7 | 4 | 4.5 | 3.5 | 6.3 |
| t_{PZH} | \overline{OE} | B | MAX | 9.9 | 6.1 | 6.1 | 6.2 | 8.2 |
| t_{PZL} | | | | 12.2 | 6.3 | 6.3 | 6.2 | 8.2 |
| t_{PHZ} | \overline{OE} | B | MAX | 8.2 | 5.3 | 5.3 | 5.9 | 7.8 |
| t_{PLZ} | | | | 9.2 | 4.8 | 4.8 | 5.4 | 7.8 |
| t_{PZH} | \overline{OE} | A | MAX | 11.1 | 5.5 | 6.1 | 5.5 | 8.2 |
| t_{PZL} | | | | 11.4 | 5.7 | 6.3 | 5.5 | 8.2 |
| t_{PHZ} | \overline{OE} | A | MAX | 9.4 | 5.6 | 5.3 | 5.9 | 7.8 |
| t_{PLZ} | | | | 7.6 | 4.5 | 4.8 | 5 | 7.8 |

UNIT: ns

25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

- 3-State True Outputs with 25-Ω Sink Resistors
- Full Parallel Access for Loading
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE

(each latch)

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | F | UNIT |
|-----------------|------------|----|------|
| I _{CC} | MAX | 66 | mA |
| I _{OH} | MAX | -3 | mA |
| I _{OL} | MAX | 12 | mA |

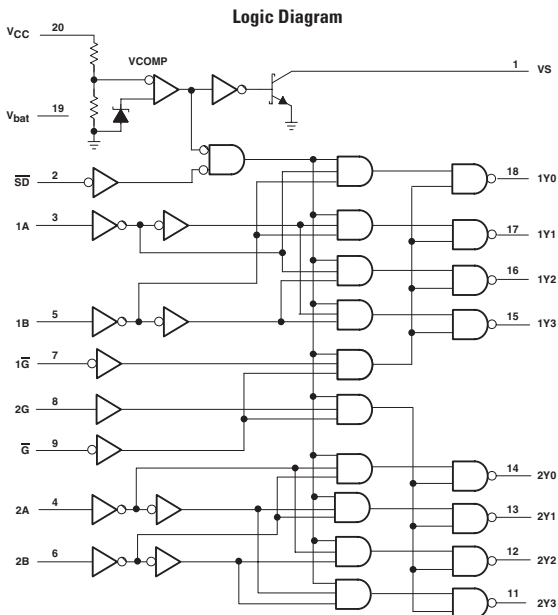
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | F |
|------------------|------------------|--------|------------|-----|
| t _w | LE high | | MIN | 6 |
| t _{su} | Data before LE ↓ | | MIN | 2 |
| t _h | Data after LE ↓ | | MIN | 6 |
| t _{PLH} | D | Q | MAX | 9 |
| t _{PHL} | | | | 7 |
| t _{PLH} | LE | Q | MAX | 13 |
| t _{PHL} | | | | 8 |
| t _{PZH} | OE | Q | MAX | 12 |
| t _{PZL} | | | | 9.5 |
| t _{PHZ} | OE | Q | MAX | 7.5 |
| t _{PLZ} | | | | 6 |

UNIT:ns

MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR

- Built-In Supply-Voltage Monitor for V_{CC}
- Separate Enable Inputs for Easy Cascading



FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | | |
|-----------|--------|----|-------|---------|-----|-----|-----|
| CONTROL | SELECT | | | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| \bar{G} | 1G | SD | 1B 1A | | | | |
| H | X | X | X X | H | H | H | H |
| X | H | X | X X | H | H | H | H |
| X | X | L | X X | H | H | H | H |
| L | L | H | L L | L | H | H | H |
| L | L | H | L H | H | L | H | H |
| L | L | H | H L | H | H | L | H |
| L | L | H | H H | H | H | H | L |

| INPUTS | | | | OUTPUTS | | | |
|-----------|--------|----|-------|---------|-----|-----|-----|
| CONTROL | SELECT | | | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| \bar{G} | 2G | SD | 2B 2A | | | | |
| H | X | X | X X | H | H | H | H |
| X | H | X | X X | H | H | H | H |
| X | X | L | X X | H | H | H | H |
| L | H | H | L L | L | H | H | H |
| L | H | H | L H | H | L | H | H |
| L | H | H | H L | H | H | L | H |
| L | H | H | H H | H | H | H | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|------------------------|------------|----------|------|
| I_{CC} | MAX | 3 | mA |
| I_{bat} (Output low) | MAX | 3 | mA |
| I_{OH} | MAX | -0.4 | mA |
| I_{OL} (Y Output) | MAX | 8 | mA |
| I_{OL} (I/S Output) | MAX | 20 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|-----------|---------------|--------|------------|----------|
| t_{PLH} | A or B | Any Y | MAX | 12 |
| t_{PHL} | | | | 12 |
| t_{PLH} | Any \bar{G} | Any Y | MAX | 10 |
| t_{PHL} | | | | 11 |
| t_{PLH} | \bar{SD} | Any Y | MAX | 12 |
| t_{PHL} | | | | 12 |
| t_{PLH} | V_{CC} | Any Y | MAX | 250 |
| t_{PHL} | | | | 250 |
| t_{PLH} | V_{CC} | VS | MAX | 250 |
| t_{PHL} | | | | 250 |

2541

OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS

- Outputs Have 25-Ω Series Resistor So No External Resistors Are Required

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

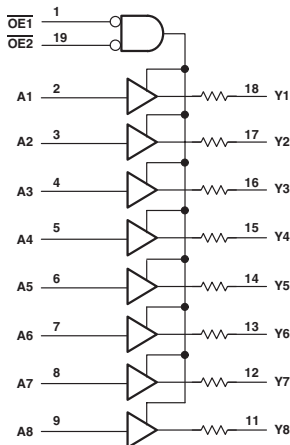
| PARAMETER | MAX or MIN | ALS | UNIT |
|------------------|------------|------|------|
| I _{CCZ} | MAX | 22 | mA |
| I _{CCL} | MAX | 25 | mA |
| I _{OH} | MAX | -0.4 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|------------------|-------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 15 |
| | | | | 12 |
| t _{PHL} | A | Y | MAX | 15 |
| | | | | 20 |
| t _{PHZ} | OE | Y | MAX | 10 |
| | | | | 12 |

UNIT: ns

Logic Diagram



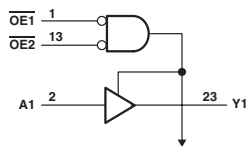
All output resistors are 25 Ω.

2827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2827)
- Output Ports Have Equivalent 25-Ω Resistors; No External Resistors Are Required (SN74BCT2827C)

Logic Diagram



To Nine Other Channels

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | ABT | UNIT |
|------------------|------------|----------|------|------|
| I _{CCZ} | MAX | 6 | 0.25 | mA |
| I _{CCL} | MAX | 40 | 40 | mA |
| I _{OH} | MAX | -1 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | ABT |
|------------------|-------|--------|------------|----------|-----|
| t _{PLH} | A | Y | MAX | 6 | 5.5 |
| | | | | 7.8 | 5.1 |
| t _{PHL} | A | Y | MAX | 10.7 | 6.7 |
| | | | | 12.9 | 7.8 |
| t _{PHZ} | OE | Y | MAX | 13 | 7.2 |
| | | | | 10 | 7.5 |

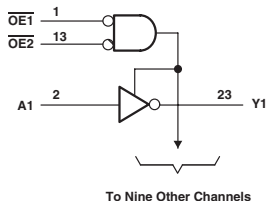
UNIT: ns

2828

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING

- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2828)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|------------------|------------|----------|------|
| I _{CCZ} | MAX | 6 | mA |
| I _{CCL} | MAX | 40 | mA |
| I _{OH} | MAX | -1 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

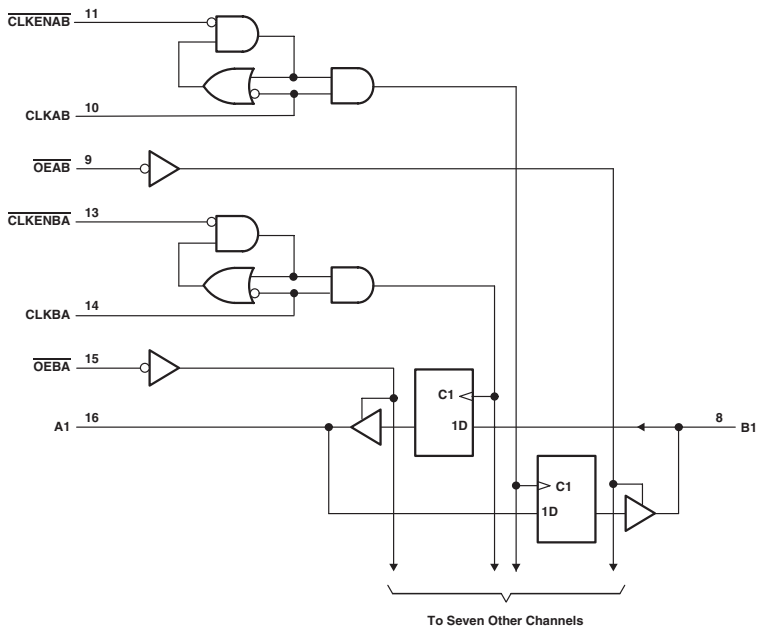
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|------------------|-----------------|--------|------------|----------|
| T _{PLH} | A | Y | MAX | 6.6 |
| T _{PHL} | | | | 5 |
| T _{PZH} | \overline{OE} | Y | MAX | 9 |
| T _{PZL} | | | | 11.5 |
| T _{PHZ} | \overline{OE} | Y | MAX | 10.8 |
| T _{PLZ} | | | | 8.7 |

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

| INPUTS | | | | OUTPUT B |
|---------|--------|------|---|----------------|
| CLKENAB | CLKAB | OEAB | A | |
| H | X | L | X | B ₀ |
| X | H or L | L | X | B ₀ |
| L | ↑ | L | L | L |
| L | ↑ | L | H | H |
| X | X | H | X | Z |

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MAX or MIN | SN74 BCT | ABT | LVTH 3V | LVC 3V | UNIT |
|-----------------|---|------------|-------------|-----|------------|-----------|------|
| I _{CC} | | MAX | 55 | 35 | 5 | 0.01 | mA |
| I _{OH} | A | MAX | -3 | -32 | -32 | -24 | mA |
| | B | | -15 | -32 | -32 | -24 | mA |
| I _{OL} | A | MAX | 24 | 64 | 64 | 24 | mA |
| | B | | 64 | 64 | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

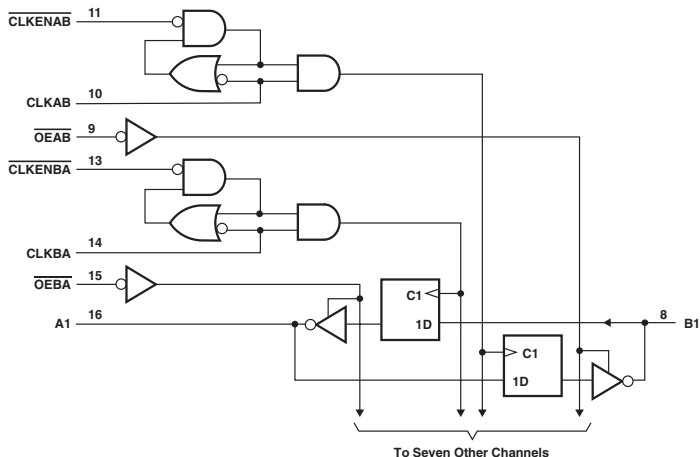
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | ABT | LVTH 3V | LVC 3V |
|------------------|-------------------------|--------|------------|-------------|-----|------------|-----------|
| t _{max} | | | MIN | 125 | 150 | 150 | 150 |
| t _w | CLK "H" | | MIN | 4 | 3.3 | 3.3 | 3.3 |
| | CLK "L" | | | 4 | 3.3 | 3.3 | 3.3 |
| t _{su} | A or B before CLK High | | MIN | 2.5 | 2.5 | 1.5 | 1.3 |
| | A or B before CLK Low | | | 2.5 | 2.5 | 1.5 | - |
| | CLKENAB or CLKENBA High | | | 2 | 3 | 1.5 | 1.1 |
| | CLKENAB or CLKENBA Low | | | 2 | 3 | 1.9 | - |
| t _h | A or B after CLK | | MIN | 1.5 | 1.5 | 1 | 1.1 |
| | CLKENAB or CLKENBA | | | 2.5 | 2 | 1.2 | 1.1 |
| t _{PLH} | CLKBA | A, B | MAX | 9 | 5.9 | 4.6 | 8.2 |
| t _{PHL} | CLKAB | | | 10.5 | 6.3 | 4.6 | 8.2 |
| t _{PZH} | OEBA | A, B | MAX | 8.2 | 5.6 | 4.6 | 7.8 |
| t _{PZL} | OEAB | | | 12.9 | 6.6 | 4.6 | 7.8 |
| t _{PHZ} | OEBA | A, B | MAX | 8.4 | 6.4 | 5.4 | 7.8 |
| t _{PLZ} | OEAB | | | 7 | 6.2 | 5.1 | 7.8 |

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

| INPUTS | | | | OUTPUT B |
|--------|-------|------|---|----------------|
| OEAB | CLKAB | OEBA | A | B |
| H | ↑ | L | X | A ₀ |
| L | ↑ | L | L | H |
| L | ↑ | L | H | L |
| X | X | H | X | Z |

† A-to-B data flow is shown; B-to-A data flow is similar but uses

CEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were

established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|-----------------|------------|----------|------|
| I _{CC} | MAX | 55 | mA |
| I _{OH} | A | -3 | mA |
| | B | -15 | mA |
| I _{OL} | A | 24 | mA |
| | B | 64 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|------------------|-------------------------|--------|------------|----------|
| f _{max} | | | MIN | 110 |
| t _v | CLK "H" | | MIN | 4.5 |
| | CLK "L" | | | |
| t _{su} | A or B High | | MIN | 2.5 |
| | A or B Low | | | |
| | CLKENAB or CLKENBA High | | | |
| | CLKENAB or CLKENBA Low | | | |
| t _h | A or B | | MIN | 1.5 |
| | CLKENAB or CLKENBA | | | |
| t _{PLH} | CLKBA | A, B | MAX | 9.5 |
| t _{PHL} | CLKAB | A, B | MAX | 10.2 |
| t _{PZH} | OEBA | A, B | MAX | 8.8 |
| t _{PZL} | OEAB | A, B | MAX | 14 |
| t _{PHZ} | OEBA | A, B | MAX | 9.1 |
| t _{PLZ} | OEAB | A, B | MAX | 7.6 |

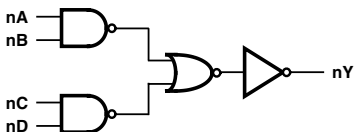
UNIT f_{max}: MHz other: ns

4002

DUAL 4-INPUT POSITIVE-NOR GATES

$$\bullet Y = \overline{A + B + C + D}$$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|---|---|---|--------|
| A | B | C | D | Y |
| L | L | L | L | H |
| H | X | X | X | L |
| X | H | X | X | L |
| X | X | H | X | L |
| X | X | X | H | L |

NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Irrelevant

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|---------|---------|------|
| I _{CC} | MAX | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

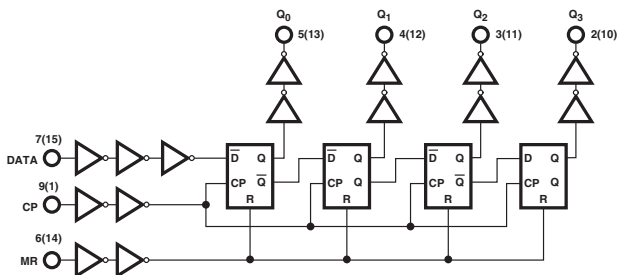
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC |
|------------------|------------|--------|------------|---------|---------|
| t _{PLH} | A, B, C, D | Y | MAX | 28 | 30 |
| t _{PHL} | | | MAX | 28 | 30 |

UNIT:ns

DUAL 4-STAGE STATIC SHIFT REGISTER

Logic Diagram



FUNCTION TABLE

| CP | INPUTS | | OUTPUT | | | |
|----|--------|---|----------------|----------------|----------------|----------------|
| | D | R | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| ↑ | I | L | L | q ₀ | q ₁ | q ₂ |
| ↑ | h | L | H | q ₀ | q ₁ | q ₂ |
| ↓ | X | L | q ₀ | q ₁ | q ₂ | q ₃ |
| X | X | H | L | L | L | L |

NOTES:

- H = High Voltage Level
h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
X = Don't Care.
↑ = Low to High Clock Transition
↓ = High to Low Clock Transition
q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------------|------------|---------|------|
| I _{CC} | MAX | 0.16 | mA |
| I _{OH} | MAX | -4 | mA |
| I _{OL} | MAX | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

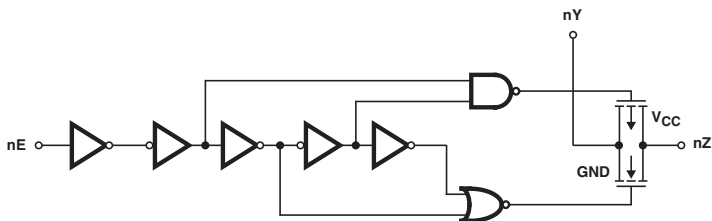
| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|------------------|---------------|--------------------------------|------------|---------|
| t _{max} | | | MIN | 20 |
| t _v | Clock | | MIN | 24 |
| | MR | | | 45 |
| t _{SUL} | Data-In to CP | | MIN | 18 |
| t _{SUH} | Data-In to CP | | MIN | 18 |
| t _H | Data-In to CP | | MIN | 0 |
| t _{PLH} | Clock | Q _n | MAX | 54 |
| t _{PHL} | | | | 54 |
| t _{PLH} | MR | Q _n (Clock High) | MAX | 83 |
| t _{PHL} | | | | 83 |
| t _{PLH} | MR | Q _n (Clock Low) | MAX | 98 |
| t _{PHL} | | | | 98 |

UNIT f_{max} : MHz other : ns

4016

QUAD BILATERAL SWITCH

Logic Diagram



FUNCTION TABLE

| INPUT nE | SWITCH |
|-------------|--------|
| L | OFF |
| H | ON |

NOTES:

H = High Level Voltage
L = Low Level Voltage

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

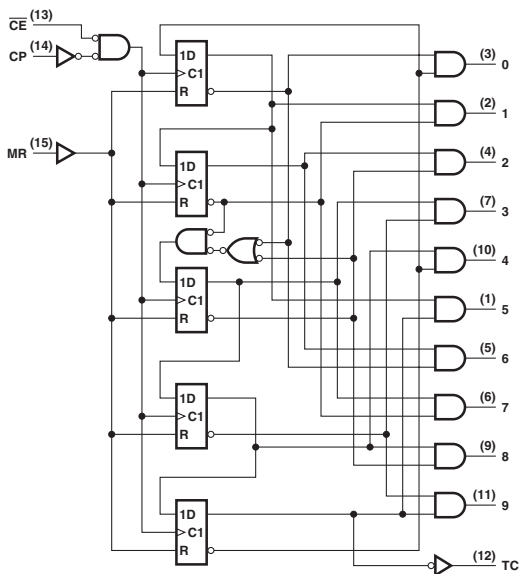
| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------------|------------|------------|------|
| I _{CC} | MAX | 0.04 | mA |
| R _{ON} | MAX | 480 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|------------------|-----------|------------|------------|------------|
| t _{PLH} | Switch In | Switch Out | MAX | 18 |
| | | | | 18 |
| t _{PZH} | En | Z | MAX | 57 |
| | | | | 57 |
| t _{PHZ} | En | Z | MAX | 44 |
| | | | | 44 |

UNIT:ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT STATE† |
|--------|----|----|----------------------|
| CP | CE | MR | |
| L | X | L | No Change |
| X | H | L | No Change |
| X | X | H | "0" = H, "1"-"9" = L |
| ↑ | L | L | Increments Counter |
| ↓ | X | L | No Change |
| X | ↑ | L | No Change |
| H | ↓ | L | Increments Counter |

NOTES:

- H = High Level
 L = Low Level
 ↑ = High to Low Transition
 ↓ = Low to High Transition
 X = Don't Care
 † If $n < 5$ TC = H, Otherwise = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|---------|---------|------|
| I _{CC} | MAX | 0.08 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC |
|------------------|--------------|--------|------------|---------|---------|
| f _{max} | | | MIN | 25 | 20 |
| t _w | CP | | MIN | 20 | 24 |
| | MR | | | 20 | 24 |
| t _{su} | CE to CP | | MIN | 13 | 22 |
| | CLK Inactive | | | 13 | - |
| t _h | CE to CP | | MIN | 5 | 0 |
| t _{PLH} | CP | 0 to 9 | MAX | 58 | 69 |
| t _{PHL} | | | | 58 | 69 |
| t _{PLH} | CE | 0 to 9 | MAX | 63 | 75 |
| t _{PHL} | | | | 63 | 75 |
| t _{PLH} | MR | 0 to 9 | MAX | 58 | 69 |
| t _{PHL} | | | | 58 | 69 |
| t _{PLH} | MR | TC | MAX | - | 69 |
| t _{PHL} | | | | 58 | 69 |

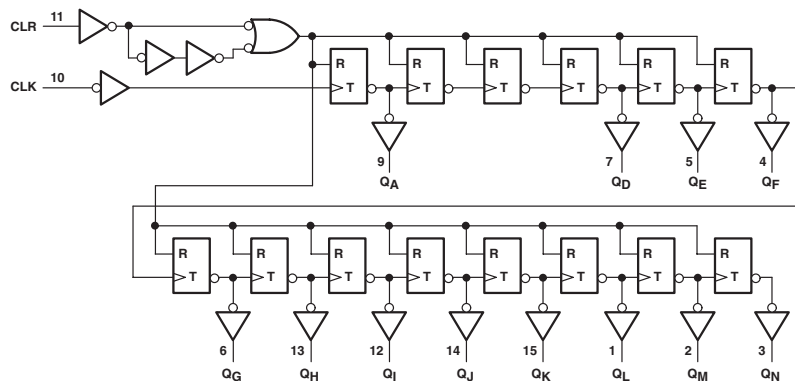
UNIT f_{max} : MHz, other : ns

4020

14-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4020
- V_{CC} : 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

| CLK | CLR | OUTPUT |
|-----|-----|-----------------------|
| ↑ | L | No Change |
| ↓ | L | Advance to Next State |
| X | H | All Outputs Are Low |

NOTE: H = High Voltage Level, L = Low Voltage Level,
 X = Don't Care, = ↑ Transition from Low to High Level,
 ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|---------|----------|------|
| I_{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 4 | 4 | 4 | mA |

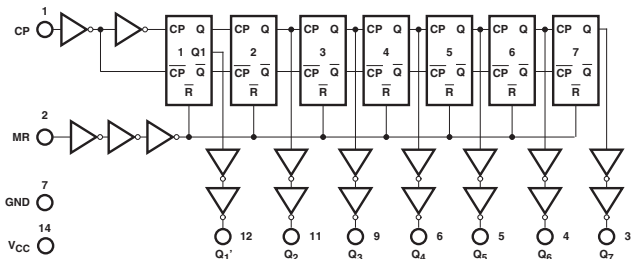
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|-----------|----------------|---------------------------|------------|---------|---------|----------|
| f_{max} | | | MIN | 22 | 20 | 16 |
| t_w | CLK (CD74: CP) | | MIN | 23 | 24 | 30 |
| | CLR high | | MIN | 18 | 24 | 30 |
| t_{su} | CLK (CD74: CP) | CLR inactive before CLK ↓ | MIN | 15 | - | - |
| t_{PLH} | CLK (CD74: CP) | Q_A (CD74: Q_1) | MAX | 38 | 42 | 60 |
| t_{PHL} | | | MAX | 38 | 42 | 60 |
| t_{PHL} | CLR (CD74: CP) | Any | MAX | 35 | 51 | 60 |

UNIT f_{max} : MHz other: ns

7-STAGE BINARY COUNTERS

Logic Diagram



FUNCTION TABLE (SN74)

| CLK | CLR | OUTPUT |
|-----|-----|-----------------------|
| ↑ | L | No Change |
| ↓ | L | Advance to Next State |
| X | H | All Outputs Are Low |

NOTE: H = High Voltage Level, L = Low Voltage Level,
 X = Don't Care, = ↑ Transition from Low to High Level,
 ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|---------|----------|------|
| I_{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|-----------|--------------------|---------|------------|---------|---------|----------|
| f_{max} | | | MIN | 22 | 20 | 16 |
| t_w | CP (CLK) | | MIN | 23 | 24 | 30 |
| | MR (CLR H) | | | 20 | 24 | 30 |
| t_{su} | CLR iow before CLK | | MIN | 20 | - | - |
| t_{PLH} | CP (CLK) | Q1 (QA) | MAX | 30 | 42 | 60 |
| t_{PHL} | | | | 30 | 42 | 60 |
| t_{PLH} | MR (CLR) | any Q | MAX | - | 51 | 60 |
| t_{PHL} | | | | 33 | 51 | 60 |

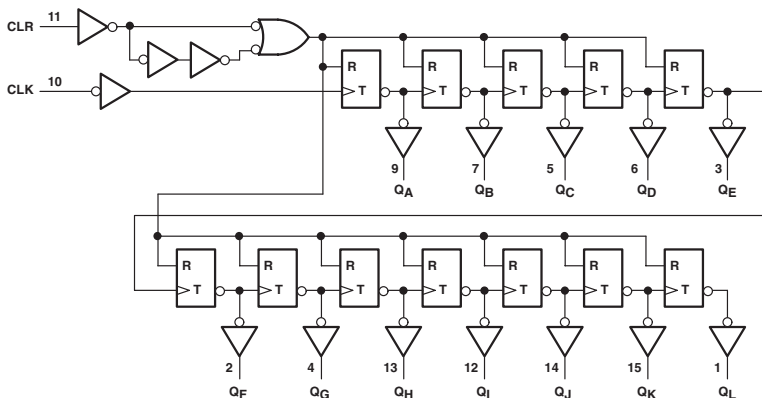
UNIT f_{max} : MHz, other : ns

4040

12-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- V_{CC} : 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE

| CLK | CLR | OUTPUT |
|-----|-----|-----------------------|
| ↑ | L | No Change |
| ↓ | L | Advance to Next State |
| X | H | All Outputs Are Low |

NOTE: H = High Voltage Level, L = Low Voltage Level,
 X = Don't Care, ↑ = Transition from Low to High Level,
 ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

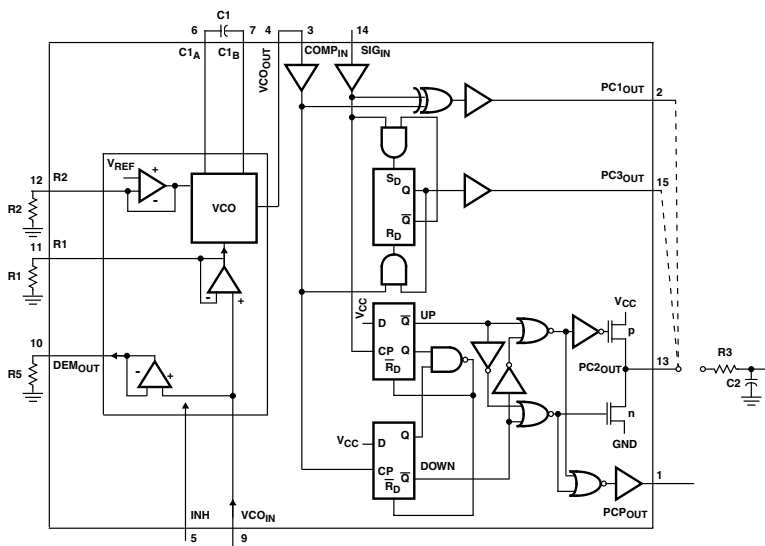
| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------|------------|---------|---------|----------|-------|-------|------|
| I_{CC} | MAX | 0.08 | 0.16 | 0.16 | - | 0.02 | mA |
| I_{OH} | MAX | -4 | -4 | -4 | -6 | -12 | mA |
| I_{OL} | MAX | 4 | 4 | 4 | 6 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|-----------|---------------|-----------------------------------|------------|---------|---------|----------|-------|-------|
| f_{max} | | | MIN | 22 | 20 | 16 | 50 | 80 |
| t_w | CLK (CP) | | MIN | 23 | 24 | 30 | 5 | 5 |
| | CLR (MR) high | | | 18 | 24 | 30 | 5 | 5 |
| t_{su} | CLK (CP) | CLR(MR) inactive before CLK(CP) ↓ | MIN | 15 | - | - | 5 | 5 |
| t_{PLH} | CLK (CP) | Q_A (Q1) | MAX | 38 | 42 | 60 | 17.5 | 10.5 |
| t_{PHL} | | | | 38 | 42 | 60 | 17.5 | 10.5 |
| t_{PHL} | CLR (MR) | Any | MAX | 35 | 51 | 60 | 18.5 | 12 |

UNIT f_{max} : MHz other: ns

Logic Diagram



Pin Descriptions

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|------------|---------------------|-------------------------------|
| 1 | PC _F OUT | Phase Comparator Pulse Output |
| 2 | PC ₁ OUT | Phase Comparator 1 Output |
| 3 | COMP _{IN} | Comparator Input |
| 4 | VCO _{OUT} | VCO Output |
| 5 | INH | Inhibit Input |
| 6 | C _{1A} | Capacitor C1 Connection A |
| 7 | C _{1B} | Capacitor C1 Connection B |
| 8 | GND | Ground (0V) |
| 9 | VCO _{IN} | VCO Input |
| 10 | DEM _{OUT} | Demodulator Output |
| 11 | R ₁ | Resistor R1 Connection |
| 12 | R ₂ | Resistor R2 Connection |
| 13 | PC ₂ OUT | Phase Comparator 2 Output |
| 14 | SIG _{IN} | Signal Input |
| 15 | PC ₃ OUT | Phase Comparator 3 Output |
| 16 | V _{CC} | Positive Supply Voltage |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{DH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

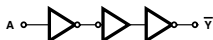
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|--------------------|--------------------|------------|---------|----------|
| t _{PLH} | SIG _{IN} | PC _{IOUT} | MAX | 60 | 68 |
| | COMP _{IN} | | | 60 | 68 |
| t _{PHL} | SIG _{IN} | PCP _{OUT} | MAX | 90 | 102 |
| | COMP _{IN} | | | 90 | 102 |
| t _{PLH} | SIG _{IN} | PC3 _{OUT} | MAX | 74 | 87 |
| | COMP _{IN} | | | 74 | 87 |
| t _{TLH} | A | \bar{Y} | MAX | 22 | 22 |
| | | | | 22 | 22 |
| t _{PZH} | SIG _{IN} | PC2 _{OUT} | MAX | 80 | 90 |
| | COMP _{IN} | | | 80 | 90 |
| t _{PZL} | SIG _{IN} | PC2 _{OUT} | MAX | 95 | 102 |
| | COMP _{IN} | | | 95 | 102 |

UNIT:ns

HEX INVERTING BUFFERS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.04 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

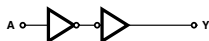
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|-----------|-------|------------|------------|---------|
| t_{PLH} | nA | $\bar{n}Y$ | MAX | 26 |
| t_{PHL} | | | | 26 |

UNIT:ns

HEX NON-INVERTING BUFFERS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

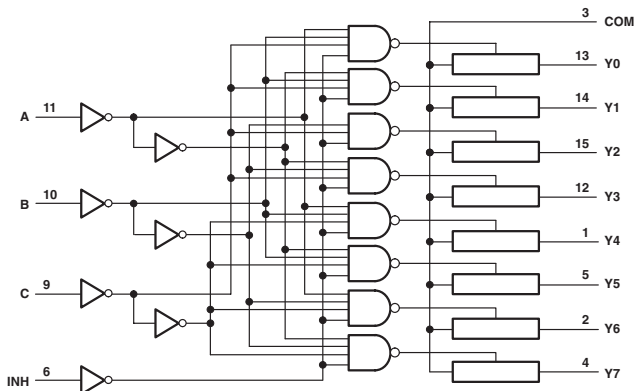
| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.04 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|-----------|-------|--------|------------|---------|
| t_{PLH} | nA | nY | MAX | 26 |
| t_{PHL} | | | | 26 |

UNIT:ns

Logic Diagram (SN74LV)

FUNCTION TABLE
(SN74)

| INPUTS | | | | ON CHANNEL |
|--------|---|---|---|------------|
| INH | C | B | A | |
| L | L | L | L | Y0 |
| L | L | L | H | Y1 |
| L | L | H | L | Y2 |
| L | L | H | H | Y3 |
| L | H | L | L | Y4 |
| L | H | L | H | Y5 |
| L | H | H | L | Y6 |
| L | H | H | H | Y7 |
| H | X | X | X | None |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

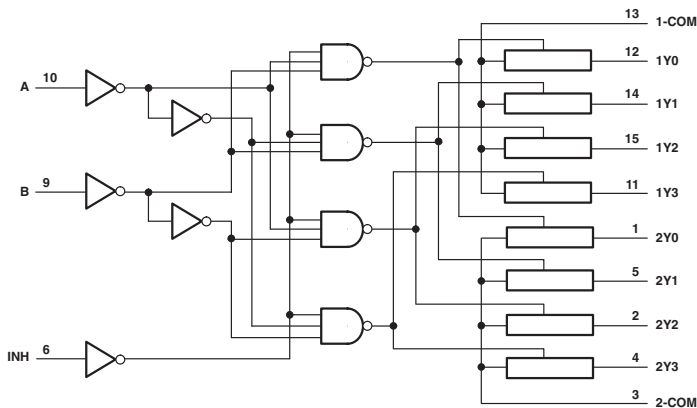
| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------|------------|---------|----------|-------|-------|----------|
| I_{CC} | MAX | 0.16 | 0.16 | - | 0.02 | mA |
| R_{ON} | MAX | 180 | 180 | 190 | 100 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|-----------|----------------|----------------|------------|---------|----------|-------|-------|
| t_{PLH} | COM or Yn (An) | Yn (An) or COM | MAX | 18 | 18 | 12 | 8 |
| t_{PHL} | | | | 18 | 18 | 12 | 8 |
| t_{PZH} | INH | COM or Yn (An) | MAX | 68 | 83 | 25 | 18 |
| t_{PZL} | | | | 68 | 83 | 25 | 18 |
| t_{PHZ} | INH | COM or Yn (An) | MAX | 68 | 68 | 25 | 18 |
| t_{PLZ} | | | | 68 | 68 | 25 | 18 |

UNIT: ns

Logic Diagram (SN74LV)

FUNCTION TABLE
(SN74)

| INPUTS | | | ON CHANNEL |
|--------|---|---|------------|
| INH | B | A | |
| L | L | L | 1Y0, 2Y0 |
| L | L | H | 1Y1, 2Y1 |
| L | H | L | 1Y2, 2Y2 |
| L | H | H | 1Y3, 2Y3 |
| H | X | X | None |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------------|------------|---------|----------|-------|-------|------|
| I _{CC} | MAX | 0.16 | 0.16 | - | 0.02 | mA |
| R _{ON} | MAX | 180 | 180 | 190 | 100 | Ω |

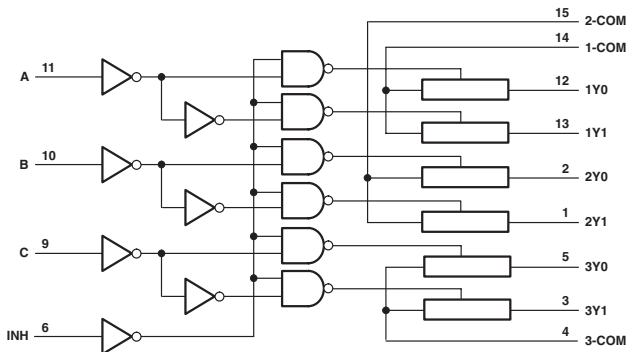
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|------------------|----------------------------|----------------------------|------------|---------|----------|-------|-------|
| t _{PLH} | COM or Y _n (An) | Y _n (An) or COM | MAX | 18 | 18 | 12 | 8 |
| | | | | 18 | 18 | 12 | 8 |
| t _{PLZ} | INH | COM or Y _n (An) | MAX | 98 | 105 | 25 | 18 |
| | | | | 98 | 105 | 25 | 18 |
| t _{PHZ} | INH | COM or Y _n (An) | MAX | 75 | 75 | 25 | 18 |
| | | | | 75 | 75 | 25 | 18 |

UNIT: ns

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

Logic Diagram (SN74LV)

FUNCTION TABLE
(SN74)

| INPUTS | | | | ON CHANNEL |
|--------|---|---|---|---------------|
| INH | C | B | A | |
| L | L | L | L | 1Y0, 2Y0, 3Y0 |
| L | L | L | H | 1Y1, 2Y0, 3Y0 |
| L | L | H | L | 1Y0, 2Y1, 3Y0 |
| L | L | H | H | 1Y1, 2Y1, 3Y0 |
| L | H | L | L | 1Y0, 2Y0, 3Y1 |
| L | H | L | H | 1Y1, 2Y0, 3Y1 |
| L | H | H | L | 1Y0, 2Y1, 3Y1 |
| L | H | H | H | 1Y1, 2Y1, 3Y1 |
| H | X | X | X | None |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

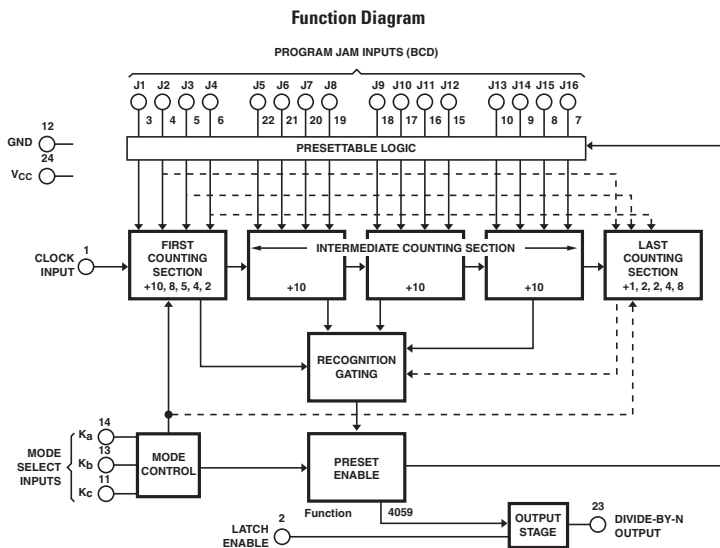
| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V | UNIT |
|-----------|------------|------------|-------------|----------|----------|----------|
| I_{CC} | MAX | 0.16 | 0.16 | - | 0.02 | mA |
| R_{ON} | MAX | 180 | 180 | 190 | 100 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT | LV 3V | LV 5V |
|-----------|---------------------------|---------------------------|------------|------------|-------------|----------|----------|
| t_{PLH} | COM or Yn (An, Bn, Cn) | Yn (An, Bn, Cn) or COM | MAX | 18 | 18 | 12 | 8 |
| t_{PHL} | | | | 18 | 18 | 12 | 8 |
| t_{PZH} | INH | COM or Yn (An, Bn, Cn) | MAX | 66 | 72 | 25 | 18 |
| t_{PZL} | | | | 66 | 72 | 25 | 18 |
| t_{PHZ} | INH | COM or Yn (An, Bn, Cn) | MAX | 63 | 66 | 25 | 18 |
| t_{PLZ} | | | | 63 | 66 | 25 | 18 |

UNIT: ns

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER



FUNCTION TABLE

| MODE | SELECT | INPUT |
|------|--------|-------|
| Ka | Kb | Kc |
| H | H | H |
| L | H | H |
| H | L | H |
| L | L | H |
| H | H | L |
| X | L | L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.16 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

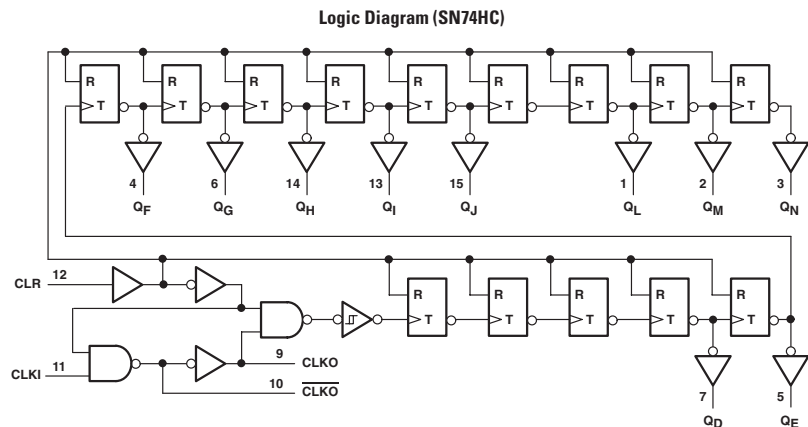
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|-----------|--------------|--------|------------|---------|
| f_{max} | CP | | MIN | 18 |
| t_w | CP | | MIN | 27 |
| t_{su} | Kb, Kc to CP | | MIN | 22 |
| t_{PLH} | CP | Q | MAX | 60 |
| t_{PHL} | | | | 60 |
| t_{PLH} | LE | Q | MAX | 53 |
| t_{PHL} | | | | 53 |

UNIT f_{max} : MHz other: ns

ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

- Same Pinouts as CMOS4060
- Allow Design of Either RC or Crystal Oscillator Circuits
- V_{CC} : 2V to 6V



FUNCTION TABLE (SN74)

| INPUTS | | OUTPUTS | | |
|--------|-----|----------------------------------|------|------|
| CLKI | CLR | Q _D to Q _N | CLKO | CLKO |
| T | L | No Change | ↑ | ↓ |
| ↓ | L | Advance to Next State | ↓ | ↑ |
| X | H | All Outputs are Low | L | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|---------|----------|------|
| I _{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

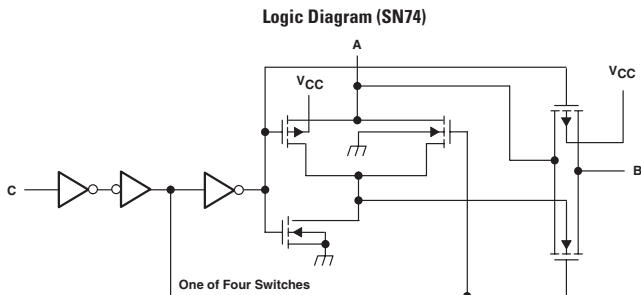
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|------------------|---------------------------|---------------------|------------|---------|---------|----------|
| f _{max} | | | MIN | 22 | 20 | 20 |
| t _w | CLKI (φ) | | MIN | 23 | 24 | 24 |
| | CLR high (MR) | | | 23 | 24 | 38 |
| t _{su} | CLR inactive before CLK ↓ | | MIN | 40 | - | - |
| t _{PLH} | CLKI (φ) | Q _D (Q4) | MAX | 123 | 90 | 100 |
| t _{PHL} | | | | 123 | 90 | 100 |
| t _{PHL} | CLR (MR) | Any | MAX | 35 | 53 | 66 |

UNIT f_{max}: MHz other: ns

4066

QUADRUPLE BILATERAL SWITCHES

- Same Pinouts as CMOS4016, 4066
- Low On-State Impedance: 50-Ω TYP at $V_{CC} = 6V$
- Individual Switch Controls
- Extremely Low Input Current
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches



FUNCTION TABLE (SN74)

| INPUT (C) | SWITCH |
|-----------|--------|
| L | OFF |
| H | ON |

NOTE:

H = High Level

L = Low Level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | AHC | LV 3V | LV 5V | UNIT |
|-----------|------------|---------|---------|----------|------|-------|-------|------|
| I_{CC} | MAX | 0.02 | 0.04 | 0.04 | 0.02 | - | 0.02 | mA |
| R_{ON} | MAX | 106 | 128 | 128 | 100 | 190 | 100 | Ω |

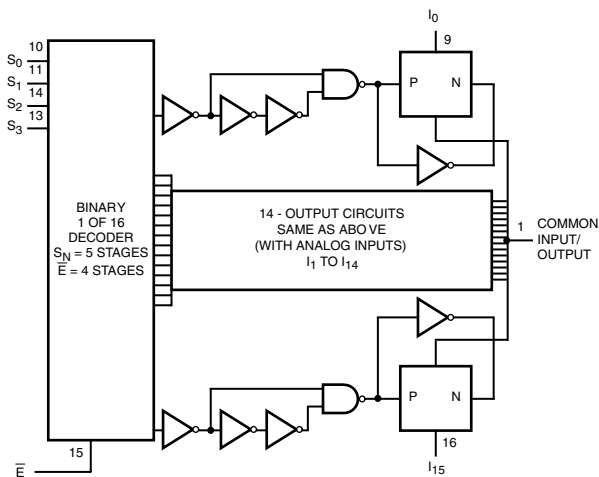
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | AHC | LV 3V | LV 5V |
|-----------|-----------------|-----------------|------------|---------|---------|----------|-----|-------|-------|
| t_{PLH} | A or B (Y or Z) | B or A (Z or Y) | MAX | 15 | 18 | 18 | 8 | 12 | 8 |
| t_{PHL} | | | | 15 | 18 | 18 | 8 | 12 | 8 |
| t_{PZH} | C (E) | A or B (Y or Z) | MAX | 45 | 30 | 36 | 16 | 22 | 16 |
| t_{PZL} | | | | 45 | 30 | 36 | 16 | 22 | 16 |
| t_{PHZ} | C (E) | A or B (Y or Z) | MAX | 50 | 45 | 53 | 16 | 22 | 16 |
| t_{PLZ} | | | | 50 | 45 | 53 | 16 | 22 | 16 |

UNIT: ns

16-CHANNEL ANALOG MULTIPLEXER/DEMULPLEXER

Function Diagram



FUNCTION TABLE

| S0 | S1 | S2 | S3 | \bar{E} | SELECTED CHANNEL |
|----|----|----|----|-----------|------------------|
| X | X | X | X | X | None |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 2 |
| 1 | 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 9 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 1 | 1 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 0 | 12 |
| 1 | 0 | 1 | 1 | 0 | 13 |
| 0 | 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 0 | 15 |

NOTES:

H = High Level
L = Low Level
X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|----------|----------|
| I_{CC} | MAX | 0.16 | 0.16 | mA |
| R_{ON} | MAX | 240 | 240 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|-----------|-----------|------------|------------|---------|----------|
| t_{PLH} | Switch In | COMMON I/O | MAX | 22 | 22 |
| t_{PHL} | | | | 22 | 22 |
| t_{PZH} | \bar{E} | COMMON I/O | MAX | 83 | 90 |
| t_{PZL} | | | | 83 | 90 |
| t_{PHZ} | \bar{E} | COMMON I/O | MAX | 83 | 83 |
| t_{PLZ} | | | | 83 | 83 |
| t_{PZH} | S_n | COMMON I/O | MAX | 90 | 90 |
| t_{PZL} | | | | 90 | 90 |
| t_{PHZ} | S_n | COMMON I/O | MAX | 87 | 87 |
| t_{PLZ} | | | | 87 | 87 |

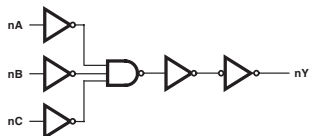
UNIT:ns

4075

TRIPLE 3-INPUT OR GATES

● $Y = A + B + C$

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| L | L | L | L |
| H | X | X | H |
| X | H | X | H |
| X | X | H | H |

NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

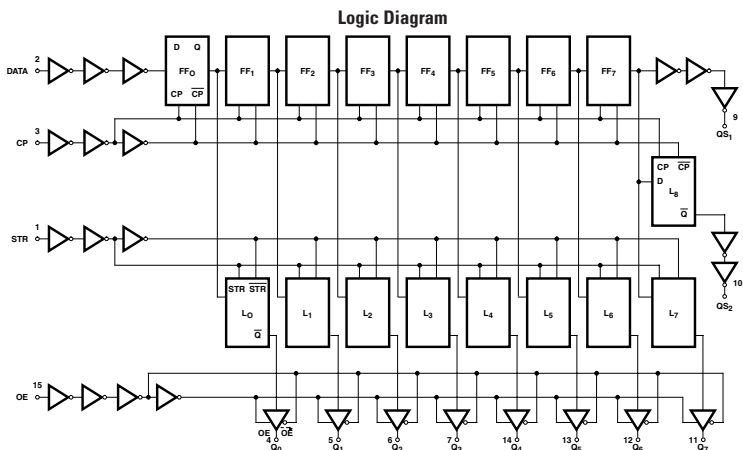
| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|------------|------------|-------------|------|
| I_{CC} | MAX | 0.02 | 0.04 | 0.04 | mA |
| I_{OH} | MAX | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 4 | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|-----------|-----------|--------|------------|------------|------------|-------------|
| t_{PLH} | A, B or C | Y | MAX | 25 | 30 | 36 |
| t_{PHL} | A, B or C | Y | MAX | 25 | 30 | 36 |

UNIT:ns

8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE

**FUNCTION TABLE**

| INPUTS | | | PARALLEL OUTPUT | | SERIAL OUTPUT | | |
|--------|----|-----|-----------------|----------------|------------------|-------------------|-----------------|
| CP | OE | STR | D | Q ₀ | Q _n | OS ₁ † | OS ₂ |
| ↑ | L | X | X | Z | Z | Q ₆ | NC |
| ↓ | L | X | X | Z | Z | NC | Q ₇ |
| ↑ | H | L | X | NC | NC | Q ₆ | NC |
| ↑ | H | H | L | L | Q _{n-1} | Q ₆ | NC |
| ↑ | H | H | H | H | Q _{n-1} | Q ₆ | NC |
| ↓ | H | H | H | NC | NC | NC | Q ₇ |

NOTES:

†: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,

NC = No charge, Z = High Impedance Off-state,

↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

‡: At the positive clock edge the information in the seventh register stage is transferred to the 8th register stage and OS₁ output.**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OL} | MAX | 4 | 4 | mA |
| I _{OH} | MAX | -4 | -4 | mA |

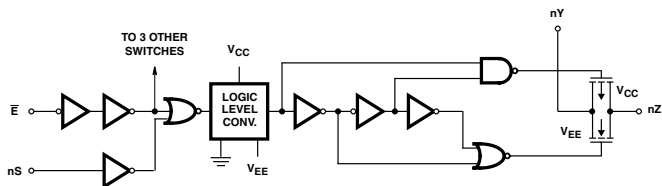
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|-------|----------------|------------|---------|----------|
| t _W | CP | | MIN | 24 | 24 |
| t _{WH} | STR | | MIN | 24 | 24 |
| t _{SU} | Data | | MIN | 15 | 15 |
| | STR | | MIN | 30 | 30 |
| t _H | Data | | MIN | 3 | 4 |
| | STR | | MIN | 0 | 0 |
| t _{PLH} | CP | QS1 | MAX | 45 | - |
| t _{PHL} | | | | 45 | - |
| t _{PLH} | CP | QS2 | MAX | 41 | - |
| t _{PHL} | | | | 41 | - |
| t _{PLH} | CP | Q _n | MAX | 59 | - |
| t _{PHL} | | | | 59 | - |
| t _{PLH} | STR | Q _n | MAX | 54 | - |
| t _{PHL} | | | | 54 | - |
| t _{PLZ} | OE | Q _n | MAX | 53 | - |
| t _{PLZ} | | | | 53 | - |
| t _{PLZ} | OE | Q _n | MAX | 38 | - |
| t _{PHZ} | | | | 38 | - |

UNIT:ns

QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

Logic Diagram



FUNCTION TABLE

| INPUTS | | SWITCH |
|-----------|---|--------|
| \bar{E} | S | |
| L | L | OFF |
| L | H | ON |
| H | X | OFF |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|----------|----------|
| I_{CC} | MAX | 0.32 | 0.32 | mA |
| R_{ON} | MAX | 270 | 270 | Ω |

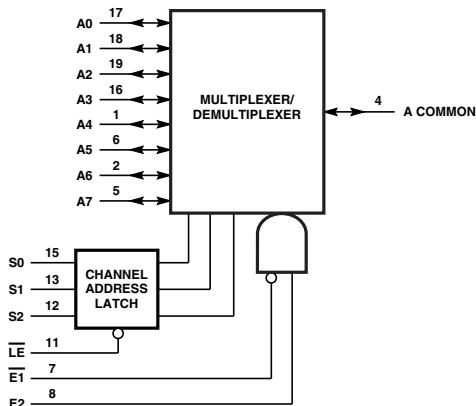
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|-----------|-----------|------------|------------|---------|----------|
| t_{PLH} | Switch in | Switch out | MAX | 18 | 18 |
| t_{PHL} | | | | 18 | 18 |
| t_{PZH} | \bar{E} | Z | MAX | 62 | 66 |
| t_{PZL} | | | | 62 | 85 |
| t_{PLZ} | \bar{E} | Z | MAX | 62 | 75 |
| t_{PHZ} | | | | 62 | - |
| t_{PZH} | nS | Z | MAX | 53 | 60 |
| t_{PZL} | | | | 53 | 75 |
| t_{PLZ} | nS | Z | MAX | 53 | - |
| t_{PHZ} | | | | 53 | 66 |

UNIT:ns

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | "ON"† SWITCHES $\overline{LE} = H$ |
|-----------------|----|----|----|----|--|
| $\overline{E1}$ | E2 | S2 | S1 | S0 | |
| L | H | L | L | L | A ₀ |
| L | H | L | L | H | A ₁ |
| L | H | L | H | L | A ₂ |
| L | H | L | H | H | A ₃ |
| L | H | H | L | L | A ₄ |
| L | H | H | L | H | A ₅ |
| L | H | H | H | L | A ₆ |
| L | H | H | H | H | A ₇ |
| H | L | X | X | X | None |

NOTES:

† When LE is low S0-S2 data are latched and switches cannot change state.

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

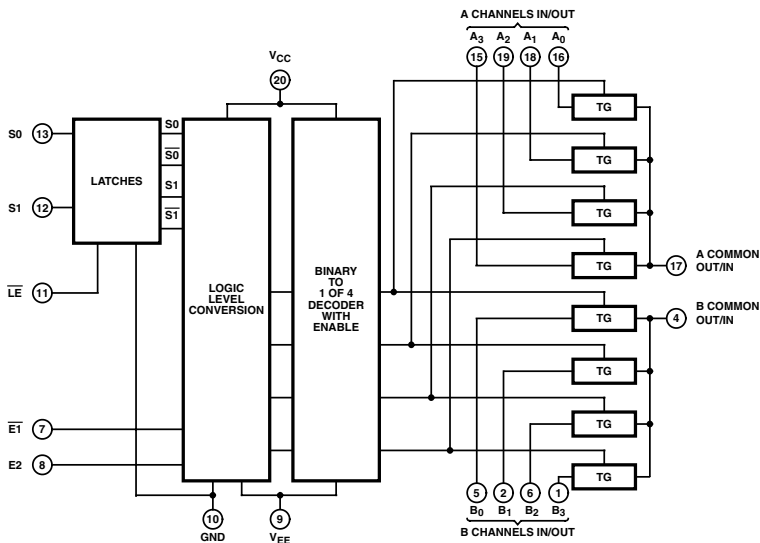
| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 0.32 | 0.32 | mA |
| R _{ON} | MAX | 240 | 240 | Ω |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|---------------------------------------|-----------------|------------|------------|-------------|
| t _V | \overline{LE} | | MIN | 30 | 28 |
| t _{su} | S _n to \overline{LE} | | MAX | 18 | 18 |
| t _h | S _n to \overline{LE} | | MIN | 5 | 5 |
| t _{PLH} | Switch In | Switch Out | MAX | 11 | 11 |
| t _{PHL} | | | | 11 | 11 |
| t _{PZH} | $\overline{E1}$, E2, \overline{LE} | V _{os} | MAX | 90 | 113 |
| t _{PZL} | | | | 90 | 113 |
| t _{FZH} | S _n | V _{os} | MAX | 90 | 113 |
| t _{FZL} | | | | 90 | 113 |
| t _{PLZ} | $\overline{E1}$ | V _{os} | MAX | 75 | 83 |
| t _{PHZ} | | | | 75 | 83 |
| t _{PLZ} | E2 | V _{os} | MAX | 75 | 90 |
| t _{PHZ} | | | | 75 | 90 |
| t _{PLZ} | \overline{LE} | V _{os} | MAX | 83 | 90 |
| t _{PHZ} | | | | 83 | 90 |
| t _{PHZ} | S _n | V _{os} | MAX | 83 | 98 |
| t _{PLZ} | | | | 83 | 98 |

UNIT:ns

Function Diagram



FUNCTION TABLE

| INPUTS | | | | "ON"† SWITCHES LE = H |
|--------|----|----|----|---------------------------------|
| E1 | E2 | S1 | S0 | |
| L | H | L | L | A ₀ , B ₀ |
| L | H | L | H | A ₁ , B ₁ |
| L | H | H | L | A ₂ , B ₂ |
| L | H | H | H | A ₃ , B ₃ |
| H | L | X | X | None |

NOTES:
 † When LE is low S0-S2 data are latched and switches cannot change state.
 H = High Voltage Level, L = Low Voltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------------|------------|---------|------|
| I _{CC} | MAX | 0.32 | mA |
| R _{ON} | MAX | 240 | Ω |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|------------------|----------------------|-----------------|------------|---------|
| t _w | LE | | MIN | 30 |
| t _{su} | S _n to LE | | MIN | - |
| t _h | S _n to LE | | MIN | 5 |
| t _{PLH} | Switch In | Switch Out | MAX | 11 |
| t _{PHL} | | | | 11 |
| t _{PZH} | E1, E2, LE | V _{os} | MAX | 105 |
| t _{PZL} | | | | 105 |
| t _{PZH} | S _n | V _{os} | MAX | 113 |
| t _{PZL} | | | | 113 |
| t _{PLZ} | E1, E2, LE | V _{os} | MAX | 83 |
| t _{PHZ} | | | | 83 |

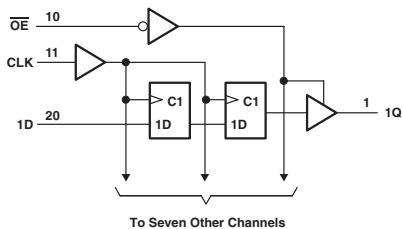
UNIT:ns

4374

OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|-----|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

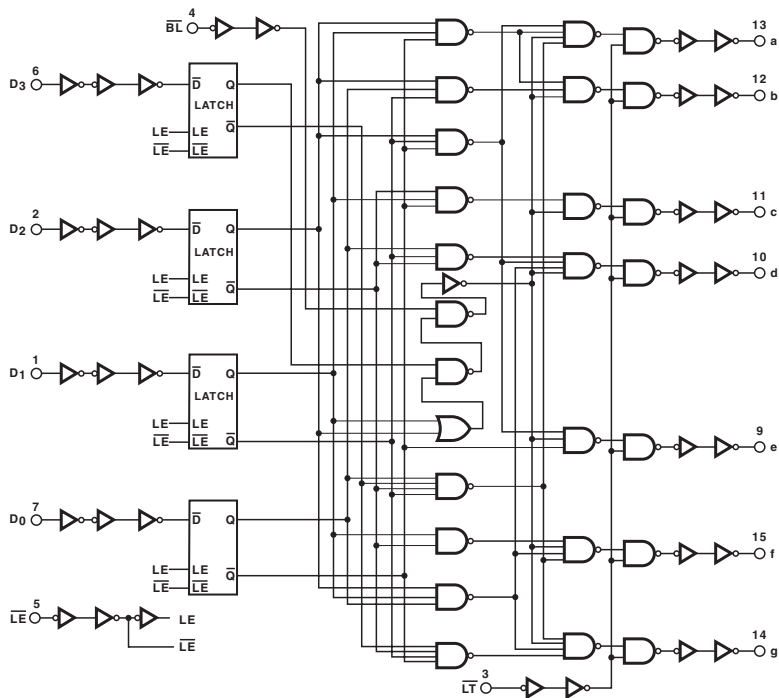
| PARAMETER | MAX or MIN | AS | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 150 | mA |
| I_{OH} | MAX | -15 | mA |
| I_{OL} | MAX | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AS |
|-----------|-----------------|--------|------------|-----|
| f_{max} | | | MIN | 125 |
| t_w | | | MIN | 4 |
| t_{su} | | | MIN | 4 |
| t_h | | | MIN | 1 |
| t_{PLH} | CLK | Q | MAX | 8 |
| t_{PHL} | | | | 8 |
| t_{PZH} | \overline{OE} | Q | MAX | 6 |
| t_{PZL} | | | | 8 |
| t_{PHZ} | \overline{OE} | Q | MAX | 6.5 |
| t_{PLZ} | | | | 7 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| \overline{LE} | \overline{BL} | \overline{LT} | D ₃ | D ₂ | D ₁ | D ₀ | a | b | c | d | e | f | g | Display |
|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|---|---|---|---|---|---|---|---------|
| X | X | L | X | X | X | X | H | H | H | H | H | H | H | 8 |
| X | L | H | X | X | X | X | L | L | L | L | L | L | L | Blank |
| L | H | H | L | L | L | L | H | H | H | H | H | H | L | 0 |
| L | H | H | L | L | L | H | L | H | H | L | L | L | L | 1 |
| L | H | H | L | L | H | L | H | H | L | H | H | L | L | 2 |
| L | H | H | L | L | H | H | H | H | H | L | L | H | H | 3 |
| L | H | H | L | H | L | L | L | H | H | L | L | H | H | 4 |
| L | H | H | L | H | L | H | L | H | H | L | H | L | H | 5 |
| L | H | H | L | H | H | L | L | L | H | H | H | H | H | 6 |
| L | H | H | L | H | H | H | H | H | H | L | L | L | L | 7 |
| L | H | H | H | L | L | L | H | H | H | H | H | H | H | 8 |
| L | H | H | H | L | L | H | H | H | H | L | L | H | H | 9 |
| L | H | H | H | L | H | L | L | L | L | L | L | L | L | Blank |
| L | H | H | H | L | H | H | L | L | L | L | L | L | L | Blank |
| L | H | H | H | H | L | L | L | L | L | L | L | L | L | Blank |
| L | H | H | H | H | L | H | L | L | L | L | L | L | L | Blank |
| L | H | H | H | H | H | L | L | L | L | L | L | L | L | Blank |
| L | H | H | X | X | X | X | † | † | † | † | † | † | † | † |

X – Don't care

† Depends on BCD code previously applied when $\overline{LE} = L$.

NOTES: Display is blank for all illegal input codes (BCD > HLLH).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -7.4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

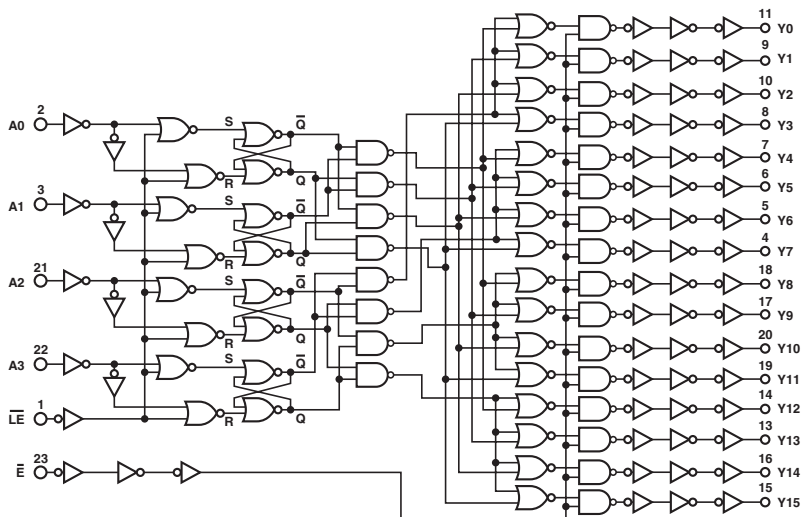
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|-----------------------|--------|------------|---------|----------|
| t _W | Latch Enable | | MIN | 24 | 24 |
| t _{su} | Dn to \overline{LE} | | MIN | 18 | 24 |
| t _h | Dn to \overline{LE} | | MIN | 3 | 5 |
| t _{PLH} | Dn | a to g | MAX | 90 | 90 |
| t _{PHL} | | | | 90 | 90 |
| t _{PLH} | \overline{LE} | a to g | MAX | 81 | 81 |
| t _{PHL} | | | | 81 | 81 |
| t _{PLH} | \overline{BL} | a to g | MAX | 66 | 66 |
| t _{PHL} | | | | 66 | 66 |
| t _{PLH} | \overline{LT} | a to g | MAX | 48 | 50 |
| t _{PHL} | | | | 48 | 50 |

UNIT:ns

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram

FUNCTION TABLE
($\overline{LE} = H$)

| \overline{E} | DECODER INPUTS | | | | ADDRESSED OUTPUT H |
|----------------|----------------|----|----|----|--------------------|
| | A3 | A2 | A1 | A0 | |
| L | L | L | L | L | Y0 |
| L | L | L | L | H | Y1 |
| L | L | L | H | L | Y2 |
| L | L | L | H | H | Y3 |
| L | L | H | L | L | Y4 |
| L | L | H | L | H | Y5 |
| L | L | H | H | L | Y6 |
| L | L | H | H | H | Y7 |
| L | H | L | L | L | Y8 |
| L | H | L | L | H | Y9 |
| L | H | L | H | L | Y10 |
| L | H | L | H | H | Y11 |
| L | H | H | L | L | Y12 |
| L | H | H | L | H | Y13 |
| L | H | H | H | L | Y14 |
| L | H | H | H | H | Y15 |
| H | X | X | X | X | All outputs = L |

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|---------|----------|------|
| I _{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | 4 | mA |

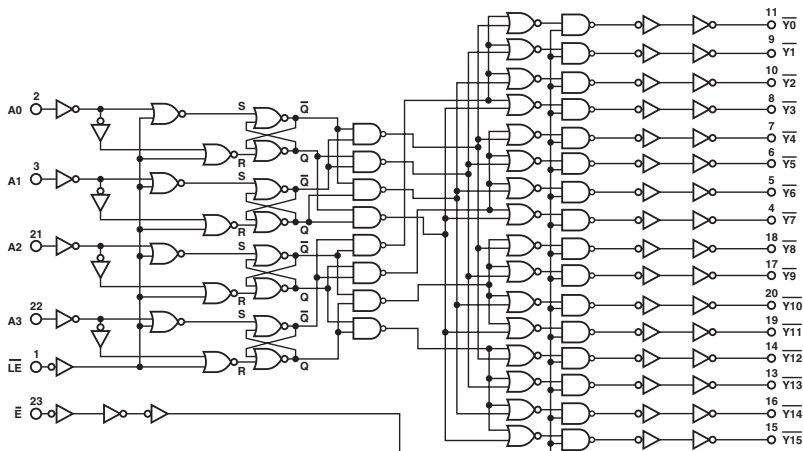
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|------------------|--------------------------|--------|------------|---------|---------|----------|
| t _{tr} | \overline{LE} (LE) | | MIN | 20 | 22 | 45 |
| t _{su} | \overline{LE} (LE) | | MIN | 25 | 30 | 30 |
| t _h | \overline{LE} (LE) | | MIN | 5 | 0 | 5 |
| t _{PLH} | A0, 1, 2, 3 (A, B, C, D) | Y | MAX | 58 | 83 | 83 |
| t _{PHL} | | | | 58 | 83 | 83 |
| t _{PLH} | \overline{LE} (LE) | Y | MAX | 58 | 68 | 75 |
| t _{PHL} | | | | 58 | 68 | 75 |
| t _{PLH} | \overline{E} (G) | Y | MAX | 44 | 53 | 60 |
| t _{PHL} | | | | 44 | 53 | 60 |

UNIT: ns

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram



FUNCTION TABLE

($\overline{LE} = H$)

| \overline{E} | DECODER INPUTS | | | | ADDRESSED OUTPUT L |
|----------------|----------------|----|----|----|-----------------------|
| | A3 | A2 | A1 | A0 | |
| L | L | L | L | L | Y0 |
| L | L | L | L | H | Y1 |
| L | L | L | H | L | Y2 |
| L | L | L | H | H | Y3 |
| L | L | H | L | L | Y4 |
| L | L | H | L | H | Y5 |
| L | L | H | H | L | Y6 |
| L | L | H | H | H | Y7 |
| L | H | L | L | L | Y8 |
| L | H | L | L | H | Y9 |
| L | H | L | H | L | Y10 |
| L | H | L | H | H | Y11 |
| L | H | H | L | L | Y12 |
| L | H | H | L | H | Y13 |
| L | H | H | H | L | Y14 |
| L | H | H | H | H | Y15 |
| H | X | X | X | X | All outputs = H |

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

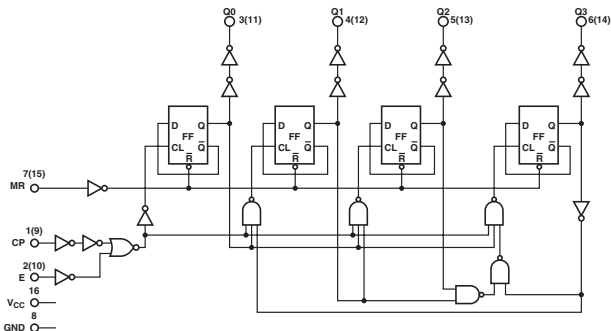
| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|---------|----------|------|
| I_{CC} | MAX | 0.08 | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -4 | -4 | -4 | mA |
| I_{OL} | MAX | 4 | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC | CD74 HCT |
|-----------|--------------------------------------|---------------------------------|------------|---------|---------|----------|
| t_{wv} | \overline{LE} (LE) | | MIN | 20 | 22 | 45 |
| t_{wv} | \overline{LE} (LE) | | MIN | 25 | 30 | 30 |
| t_b | \overline{LE} (LE) | | MIN | 5 | 0 | 5 |
| t_{PLH} | A0, 1, 2, 3 (A, B, C, D) | CD74HCT:Y (\overline{Y}) | MAX | 58 | 83 | 83 |
| t_{PHL} | | | | 58 | 83 | 83 |
| t_{PLH} | \overline{LE} (LE) | CD74HCT:Y (\overline{Y}) | MAX | 58 | 68 | 75 |
| t_{PHL} | | | | 58 | 68 | 75 |
| t_{PLH} | \overline{E} (\overline{G}) | CD74HCT:Y (\overline{Y}) | MAX | 44 | 53 | 60 |
| t_{PHL} | | | | 44 | 53 | 60 |

UNIT:ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT STATE |
|--------|---|----|--|
| CP | E | MR | |
| ↑ | H | L | Increment Counter |
| ↓ | X | L | Increment Counter |
| ↓ | X | L | No Change |
| H | ↑ | L | No Change |
| ↑ | L | L | No Change |
| H | ↓ | L | No Change |
| L | X | H | Q ₀ thru Q ₃ = L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | UNIT |
|-----------------|------------|---------|------|
| I _{CC} | MAX | 0.16 | mA |
| I _{OH} | MAX | -4 | mA |
| I _{OL} | MAX | 4 | mA |

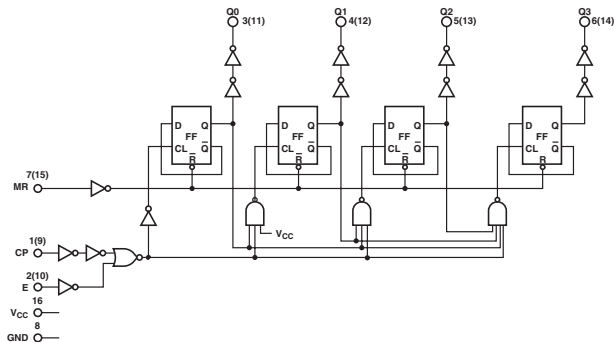
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC |
|------------------|--------------|----------------|------------|---------|
| f _{max} | | | MIN | 20 |
| t _w | CP | | MIN | 24 |
| | MR | | | 30 |
| t _{su} | Enable to CP | | MIN | 24 |
| | CP to Enable | | | 24 |
| t _{PLH} | CP | Q _n | MAX | 72 |
| t _{PHL} | | | | 72 |
| t _{PLH} | Enable | Q _n | MAX | 72 |
| t _{PHL} | | | | 72 |
| t _{PLH} | MR | Q _n | MAX | 45 |
| t _{PHL} | | | | 45 |

UNIT f_{max} : MHz other : ns

DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT STATE |
|--------|---|----|--|
| CP | E | MR | |
| ↑ | H | L | Increment Counter |
| ↓ | ↓ | L | Increment Counter |
| ↓ | X | L | No Change |
| X | ↑ | L | No Change |
| ↑ | L | L | No Change |
| H | ↓ | L | No Change |
| X | X | H | Q ₀ thru Q ₃ = L |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

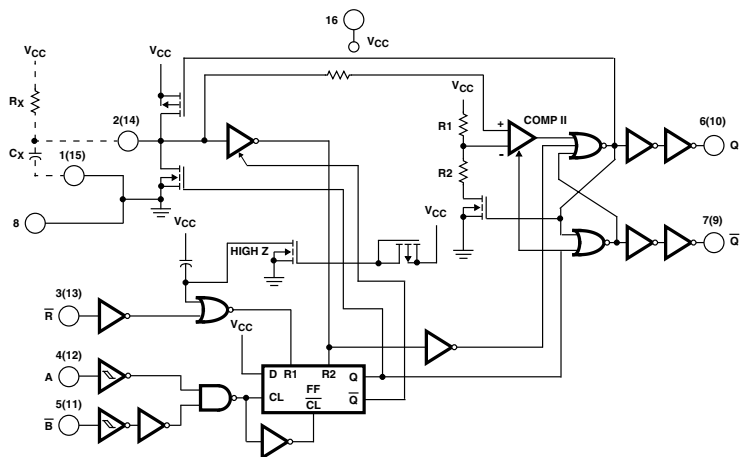
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|--------------|----------------|------------|---------|----------|
| f _{max} | | | MIN | 20 | 17 |
| t _w | CP | | MIN | 24 | 30 |
| | MR | | | 30 | 30 |
| t _{su} | Enable to CP | | MIN | 24 | 24 |
| | CP to Enable | | | 24 | - |
| t _{PLH} | CP | Q _n | MAX | 72 | 80 |
| t _{PHL} | | | | 72 | 80 |
| t _{PLH} | Enable | Q _n | MAX | 72 | 83 |
| t _{PHL} | | | | 72 | 83 |
| t _{PLH} | MR | Q _n | MAX | 45 | 53 |
| t _{PHL} | | | | 45 | 53 |

UNIT f_{max}: MHz other: ns

DUAL RETRIGGERABLE PRECISION MONO STABLE MULTIVIBRATOR

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|-----------|---|---|---------|-----------|
| \bar{R} | A | B | E | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | JL | LJ |
| H | ↑ | H | JL | LJ |

H = High Level, L = Low Level, ↑ = Transition from Low to High,
 ↓ = Transition from High to Low, JL One High Level Pulse,
 LJ One Low Level Pulse, X = Irrelevant.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

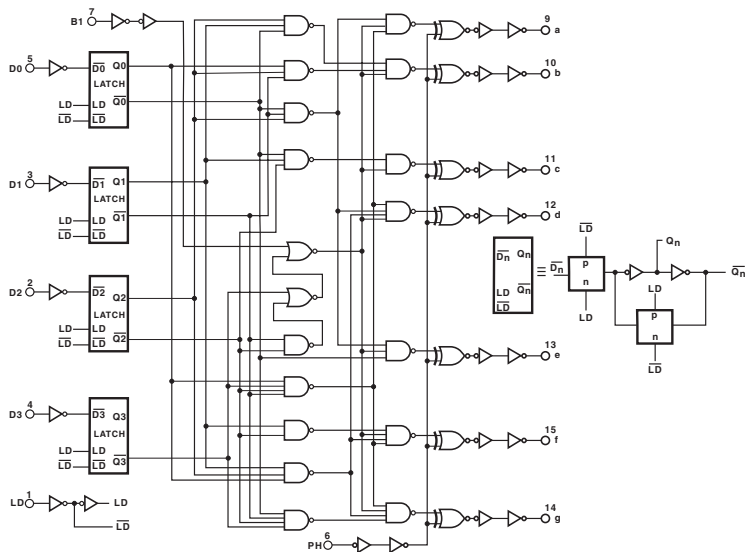
| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|---------------|-----------|------------|---------|----------|
| t _{WH} | A, \bar{B} | | MIN | 24 | 24 |
| t _{WL} | A, \bar{B} | | | 24 | 24 |
| t _{WL} | \bar{R} | | | 24 | 30 |
| t _{PLH} | \bar{A} , B | Q | MAX | 75 | 83 |
| t _{PHL} | | \bar{Q} | | 75 | 83 |
| t _{PLH} | \bar{R} | Q | MAX | 75 | 75 |
| t _{PHL} | | \bar{Q} | | 75 | 60 |

UNIT:ns

Logic Diagram



FUNCTION TABLE

| LD | B1 | PH | D3 | D2 | D1 | D0 | a | b | c | d | e | f | g | Display |
|----------|----|----|----|----|----------|----|---|---|---|---------------|---|---|---|----------|
| X | H | L | X | X | X | X | L | L | L | L | L | L | L | Blank |
| H | L | L | L | L | L | L | H | H | H | H | H | H | L | 0 |
| H | L | L | L | L | L | H | L | H | H | L | L | L | L | 1 |
| H | L | L | L | L | H | L | H | H | L | H | L | L | H | 2 |
| H | L | L | L | L | H | H | H | H | H | L | L | H | H | 3 |
| H | L | L | L | H | L | L | L | H | H | L | L | H | H | 4 |
| H | L | L | L | H | L | H | H | L | H | L | H | L | H | 5 |
| H | L | L | L | H | H | L | H | L | H | H | H | H | H | 6 |
| H | L | L | L | H | H | H | H | H | H | L | L | L | L | 7 |
| H | L | L | L | H | L | L | L | H | H | H | H | H | H | 8 |
| H | L | L | L | H | L | L | H | H | H | H | L | H | H | 9 |
| H | L | L | L | H | L | H | L | L | L | L | L | L | L | Blank |
| H | L | L | L | H | H | L | L | L | L | L | L | L | L | Blank |
| H | L | L | L | H | H | L | L | L | L | L | L | L | L | Blank |
| H | L | L | L | H | H | L | L | L | L | L | L | L | L | Blank |
| H | L | L | L | H | H | H | L | L | L | L | L | L | L | Blank |
| H | L | L | L | H | H | H | L | L | L | L | L | L | L | Blank |
| L | L | L | X | X | X | X | | | | | | | | NOTE |
| as above | | N | | | as above | | | | | inverse above | | | | as above |

NOTE:

Depends open the BCD code previously applied when LE = High

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -1 | -4 | mA |
| I _{OL} | MAX | 1 | 4 | mA |

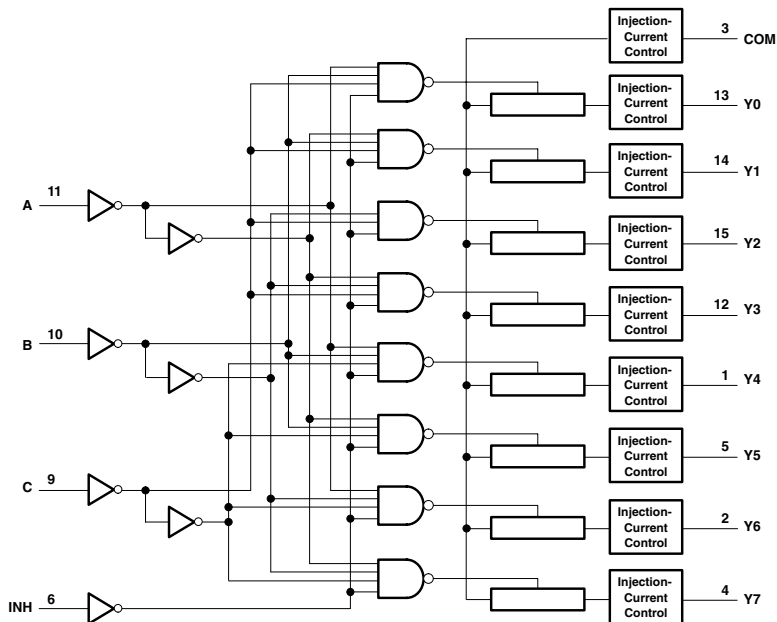
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|---------------|--------|------------|---------|----------|
| t _w | Latch Disable | | MIN | 15 | 15 |
| t _{su} | Dn to LD | | MIN | 18 | 18 |
| t _h | Dn to LD | | MIN | 9 | 12 |
| t _{PLH} | Dn | a - g | MAX | 102 | 120 |
| t _{PHL} | | | | 102 | 120 |
| t _{PLH} | LD | a - g | MAX | 111 | 116 |
| t _{PHL} | | | | 111 | 116 |
| t _{PLH} | BI | a - g | MAX | 80 | 99 |
| t _{PHL} | | | | 80 | 99 |
| t _{PLH} | PH | a - g | MAX | 60 | 99 |
| t _{PHL} | | | | 60 | 99 |

UNIT:ns

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | UNIT |
|-----------|------------|---------|----------|
| I_{CC} | MAX | 0.01 | mA |
| R_{ON} | MAX | 250 | Ω |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC |
|-----------|--------------|--------------|------------|---------|
| t_{PLH} | COM or Y_n | Y_n or COM | MAX | 12.5 |
| t_{PHL} | | | | 12.5 |
| t_{PLH} | INH | COM or Y_n | MAX | 15 |
| t_{PHL} | | | | 15 |
| t_{PLH} | INH | COM or Y_n | MAX | 90 |
| t_{PHL} | | | | 90 |
| t_{PLH} | INH | COM or Y_n | MAX | 90 |
| t_{PHL} | | | | 90 |

UNIT: ns

FUNCTION TABLE

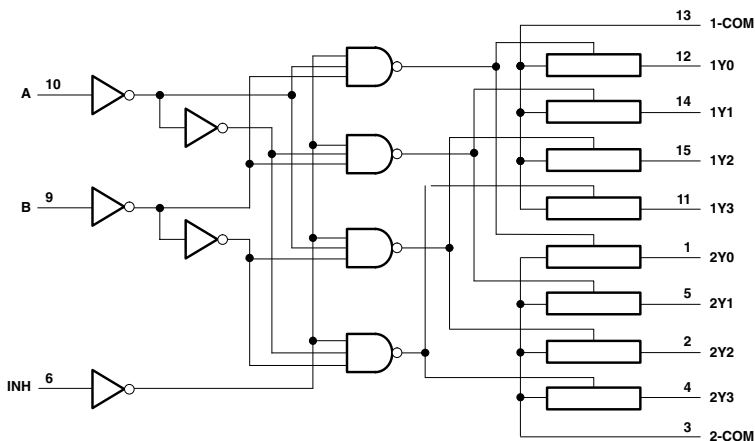
| INPUTS | | | | ON CHANNEL |
|--------|---|---|---|------------|
| INH | C | B | A | |
| L | L | L | L | Y0 |
| L | L | L | H | Y1 |
| L | L | H | L | Y2 |
| L | L | H | H | Y3 |
| L | H | L | L | Y4 |
| L | H | L | H | Y5 |
| L | H | H | L | Y6 |
| L | H | H | H | Y7 |
| H | X | X | X | None |

4852

DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

- Low Crosstalk Between Switches
- Pin Compatible with SN74HC4052

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | UNIT |
|-----------------|------------|---------|------|
| I _{CC} | MAX | 0.01 | mA |
| R _{ON} | MAX | 270 | Ω |

FUNCTION TABLE

| INPUTS | | | ON CHANNEL |
|--------|---|---|------------|
| INH | B | A | CHANNEL |
| L | L | L | 1Y0, 2Y0 |
| L | L | H | 1Y1, 2Y1 |
| L | H | L | 1Y2, 2Y2 |
| L | H | H | 1Y3, 2Y3 |
| H | X | X | None |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC |
|------------------|-----------------------|-----------------------|------------|---------|
| t _{PLH} | COM or Y _n | Y _n or COM | MAX | 12.5 |
| | | | | 12.5 |
| t _{PHL} | Channel Select | COM or Y _n | MAX | 15 |
| | | | | 15 |
| t _{PLH} | INH | COM or Y _n | MAX | 45 |
| | | | | 45 |
| t _{PHL} | INH | COM or Y _n | MAX | 90 |
| | | | | 90 |

UNIT: ns

5400

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5400A)

FUNCTION TABLE

| INPUTS | | | INPUT |
|--------|-----|---|-------|
| OE1 | OE2 | D | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

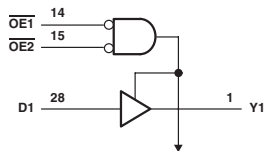
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 45 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | D | Y | MAX | 6.2 |
| t _{PHL} | | | | 5.6 |
| t _{PZH} | \overline{OE} | Y | MAX | 8.7 |
| t _{PZL} | | | | 7.5 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.2 |
| t _{PLZ} | | | | 6.9 |

Logic Diagram



To Ten Other Channels

5401

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5401)

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | D | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

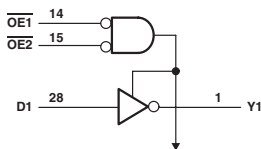
| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 45 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | D | Y | MAX | 6.9 |
| t _{PHL} | | | | 5.7 |
| t _{PZH} | \overline{OE} | Y | MAX | 8.5 |
| t _{PZL} | | | | 6.8 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.2 |
| t _{PLZ} | | | | 6.9 |

UNIT: ns

Logic Diagram



To Ten Other Channels

5402

12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5402A)

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | D | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

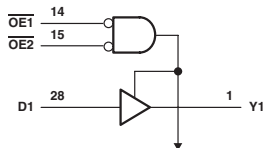
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 48 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | D | Y | MAX | 6.2 |
| | | | | 5.6 |
| t _{PZH} | \overline{OE} | Y | MAX | 8.7 |
| | | | | 7.5 |
| t _{PZL} | \overline{OE} | Y | MAX | 5.2 |
| | | | | 6.9 |

Logic Diagram



To Eleven Other Channels

5403

12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5403)

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | D | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

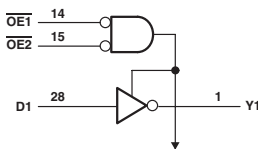
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 45 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | D | Y | MAX | 6.9 |
| | | | | 5.7 |
| t _{PZH} | \overline{OE} | Y | MAX | 8.5 |
| | | | | 6.8 |
| t _{PZL} | \overline{OE} | Y | MAX | 5.2 |
| | | | | 6.9 |

Logic Diagram



To 11 Other Channels

7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC08
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A \cdot B$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

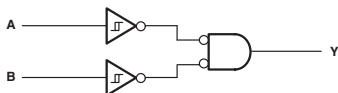
| PARAMETER | MAX or MIN | SN74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.02 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC |
|-----------|--------|--------|------------|---------|
| t_{PLH} | A or B | Y | MAX | 33 |
| t_{PHL} | | | | 33 |

UNIT: ns

Logic Diagram



7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC36
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = \overline{A + B}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

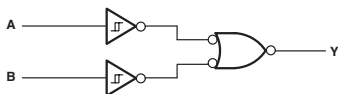
| PARAMETER | MAX or MIN | SN74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.02 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC |
|-----------|--------|--------|------------|---------|
| t_{PLH} | A or B | Y | MAX | 33 |
| t_{PHL} | | | | 33 |

UNIT: ns

Logic Diagram

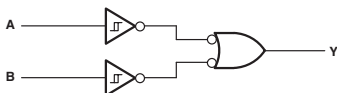


7032

QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC32
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A + B$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | UNIT |
|-----------|------------|---------|------|
| I_{CC} | MAX | 0.02 | mA |
| I_{OH} | MAX | -4 | mA |
| I_{OL} | MAX | 4 | mA |

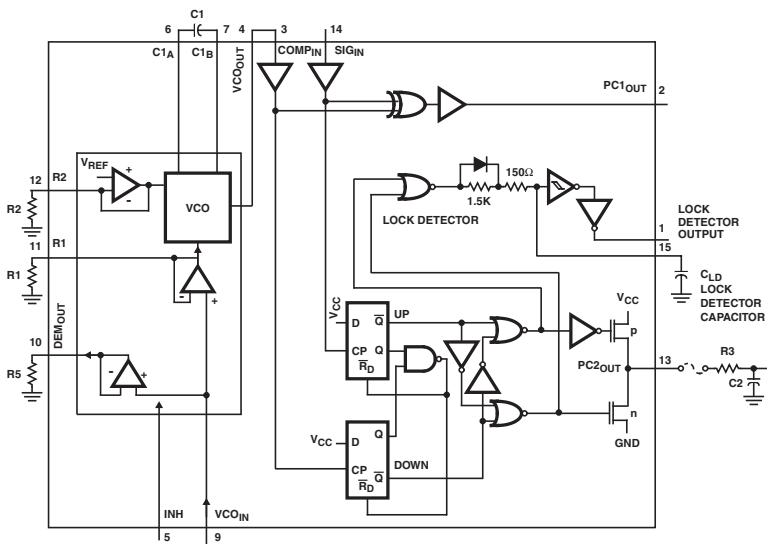
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC |
|-----------|--------|--------|------------|---------|
| t_{PLH} | A or B | Y | MAX | 33 |
| t_{PHL} | | | | 33 |

UNIT: ns

PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------|------------|---------|----------|------|
| I_{CC} | MAX | 0.16 | 0.16 | mA |
| I_{OH} | MAX | -4 | -4 | mA |
| I_{OL} | MAX | 4 | 4 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|-----------|---------------|--------|------------|---------|----------|
| t_{PLH} | SIGIN, COMPIN | PC1OUT | MAX | 60 | 68 |
| t_{PHL} | | | | 60 | 68 |
| t_{PZH} | SIGIN, COMPIN | PC2OUT | MAX | 84 | 90 |
| t_{PZL} | | | | 84 | 90 |
| t_{PHZ} | SIGIN, COMPIN | PC2OUT | MAX | 98 | 105 |
| t_{PLZ} | | | | 98 | 105 |

UNIT:ns

QUAD 2-INPUT EXCLUSIVE-NOR GATES

$$Y = A \oplus B$$

FUNCTION TABLE

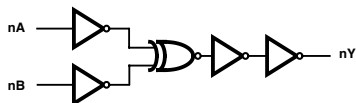
| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

NOTES:

H = High Voltage Level

L = Low Voltage Level

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 HC | CD74 HC | UNIT |
|-----------------|------------|------------|------------|------|
| I _{CC} | MAX | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -4 | -4 | V |
| I _{OL} | MAX | 4 | 4 | V |

SWITCHING CHARACTERISTICS

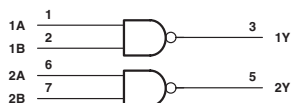
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 HC | CD74 HC |
|------------------|--------|--------|------------|------------|------------|
| t _{PLH} | A or B | Y | MAX | 25 | 35 |
| t _{PHL} | | Y | MAX | 25 | 35 |

UNIT: ns

8003

DUAL 2-INPUT POSITIVE-NAND GATES

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

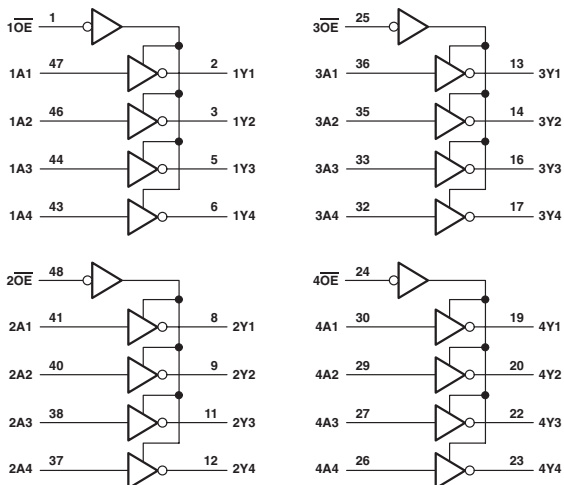
| PARAMETER | MAX or MIN | ALS | AS | UNIT |
|-----------------|------------|------|-----|------|
| I _{CC} | MAX | 1.5 | 8.7 | mA |
| I _{OH} | MAX | -0.4 | -2 | mA |
| I _{OL} | MAX | 8 | 20 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | AS |
|------------------|--------|--------|------------|-----|-----|
| t _{PLH} | A or B | Y | MAX | 11 | 4.5 |
| t _{PHL} | | | | 8 | 4 |

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT | |
|--------|---|--------|---|
| OE | A | Y | |
| L | H | L | L |
| L | L | H | H |
| H | X | L | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVT 3V | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT | LVCH 3V | LVCZ 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|-----------|------------|-------------|------|------|------|------|------------|------------|-------------|------|
| I _{CC} | MAX | 34 | 5 | 5 | 5 | 0.08 | 0.08 | 0.04 | 0.04 | 0.02 | 0.1 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -32 | -24 | -24 | -8 | -8 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 64 | 24 | 24 | 8 | 8 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|-------------|-------------|------|
| I _{CC} | MAX | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -8 | -9 | mA |
| I _{OL} | MAX | 8 | 9 | mA |

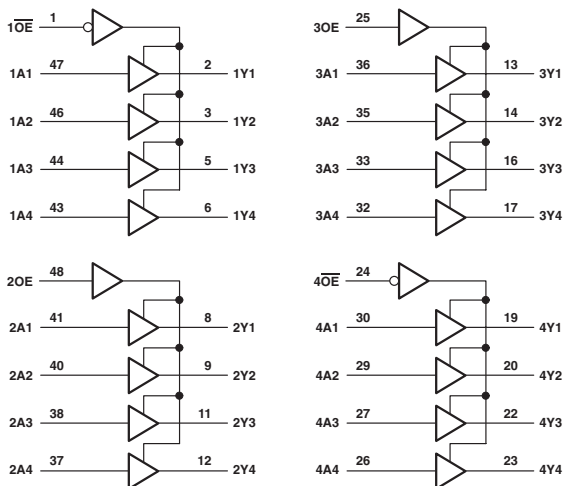
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT |
|------------------|-----------------|--------|------------|-----|-----------|------------|-------------|-----|------|------|------|
| t _{PLH} | A | Y | MAX | 4.7 | 3.5 | 3.5 | 3.3 | 5.8 | 8.5 | 8.5 | 10.5 |
| | | | | 4.8 | 3.5 | 3.5 | 3.2 | 7.1 | 10.2 | 8.5 | 10.5 |
| t _{PZH} | \overline{OE} | Y | MAX | 5.3 | 4 | 4 | 3.7 | 6.6 | 9.4 | 10.5 | 13 |
| | | | | 7.1 | 4.4 | 4.4 | 3.1 | 8.1 | 11.4 | 10.5 | 13 |
| t _{PZL} | \overline{OE} | Y | MAX | 6.1 | 4.5 | 4.5 | 5 | 8.1 | 12 | 10.5 | 13 |
| | | | | 5.6 | 4.2 | 4.2 | 4.1 | 7.3 | 10.7 | 10.5 | 13 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCH 3V | LVCZ 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V |
|------------------|-----------------|--------|------------|------------|------------|-------------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 4.2 | 4.2 | 3.9 | 2.0 | 1.6 |
| | | | | 4.2 | 4.2 | 3.9 | 2.0 | 1.6 |
| t _{PZH} | \overline{OE} | Y | MAX | 4.7 | 4.7 | 5 | 2.5 | 2 |
| | | | | 4.7 | 4.7 | 5 | 2.5 | 2 |
| t _{PZL} | \overline{OE} | Y | MAX | 5.9 | 5.9 | 4.4 | 4.5 | 2.3 |
| | | | | 5.9 | 5.9 | 4.4 | 4.5 | 2.3 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUTS |
|----------|--------|---------|
| 1OE, 4OE | 1A, 4A | 1Y, 4Y |
| L | H | L |
| L | L | H |
| H | X | Z |

| INPUTS | | OUTPUTS |
|----------|--------|---------|
| 2OE, 3OE | 2A, 3A | 2Y, 3Y |
| H | H | H |
| H | L | L |
| L | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

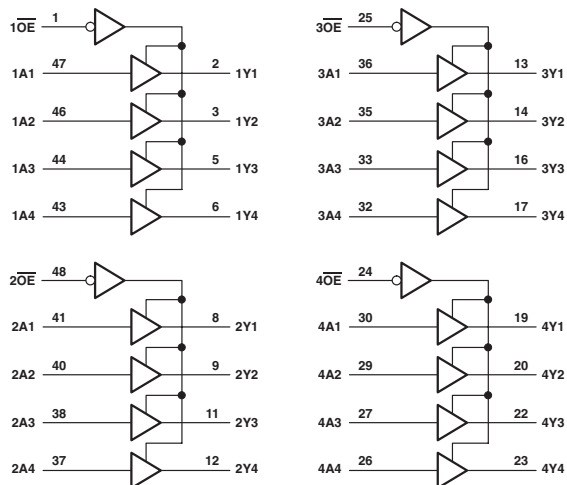
| PARAMETER | MAX or MIN | ABT | LVTH 3V | ACT | UNIT |
|-----------------|------------|-----|------------|------|------|
| I _{CC} | MAX | 34 | 5 | 0.08 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ACT |
|------------------|-----------------------|--------|------------|-----|------------|------|
| t _{PLH} | A | Y | MAX | 3.7 | 3.5 | 9.5 |
| t _{PHL} | | | | 4.5 | 3.5 | 9.1 |
| t _{PZH} | $\overline{0E}$ or OE | Y | MAX | 5 | 4.5 | 9.4 |
| t _{PZL} | | | | 6.9 | 4.5 | 10.5 |
| t _{PHZ} | $\overline{0E}$ or OE | Y | MAX | 6.2 | 5.3 | 11.6 |
| t _{PHZ} | | | | 5.6 | 4.9 | 10.7 |

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALB 3V | ALVTH 3V | AC | ACT | AHC | AHCT | LVC 3V | UNIT |
|-----------------|------------|-----|------|--------|---------|--------|----------|------|------|------|------|--------|------|
| I _{CC} | MAX | 32 | 32 | 5 | 5 | 5.6 | 5 | 0.08 | 0.08 | 0.04 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -32 | -25 | -32 | -24 | -24 | -8 | -8 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 64 | 25 | 64 | 24 | 24 | 8 | 8 | 24 | mA |

| PARAMETER | MAX or MIN | LVCH 3V | LVCZ 3V | ALVC 3V | ALVCH 3V | AVC 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------------|------------|---------|---------|---------|----------|--------|----------|----------|-----------|-----------|------|
| I _{CC} | MAX | 0.02 | 0.1 | 0.04 | 0.04 | 0.04 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -24 | -24 | -24 | -24 | -12 | -8 | -9 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 24 | 24 | 12 | 8 | 9 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALB 3V | ALVTH 3V | AC | ACT |
|------------------|-------|--------|------------|-----|------|--------|---------|--------|----------|------|------|
| t _{PLH} | A | Y | MAX | 3.5 | 3.5 | 3.2 | 3.2 | 2 | 2.4 | 7.1 | 9.4 |
| t _{PHL} | | | | 4.1 | 4.1 | 3.2 | 3.2 | 2 | 2.5 | 7.9 | 9.5 |
| t _{PZH} | OE | Y | MAX | 4.8 | 4.8 | 4 | 4 | 4.7 | 3.8 | 7.5 | 8.9 |
| t _{PZL} | | | | 4.8 | 4.8 | 4 | 4 | 4.7 | 2.9 | 9 | 10.3 |
| t _{PHZ} | OE | Y | MAX | 4.8 | 4.8 | 4.5 | 4.5 | 4.2 | 4.2 | 8.4 | 11.3 |
| t _{PLZ} | | | | 4.1 | 4.1 | 4.2 | 4.2 | 3.6 | 7.6 | 10.3 | |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AHC | AHCT | LVC 3V | LVCH 3V | LVCZ 3V | ALVC 3V | ALVCH 3V | AVC 3V |
|------------------|-------|--------|------------|------|------|--------|---------|---------|---------|----------|--------|
| t _{PLH} | A | Y | MAX | 8.5 | 10.5 | 4.1 | 4.1 | 4.1 | 3 | 3 | 1.7 |
| t _{PHL} | | | | 8.5 | 10.5 | 4.1 | 4.1 | 4.1 | 3 | 3 | 1.7 |
| t _{PZH} | OE | Y | MAX | 10.5 | 13 | 4.6 | 4.6 | 4.6 | 4.4 | 4.4 | 3.5 |
| t _{PZL} | | | | 10.5 | 13 | 4.6 | 4.6 | 4.4 | 4.4 | 3.5 | |
| t _{PHZ} | OE | Y | MAX | 10.5 | 13 | 5.8 | 5.8 | 5.8 | 4.1 | 4.1 | 3.5 |
| t _{PLZ} | | | | 10.5 | 13 | 5.8 | 5.8 | 4.1 | 4.1 | 3.5 | |

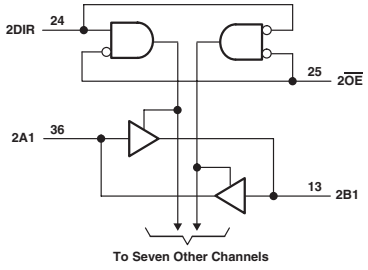
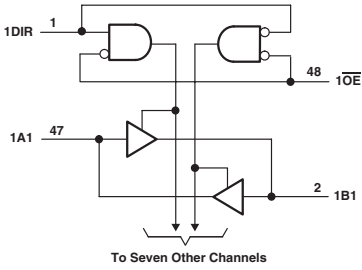
| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|------------------|-------|--------|------------|----------|----------|-----------|-----------|
| t _{PLH} | A | Y | MAX | 1.8 | 1.8 | 1.8 | 1.8 |
| t _{PHL} | | | | 1.8 | 1.8 | 1.8 | 1.8 |
| t _{PZH} | OE | Y | MAX | 2.5 | 1.9 | 2.5 | 1.9 |
| t _{PZL} | | | | 2.5 | 1.9 | 2.5 | 1.9 |
| t _{PHZ} | OE | Y | MAX | 4.0 | 2 | 4.0 | 2 |
| t _{PLZ} | | | | 4.0 | 2 | 4.0 | 2 |

UNIT: ns

16245

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALB 3V | ALVTH 3V | ALVT HR 3V | AC | ACT | AHCT | UNIT |
|-----------------|------------|-----|------|--------|---------|--------|----------|------------|------|------|------|------|
| I _{CC} | MAX | 32 | 32 | 5 | 5 | 5.6 | 5 | 5 | 0.08 | 0.08 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -32 | -25 | -32 | -12 | -24 | -24 | -8 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 64 | 25 | 64 | 12 | 24 | 24 | 8 | mA |

| PARAMETER | MAX or MIN | LVC 3V | LVCH 3V | LVCHR 3V | LVCR 3V | LVCZ 3V | ALVCH 3V | ALVC HR 3V | AVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|--------|---------|----------|---------|---------|----------|------------|--------|----------|----------|------|
| I _{CC} | MAX | 0.02 | 0.02 | 0.02 | 0.02 | 0.06 | 0.04 | 0.04 | 0.04 | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -24 | -24 | -12 | -12 | -24 | -24 | -12 | -12 | -8 | -9 | mA |
| I _{OL} | MAX | 24 | 24 | 12 | 12 | 24 | 24 | 12 | 12 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

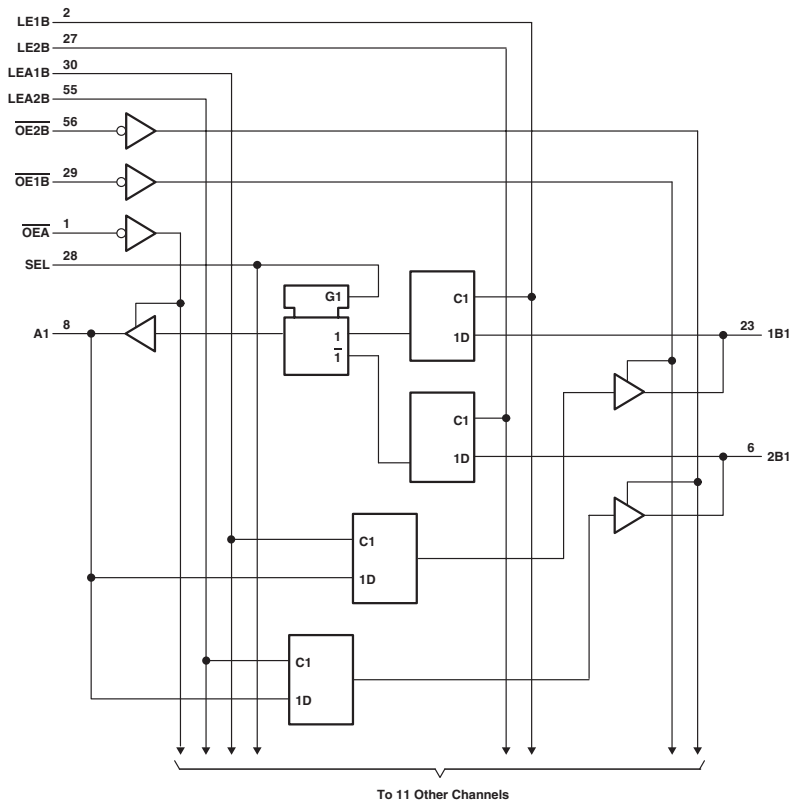
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALB 3V | ALVTH 3V | ALVT HR 3V | AC |
|------------------|-----------------|--------|------------|-----|------|--------|---------|--------|----------|------------|------|
| t _{PLH} | A or B | B or A | MAX | 3.9 | 3.9 | 3.3 | 3.3 | 2 | 3.1 | 3.7 | 7.9 |
| t _{PHL} | | | | 4.2 | 4.2 | 3.3 | 3.3 | 2 | 2.9 | 3.9 | 8.9 |
| t _{PZH} | \overline{OE} | B or A | MAX | 6.3 | 6.3 | 4.5 | 4.5 | 6 | 4.2 | 5.2 | 8.6 |
| t _{PZL} | | | | 6.4 | 6.4 | 4.6 | 4.6 | 6 | 3.5 | 4 | 10.7 |
| t _{PHZ} | \overline{OE} | B or A | MAX | 6.3 | 6.3 | 5.1 | 5.1 | 4.2 | 5.3 | 5.1 | 9.8 |
| t _{PLZ} | | | | 5.2 | 5.2 | 5.1 | 5.1 | 4.2 | 5 | 4.8 | 8.7 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT | AHCT | LVC 3V | LVCH 3V | LVCHR 3V | LVCR 3V | LVCZ 3V | ALVCH 3V |
|------------------|-----------------|--------|------------|------|------|--------|---------|----------|---------|---------|----------|
| t _{PLH} | A or B | B or A | MAX | 10.5 | 10.5 | 4 | 4 | 4.8 | 4.8 | 4 | 3 |
| t _{PHL} | | | | 10.2 | 10.5 | 4 | 4 | 4.8 | 4.8 | 4 | 3 |
| t _{PZH} | \overline{OE} | B or A | MAX | 10 | 15 | 5.5 | 5.5 | 6.3 | 6.3 | 5.6 | 4.4 |
| t _{PZL} | | | | 11.6 | 15 | 5.5 | 5.5 | 6.3 | 6.3 | 5.6 | 4.4 |
| t _{PHZ} | \overline{OE} | B or A | MAX | 12.6 | 15 | 6.6 | 6.6 | 7.4 | 7.4 | 6.6 | 4.1 |
| t _{PLZ} | | | | 11.8 | 15 | 6.6 | 6.6 | 7.4 | 7.4 | 6.6 | 4.1 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC HR 3V | AVC 3V | AUC 1.8V | AUC 2.3V |
|------------------|-----------------|--------|------------|------------|--------|----------|----------|
| t _{PLH} | A or B | B or A | MAX | 4.2 | 1.7 | 2 | 1.9 |
| t _{PHL} | | | | 4.2 | 1.7 | 2 | 1.9 |
| t _{PZH} | \overline{OE} | B or A | MAX | 5.6 | 3.7 | 3.1 | 2.6 |
| t _{PZL} | | | | 5.6 | 3.7 | 3.1 | 2.6 |
| t _{PHZ} | \overline{OE} | B or A | MAX | 5.5 | 3.9 | 4.8 | 2.9 |
| t _{PLZ} | | | | 5.5 | 3.9 | 4.8 | 2.9 |

UNIT: ns

Logic Diagram



FUNCTION TABLE
B TO A ($\overline{OE}B = H$)

| INPUTS | | | | | | OUTPUT |
|--------|----|-----|------|------|-------------------|----------------|
| 1B | 2B | SEL | LE1B | LE2B | OE \overline{A} | A |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | A ₀ |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | A ₀ |
| X | X | X | X | X | H | Z |

A TO B ($\overline{OE}A = H$)

| INPUTS | | | | | OUTPUTS | |
|--------|-------|-------|------|------|-----------------|-----------------|
| 1B | LEA1B | LEA2B | OE1B | OE2B | 1B | 2B |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | 2B ₀ |
| L | H | L | L | L | L | 2B ₀ |
| H | L | H | L | L | 1B ₀ | H |
| L | L | H | L | L | 1B ₀ | L |
| X | L | L | L | L | 1B ₀ | 2B ₀ |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | ALVCH 3V | UNIT |
|-----------------|------------|------|-------------|------|
| I _{CC} | MAX | 63 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

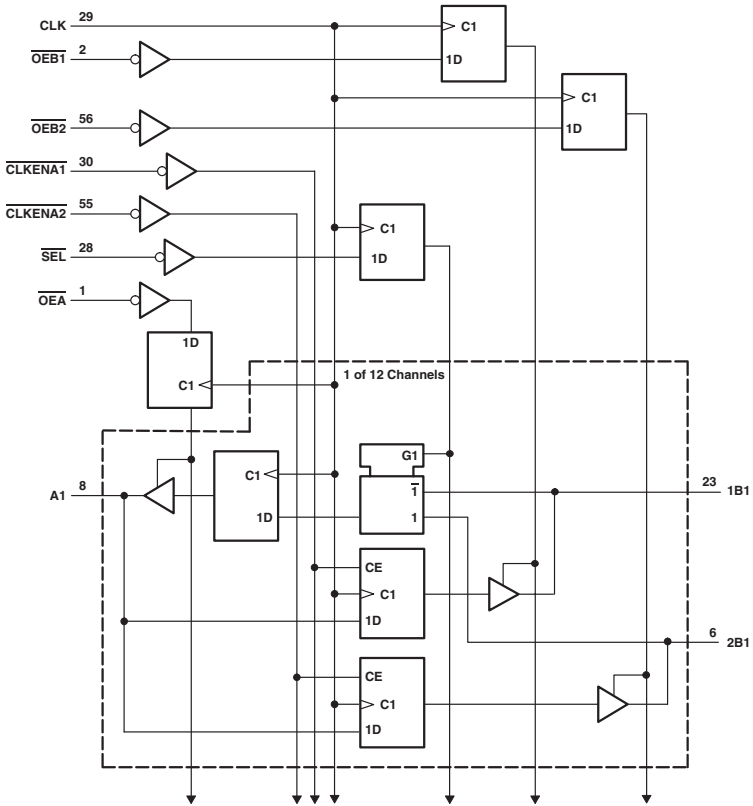
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH | ALVCH 3V |
|---|----------|--------|------------|------|-------------|
| t _w Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high | | | MIN | 3.3 | 3.3 |
| t _{su} Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓ | | | MIN | 1.5 | 1.1 |
| t _h Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓ | | | MIN | 1 | 1.5 |
| t _{PLH} | A or B | B or A | MAX | 5.6 | 4.3 |
| t _{PHL} | | | | 5.9 | 4.3 |
| t _{PLH} | LE | A or B | MAX | 5.8 | 4.4 |
| t _{PHL} | | | | 5.3 | 4.4 |
| t _{PLH} | SEL (B1) | A | MAX | 5.3 | 5.6 |
| | SEL (B2) | | | 6 | 5.6 |
| t _{PHL} | SEL (B1) | A | MAX | 4.4 | 5.6 |
| | SEL (B2) | | | 5.9 | 5.6 |
| t _{PZH} | OE | A or B | MAX | 5.7 | 5.4 |
| t _{PZL} | | | | 5.8 | 5.4 |
| t _{PHZ} | OE | A or B | MAX | 6.4 | 4.6 |
| t _{PLZ} | | | | 4.8 | 4.6 |

UNIT: ns

12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|--------------|--------------|---------|--------|
| CLK | OE \bar{A} | OE \bar{B} | A | 1B,2B |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

A-TO-B STORAGE (OE \bar{B} = L)

| INPUTS | | | OUTPUTS | | |
|---------|---------|-----|---------|---------------|---------------|
| CLKENA1 | CLKENA2 | CLK | A | 1B | 2B |
| H | H | X | X | 1B \uparrow | 2B \uparrow |
| L | X | ↑ | L | L | X |
| L | X | ↑ | H | H | X |
| X | L | ↑ | L | X | L |
| X | L | ↑ | H | X | H |

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OE \bar{A} = L)

| INPUTS | | | | OUTPUT |
|--------|-----|----|----|--------------|
| CLK | SEL | 1B | 2B | A |
| X | H | X | X | A \uparrow |
| X | L | X | X | A \uparrow |
| ↑ | H | H | X | L |
| ↑ | H | L | X | H |
| ↑ | L | X | L | L |
| ↑ | L | X | H | H |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

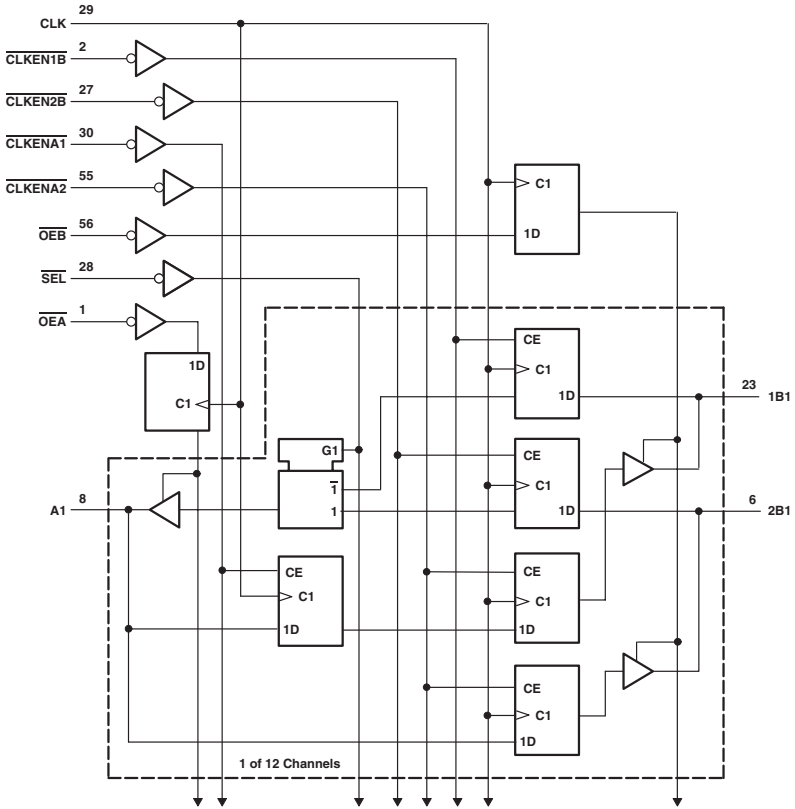
| PARAMETER | MAX or MIN | ALVCH 3V | ALVCHR 3V | AVC 3V | UNIT |
|-----------------|------------|-------------|--------------|-----------|------|
| I _{CC} | MAX | 0.04 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -24 | -12 | -12 | mA |
| I _{OL} | MAX | 24 | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | ALVCHR 3V | AVC 3V |
|--|---------------------------------|--------|------------|-------------|--------------|-----------|
| f _{max} | | | MIN | 135 | 135 | 175 |
| t _w Pulse duration, CLK high or low | | | MIN | 3.3 | 3.3 | 3.5 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 1.7 | 1 | 1.9 |
| | B data before CLK ↑ | | MIN | 1.8 | 1.1 | 1.9 |
| | SEL before CLK ↑ | | MIN | 1.3 | 1.3 | 1.3 |
| | CLKENAT or CLKENA2 before CLK ↑ | | MIN | 0.9 | 0.8 | 1.1 |
| | OE before CLK ↑ | | MIN | 1.3 | 1.2 | 1.1 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.6 | 1.2 | 1 |
| | B data after CLK ↑ | | MIN | 0.6 | 1 | 0.7 |
| | SEL after CLK ↑ | | MIN | 0.7 | 1.7 | 0.4 |
| | CLKENAT or CLKENA2 after CLK ↑ | | MIN | 1.1 | 1.6 | 1 |
| | OE after CLK ↑ | | MIN | 0.8 | 1.2 | 0.3 |
| t _{pd} | CLK | B | MAX | 6.2 | 5.8 | 3 |
| | | A | | 5 | 5.2 | 2.7 |
| t _{en} | CLK | B | MAX | 6.1 | 5.8 | 3.8 |
| | | A | | 5.9 | 5.3 | 3.4 |
| t _{fis} | CLK | B | MAX | 6.1 | 6 | 3.7 |
| | | A | | 5.6 | 6 | 3.4 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|-----|-----|---------|--------|
| CLK | OEA | OEB | A | 1B,2B |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

A-TO-B STORAGE ($\overline{OEB} = L$)

| INPUTS | | | OUTPUTS | | |
|---------|---------|-----|---------|------------------------------|------------------------------|
| CLKENA1 | CLKENA2 | CLK | A | 1B | 2B |
| L | H | ↑ | L | L [†] | 2B ₀ [†] |
| L | H | ↑ | H | H [†] | 2B ₀ [†] |
| L | L | ↑ | L | L [†] | L |
| L | L | ↑ | H | H [†] | H |
| H | L | ↑ | L | 1B ₀ [†] | L |
| H | L | ↑ | H | 1B ₀ [†] | H |
| H | H | X | X | 1B ₀ [†] | 2B ₀ [†] |

[†] Two CLK edges are needed to propagate data.

[†] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

| INPUTS | | | | | OUTPUT | |
|---------|---------|-----|-----|----|--------|-----------------------------|
| CLKEN1B | CLKEN2B | CLK | SEL | 1B | 2B | A |
| H | X | X | H | X | X | A ₀ [†] |
| X | H | X | L | X | X | A ₀ [†] |
| L | X | ↑ | H | H | X | L |
| L | X | ↑ | H | L | X | H |
| X | L | ↑ | L | X | L | L |
| X | L | ↑ | L | X | H | H |

[†] Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

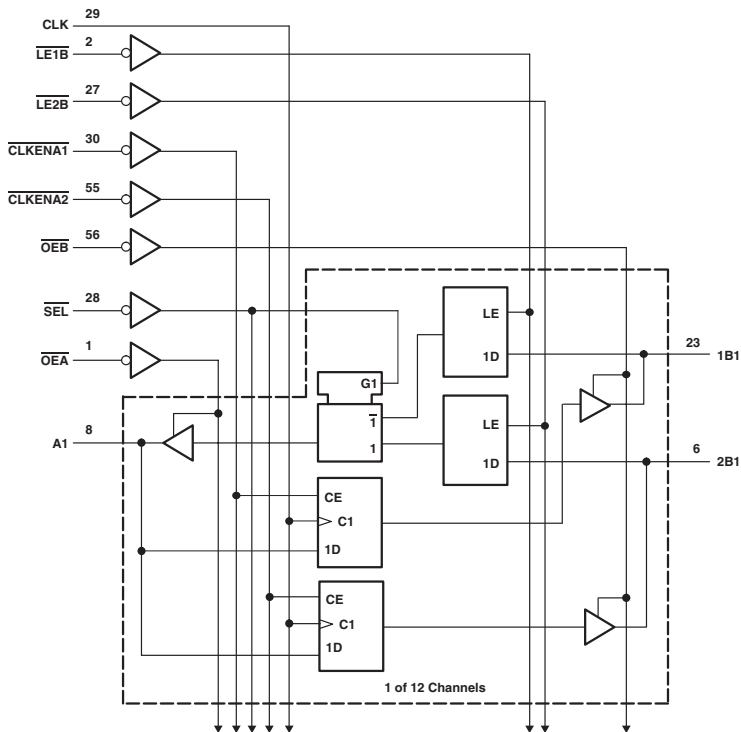
| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|------------------|---------------------------------|---------------------------------|------------|-------------|
| t _{max} | | | MIN | 150 |
| t _w | Pulse duration, CLK high or low | | MIN | 3.3 |
| t _{su} | Setup time | A data before CLK ↑ | MIN | 3.1 |
| | | B data before CLK ↑ | MIN | 0.9 |
| | | CLKENA1 or CLKENA2 before CLK ↑ | MIN | 2.7 |
| | | CLKEN1B or CLKEN2B before CLK ↑ | MIN | 2.6 |
| | | \overline{OE} before CLK ↑ | MIN | 3.2 |
| t _h | Hold time | A data after CLK ↑ | MIN | 0.2 |
| | | B data after CLK ↑ | MIN | 1.7 |
| | | CLKENA1 or CLKENA2 after CLK ↑ | MIN | 0.3 |
| | | CLKEN1B or CLKEN2B after CLK ↑ | MIN | 0.6 |
| | | \overline{OE} after CLK ↑ | MIN | 0.1 |
| t _{pd} | CLK | A or B | MAX | 5.1 |
| | \overline{SEL} | A | MAX | 4.7 |
| t _{en} | CLK | A or B | MAX | 5.5 |
| | | | | 6 |
| t _{dis} | CLK | A or B | MAX | 6 |
| | | | | 5.8 |
| | | | | 5.8 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

OUTPUT ENABLE

| INPUTS | | OUTPUTS | |
|--------|-----|---------|--------|
| OEA | OEB | A | 1B, 2B |
| H | X | Z | Z |
| L | L | Z | Active |
| L | H | Active | Z |
| L | L | Active | Active |

A-TO-B STORAGE ($\overline{OEB} = L$)

| INPUTS | | | | OUTPUTS | |
|---------|---------|-----|---|-------------------|-------------------|
| CLKENA1 | CLKENA2 | CLK | A | 1B | 2B |
| H | H | X | X | 1B ₀ † | 2B ₀ † |
| L | X | ↑ | L | L | X |
| L | X | ↑ | H | H | X |
| X | L | ↑ | L | X | L |
| X | L | ↑ | H | A ₀ | H |

B-TO-A STORAGE ($\overline{OEA} = L$)

| INPUTS | | | | OUTPUTA |
|--------|-----|----|----|------------------|
| LE | SEL | 1B | 2B | |
| H | X | X | X | A ₀ † |
| H | X | X | X | A ₀ † |
| L | H | L | X | L |
| L | H | H | X | H |
| L | L | X | L | L |
| L | L | X | H | H |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

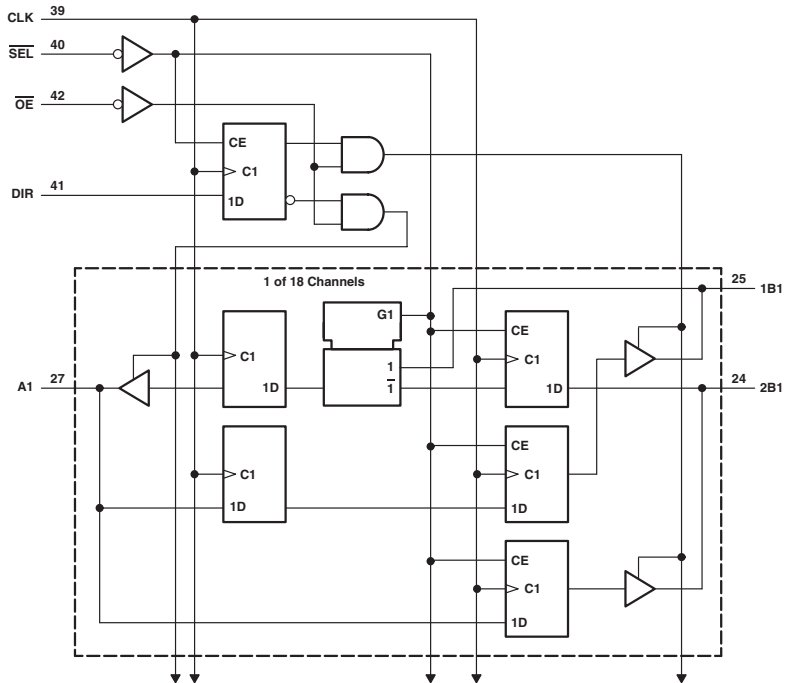
| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|--|--------------------------------------|--------|------------|-------------|
| f _{max} | | | MIN | 130 |
| t _w Pulse duration, CLK high or low | | | MIN | 3.3 |
| t _{su} Setup time | A before CLK ↑ | | MIN | 1.7 |
| | B before \overline{LE} | | MIN | 1.3 |
| | CLKEN before CLK ↑ | | MIN | 1 |
| t _h Hold time | A after CLK ↑ | | MIN | 0.7 |
| | B after \overline{LE} | | MIN | 1.1 |
| | CLKEN after CLK ↑ | | MIN | 0.9 |
| t _{pd} | CLK | B | MAX | 4.3 |
| | B | A | MAX | 4 |
| | \overline{LE} | | | 4.8 |
| | SEL | | | 5.2 |
| t _{en} | \overline{OEB} or \overline{OEA} | B or A | MAX | 5.1 |
| t _{dis} | \overline{OEB} or \overline{OEA} | B or A | MAX | 4.2 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

| INPUTS | | | OUTPUTS | |
|--------|-----|---|-------------------|-------------------|
| SEL | CLK | A | 1B | 2B |
| H | X | X | 1B ₀ † | 2B ₀ † |
| L | ↑ | L | L† | X |
| L | ↑ | H | H† | X |

† Output level before the indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

| INPUTS | | | | OUTPUT |
|--------|-----|----|----|--------|
| CLK | SEL | 1B | 2B | A |
| ↑ | H | X | L | L§ |
| ↑ | H | X | H | H§ |
| ↑ | L | L | X | L |
| ↑ | L | H | X | H |

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|-----------------|-----|---------|--------|
| CLK | \overline{OE} | DIR | A | 1B, 2B |
| ↑ | H | X | Z | Z |
| ↑ | L | L | Z | Active |
| ↑ | L | H | Active | Z |

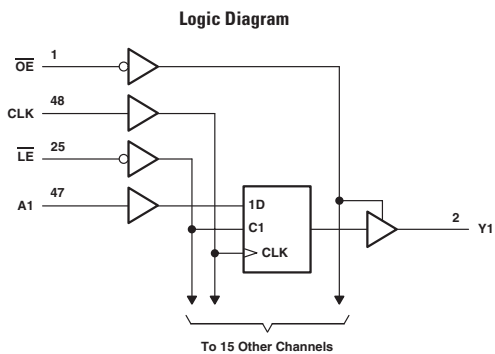
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|----------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|--|---------------------|--------|------------|----------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration, CLK high or low | | | MIN | 3.3 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 2 |
| | B data before CLK ↑ | | MIN | 1.8 |
| | DIR before CLK ↑ | | MIN | 1.7 |
| | SEL before CLK ↑ | | MIN | 1.8 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.7 |
| | B data after CLK ↑ | | MIN | 0.6 |
| | DIR after CLK ↑ | | MIN | 0.5 |
| | SEL after CLK ↑ | | MIN | 0.8 |
| t _{pd} | CLK | A | MAX | 5 |
| | | B | | 5.3 |
| t _{en} | \overline{OE} | A | MAX | 5.7 |
| | | B | | 7.4 |
| t _{dis} | \overline{OE} | A | MAX | 5.7 |
| | | B | | 6.4 |

UNIT f_{max} : MHz other : ns



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|--------|---|------------------|
| OE | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | Y ₀ ↑ |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCH 3V | AVC 3V | UNIT |
|-----------------|------------|------------|-------------|-----------|------|
| I _{CC} | MAX | 0.04 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -24 | -24 | -12 | mA |
| I _{OL} | MAX | 24 | 24 | 12 | mA |

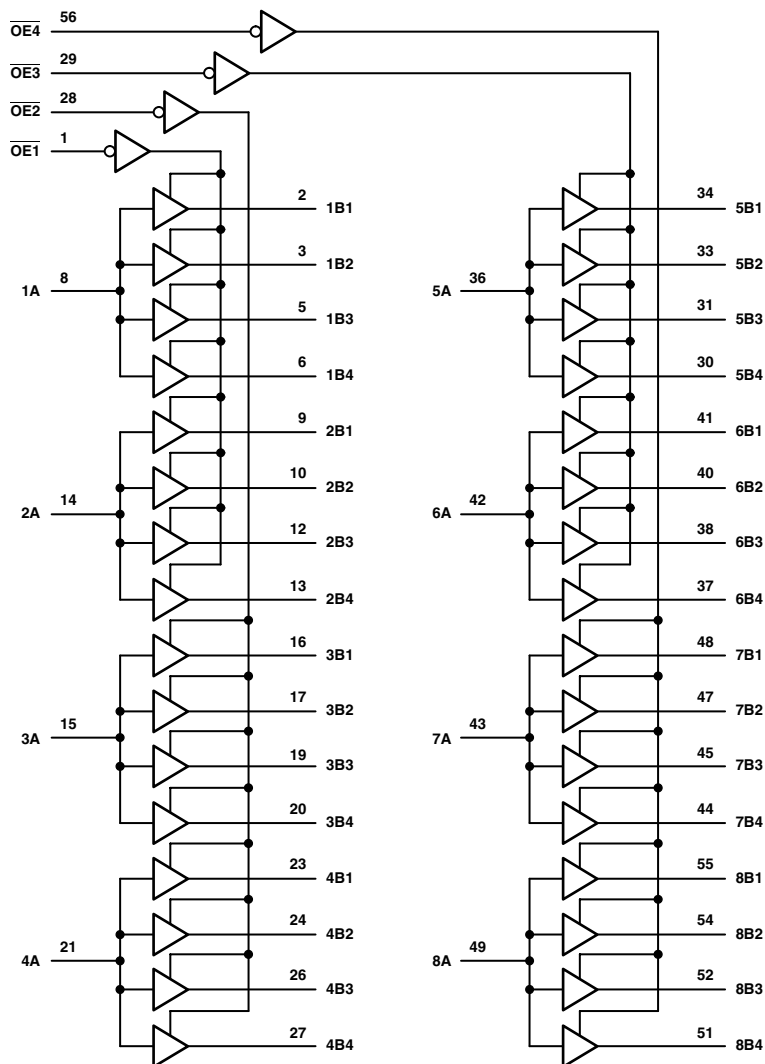
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCH 3V | AVC 3V |
|-------------------------------|---------------------------|--------|------------|------------|-------------|-----------|
| f _{max} | | | MIN | 150 | 150 | 150 |
| t _w Pulse duration | LE low | | | 3.3 | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.5 | 1.5 | 0.7 |
| | Data before LE ↑ CLK high | | MIN | 1.3 | 1.3 | 0.9 |
| | Data before LE ↑ CLK low | | MIN | 1.2 | 1.2 | 1 |
| t _h Hold time | Data after CLK ↑ | | MIN | 0.9 | 0.9 | 0.7 |
| | Data after LE ↑ CLK high | | MIN | 1.1 | 1.1 | 1.5 |
| | Data after LE ↑ CLK low | | MIN | 1.1 | 1.1 | 1.3 |
| t _{pd} | A | | MAX | 3.3 | 3.3 | 2.5 |
| | LE | Y | | 4.4 | 4.4 | 4 |
| | CLK | | MAX | 4.1 | 4.1 | 3.1 |
| t _{en} | OE | Y | | 4.6 | 4.6 | 6.2 |
| t _{dis} | OE | Y | MAX | 4.4 | 4.4 | 5.3 |

UNIT f_{max} : MHz other : ns

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Bn |
| L | H | H |
| L | L | L |
| H | H | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

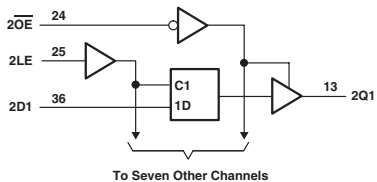
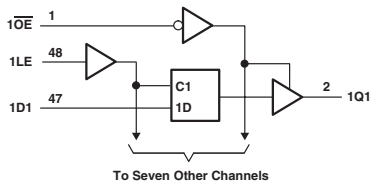
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|------------------|-------|--------|------------|-------------|
| t _{PLH} | A | B | MAX | 4 |
| t _{PHL} | | | | 4 |
| t _{PZH} | OE | B | MAX | 5.1 |
| t _{PZL} | | | | 5.1 |
| t _{PHZ} | OE | B | MAX | 4 |
| t _{PLZ} | | | | 4 |

UNIT: ns

16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q _O |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT | LVC 3V | LVC ver.A 3V | LVCH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|------------|-------------|------|------|------|------|-----------|--------------------|------------|-------------|------|
| I _{cc} | MAX | 85 | 5 | 5 | 0.08 | 0.08 | 0.04 | 0.04 | 0.04 | 0.02 | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -8 | -8 | -24 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 8 | 8 | 24 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | AVC 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|-----------|-------------|-------------|------|
| I _{cc} | MAX | 0.04 | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -12 | -8 | -9 | mA |
| I _{OL} | MAX | 12 | 8 | 9 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

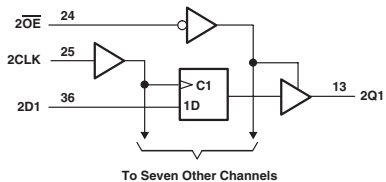
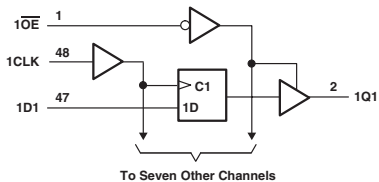
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT |
|---|-------|-----------------------------|------------|-----|------------|-------------|------|------|------|------|
| t _w Pulse duration, LE high or low | | | MIN | 3.3 | 3 | 1.5 | 4 | 1 | 5 | 6.5 |
| t _{su} Setup time | | Data before LE ↓, data high | MIN | 1.5 | 1 | 1.4 | 1.5 | 1 | 4 | 1.5 |
| | | Data before LE ↓, data low | MIN | 1.5 | 1 | 0.9 | 1.5 | 1 | 4 | 1.5 |
| t _h Hold time | | Data after LE ↓, data high | MIN | 1 | 1 | 0.9 | 2.4 | 5 | 1 | 3.5 |
| | | Data after LE ↓, data low | MIN | 1 | 1 | 1.4 | 2.4 | 5 | 1 | 3.5 |
| ↑PLH | D | Q | MAX | 6.3 | 3.8 | 3.1 | 9.7 | 11.1 | 10.5 | 10.5 |
| ↑PHL | | | | 6.2 | 3.6 | 3.3 | 10.1 | 12.3 | 10.5 | 10.5 |
| ↑PLH | LE | Q | MAX | 6.7 | 4.3 | 3.3 | 11.9 | 12.8 | 10.5 | 10.5 |
| ↑PHL | | | | 6.1 | 4 | 3.5 | 10.9 | 12.2 | 10.5 | 10.5 |
| ↑PZH | OE | Q | MAX | 6.1 | 4.3 | 4 | 10.8 | 12.1 | 11.5 | 11.5 |
| ↑PZL | | | | 5.6 | 4.3 | 3.4 | 12.8 | 14.2 | 11.5 | 11.5 |
| ↑PHZ | OE | Q | MAX | 8.1 | 5 | 4.9 | 8.8 | 10.7 | 11.5 | 12 |
| ↑PIZ | | | | 6.5 | 4.7 | 4.5 | 8.1 | 9.4 | 11.5 | 12 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC 3V | LVC ver.A 3V | LVCH 3V | ALVCH 3V | AVC 3V | AUC 1.8V | AUC 2.3V |
|---|-------|-----------------------------|------------|-----------|--------------------|------------|-------------|-----------|-------------|-------------|
| t _w Pulse duration, LE high or low | | | MIN | 4 | 3.3 | 3.3 | 3.3 | 1.8 | 2.1 | 1.7 |
| t _{su} Setup time | | Data before LE ↓, data high | MIN | 2 | 1.7 | 1.7 | 1.1 | 0.8 | 0.4 | 0.4 |
| | | Data before LE ↓, data low | MIN | 2 | 1.7 | 1.7 | 1.1 | 0.8 | 0.4 | 0.4 |
| t _h Hold time | | Data after LE ↓, data high | MIN | 2 | 1.2 | 1.2 | 1.4 | 1 | 0.7 | 0.6 |
| | | Data after LE ↓, data low | MIN | 2 | 1.2 | 1.2 | 1.4 | 1 | 0.7 | 0.6 |
| ↑PLH | D | Q | MAX | 7 | 4.2 | 4.2 | 3.6 | 2.8 | 2.4 | 1.9 |
| ↑PHL | | | | 7 | 4.2 | 4.2 | 3.6 | 2.8 | 2.4 | 1.9 |
| ↑PLH | LE | Q | MAX | 8 | 4.6 | 4.6 | 3.9 | 3.2 | 2.8 | 2.1 |
| ↑PHL | | | | 8 | 4.6 | 4.6 | 3.9 | 3.2 | 2.8 | 2.1 |
| ↑PZH | OE | Q | MAX | 8 | 4.7 | 4.7 | 4.7 | 3.4 | 2.9 | 2.2 |
| ↑PZL | | | | 8 | 4.7 | 4.7 | 4.7 | 3.4 | 2.9 | 2.2 |
| ↑PHZ | OE | Q | MAX | 7 | 5.9 | 5.9 | 4.1 | 3.9 | 4.6 | 2.5 |
| ↑PIZ | | | | 7 | 5.9 | 5.9 | 4.1 | 3.9 | 4.6 | 2.5 |

UNIT: ns

AUC: Preview

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|--------|--------|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q _O |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT | LVC 3V | LVC verA 3V | LVCH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|---------|----------|------|------|------|------|--------|-------------|---------|----------|------|
| I _{CC} | MAX | 72 | 5 | 5 | 0.08 | 0.08 | 0.04 | 0.04 | 0.04 | 0.02 | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -8 | -8 | -24 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 8 | 8 | 24 | 24 | 24 | 24 | mA |

| PARAMETER | MAX or MIN | AVC 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------------|------------|--------|----------|----------|-----------|-----------|------|
| I _{CC} | MAX | 0.04 | 0.02 | 0.02 | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -12 | -8 | -9 | -8 | -9 | mA |
| I _{OL} | MAX | 12 | 8 | 9 | 8 | 9 | mA |

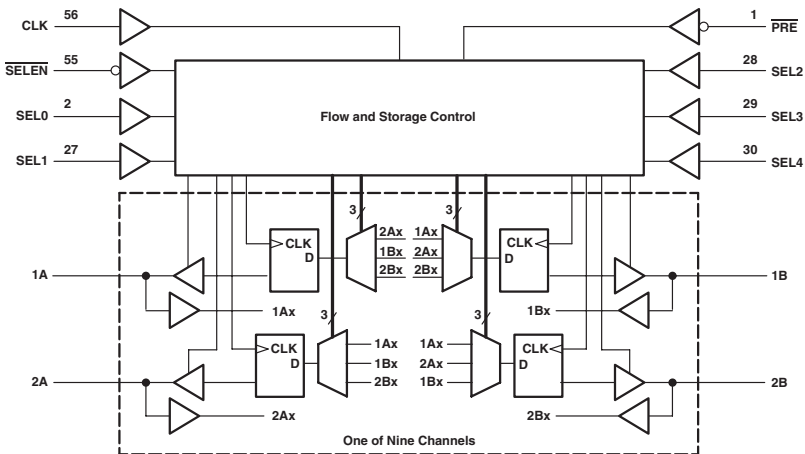
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ALVTH 3V | AC | ACT | AHC | AHCT | LVC 3V |
|-------------------------------|------------------------------|--------|------------|-----|---------|----------|------|------|------|------|--------|
| f _{max} | | | MIN | 150 | 160 | 250 | 100 | 65 | 110 | 110 | 100 |
| t _w Pulse duration | CLK high | | MIN | 3.3 | 3 | 1.5 | 5 | 7.5 | 5 | 6.5 | 4 |
| | CLK low | | | 3.3 | 3 | 1.5 | 5 | 4.5 | 5 | 6.5 | 4 |
| t _{su} Setup time | Data before CLK ↑, data high | | MIN | 1.1 | 1.8 | 1 | 5 | 4.5 | 3 | 2.5 | 2 |
| | Data before CLK ↑, data low | | | 1.1 | 1.8 | 1.5 | 5 | 4.5 | 3 | 2.5 | 2 |
| t _h Hold time | Data after CLK ↑, data high | | MIN | 1.3 | 0.8 | 0.5 | 0 | 6.5 | 2 | 2.5 | 1.5 |
| | Data after CLK ↑, data low | | | 1.3 | 0.8 | 1 | 0 | 6.5 | 2 | 2.5 | 1.5 |
| TP _{LH} | CLK | Q | MAX | 6.2 | 4.5 | 3.2 | 10.8 | 12.4 | 11.5 | 11.5 | 7.5 |
| TP _{HL} | | | | 5.9 | 4 | 3.2 | 10.6 | 12.2 | 11.5 | 11.5 | 7.5 |
| TP _{ZH} | OE | Q | MAX | 5.6 | 4.5 | 3.8 | 10.2 | 11.9 | 11.5 | 11.5 | 7.5 |
| TP _{ZL} | | | | 5.3 | 4.4 | 3.3 | 12.1 | 13.4 | 11.5 | 11.5 | 7.5 |
| TP _{HZ} | OE | Q | MAX | 8.2 | 5 | 4.6 | 8.2 | 10.4 | 11.5 | 12 | 7 |
| TP _{LZ} | | | | 6.6 | 4.6 | 4.2 | 7.9 | 9.8 | 11.5 | 12 | 7 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVC verA 3V | LVCH 3V | ALVCH 3V | AVC 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|-------------------------------|------------------------------|--------|------------|-------------|---------|----------|--------|----------|----------|-----------|-----------|
| f _{max} | | | MIN | 150 | 150 | 150 | 200 | 250 | 250 | 250 | 250 |
| t _w Pulse duration | CLK high | | MIN | 3.3 | 3.3 | 3.3 | 2.5 | 1.9 | 1.9 | 1.9 | 1.9 |
| | CLK low | | | 3.3 | 3.3 | 3.3 | 2.5 | 1.9 | 1.9 | 1.9 | 1.9 |
| t _{su} Setup time | Data before CLK ↑, data high | | MIN | 1.9 | 1.9 | 1.9 | 1.4 | 0.6 | 0.6 | 0.6 | 0.6 |
| | Data before CLK ↑, data low | | | 1.9 | 1.9 | 1.9 | 1.4 | 0.6 | 0.6 | 0.6 | 0.6 |
| t _h Hold time | Data after CLK ↑, data high | | MIN | 1.9 | 1.1 | 0.5 | 1.1 | 0.4 | 0.4 | 0.4 | 0.4 |
| | Data after CLK ↑, data low | | | 1.9 | 1.1 | 0.5 | 1.1 | 0.4 | 0.4 | 0.4 | 0.4 |
| TP _{LH} | CLK | Q | MAX | 4.5 | 4.5 | 4.2 | 3.3 | 2.8 | 2.2 | 2.8 | 2.2 |
| TP _{HL} | | | | 4.5 | 4.5 | 4.2 | 3.3 | 2.8 | 2.2 | 2.8 | 2.2 |
| TP _{ZH} | OE | Q | MAX | 4.6 | 4.6 | 4.8 | 3.4 | 2.9 | 2.2 | 2.9 | 2.2 |
| TP _{ZL} | | | | 4.6 | 4.6 | 4.8 | 3.4 | 2.9 | 2.2 | 2.9 | 2.2 |
| TP _{HZ} | OE | Q | MAX | 5.5 | 5.5 | 4.3 | 3.9 | 4.5 | 2.2 | 4.5 | 2.2 |
| TP _{LZ} | | | | 5.5 | 5.5 | 4.3 | 3.9 | 4.5 | 2.2 | 4.5 | 2.2 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|-----------|------------------|
| CLK | SEND PORT | RECEIVE PORT |
| X | X | B ₀ ↑ |
| X | L | L |
| X | H | H |
| ↑ | L | L |
| ↑ | H | H |
| H | X | B ₀ ↑ |
| L | X | B ₀ ↑ |

↑ Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

| PRE | SELEN | CLK | INPUTS | | | | | | DATA FLOW |
|-----|-------|-----|--------|------|------|------|------|---|-----------------------|
| | | | SEL0 | SEL1 | SEL2 | SEL3 | SEL4 | | |
| H | X | X | X | X | X | X | X | X | All outputs disabled |
| L | H | ↑ | X | X | X | X | X | X | No change |
| L | L | ↑ | 0 | 0 | 0 | 0 | 0 | 0 | None, all I/Os off |
| L | L | ↑ | 0 | 0 | 0 | 0 | 0 | 1 | Not used |
| L | L | ↑ | 0 | 0 | 0 | 0 | 1 | 0 | Not used |
| L | L | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | Not used |
| L | L | ↑ | 0 | 0 | 0 | 1 | 0 | 0 | Not used |
| L | L | ↑ | 0 | 0 | 0 | 1 | 0 | 1 | Not used |
| L | L | ↑ | 0 | 0 | 1 | 1 | 1 | 0 | Not used |
| L | L | ↑ | 0 | 0 | 1 | 1 | 1 | 1 | Not used |
| L | L | ↑ | 0 | 1 | 0 | 0 | 0 | 0 | 2A to 1A and 1B to 2B |
| L | L | ↑ | 0 | 1 | 0 | 0 | 0 | 1 | 2A to 1A |
| L | L | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 2B to 1B |
| L | L | ↑ | 0 | 1 | 0 | 1 | 1 | 1 | 2A to 1A and 2B to 1B |
| L | L | ↑ | 0 | 1 | 1 | 0 | 0 | 0 | 1A to 2A and 1B to 2B |
| L | L | ↑ | 0 | 1 | 1 | 0 | 1 | 0 | 1A to 2A |
| L | L | ↑ | 0 | 1 | 1 | 1 | 1 | 0 | 1B to 2B |
| L | L | ↑ | 0 | 1 | 1 | 1 | 1 | 1 | 1A to 2A and 2B to 1B |
| L | L | ↑ | 1 | 0 | 0 | 0 | 0 | 0 | 1A to 1B and 2B to 2A |
| L | L | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 1A to 1B |
| L | L | ↑ | 1 | 0 | 0 | 0 | 1 | 0 | 2A to 2B |
| L | L | ↑ | 1 | 0 | 0 | 1 | 1 | 1 | 1A to 1B and 2A to 2B |
| L | L | ↑ | 1 | 0 | 1 | 0 | 0 | 0 | 1B to 1A and 2A to 2B |
| L | L | ↑ | 1 | 0 | 1 | 0 | 1 | 1 | 1B to 1A |
| L | L | ↑ | 1 | 0 | 1 | 1 | 0 | 0 | 2B to 2A |
| L | L | ↑ | 1 | 0 | 1 | 1 | 1 | 1 | 1B to 1A and 2B to 2A |
| L | L | ↑ | 1 | 1 | 0 | 0 | 0 | 0 | 2B to 1A and 2A to 1B |
| L | L | ↑ | 1 | 1 | 0 | 0 | 0 | 1 | 1B to 2A |
| L | L | ↑ | 1 | 1 | 0 | 1 | 0 | 0 | 2B to 1A |
| L | L | ↑ | 1 | 1 | 0 | 1 | 1 | 1 | 2B to 1A and 1B to 2A |
| L | L | ↑ | 1 | 1 | 1 | 0 | 0 | 0 | 1A to 2B and 1B to 2A |
| L | L | ↑ | 1 | 1 | 1 | 0 | 1 | 0 | 1A to 2B |
| L | L | ↑ | 1 | 1 | 1 | 1 | 0 | 0 | 2A to 1B |
| L | L | ↑ | 1 | 1 | 1 | 1 | 1 | 1 | 1A to 2B and 2A to 1B |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

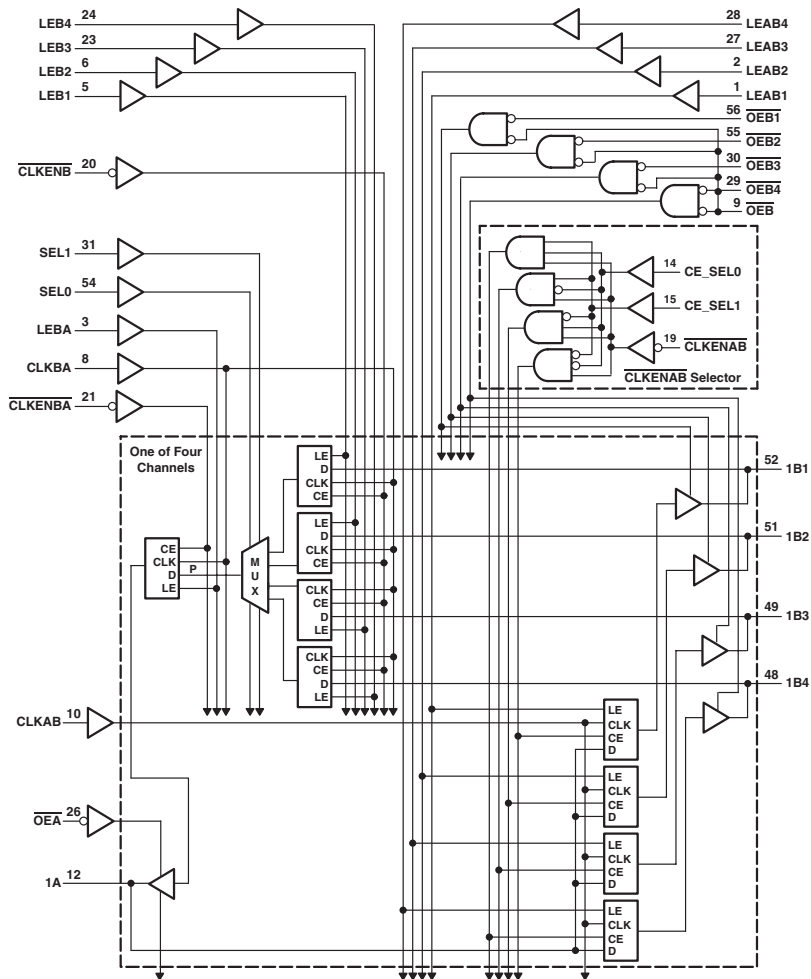
| PARAMETER | MAX or MIN | ALVCH 3V | ALVC HR 3V | UNIT |
|-----------------|------------|-------------|------------------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -24 | -12 | mA |
| I _{OL} | MAX | 24 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | ALVC HR 3V |
|--|--------------------------|--------|------------|-------------|------------------|
| f _{max} | | | MIN | 120 | 120 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 | 3 |
| t _{su} Setup time | A or B data before CLK ↑ | | MIN | 1.4 | 1.4 |
| | SEL before CLK ↑ | | MIN | 3.5 | 3.5 |
| | SELEN before CLK ↑ | | MIN | 1.8 | 1.8 |
| | PRE before CLK ↑ | | MIN | 0.7 | 0.7 |
| t _h Hold time | A or B data after CLK ↑ | | MIN | 1 | 1 |
| | SEL after CLK ↑ | | MIN | 0 | 0 |
| | SELEN after CLK ↑ | | MIN | 0.8 | 0.8 |
| t _{pd} | CLK | A or B | MAX | 5.1 | 6.2 |
| t _{en} | CLK | A or B | MAX | 5.7 | 6.8 |
| t _{ris} | CLK | A or B | MAX | 5.7 | 6.1 |
| | PRE | | | 6.1 | 6.4 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE
A-TO-B OUTPUT ENABLE

| INPUTS | | OUTPUT |
|--------|------|--------|
| OEB | OEBn | Bn |
| H | H | Z |
| H | L | Z |
| L | H | Z |
| L | L | Active |

Tn = 1, 2, 3, 4

A-TO-B OUTPUT ENABLE
 (assuming OEB = L, OEBn = L) ‡

| INPUTS | | | | | | | | OUTPUTS | | | |
|---------|---------|---------|-------|--------|-------|-------|-------|---------|----|----|----|
| CLKENAB | CE_SEL1 | CE_SEL0 | CLKAB | LEAB1 | LEAB2 | LEAB3 | LEAB4 | B1 | B2 | B3 | B4 |
| X | X | X | X | H or L | H | L | L | A | A0 | A0 | A0 |
| X | X | X | X | H or L | H | L | L | A | A | A | A0 |
| L | X | X | L | L | L | L | L | A0 | A0 | A0 | A0 |
| L | L | L | L | ↑ | L | L | L | A | A0 | A0 | A0 |
| L | L | L | H | ↑ | L | L | L | A0 | A | A0 | A0 |
| L | L | H | L | ↑ | L | L | L | A0 | A0 | A | A0 |
| L | H | H | L | ↑ | L | L | L | A0 | A0 | A0 | A |
| L | H | H | ↑ | L | L | L | L | A0 | A0 | A0 | A0 |
| H | X | X | ↑ | L | L | L | L | A0 | A0 | A0 | A0 |

B-TO-A STORAGE

(after point P)

| INPUTS | | | | | | | | P |
|--------|-------|------|------|------|------|------|------|------|
| CLKENB | CLKBA | LEB1 | LEB2 | LEB3 | LEB4 | SEL1 | SEL0 | P |
| X | X | H | L | L | L | L | L | B1 |
| X | X | L | H | L | L | L | H | B2 |
| X | X | L | L | H | L | H | L | B3 |
| X | X | L | L | L | H | H | H | B4 |
| L | ↑ | L | L | L | L | L | L | B1 |
| L | ↑ | L | L | L | L | L | L | B2 |
| L | ↑ | L | L | L | L | L | L | B3 |
| L | ↑ | L | L | L | L | L | L | B4 |
| L | L | L | L | L | L | L | L | B10† |
| L | L | L | L | L | L | L | L | B20† |
| L | L | L | L | L | L | L | L | B30† |
| L | L | L | L | L | L | L | L | B40† |

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE

(after point P)

| INPUTS | | | | | | OUTPUT | |
|---------|-------|------|-----|---|---|--------|-----|
| CLKENBA | CLKBA | LEBA | OEA | B | A | A | A |
| X | X | X | H | X | X | Z | Z |
| X | X | X | H | L | L | L | L |
| X | X | H | L | H | H | H | H |
| H | X | L | L | X | X | A0† | A0† |
| L | ↑ | L | L | L | L | L | L |
| L | ↑ | L | L | L | H | H | H |
| L | L | L | L | X | X | A0† | A0† |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | UNIT |
|-----------|------------|------|------|
| Icc | MAX | 32 | mA |
| Ioh | MAX | -32 | mA |
| Iol | MAX | 64 | mA |

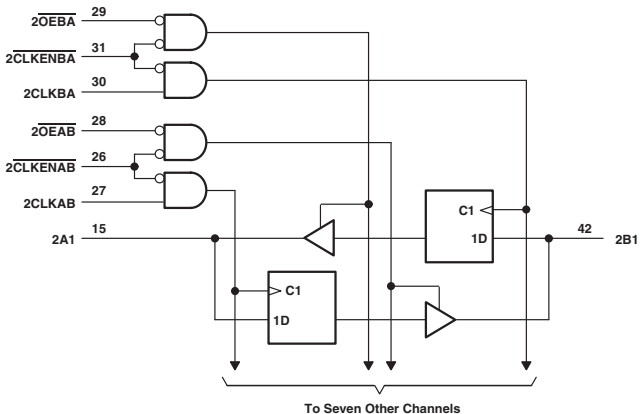
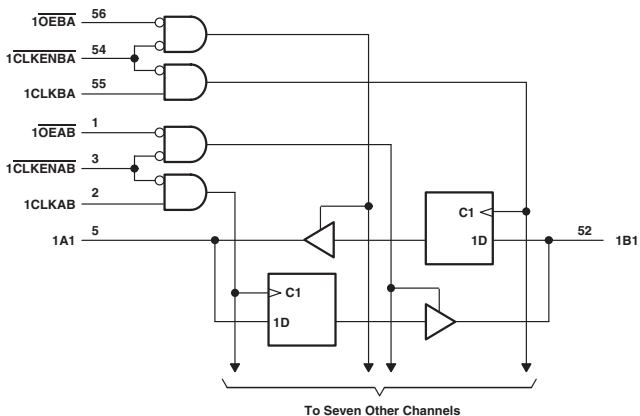
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | MAX or MIN | ABTH |
|-------------------------------|----------------------------------|-----------------|---------|
| t _{max} | | MIN | 160 |
| t _w Pulse duration | CLKAB high or low | MIN | 3.8 |
| | CLKBA high or low | MIN | 4.5 |
| | LEAB1, 2, 3 or 4 high | MIN | 2.2 |
| | LEBA high | MIN | 2.1 |
| | LEB1, 2, 3 or 4 high | MIN | 2.4 |
| t _{su} Setup time | Before CLKAB ↑ | A bus | MIN 2.5 |
| | | CE_SEL0/1 | MIN 3.2 |
| | | CLKENAB | MIN 3.2 |
| | Before LEAB1, 2, 3, or 4 ↓ A bus | A bus | MIN 3.6 |
| | | B bus | MIN 3.8 |
| | | CLKENB | MIN 2.3 |
| | Before CLKBA ↑ | CLKENBA | MIN 2.5 |
| | | LEB1, 2, 3 or 4 | MIN 4.3 |
| | | SEL0/1 | MIN 4.5 |
| | Before LEB1, 2, 3, or 4 ↓ B bus | B bus | MIN 3.2 |
| | | B bus | MIN 4 |
| | | LEB1, 2, 3 or 4 | MIN 4.4 |
| t _h Hold time | after CLKAB ↑ | SEL0/1 | MIN 4.3 |
| | | A bus | MIN 0.5 |
| | | CE_SEL0/1 | MIN 1.1 |
| | after LEAB1, 2, 3, or 4 ↓ A bus | CLKENAB | MIN 0.5 |
| | | A bus | MIN 1.2 |
| | | B bus | MIN 1.3 |
| | after CLKBA ↑ | CLKENB | MIN 1 |
| | | CLKENBA | MIN 1 |
| | | SEL0/1 | MIN 0 |
| | after LEB1, 2, 3, or 4 ↓ B bus | B bus | MIN 1.5 |
| | | B bus | MIN 0.4 |
| | | SEL0/1 | MIN 0.1 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH |
|------------------|----------------------------|--------|------------|------|
| TP _{LH} | B | A | MAX | 6.5 |
| TP _{HL} | | | | 6.5 |
| IP _{ZH} | \overline{OEA} | A | MAX | 5.6 |
| IP _{ZL} | | | | 5.2 |
| IP _{HZ} | \overline{OEA} | A | MAX | 5.9 |
| IP _{LZ} | | | | 6.5 |
| EP _{LH} | A | B | MAX | 5.7 |
| EP _{HL} | | | | 5.7 |
| IP _{ZH} | \overline{OEB} | B | MAX | 6.4 |
| IP _{ZL} | | | | 6.3 |
| TP _{HZ} | \overline{OEB} | B | MAX | 7 |
| IP _{LZ} | | | | 6.1 |
| IP _{ZH} | $\overline{OEB1, 2, 3, 4}$ | B | MAX | 5.8 |
| IP _{ZL} | | | | 5.6 |
| IP _{HZ} | $\overline{OEB1, 2, 3, 4}$ | B | MAX | 6.1 |
| IP _{LZ} | | | | 5.3 |
| EP _{LH} | CLKBA | A | MAX | 7.4 |
| EP _{HL} | | | | 7.7 |
| TP _{LH} | CLKAB | B | MAX | 6.2 |
| TP _{HL} | | | | 5.9 |
| IP _{ZH} | LEBA | A | MAX | 5.6 |
| IP _{ZL} | | | | 5.3 |
| EP _{LH} | LEAB1, 2, 3, 4 | B | MAX | 5.8 |
| EP _{HL} | | | | 5.6 |
| TP _{LH} | LEBA1, 2, 3, 4 | A | MAX | 7.2 |
| TP _{HL} | | | | 6.8 |
| IP _{LH} | SEL | A | MAX | 7.5 |
| IP _{HL} | | | | 6.9 |

 UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---------|-------|------|---|------------------|
| CLKENAB | CLKAB | OEAB | A | B |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | L | L | X | B ₀ † |
| L | ↑ | L | L | L |
| L | ↑ | L | H | H |

† A-to-B data flow is shown: B-to-A flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

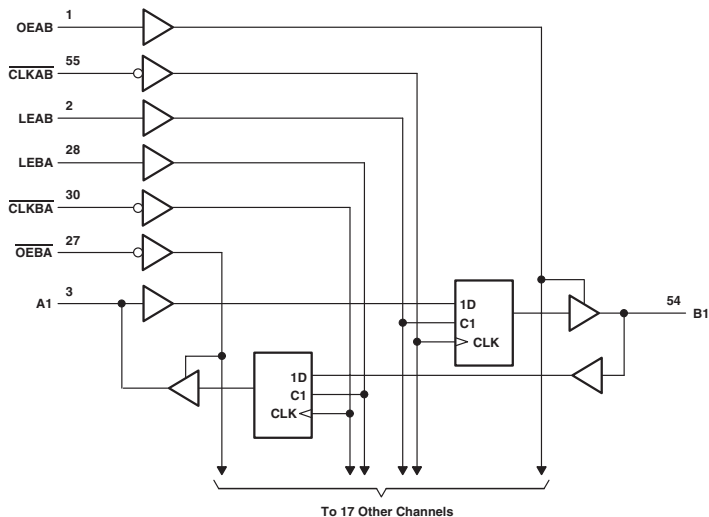
| PARAMETER | MAX or MIN | ABT | ACT | UNIT |
|-----------------|------------|-----|------|------|
| I _{CC} | MAX | 35 | 0.08 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT |
|--|-------|--------|------------|-----|------|
| f _{max} | | | MIN | 150 | 55 |
| t _w Pulse duration, CLKAB or CLKBA high | | | MIN | 3.3 | 4 |
| t _w Pulse duration, CLKAB or CLKBA low | | | | 3.3 | 8.5 |
| t _{su} Setup time, data before CLKAB ↑ or CLKBA ↑ | | | MIN | 4 | 6 |
| t _h Hold time, data after CLKAB ↑ or CLKBA ↑ | | | MIN | 1 | 1 |
| t _{PLH} | CLK | A or B | MAX | 4.9 | 11.8 |
| t _{PHL} | | | | 4.9 | 11.7 |
| t _{PZH} | OE | A or B | MAX | 4.9 | 11.9 |
| t _{PZL} | | | | 6.8 | 13.4 |
| t _{PHZ} | OE | A or B | MAX | 5.5 | 9.9 |
| t _{PLZ} | | | | 5.3 | 9.5 |
| t _{PZH} | CLKEN | A or B | MAX | 5.7 | 12.5 |
| t _{PZL} | | | | 7.2 | 14.3 |
| t _{PHZ} | CLKEN | A or B | MAX | 5.8 | 11.2 |
| t _{PLZ} | | | | 5.4 | 10.9 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|------|-------|---|-----------------------------|
| OEAB | LEAB | CLKAB | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↓ | L | L |
| H | L | ↓ | H | H |
| H | L | H | X | B ₀ [†] |
| H | L | L | X | B ₀ [‡] |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

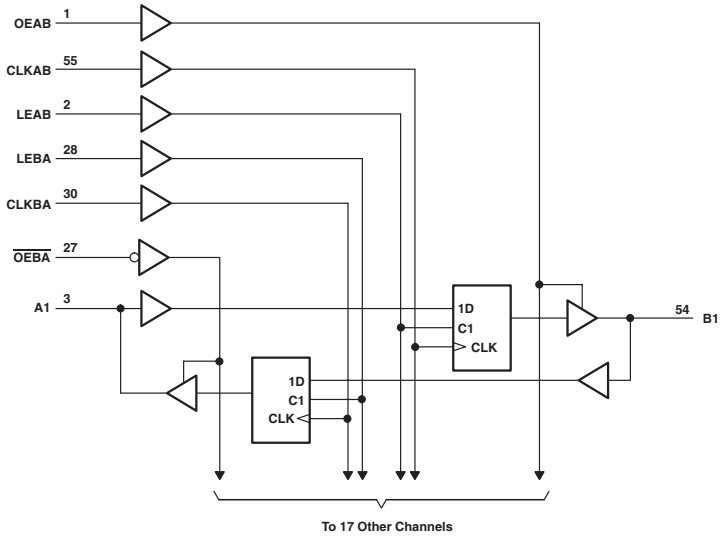
| PARAMETER | MAX or MIN | ABT | LVTH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|------------|-------------|------|
| I _{CC} | MAX | 36 | 5 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ALVCH 3V |
|-------------------------------|---------------------------------------|--------|------------|-----|------------|-------------|
| f _{max} | | | MIN | 150 | 150 | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 2.5 | 3.3 | 3.3 |
| | CLKAB or CLKBA high or low | | | 3 | 3.3 | 3.3 |
| t _{su} Setup time | A before CLKAB ↓ | | MIN | 3 | 2.9 | 1.3 |
| | B before CLKBA ↓ | | | 3 | 2.9 | 1.3 |
| | A before LEAB ↓ or LEBA ↓ CLK high | | | 1 | 1.4 | 1 |
| | A before LEAB ↓ or LEBA ↓ CLK low | | | 2.5 | 2.9 | 1.4 |
| t _h Hold time | A after CLKAB ↓ or B after CLKBA ↓ | | MIN | 0 | 0.4 | 1.3 |
| | A after LEAB ↓ or B after LEBA ↓ high | | | 2 | 1.6 | 1.5 |
| | A after LEAB ↓ or B after LEBA ↓ low | | | 2 | 1.6 | 1.2 |
| t _{PLH} | A or B | B or A | MAX | 4 | 3.7 | 3.9 |
| t _{PHL} | | | | 4.9 | 3.7 | 3.9 |
| t _{PZH} | LEAB or LEBA | B or A | MAX | 5 | 5.1 | 4.7 |
| t _{PZL} | | | | 5 | 5.1 | 4.7 |
| t _{PHZ} | CLKAB or CLKBA | B or A | MAX | 5.3 | 5 | 5.5 |
| t _{PLZ} | | | | 5.3 | 5 | 5.5 |
| t _{PZH} | OEAB | B | MAX | 5.1 | 4.8 | 4.6 |
| t _{PZL} | | | | 5.4 | 4.8 | 4.6 |
| t _{PHZ} | OEAB | B | MAX | 6.5 | 5.8 | 5 |
| t _{PLZ} | | | | 5.4 | 5.8 | 5 |
| t _{PZH} | OEBA | A | MAX | 5.1 | 4.8 | 5.2 |
| t _{PZL} | | | | 5.4 | 4.8 | 5.2 |
| t _{PHZ} | OEBA | A | MAX | 6.5 | 5.8 | 4.3 |
| t _{PLZ} | | | | 5.4 | 5.8 | 4.3 |

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|------|-------|---|-----------------------------|
| OEAB | LEAB | CLKAB | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | H | X | B ₀ [†] |
| H | L | L | X | B ₀ [‡] |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVTH 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|-----|------------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 76 | 5 | 0.04 | 0.02 | 0.02 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 8 | 9 | mA |

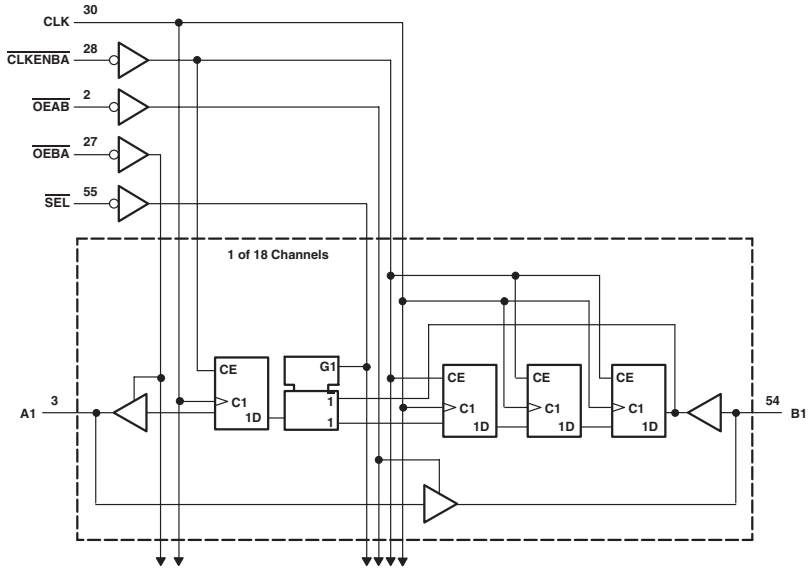
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V |
|-------------------------------|------------------------------------|--------|------------|-----|------------|-------------|-------------|-------------|
| f _{max} | | | MIN | 105 | 150 | 150 | 300 | 350 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 3.3 | 3.3 | 3.3 | 1.5 | 1.5 |
| | CLKAB or CLKBA high or low | | MIN | 4.7 | 3.3 | 3.3 | 1.5 | 1.5 |
| t _{su} Setup time | A before CLKAB ↑ | | MIN | 3.5 | 2.1 | 1.7 | 0.6 | 0.6 |
| | B before CLKBA ↑ | | MIN | 3.5 | 2.1 | 1.7 | 0.6 | 0.6 |
| | A before LEAB ↓ or LEBA ↓ CLK high | | MIN | 4 | 2.4 | 1.5 | 0.3 | 0.3 |
| t _h Hold time | A before LEAB ↓ or LEBA ↓ CLK low | | MIN | 1.5 | 1.4 | 1 | 0.3 | 0.3 |
| | A after CLKAB ↑ or B after CLKBA ↑ | | MIN | 1 | 1 | 0.7 | 0.9 | 0.9 |
| | A after LEAB ↓ or B after LEBA ↓ | | MIN | 2.5 | 1.7 | 1.4 | 1.2 | 1.2 |
| TP _{LH} | A or B | B or A | MAX | 3.7 | 3.7 | 3.9 | 2.8 | 2.3 |
| TP _{HL} | | | | 4 | 3.7 | 3.9 | 2.8 | 2.3 |
| TP _{ZH} | LEAB or LEBA | B or A | MAX | 5.1 | 5.1 | 4.6 | 3.8 | 3 |
| TP _{ZL} | | | | 4.4 | 5.1 | 4.6 | 3.8 | 3 |
| TP _{HZ} | CLKAB or CLKBA | B or A | MAX | 5 | 5.1 | 4.9 | 3.3 | 2.7 |
| TP _{LZ} | | | | 4.4 | 5.1 | 4.9 | 3.3 | 2.7 |
| TP _{ZH} | OEAB | B | MAX | 4.7 | 4.8 | 4.6 | 3.4 | 2.8 |
| TP _{ZL} | | | | 6.5 | 4.8 | 4.6 | 3.4 | 2.8 |
| TP _{HZ} | OEAB | B | MAX | 5.8 | 5.8 | 5 | 3.2 | 3.1 |
| TP _{LZ} | | | | 4.9 | 5.8 | 5 | 3.2 | 3.1 |
| TP _{ZH} | OEBA | A | MAX | 4.7 | 4.8 | 5 | 3.7 | 3 |
| TP _{ZL} | | | | 6.5 | 4.8 | 5 | 3.7 | 3 |
| TP _{HZ} | OEBA | A | MAX | 5.8 | 5.8 | 4.2 | 5.2 | 3 |
| TP _{LZ} | | | | 4.9 | 5.8 | 4.2 | 5.2 | 3 |

UNIT f_{max} : MHz other : ns

AUC:Preview

Logic Diagram



FUNCTION TABLE
B-TO-A STORAGE (OEBA = L)

| CLKENBA | INPUTS | | | OUTPUT A |
|---------|--------|-----|---|------------------|
| | CLK | SEL | B | |
| H | X | X | X | A ₀ † |
| L | ↑ | H | L | L |
| L | ↑ | H | H | H |
| L | ↑ | L | L | L‡ |
| L | ↑ | L | H | H‡ |

† Output level before the indicated steady-state input conditions were established.

‡ Four positive CLK edges are needed to propagate data from B to A when SEL is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

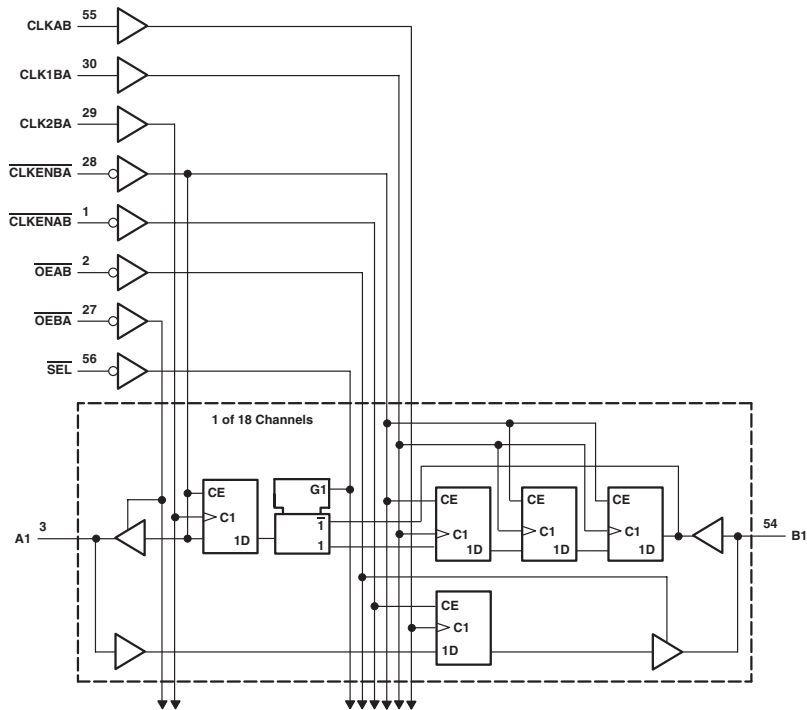
| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|--|----------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 |
| t _{su} Setup time | B data before CLK ↑ | | MIN | 1.1 |
| | SEL before CLK ↑ | | MIN | 2.1 |
| | CLKENBA before CLK ↑ | | MIN | 2 |
| t _h Hold time | B data after CLK ↑ | | MIN | 1.2 |
| | SEL after CLK ↑ | | MIN | 0.8 |
| | CLKENBA after CLK ↑ | | MIN | 0.3 |
| t _{pd} | A | B | MAX | 3.2 |
| | CLK | A | | 5.2 |
| t _{en} | OEAB or OEBA | A or B | MAX | 5.1 |
| t _{is} | OEAB or OEBA | A or B | MAX | 4.9 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

A-TO-B STORAGE ($\overline{OEAB} = L$)

| INPUTS | | | OUTPUT B |
|---------|-------|---|----------|
| CLKENAB | CLKAB | A | B |
| H | X | X | Bg† |
| L | ↑ | L | L |
| L | ↑ | H | H |

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA} = L$)

| INPUTS | | | | | OUTPUT A |
|--------|--------|--------|-----|---|----------|
| CLKENA | CLK2BA | CLK1BA | SEL | B | A |
| H | X | X | X | X | Ag† |
| L | ↑ | X | H | L | L |
| L | ↑ | X | H | H | H |
| L | ↑ | ↑ | L | L | L‡ |
| L | ↑ | ↑ | L | H | H‡ |

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------|------------|-------------|------|
| Icc | MAX | 0.04 | mA |
| Ioh | MAX | -24 | mA |
| Iol | MAX | 24 | mA |

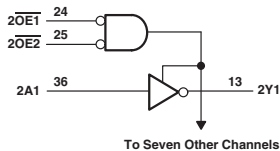
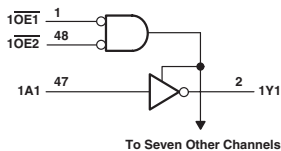
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|------------------|--|-------------------------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w | Pulse duration, CLK high or low | | MIN | 3 |
| t _{su} | Setup time | A data before CLKAB ↑ | MIN | 1.3 |
| | | B data before CLK2BA ↑ | MIN | 1.7 |
| | | B data before CLK1BA ↑ | MIN | 1.1 |
| | | SEL before CLK2BA ↑ | MIN | 3.3 |
| | | CLKENAB before CLKAB ↑ | MIN | 1.6 |
| | | CLKENBA before CLK1BA ↑ | MIN | 2.1 |
| t _h | Hold time | CLKENBA before CLK2BA ↑ | MIN | 2.2 |
| | | A data after CLKAB ↑ | MIN | 0.9 |
| | | B data after CLK2BA ↑ | MIN | 0.6 |
| | | B data after CLK1BA ↑ | MIN | 1 |
| | | SEL after CLK2BA ↑ | MIN | 0.1 |
| | | CLKENAB after CLKAB ↑ | MIN | 0.3 |
| | | CLKENBA after CLK1BA ↑ | MIN | 0.1 |
| | | CLKENBA after CLK2BA ↑ | MIN | 0 |
| t _{pd} | CLKAB or CLK2BA | A or B | MAX | 4.2 |
| t _{en} | \overline{OEAB} or \overline{OEBA} | A or B | MAX | 5.1 |
| t _{dis} | \overline{OEAB} or \overline{OEBA} | A or B | MAX | 4.9 |

UNIT f_{max} : MHz other : ns

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | AHC | AHCT | LVCH 3V | UNIT |
|-----------------|------------|-----|------|------|------|------------|------|
| I _{CC} | MAX | 34 | 0.08 | 0.04 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -32 | -24 | -8 | -8 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 8 | 8 | 24 | mA |

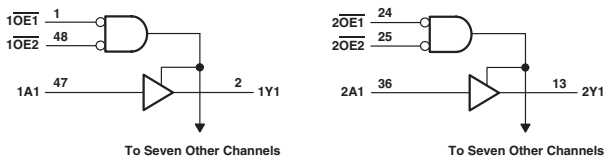
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT | AHC | AHCT | LVCH 3V |
|------------------|-----------------|--------|------------|-----|------|------|------|------------|
| t _{PLH} | A | Y | MAX | 4.1 | 7.5 | 8.5 | 10.5 | 3.7 |
| t _{PHL} | | | | 4.3 | 9.5 | 8.5 | 10.5 | 3.7 |
| t _{PZH} | \overline{OE} | Y | MAX | 5.1 | 8.9 | 10.5 | 13 | 4.8 |
| t _{PZL} | | | | 5.9 | 10.5 | 10.5 | 13 | 4.8 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.7 | 11.9 | 10.5 | 13 | 5.9 |
| t _{PLZ} | | | | 4.7 | 11.1 | 10.5 | 13 | 5.9 |

UNIT: ns

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVTH 3V | ACT | AHC | AHCT | LVCH 3V | UNIT |
|-----------------|------------|-----|------------|------|------|------|------------|------|
| I _{CC} | MAX | 34 | 5 | 0.08 | 0.04 | 0.04 | 0.02 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -8 | -8 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 8 | 8 | 24 | mA |

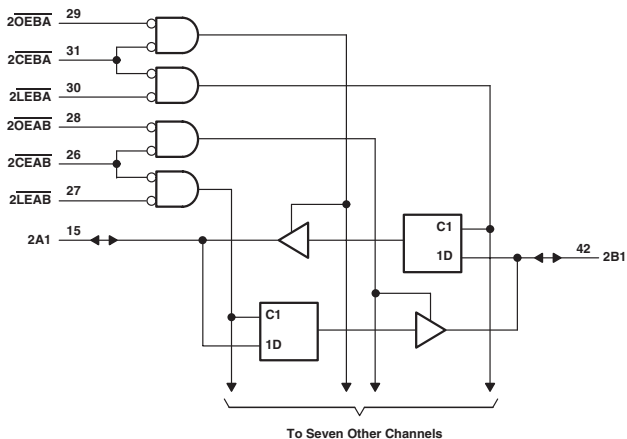
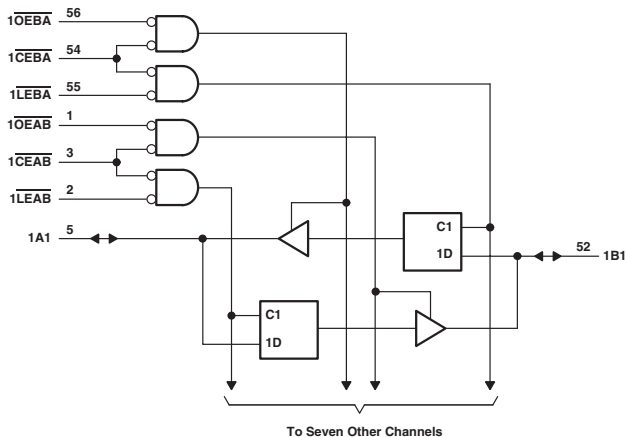
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | ACT | AHC | AHCT | LVCH 3V |
|------------------|-----------------|--------|------------|-----|------------|------|------|------|------------|
| t _{PLH} | A | Y | MAX | 3.4 | 3.5 | 9 | 8.5 | 10.5 | 4.2 |
| | | | | 4.2 | 3.5 | 9.2 | 8.5 | 10.5 | 4.2 |
| t _{PZH} | \overline{OE} | Y | MAX | 5.2 | 4.6 | 9.7 | 10.5 | 13 | 5.6 |
| | | | | 6 | 4.6 | 11 | 10.5 | 13 | 5.6 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.4 | 5.9 | 11.3 | 10.5 | 13 | 6.8 |
| | | | | 4.3 | 5.4 | 10.7 | 10.5 | 13 | 6.8 |

UNIT: ns

16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | | | OUTPUT |
|--------|------|------|---|------------------|
| CEAB | LEAB | OEAB | A | B |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B ₀ † |
| L | L | L | L | L |
| L | L | L | H | H |

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

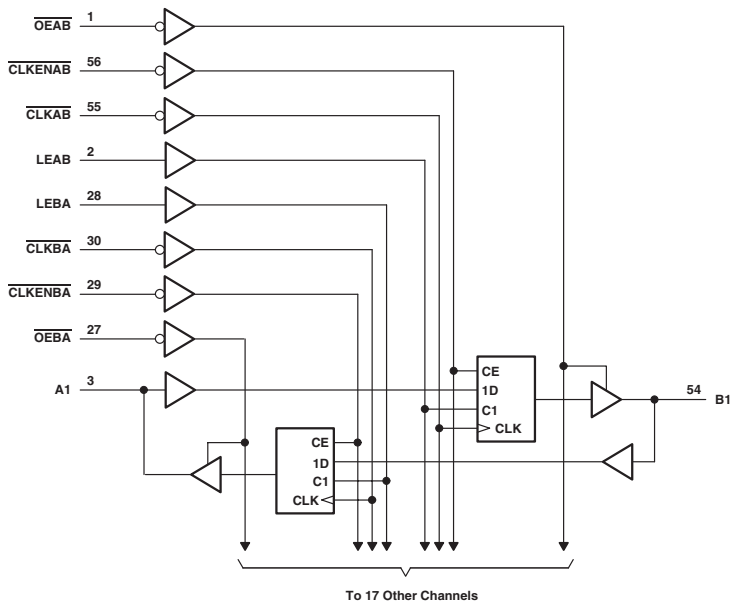
| PARAMETER | MAX or MIN | ABT | LVT 3V | LVTH 3V | AC | ACT | LVCH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|--------|---------|------|------|---------|----------|------|
| I _{CC} | MAX | 35 | 5 | 5 | 0.08 | 0.08 | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | AC | ACT | LVCH 3V | ALVCH 3V |
|---|------------------------------------|--------|------------|-----|--------|---------|------|------|---------|----------|
| t _w Pulse duration, LEAB or LEBA low | | | MIN | 4 | 3.3 | 3.3 | 4 | 7.5 | 3.3 | 3.3 |
| t _{su} Setup time | Data before LEAB † or LEBA †, high | | MIN | 1.5 | 0.8 | 0.5 | 1 | 2.5 | 1.1 | 1.2 |
| | Data before LEAB † or LEBA †, low | | MIN | 3.5 | 1.5 | 0.8 | 1 | 2.5 | 1.1 | 1.2 |
| | Data before CEAB † or CEBA †, high | | MIN | - | 0.7 | 0 | - | - | 1.1 | 1.2 |
| | Data before CEAB † or CEBA †, low | | MIN | - | 1.6 | 0.6 | - | - | 1.1 | 1.2 |
| t _h Hold time | Data after LEAB † or LEBA †, high | | MIN | 1.5 | 0.8 | 1.5 | 3 | 4 | 1.9 | 1.3 |
| | Data after LEAB † or LEBA †, low | | MIN | 2 | 1.2 | 1.2 | 3 | 4 | 1.9 | 1.3 |
| | Data after CEAB † or CEBA †, high | | MIN | - | 0.8 | 1.7 | - | - | 1.9 | 1.3 |
| | Data after CEAB † or CEBA †, low | | MIN | - | 1.3 | 1.6 | - | - | 1.9 | 1.3 |
| †P _{LH} | A or B | B or A | MAX | 3.8 | 4.6 | 3.2 | 8.8 | 10.5 | 5.4 | 4.3 |
| †P _{HL} | | | | 5.1 | 4.6 | 3.2 | 9.2 | 11.6 | 5.4 | 4.3 |
| †P _{LH} | LE | A or B | MAX | 5.2 | 6.3 | 3.9 | 11.5 | 13.8 | 6.1 | 5 |
| †P _{HL} | | | | 5.6 | 6 | 3.9 | 10.9 | 13.5 | 6.1 | 5 |
| †P _{ZH} | OE | A or B | MAX | 5.2 | 5.8 | 4.3 | 9.6 | 11.4 | 6.3 | 5.3 |
| †P _{ZL} | | | | 7 | 6.2 | 4.3 | 11.3 | 13.2 | 6.3 | 5.3 |
| †P _{PHZ} | OE | A or B | MAX | 5.7 | 6.5 | 4.7 | 8.9 | 11.1 | 6.3 | 4.6 |
| †P _{PLZ} | | | | 4.6 | 5.8 | 4.4 | 8.4 | 9.6 | 6.3 | 4.6 |
| †P _{ZH} | CE | A or B | MAX | 6.2 | 6 | 4.5 | 9.8 | 11.7 | 6.6 | 5.6 |
| †P _{ZL} | | | | 7.8 | 6.4 | 4.5 | 11.5 | 13.5 | 6.6 | 5.6 |
| †P _{PHZ} | CE | A or B | MAX | 6.6 | 6.4 | 4.9 | 9.3 | 11.6 | 6.6 | 5.1 |
| †P _{PLZ} | | | | 5.4 | 5.4 | 4.7 | 8.8 | 10.5 | 6.6 | 5.1 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|---------|------|------|-------|---|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | B |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B ₀ † |
| H | L | L | X | X | B ₀ † |
| L | L | L | ↓ | L | L |
| L | L | L | ↓ | H | H |
| L | L | L | H | X | B ₀ † |
| L | L | L | L | X | B ₀ ‡ |

† A-to-B data flow is shown. B-to-A flow is similar but uses OEBA, LEBA, CLKBA and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

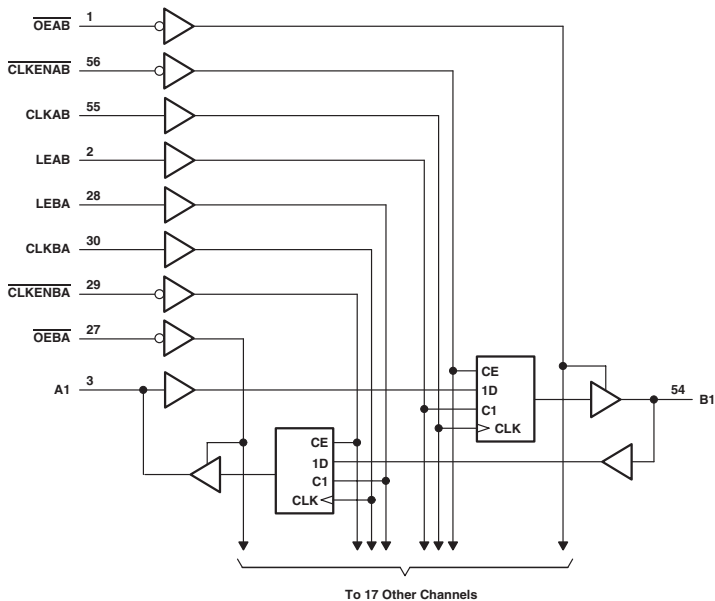
| PARAMETER | MAX or MIN | ABT | ALVCH 3V | UNIT |
|-----------------|------------|-----|-------------|------|
| I _{cc} | MAX | 36 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVCH 3V |
|-------------------------------|--|--------|------------|-----|-------------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 2.5 | 3.3 |
| | CLKAB or CLKBA high or low | | MIN | 3 | 3.3 |
| t _{su} Setup time | A before CLKAB ↓ or B before CLKBA ↓ | | MIN | 3 | - |
| | Data before CLK ↑ | | | - | 1.2 |
| | A before LEAB ↓ or B before LEBA ↓, CLK high | | MIN | 2.5 | 1.1 |
| | A before LEAB ↓ or B before LEBA ↓, CLK low | | MIN | 2.5 | 1.5 |
| | CLKEN after CLK ↓ | | | 2.5 | - |
| | CLKEN after CLK ↑ | | MIN | 2.5 | 0.8 |
| t _h Hold time | A after CLKAB ↓ or B after CLKBA ↓ | | MIN | 0 | - |
| | Data after CLK ↑ | | | - | 1.5 |
| | A after LEAB ↓ or B after LEBA ↓, CLK high | | MIN | 2 | 1.6 |
| | A after LEAB ↓ or B after LEBA ↓, CLK low | | MIN | 2 | 1.3 |
| | CLKEN after CLK ↓ | | | 1 | - |
| | CLKEN after CLK ↑ | | MIN | - | 1.4 |
| t _{PLH} | | | | 4 | 4 |
| t _{PHL} | A or B | B or A | MAX | 4.9 | 4 |
| t _{PLH} | LEAB or LEBA | B or A | MAX | 5 | 4.8 |
| t _{PHL} | | | | 5 | 4.8 |
| t _{PLH} | CLKAB or CLKBA | B or A | MAX | 5.3 | 5.7 |
| t _{PHL} | | | | 5 | 5.7 |
| t _{PZH} | OEAB | B | MAX | 5.1 | 5.2 |
| t _{PZL} | | | | 5.4 | 5.2 |
| t _{PHZ} | OEAB | B | MAX | 6.2 | 4.4 |
| t _{PLZ} | | | | 5.4 | 4.4 |
| t _{PZH} | OEBA | A | MAX | 5.1 | 5.2 |
| t _{PZL} | | | | 5.4 | 5.2 |
| t _{PHZ} | OEBA | A | MAX | 6.2 | 4.4 |
| t _{PLZ} | | | | 5.4 | 4.4 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|---------|------|------|-------|---|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | B |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B ₀ † |
| H | L | L | X | X | B ₀ † |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | B ₀ † |
| L | L | L | H | X | B ₀ ‡ |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

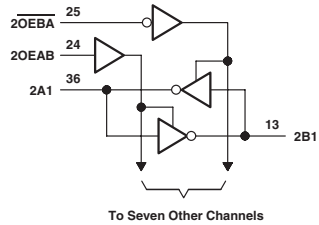
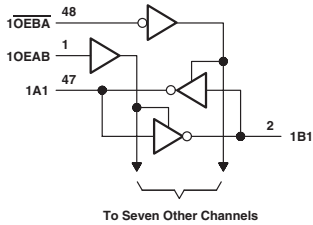
| PARAMETER | MAX or MIN | ABT | ALVTH 3V | ALVCH 3V | ALVCHR 3V |
|-----------------|------------|-----|-------------|-------------|--------------|
| I _{CC} | MAX | 36 | 5 | 0.04 | 0.04 |
| I _{OH} | MAX | -32 | -32 | -24 | -12 |
| I _{OL} | MAX | 64 | 64 | 24 | 12 |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVTH 3V | ALVCH 3V | ALVCHR 3V |
|-------------------------------|--|--------|------------|-----|-------------|-------------|--------------|
| f _{max} | | | MIN | 150 | 150 | 150 | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 2.5 | 1.8 | 3.3 | 3.3 |
| | CLKAB or CLKBA high or low | | MIN | 3 | 2.3 | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ high | | MIN | 4 | 2.4 | 2.1 | 2.1 |
| | Data before CLK ↑ low | | | 4 | 3.8 | 2.1 | 2.1 |
| | A before LEAB ↓ or B before LEBA ↓, CLK high | | MIN | 2.5 | 1 | 1.6 | 1.6 |
| | A before LEAB ↓ or B before LEBA ↓, CLK low | | MIN | 1 | 0.6 | 1.1 | 1.1 |
| | CLKEN before ↑ high | | MIN | 2.5 | 1.4 | 1.7 | 1.7 |
| CLKEN before ↑ low | | 2.5 | | 1.9 | 1.7 | 1.7 | |
| t _h Hold time | Data after CLK ↑ high | | MIN | 0 | 0.5 | 0.8 | 0.8 |
| | Data after CLK ↑ low | | | 0 | 0.5 | 0.8 | 0.8 |
| | A after LEAB ↓ or B after LEBA ↓, CLK high | | MIN | 2 | 2 | 1.4 | 1.4 |
| | A after LEAB ↓ or B after LEBA ↓, CLK low | | MIN | 2 | 2.3 | 1.7 | 1.7 |
| | CLKEN after ↑ high | | MIN | 0 | 0.6 | 0.6 | 0.6 |
| | CLKEN after ↑ low | | | 0 | 0.5 | 0.6 | 0.6 |
| t _{PLH} | A or B | B or A | MAX | 4 | 3.9 | 4.1 | 4.4 |
| t _{PHL} | | | | 4.9 | 3.9 | 4.1 | 4.4 |
| t _{PLH} | LEAB or LEBA | B or A | MAX | 5 | 4.6 | 4.7 | 5.1 |
| t _{PHL} | | | | 5.2 | 4.6 | 4.7 | 5.1 |
| t _{PLH} | CLKAB or CLKBA | B or A | MAX | 4.7 | 4.5 | 5 | 5.4 |
| t _{PHL} | | | | 4.6 | 4.6 | 5 | 5.4 |
| t _{PZH} | OEAB | B | MAX | 5.5 | 4.2 | 5.2 | 5.6 |
| t _{PZL} | | | | 5.8 | 4.4 | 5.2 | 5.6 |
| t _{PHZ} | OEAB | B | MAX | 6.2 | 5.3 | 4.4 | 4.7 |
| t _{PLZ} | | | | 5.4 | 4.6 | 4.4 | 4.7 |
| t _{PZH} | OEBA | A | MAX | 5.5 | 4.2 | 5.2 | 5.6 |
| t _{PZL} | | | | 5.8 | 4.4 | 5.2 | 5.6 |
| t _{PHZ} | OEBA | A | MAX | 6.2 | 5.3 | 4.4 | 4.7 |
| t _{PLZ} | | | | 5.4 | 4.6 | 4.4 | 4.7 |

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|------|---|
| OEBA | OEAB | |
| L | L | \overline{B} data to A bus |
| L | H | \overline{B} data to A bus, \overline{A} data to B bus |
| H | L | Isolation |
| H | H | \overline{A} data to B bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AC | ACT | UNIT |
|-----------------|------------|------|------|------|
| I _{CC} | MAX | 0.08 | 0.08 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

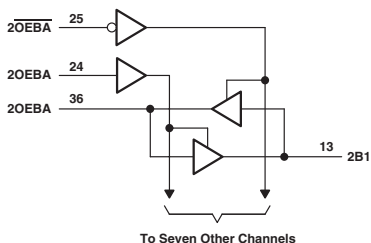
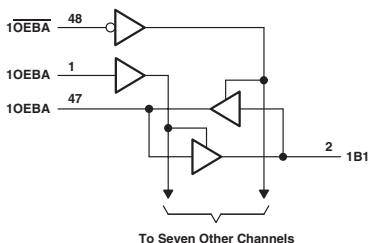
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AC | ACT |
|------------------|-------------------|--------|------------|-----|------|
| t _{PLH} | A | B | MAX | 6.8 | 8.5 |
| t _{PHL} | | | | 8.2 | 10.5 |
| t _{PLH} | B | A | MAX | 6.8 | 8.5 |
| t _{PHL} | | | | 8.2 | 10.5 |
| t _{PZH} | \overline{OEBA} | A | MAX | 7.9 | 9.1 |
| t _{PZL} | | | | 9.4 | 10.9 |
| t _{PHZ} | \overline{OEBA} | A | MAX | 9.2 | 11.9 |
| t _{PLZ} | | | | 8.3 | 10.6 |
| t _{PZH} | OEAB | B | MAX | 7.3 | 8.9 |
| t _{PZL} | | | | 9.1 | 10.5 |
| t _{PHZ} | OEAB | B | MAX | 9 | 10.8 |
| t _{PLZ} | | | | 8 | 9.6 |

UNIT: ns

16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|-------------------|------|-------------------------------------|
| \overline{OEBA} | OEAB | |
| L | L | B data to A bus |
| L | H | B data to A bus, A data to B bus |
| H | L | Isolation |
| H | H | A data to B bus |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | UNIT |
|-----------|------------|-----|------|------|
| I_{CC} | MAX | 35 | 0.08 | mA |
| I_{DH} | MAX | -32 | -24 | mA |
| I_{OL} | MAX | 64 | 24 | mA |

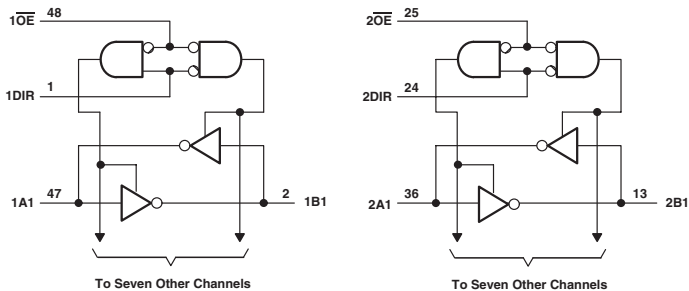
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT |
|-----------|-------------------|--------|------------|-----|------|
| t_{PLH} | A or B | B or A | MAX | 3.6 | 7.7 |
| t_{PHL} | | | | 4.3 | 8.6 |
| t_{PZH} | \overline{OEBA} | A | MAX | 4.9 | 9.5 |
| t_{PZL} | | | | 6 | 11.1 |
| t_{PHZ} | \overline{OEBA} | A | MAX | 6 | 12 |
| t_{PLZ} | | | | 5.4 | 10.7 |
| t_{PZH} | OEAB | B | MAX | 4.9 | 9.3 |
| t_{PZL} | | | | 6 | 10.6 |
| t_{PHZ} | OEAB | B | MAX | 6 | 10.4 |
| t_{PLZ} | | | | 5.4 | 9.5 |

UNIT: ns

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|--------|-----|-------------------------|
| OE | DIR | |
| L | L | \bar{B} data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | AC | ACT | UNIT |
|-----------------|------------|-----|------|------|------|
| I _{CC} | MAX | 32 | 0.08 | 0.08 | mA |
| I _{OH} | MAX | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 24 | mA |

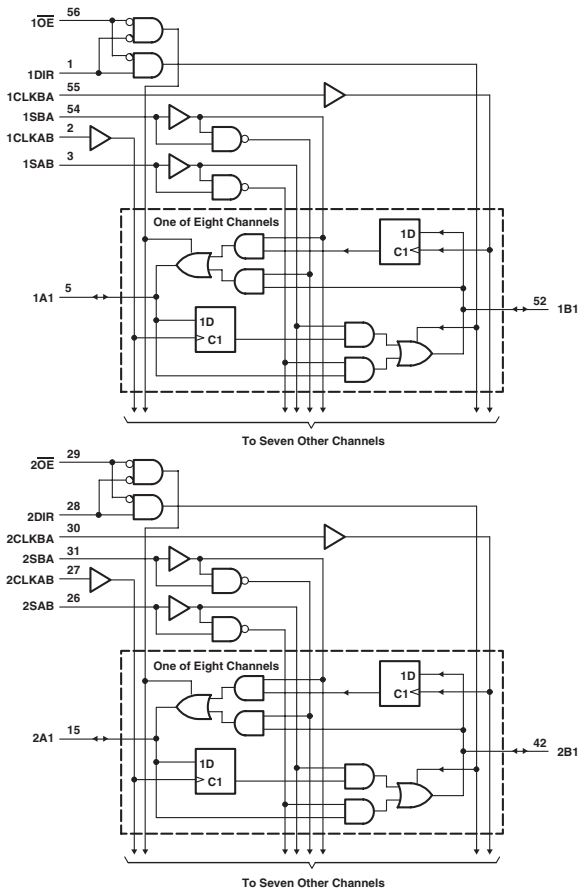
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | AC | ACT |
|------------------|-----------------|--------|------------|-----|-----|------|
| t _{PLH} | A or B | B or A | MAX | 4.3 | 7.3 | 9.1 |
| | | | | 3.9 | 8.6 | 10.5 |
| t _{PHL} | A or B | B or A | MAX | 5.5 | 8 | 9.8 |
| | | | | 6.3 | 9.9 | 11.5 |
| t _{PZH} | \overline{OE} | A or B | MAX | 6.3 | 9.9 | 12.5 |
| | | | | 4.2 | 9 | 11 |
| t _{PZL} | \overline{OE} | A or B | MAX | 6.3 | 9.9 | 12.5 |
| | | | | 4.2 | 9 | 11 |

UNIT: ns

16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | | | OPERATION OR FUNCTION |
|--------|-----|--------|--------|-----|-----|----------------|----------------|--|--|---------------------------|
| OE | DIR | CLKAB | CLKBA | SAB | SBA | A1 THRU A8 | B1 THRU B8 | | | |
| X | X | ↑ | X | X | X | Input | Unspecified † | | | Store A, B unspecified † |
| X | X | X | ↑ | X | X | Unspecified † | Input | | | Store B, A unspecified † |
| H | X | ↑ | ↑ | X | X | Input | Input | | | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | | | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | | | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | | | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | | | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | | | Stored A data to B bus |

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVT 3V | LVTH 3V | AC | ACT | LVC 3V | LVCH 3V | ALVCH 3V | AVC 3V | UNIT |
|-----------------|------------|-----|-----------|------------|------|------|-----------|------------|-------------|-----------|------|
| I _{CC} | MAX | 32 | 5 | 5 | 0.08 | 0.08 | 0.02 | 0.02 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -24 | -24 | -24 | -12 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 24 | 24 | 24 | 12 | mA |

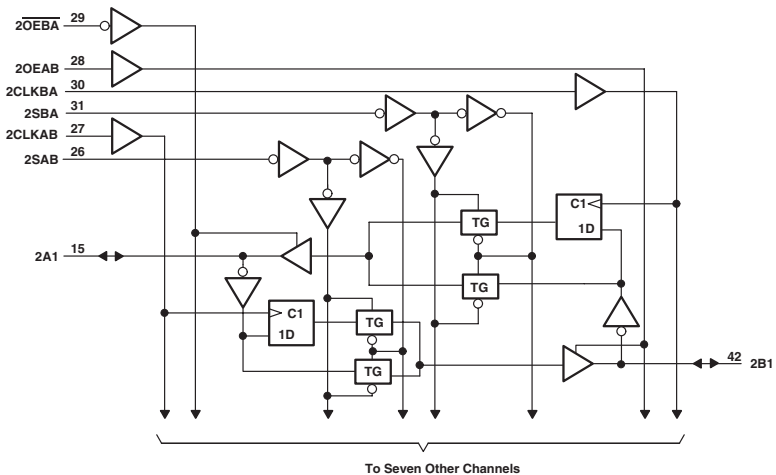
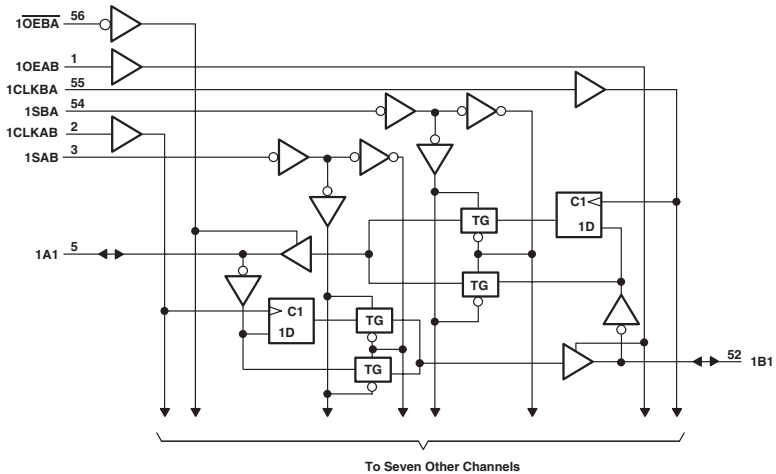
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | AC | ACT | LVC 3V | LVCH 3V |
|-------------------------------|---|--------|------------|-----|-----------|------------|------|------|-----------|------------|
| f _{max} | | | MIN | 125 | 150 | 150 | 75 | 90 | 150 | 150 |
| t _w Pulse duration | CLKAB or CLKBA high or low | | MIN | 4.3 | 3.3 | 3.3 | 6.5 | 5.5 | 3.3 | 3.3 |
| t _{su} Setup time | A or B before CLKAB ↑ or CLKBA ↑, data high | | MIN | 3 | 1.3 | 1.2 | 5 | 4 | 2.7 | 2.9 |
| | A or B before CLKAB ↑ or CLKBA ↑, data low | | MIN | 3 | 2.4 | 2 | 5 | 6 | 2.7 | 2.9 |
| t _h Hold time | A or B after CLKAB ↑ or CLKBA ↑, data high | | MIN | 0 | 0.5 | 0.5 | 1 | 1.5 | 0.3 | 0.3 |
| | A or B after CLKAB ↑ or CLKBA ↑, data low | | MIN | 0 | 0.5 | 0.5 | 1 | 1.5 | 0.3 | 0.3 |
| t _{PLH} | CLKAB or CLKBA | B or A | MAX | 4.9 | 5.7 | 4.2 | 12.1 | 12.2 | 6 | 6.7 |
| | | | | 4.7 | 5.7 | 4.2 | 11.9 | 12.3 | 6 | 6.7 |
| t _{PHL} | A or B | B or A | MAX | 3.9 | 4.7 | 3.4 | 9.5 | 10.6 | 5.2 | 5.7 |
| | | | | 4.6 | 4.7 | 3.4 | 9.7 | 11.4 | 5.2 | 5.7 |
| t _{PLH} | SAB or SBA | B or A | MAX | 5 | 6.2 | 4.5 | 12.5 | 15.6 | 6.1 | 7.7 |
| | | | | 5 | 6.2 | 4.5 | 13.1 | 16.7 | 6.1 | 7.7 |
| t _{PZH} | OE | A or B | MAX | 5.5 | 5.4 | 4.3 | 10.5 | 11.9 | 6.9 | 6.9 |
| | | | | 5.7 | 5.6 | 4.3 | 12.2 | 13.5 | 6.9 | 6.9 |
| t _{PHZ} | OE | A or B | MAX | 5.4 | 6.5 | 5.6 | 8.9 | 10.2 | 6.9 | 6.9 |
| | | | | 4.5 | 5.8 | 5.4 | 8.6 | 9.9 | 6.9 | 6.9 |
| t _{PZH} | DIR | A or B | MAX | 5.4 | 5.7 | 4.4 | 10.9 | 15.2 | 7.2 | 7.2 |
| | | | | 5.6 | 5.8 | 4.4 | 12.2 | 13.1 | 7.2 | 7.2 |
| t _{PHZ} | DIR | A or B | MAX | 6.7 | 7.2 | 5.7 | 9.4 | 10.8 | 7 | 7 |
| | | | | 5.9 | 6.6 | 5.2 | 8.8 | 10.4 | 7 | 7 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | AVC 3V |
|-------------------------------|---|--------|------------|-------------|-----------|
| f _{max} | | | MIN | 150 | 350 |
| t _w Pulse duration | CLKAB or CLKBA high or low | | MIN | 3.3 | 1.4 |
| t _{su} Setup time | A or B before CLKAB ↑ or CLKBA ↑, data high | | MIN | 1.4 | 0.8 |
| | A or B before CLKAB ↑ or CLKBA ↑, data low | | MIN | 1.4 | 0.8 |
| t _h Hold time | A or B after CLKAB ↑ or CLKBA ↑, data high | | MIN | 0.7 | 0.6 |
| | A or B after CLKAB ↑ or CLKBA ↑, data low | | MIN | 0.7 | 0.6 |
| t _{PLH} | CLKAB or CLKBA | B or A | MAX | 4.5 | 3.3 |
| | | | | 4.5 | 3.3 |
| t _{PHL} | A or B | B or A | MAX | 3.9 | 2.6 |
| | | | | 3.9 | 2.6 |
| t _{PLH} | SAB or SBA | B or A | MAX | 5.3 | 4 |
| | | | | 5.3 | 4 |
| t _{PZH} | OE | A or B | MAX | 5.1 | 4 |
| | | | | 5.1 | 4 |
| t _{PHZ} | OE | A or B | MAX | 4.7 | 4.2 |
| | | | | 4.7 | 4.2 |
| t _{PZH} | DIR | A or B | MAX | 5.1 | 4.3 |
| | | | | 5.1 | 4.3 |
| t _{PHZ} | DIR | A or B | MAX | 5.3 | 4.3 |
| | | | | 5.3 | 4.3 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O † | | OPERATION OR FUNCTION |
|--------|------|-------|-------|-----|-----|--------------|--------------|---|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 | |
| L | H | L | L | X | X | Input | Input | Isolation |
| L | H | † | † | X | X | Input | Input | Store A and B data |
| X | H | † | L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | † | † | X† | X | Input | Output | Store A in both registers |
| L | X | L | † | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | † | † | X | X† | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | L | X | H | Output | Input | Store B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | L | X | H | X | Input | Output | Store A data to B bus |
| H | L | L | L | H | H | Output | Output | Store A data to B bus and Store B data to A bus |

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

§ Select control = H; clocks must be staggered to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

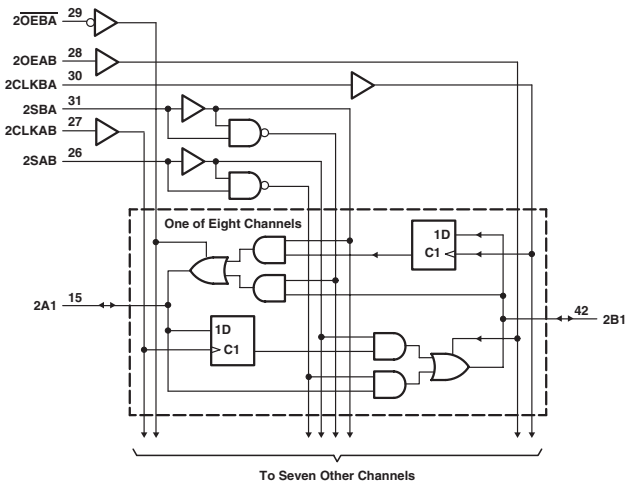
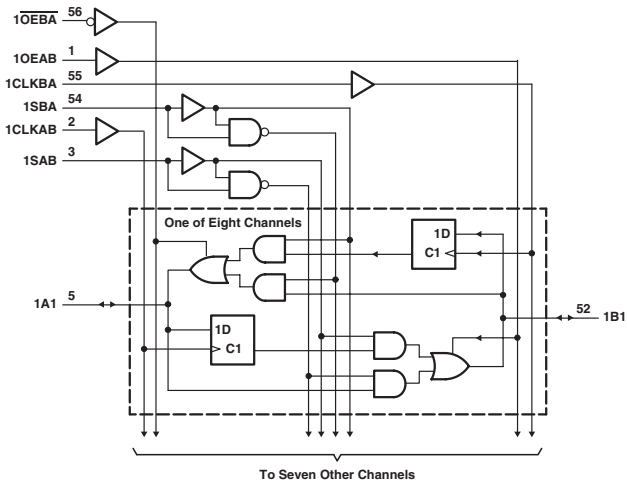
| PARAMETER | MAX or MIN | ACT | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 0.08 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT |
|-------------------------------|--------------------------------------|--------|------------|------|
| f _{max} | | | MIN | 90 |
| t _w Pulse duration | CLKAB or CLKBA high or low | | MIN | 5.5 |
| t _{su} Setup time | A before CLKAB † or B before CLKBA † | | MIN | 5.3 |
| t _h Hold time | A after CLKAB † or B after CLKBA † | | MIN | 1 |
| t _{PLH} | A or B | B or A | MAX | 11.3 |
| t _{PHL} | | | | 11.9 |
| t _{PLH} | CLKAB or CLKBA | A or B | MAX | 13.7 |
| t _{PHL} | | | | 13.6 |
| t _{PLH} | SAB or SBA | A or B | MAX | 17.3 |
| t _{PHL} | | | | 17.8 |
| t _{PZH} | OEBA | A | MAX | 12.3 |
| t _{PZL} | | | | 13.9 |
| t _{PHZ} | OEBA | A | MAX | 10.6 |
| t _{PLZ} | | | | 10.8 |
| t _{PZH} | OEAB | B | MAX | 11.9 |
| t _{PZL} | | | | 13.5 |
| t _{PHZ} | OEAB | B | MAX | 11.4 |
| t _{PLZ} | | | | 11.6 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|--------|------|--------|--------|-----|-----|---------------|---------------|--|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1 THRU A8 | B1 THRU B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified ‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Unspecified ‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Store A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A data to B bus and stored B data A bus |

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

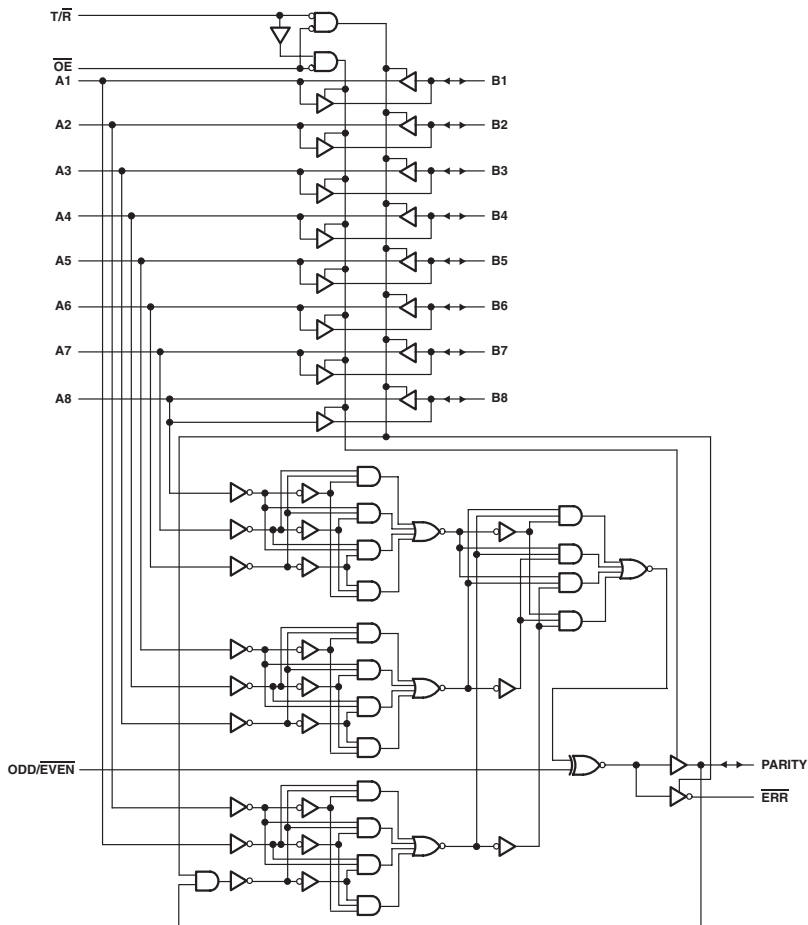
| PARAMETER | MAX or MIN | ABT | LVTH 3V | AC | ACT | LVCH 3V | UNIT |
|-----------------|------------|-----|------------|------|------|------------|------|
| I _{CC} | MAX | 32 | 5 | 0.08 | 0.08 | 0.02 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVTH 3V | AC | ACT | LVCH 3V |
|-------------------------------|--|--------|------------|-----|------------|------|------|------------|
| f _{max} | | | MIN | 125 | 150 | 95 | 90 | 150 |
| t _w Pulse duration | CLKAB or CLKBA high or low | | MIN | 4.3 | 3.3 | 5 | 5.5 | 3.3 |
| t _{su} Setup time | A before CLKAB ↑ or B before CLKBA ↑, high | | MIN | 3 | 1.2 | 4.5 | 4.5 | 3 |
| | A before CLKAB ↑ or B before CLKBA ↑, low | | MIN | 3 | 2 | 4.5 | 4.5 | 3 |
| t _h Hold time | A after CLKAB ↑ or B after CLKBA ↑, high | | MIN | 0 | 0.5 | 0 | 1 | 0.2 |
| | A after CLKAB ↑ or B after CLKBA ↑, low | | MIN | 0 | 0.5 | 0 | 1 | 0.2 |
| †P _{LH} | CLKAB or CLKBA | A or B | MAX | 4.9 | 4.2 | 12.2 | 12.3 | 6.4 |
| †P _{HL} | | | | 4.7 | 4.2 | 12.3 | 12.3 | 6.4 |
| †P _{LH} | A or B | B or A | MAX | 3.9 | 3.4 | 9.9 | 10.5 | 6.3 |
| †P _{HL} | | | | 4.6 | 3.4 | 10.2 | 11.6 | 6.3 |
| †P _{LH} | SAB or SBA | A or B | MAX | 5 | 4.5 | 13.8 | 16 | 7.4 |
| †P _{HL} | | | | 5 | 4.5 | 13.8 | 16.9 | 7.4 |
| †P _{ZH} | OEBA | A | MAX | 5 | 4.3 | 10.7 | 11.7 | 6.3 |
| †P _{ZL} | | | | 5.3 | 4.3 | 13.2 | 13.4 | 6.3 |
| †P _{HZ} | OEBA | A | MAX | 4.9 | 5.6 | 8.8 | 9.5 | 6.2 |
| †P _{LZ} | | | | 4 | 5.4 | 8.7 | 9.2 | 6.2 |
| †P _{ZH} | OEAB | B | MAX | 4.2 | 4.2 | 10.5 | 10.8 | 6.3 |
| †P _{ZL} | | | | 4.6 | 4.2 | 13 | 12.4 | 6.3 |
| †P _{HZ} | OEAB | B | MAX | 5.9 | 5.5 | 8 | 10.5 | 6.2 |
| †P _{LZ} | | | | 5.2 | 5.5 | 7.8 | 9.9 | 6.2 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

(each 8-bit section)

| NUMBER OF A OR B INPUTS THAT ARE HIGH | INPUTS | | | INPUT/OUTPUT | OUTPUTS | |
|--|--------|-----|----------|--------------|---------|-------------|
| | OE | T/R | ODD/EVEN | PARITY | ERR | OUTPUT MODE |
| 0, 2, 4, 6, 8 | L | H | H | H | Z | Transmit |
| | L | H | L | L | Z | Transmit |
| | L | L | H | H | H | Receive |
| | L | L | H | L | L | Receive |
| | L | L | L | H | L | Receive |
| | L | L | L | L | H | Receive |
| 1, 3, 5, 7 | L | H | H | L | Z | Transmit |
| | L | H | L | H | Z | Transmit |
| | L | L | H | H | L | Receive |
| | L | L | H | L | H | Receive |
| | L | L | L | H | H | Receive |
| | L | L | L | L | L | Receive |
| Don't care | H | X | X | Z | Z | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | UNIT |
|-----------------|------------|-----|------|------|
| I _{CC} | MAX | 36 | 0.08 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

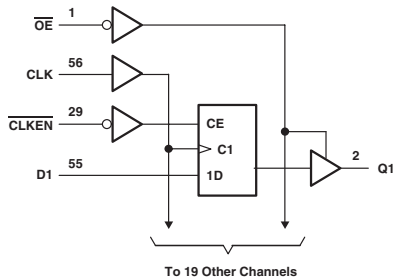
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT |
|------------------|------------------------|---------------------------------|------------|-----|------|
| t _{PLH} | A or B | B or A | MAX | 4.1 | 10.7 |
| | | | | 4.3 | 10.6 |
| t _{PHL} | A or B | PARITY | MAX | 6.7 | 14.3 |
| | | | | 6.1 | 14.3 |
| t _{PLH} | ODD / EVEN | PARITY, ERR | MAX | 6.7 | 13.7 |
| | | | | 6.1 | 14.1 |
| t _{PHL} | B | $\overline{\text{ERR}}$ | MAX | 6.7 | 14.6 |
| | | | | 6.1 | 14.7 |
| t _{PLH} | PARITY | ERR | MAX | 6.7 | 13.8 |
| | | | | 6.1 | 14.2 |
| t _{PZH} | $\overline{\text{OE}}$ | A or B | MAX | 5.6 | 11.3 |
| | | | | 6 | 13 |
| t _{PHZ} | $\overline{\text{OE}}$ | A or B | MAX | 5.4 | 11.2 |
| | | | | 4.3 | 10.5 |
| t _{PZH} | $\overline{\text{OE}}$ | PARITY, $\overline{\text{ERR}}$ | MAX | 5.6 | 11.3 |
| | | | | 6 | 13 |
| t _{PHZ} | $\overline{\text{OE}}$ | PARITY, $\overline{\text{ERR}}$ | MAX | 5.4 | 11.2 |
| | | | | 4.3 | 10.5 |

UNIT: ns

20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUT Q |
|--------|-------|-----|---|----------------|
| OE | CLKEN | CLK | D | |
| L | H | X | H | Q ₀ |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | L | X | Q ₀ |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

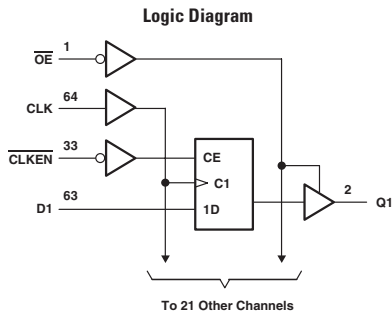
| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|--------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 3.1 |
| | CLKEN before CLK ↑ | | MIN | 2.7 |
| t _h Hold time | Data after CLK ↑ | | MIN | 0 |
| | CLKEN after CLK ↑ | | MIN | 0 |
| TP _{LH} | CLK | Q | MAX | 4.3 |
| TP _{HL} | | | | 4.3 |
| TP _{ZH} | OE | Q | MAX | 4.8 |
| TP _{ZL} | | | | 4.8 |
| TP _{HZ} | OE | Q | MAX | 4.4 |
| TP _{LZ} | | | | 4.4 |

UNIT f_{max} : MHz other : ns

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUT |
|--------|-------|--------|---|----------------|
| OE | CLKEN | CLK | D | Q |
| L | H | X | X | Q ₀ |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | L or H | X | Q ₀ |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | AVC 3V | UNIT |
|-----------------|------------|-----------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

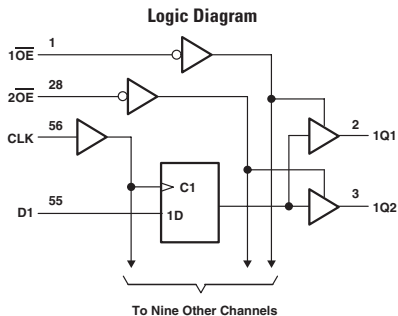
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AVC 3V |
|-------------------------------|--------------------|--------|------------|-----------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 2.8 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 2.5 |
| | CLKEN before CLK ↑ | | MIN | 1.4 |
| t _h Hold time | Data after CLK ↑ | | MIN | 0 |
| | CLKEN after CLK ↑ | | MIN | 1.2 |
| t _{PLH} | CLK | Q | MAX | 2.6 |
| t _{PHL} | | | | 2.6 |
| t _{PZH} | OE | Q | MAX | 4.3 |
| t _{PZL} | | | | 4.3 |
| t _{PHZ} | OE | Q | MAX | 3.4 |
| t _{PLZ} | | | | 3.4 |

UNIT f_{max} : MHz other : ns

16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|---------------------------|-----|---|---------------|
| \overline{OE}_n^\dagger | CLK | D | Q_n^\dagger |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

$^\dagger n = 1, 2$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------|------------|-------------|------|
| I_{CC} | MAX | 0.04 | mA |
| I_{DH} | MAX | -24 | mA |
| I_{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

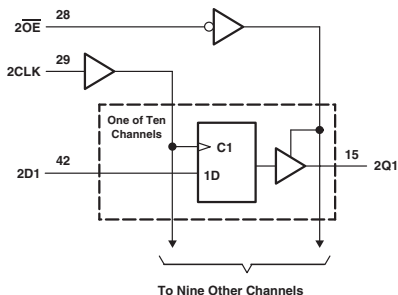
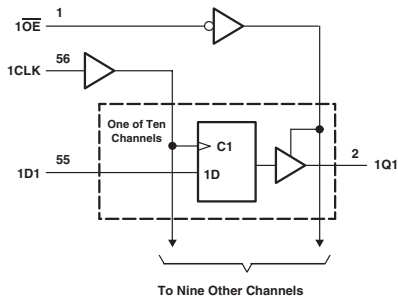
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|----------------------|-------------------|--------|------------|-------------|
| t_{max} | | | MIN | 150 |
| t_w Pulse duration | CLK high or low | | MIN | 3.3 |
| t_{su} Setup time | Data before CLK ↑ | | MIN | 1.4 |
| t_h Hold time | Data after CLK ↑ | | MIN | 1 |
| t_{PLH} | CLK | Q | MAX | 4.8 |
| t_{PHL} | | | | 4.8 |
| t_{PZH} | \overline{OE} | Q | MAX | 5 |
| t_{PZL} | | | | 5 |
| t_{PHZ} | \overline{OE} | Q | MAX | 4.5 |
| t_{PLZ} | | | | 4.5 |

UNIT fmax : MHz other : ns

16821

20-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|------------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | \uparrow | H | H |
| L | \uparrow | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ALVTH 3V | ACT | ALVCH 3V | UNIT |
|-----------|------------|-----|-------------|------|-------------|------|
| I_{CC} | MAX | 89 | 5 | 0.08 | 0.04 | mA |
| I_{OH} | MAX | -32 | -32 | -24 | -24 | mA |
| I_{OL} | MAX | 64 | 64 | 24 | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVTH 3V | ACT | ALVCH 3V |
|----------------------|-----------------------------------|--------|------------|-----|-------------|------|-------------|
| f_{max} | | | MIN | 150 | 150 | 70 | 150 |
| t_w Pulse duration | CLK high or low | | MIN | 3.3 | 1.5 | 7 | 3.3 |
| t_{su} Setup time | Data before CLK \uparrow , low | | MIN | 1.8 | 1.5 | 7.5 | 3.4 |
| | Data before CLK \uparrow , high | | MIN | 1.8 | 1.5 | 7.5 | 3.4 |
| t_h Hold time | Data after CLK \uparrow , high | | MIN | 1.3 | 1 | 0.5 | 0 |
| | Data after CLK \uparrow , low | | MIN | 1.3 | 1 | 0.5 | 0 |
| t_{PLH} | CLK | Q | MAX | 6.1 | 3.5 | 13.4 | 4.5 |
| t_{PHL} | | | | 5.4 | 3.5 | 14 | 4.5 |
| t_{PZH} | \overline{OE} | Q | MAX | 5.7 | 4.1 | 11.9 | 5.1 |
| t_{PZL} | | | | 5.6 | 3.6 | 14.7 | 5.1 |
| t_{PHZ} | \overline{OE} | Q | MAX | 6.5 | 4.8 | 10.7 | 4.6 |
| t_{PLZ} | | | | 7.1 | 4.8 | 10 | 4.6 |

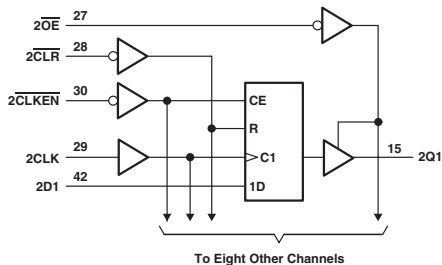
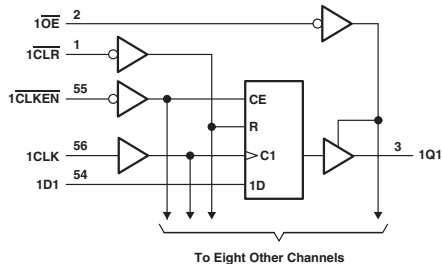
UNIT f_{max} : MHz other : ns

18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS

FUNCTION TABLE
(each 9-bit flip-flop)

| INPUTS | | | | | | OUTPUT Q |
|-----------------|-----|-------|------------|---|-------|-------------|
| \overline{OE} | CLR | CLKEN | CLK | D | | |
| L | L | X | X | X | L | |
| L | H | L | \uparrow | H | H | |
| L | H | L | \uparrow | L | L | |
| L | H | L | X | X | Q_0 | |
| L | H | H | X | X | Q_0 | |
| H | X | X | X | X | Z | |

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ABTH | AC | ACT | ALVCH 3V | UNIT |
|-----------|------------|-----|------|------|------|-------------|------|
| I_{CC} | MAX | 80 | 80 | 0.08 | 0.08 | 0.04 | mA |
| I_{OH} | MAX | -32 | -32 | -24 | -24 | -24 | mA |
| I_{OL} | MAX | 64 | 64 | 24 | 24 | 24 | mA |

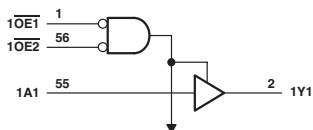
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABTH | AC | ACT | ALVCH 3V |
|----------------------|---------------------------------|--------|------------|-----|------|------|------|-------------|
| f_{max} | | | MIN | 150 | 150 | 115 | 90 | 150 |
| t_w Pulse duration | CLR low | | MIN | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 | 4.4 | 5.5 | 3.3 |
| t_{su} Setup time | CLR inactive | | MIN | 1.6 | 1.6 | 0.6 | 0.5 | 0.8 |
| | Data high before CLK \uparrow | | MIN | 1.7 | 1.7 | 5 | 7 | 1 |
| | Data low before CLK \uparrow | | MIN | 1.7 | 1.7 | 5 | 7 | 1.3 |
| | CLKEN low before CLK \uparrow | | MIN | 2.8 | 2.8 | 4.2 | 3.5 | 1.5 |
| t_h Hold time | Data high after CLK \uparrow | | MIN | 1.2 | 1.2 | 1.3 | 0.5 | 0.8 |
| | Data low after CLK \uparrow | | MIN | 1.2 | 1.2 | 1.3 | 0.5 | 0.5 |
| | CLKEN low after CLK \uparrow | | MIN | 0.6 | 0.6 | 1.4 | 2.5 | 0.4 |
| t_{PLH} | | | | 6.8 | 6.8 | 12 | 12.1 | 4.5 |
| t_{PHL} | CLK | Q | MAX | 6 | 6 | 12.7 | 12.9 | 4.5 |
| t_{PLH} | | | | - | - | - | - | 4.6 |
| t_{PHL} | CLR | Q | MAX | 6.1 | 6.7 | 11 | 12.5 | 4.6 |
| t_{PZH} | | | | 4.9 | 4.9 | 9.7 | 10.7 | 4.8 |
| t_{PZL} | \overline{OE} | Q | MAX | 5.5 | 5.5 | 11.8 | 12.8 | 4.8 |
| t_{PHZ} | | | | 6.1 | 6.1 | 9.3 | 10.3 | 4.5 |
| t_{PLZ} | \overline{OE} | Q | MAX | 8.7 | 8.7 | 8.6 | 9.4 | 4.5 |

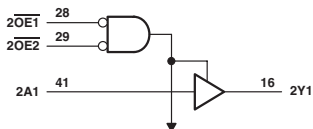
UNIT f_{max} : MHz other: ns

18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



To Eight Other Channels



To Eight Other Channels

FUNCTION TABLE
(each 9-bit section)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | ALVCH 3V | UNIT |
|-----------------|------------|-----|------|-------------|------|
| I _{CC} | MAX | 32 | 0.08 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 24 | mA |

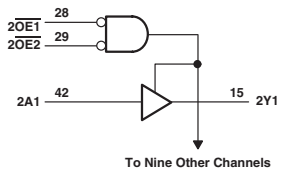
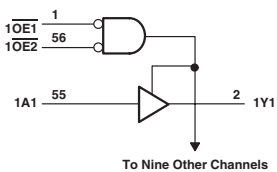
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT | ALVCH 3V |
|------------------|-----------------|--------|------------|-----|------|-------------|
| t _{PLH} | A | Y | MAX | 3.9 | 10.5 | 3.4 |
| | | | | 4.4 | 10.3 | 3.4 |
| t _{PZH} | \overline{OE} | Y | MAX | 6.1 | 11 | 4.7 |
| | | | | 6 | 13.2 | 4.7 |
| t _{PHZ} | \overline{OE} | Y | MAX | 6.9 | 11.5 | 4.5 |
| | | | | 6.6 | 10.6 | 4.5 |

UNIT: ns

20-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

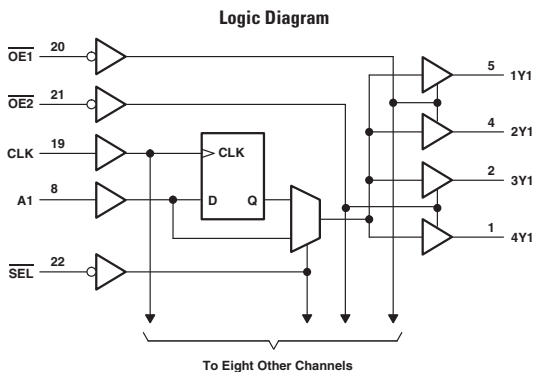
| PARAMETER | MAX or MIN | ABT | ALVTH 3V | ACT | ALVCH 3V | AVC 3V | UNIT |
|-----------------|------------|-----|-------------|------|-------------|-----------|------|
| I _{CC} | MAX | 32 | 6 | 0.08 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -24 | -12 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 24 | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVTH 3V | ACT | ALVCH 3V | AVC 3V |
|------------------|-----------------|--------|------------|-----|-------------|------|-------------|-----------|
| t _{PLH} | A | Y | MAX | 3.4 | 3 | 11 | 3.4 | 1.7 |
| t _{PHL} | | | | 4.2 | 2.8 | 10.8 | 3.4 | 1.7 |
| t _{PZH} | \overline{OE} | Y | MAX | 5.6 | 3.9 | 11.7 | 4.7 | 5.1 |
| t _{PZL} | | | | 5.5 | 3.4 | 14 | 4.7 | 5.1 |
| t _{PHZ} | \overline{OE} | Y | MAX | 6.6 | 5.8 | 12.4 | 4.5 | 4.7 |
| t _{PLZ} | | | | 6.1 | 4.6 | 11.5 | 4.5 | 4.7 |

UNIT: ns

1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS



FUNCTION TABLE

| OE | INPUTS | | | A | Y |
|----|--------|-----|---|---|---|
| | SEL | CLK | | | |
| H | X | X | X | Z | |
| L | H | X | L | L | |
| L | H | X | H | H | |
| L | L | ↑ | L | L | |
| L | L | ↑ | H | H | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------|------------|-------------|------|
| I_{CC} | MAX | 0.04 | mA |
| I_{OH} | MAX | -24 | mA |
| I_{OL} | MAX | 24 | mA |

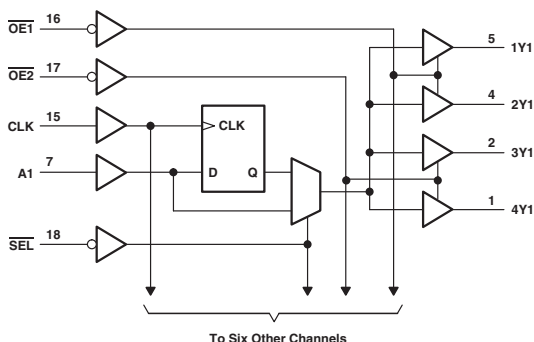
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|----------------------|---------------------|--------|------------|-------------|
| f_{max} | | | MIN | 150 |
| t_w Pulse duration | CLK high or low | | MIN | 3.3 |
| t_{su} Setup time | A data before CLK ↑ | | MIN | 1.6 |
| t_h Hold time | A data after CLK ↑ | | MIN | 1.1 |
| t_{PLH} | A | Y | MAX | 3.6 |
| t_{PHL} | | | | 3.6 |
| t_{PLH} | CLK | Y | MAX | 3.9 |
| t_{PHL} | | | | 3.9 |
| t_{PLH} | SEL | Y | MAX | 4.4 |
| t_{PHL} | | | | 4.4 |
| t_{PZH} | \overline{OE} | Y | MAX | 4.3 |
| t_{PZL} | | | | 4.3 |
| t_{PHZ} | \overline{OE} | Y | MAX | 4.5 |
| t_{PLZ} | | | | 4.5 |

UNIT f_{max} : MHz other: ns

1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|-----|-----|---|--------|
| OE | SEL | CLK | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

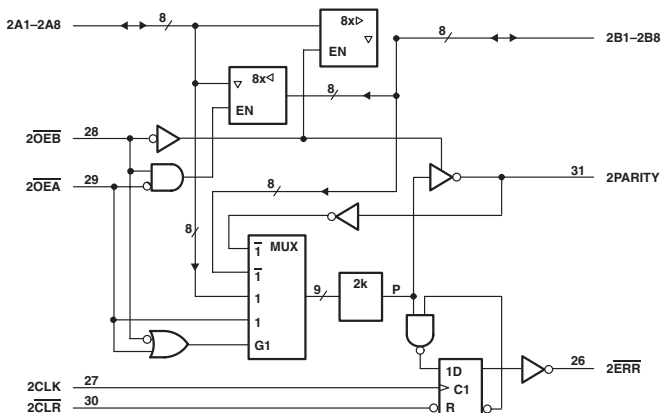
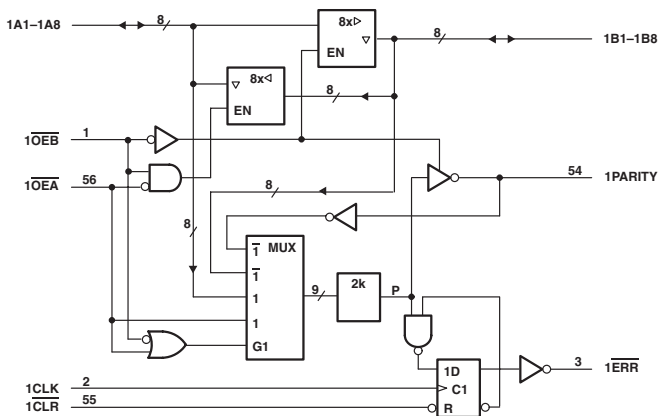
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|---------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 1.6 |
| t _h Hold time | A data after CLK ↑ | | MIN | 1.1 |
| t _{PLH} | A | Y | MAX | 3.6 |
| t _{PHL} | | | | 3.6 |
| t _{PLH} | CLK | Y | MAX | 3.9 |
| t _{PHL} | | | | 3.9 |
| t _{PLH} | SEL | Y | MAX | 4.4 |
| t _{PHL} | | | | 4.4 |
| t _{PZH} | OE | Y | MAX | 4.3 |
| t _{PZL} | | | | 4.3 |
| t _{PHZ} | OE | Y | MAX | 4.5 |
| t _{PLZ} | | | | 4.5 |

UNIT f_{max} : MHz other : ns

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | OUTPUT AND I/O | | | | FUNCTION |
|--------|--------------|-----|--|---|-----------------------------|----------------|----|--------|-------------------|--|
| OEB | OE \bar{A} | CLR | CLK | A Σ OF H | BI \uparrow Σ OF H | A | B | PARITY | ERR \ddagger | |
| L | H | X | X | Odd Even | NA | NA | A | L H | NA | A data to B bus and generate parity |
| H | L | H | \uparrow | NA | Odd Even | B | NA | NA | H L | B data to A bus and check parity |
| X | X | L | X | X | X | X | NA | NA | H | Check error flag register |
| H | H | H | No \uparrow L H H \uparrow | X No \uparrow X \uparrow Odd Even | X | Z | Z | Z | NC H H L | Isolation§ |
| L | L | X | X | Odd Even | NA | NA | A | H L | NA | A data to B bus and generate inverted parity |

NA = not applicable, NC = no change, X = don't care

 \uparrow Output states shown assume ERR was previously high.

 \ddagger Summation of high-level inputs includes PARITY along with BI inputs.

 \S In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

| INPUTS | | INTERNAL TO DEVICE | | OUTPUT PRE-STATE | | OUTPUT ERR | | FUNCTION |
|--------|------------|--------------------|---|----------------------|---|------------|---|----------|
| CLR | CLK | POINT P | | ERR $_{n-1}\uparrow$ | | ERR | | |
| H | \uparrow | H | H | H | H | H | L | Sample |
| H | \uparrow | X | X | L | L | L | L | |
| H | \uparrow | L | L | X | X | L | L | |
| L | X | X | X | X | X | H | H | Clear |

 \uparrow State of ERR before any changes at CLR, CLK, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | UNIT |
|-----------------|------------|-----|------|------|
| I _{CC} | MAX | 36 | 0.08 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

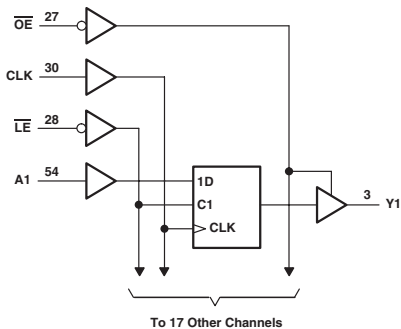
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT |
|-------------------------------|--|--------|------------|-----|------|
| t _w Pulse duration | CLK high or low | | MIN | 3 | 4 |
| | CLR low | | | - | - |
| t _{su} Setup time | A data before CLK \uparrow , A port | | MIN | 4.5 | - |
| | A data before CLK \uparrow , CLR | | | 1 | 1.5 |
| | A data before CLK \uparrow , OE \bar{A} | | | 5 | - |
| t _h Hold time | A data after CLK \uparrow , A port or OE \bar{A} | | MIN | 0 | 0 |
| t _{PLH} | A or B | B or A | MAX | 4.1 | 10.4 |
| t _{PHL} | | | | 4.3 | 10.7 |
| t _{PLH} | A | PARITY | MAX | 6.7 | 13.5 |
| t _{PHL} | | | | 6.1 | 13.8 |
| t _{PZH} | OE \bar{B} or OE \bar{A} | A or B | MAX | 5.6 | 11.2 |
| t _{PZL} | | | | 6 | 13 |
| t _{PHZ} | OE \bar{B} or OE \bar{A} | A or B | MAX | 5.4 | 10.8 |
| t _{PLZ} | | | | 4.3 | 10.1 |
| t _{PLH} | CLK, CLR | ERR | MAX | 4.6 | 15.8 |
| t _{PHL} | CLK | | | 3.9 | 11.6 |
| t _{PLH} | OE \bar{B} | PARITY | MAX | 6.7 | - |
| t _{PHL} | | | | 6.1 | - |
| t _{PLH} | OE \bar{A} | PARITY | MAX | 6.7 | 13.2 |
| t _{PHL} | | | | 6.1 | 13.6 |
| t _{PZH} | OE \bar{B} | PARITY | MAX | 5.7 | 9.5 |
| t _{PZL} | | | | 6.5 | 10.7 |
| t _{PHZ} | OE \bar{B} | PARITY | MAX | 4.7 | 10.2 |
| t _{PLZ} | | | | 4.1 | 9.7 |
| t _{PZH} | OE \bar{A} | PARITY | MAX | 5.7 | - |
| t _{PZL} | | | | 6.5 | - |
| t _{PHZ} | OE \bar{A} | PARITY | MAX | 4.7 | - |
| t _{PLZ} | | | | 4.1 | - |

UNIT: ns

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|-----|---|-----------------|
| OE | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | H | X | Y0 [†] |
| L | H | L | X | Y0 [‡] |

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high.

‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | AVC 3V | UNIT |
|-----------------|------------|------------|-----------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -24 | -12 | mA |
| I _{OL} | MAX | 24 | 12 | mA |

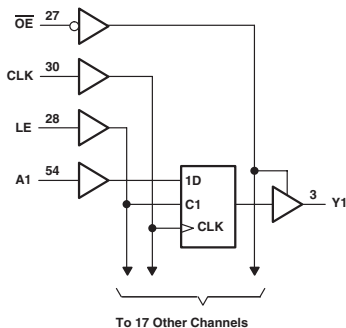
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | AVC 3V |
|-------------------------------|----------------------------|--------|------------|------------|-----------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LE low | | MIN | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.7 | 0.7 |
| | Data before LE ↑, CLK high | | MIN | 1.9 | 1 |
| | Data before LE ↑, CLK low | | | 1.5 | 1 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.7 | 0.9 |
| | Data after LE ↑, CLK high | | MIN | 0.9 | 1.4 |
| | Data after LE ↑, CLK low | | | 0.9 | 1.3 |
| I _{PLH} | A | Y | MAX | 3.6 | 2.5 |
| | | | | 3.6 | 2.5 |
| I _{PHL} | LE | Y | MAX | 4.9 | 4 |
| | | | | 4.9 | 4 |
| I _{PLH} | CLK | Y | MAX | 4.6 | 3.1 |
| | | | | 4.6 | 3.1 |
| I _{PZH} | OE | Y | MAX | 5 | 6.2 |
| | | | | 5 | 6.2 |
| I _{PHZ} | OE | Y | MAX | 4.5 | 5.3 |
| | | | | 4.5 | 5.3 |

UNIT f_{max}: MHz other: ns

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|-----|---|------------------|
| OE | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | L | H | X | Y ₀ † |
| L | L | L | X | Y ₀ ‡ |

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.

‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | ALVC 3V | ALVCH 3V | AVC 3V | UNIT |
|-----------------|------------|------------|------------|-------------|-----------|------|
| I _{cc} | MAX | 5 | 0.04 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | -24 | -12 | mA |
| I _{OL} | MAX | 64 | 24 | 24 | 12 | mA |

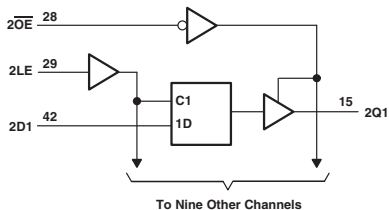
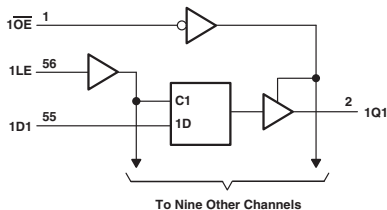
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | ALVC 3V | ALVCH 3V | AVC 3V |
|-------------------------------|----------------------------|--------|------------|------------|------------|-------------|-----------|
| f _{max} | | | MIN | 150 | 150 | 150 | 150 |
| t _w Pulse duration | LE low | | MIN | 3.3 | 3.3 | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 2.1 | 1.7 | 1.7 | 0.7 |
| | Data before LE ↓, CLK high | | MIN | 2.3 | 1.5 | 1.5 | 0.8 |
| | Data before LE ↓, CLK low | | MIN | 1.5 | 1 | 1 | 0.5 |
| t _h Hold time | A data after CLK ↑ | | MIN | 1 | 0.7 | 0.7 | 1.3 |
| | Data after LE ↓, CLK high | | MIN | 0.8 | 1.4 | 1.4 | 1.6 |
| | Data after LE ↓, CLK low | | MIN | 0.8 | 1.4 | 1.4 | 1.4 |
| t _{PLH} | A | Y | MAX | 3.7 | 3.6 | 3.6 | 2.5 |
| t _{PHL} | | | | 3.7 | 3.6 | 3.6 | 2.5 |
| t _{PLH} | LE | Y | MAX | 5.1 | 4.2 | 4.2 | 3.8 |
| t _{PHL} | | | | 5.1 | 4.2 | 4.2 | 3.8 |
| t _{PLH} | CLK | Y | MAX | 5.1 | 4.5 | 4.5 | 3.1 |
| t _{PHL} | | | | 5.1 | 4.5 | 4.5 | 3.1 |
| t _{PZH} | OE | Y | MAX | 4.6 | 4.6 | 4.6 | 6.2 |
| t _{PZL} | | | | 4.6 | 4.6 | 4.6 | 6.2 |
| t _{PHZ} | OE | Y | MAX | 5.8 | 3.9 | 3.9 | 5.3 |
| t _{PLZ} | | | | 5.8 | 3.9 | 3.9 | 5.3 |

UNIT f_{max} : MHz other : ns

20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram


FUNCTION TABLE
 (each 10-bit latch)

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | ALVCH 3V | UNIT |
|-----------------|------------|-----|------|-------------|------|
| I _{CC} | MAX | 89 | 0.08 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 24 | mA |

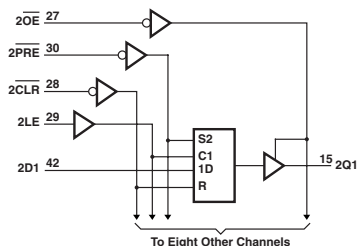
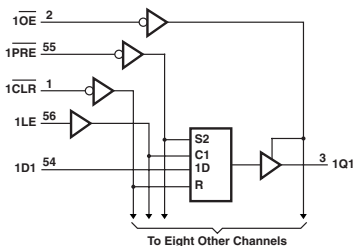
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | | OUTPUT | MAX or MIN | ABT | ACT | ALVCH 3V |
|-------------------------------|------------------|-------------|--------|------------|------|-----|-------------|
| | LE | high low | | | | | |
| t _w Pulse duration | LE | high | Q | MIN | 4 | 4 | 3.3 |
| | | low | | | 4 | - | 3.3 |
| t _{su} Setup time | Data before LE ↓ | | Q | MIN | 1 | 1.5 | - |
| | Data before LE ↑ | | | | - | - | 1.1 |
| t _h Hold time | Data after LE ↓ | high | Q | MIN | 2 | 3 | - |
| | | low | | | 2 | 4.5 | - |
| | Data after LE ↑ | | Q | MIN | - | - | 1.1 |
| t _{PLH} | D | Q | MAX | 5 | 11.8 | 3.9 | |
| t _{PHL} | | | | 5.1 | 12.2 | 3.9 | |
| t _{PLH} | LE | Q | MAX | 5 | 12.7 | 4.3 | |
| t _{PHL} | | | | 5 | 12.7 | 4.3 | |
| t _{PZH} | \overline{OE} | Q | MAX | 5.7 | 11.3 | 4.9 | |
| t _{PZL} | | | | 5.6 | 13.7 | 4.9 | |
| t _{PHZ} | \overline{OE} | Q | MAX | 6.5 | 10.2 | 4.1 | |
| t _{PLZ} | | | | 7.1 | 9.6 | 4.1 | |

UNIT : ns

18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit latch)

| INPUTS | | | | | OUTPUT |
|--------|-----|----|----|---|----------------|
| PRE | CLR | OE | LE | D | Q |
| L | X | L | X | X | H |
| H | L | L | X | X | L |
| H | H | L | H | L | L |
| H | H | L | H | H | H |
| H | H | L | L | X | Q ₀ |
| X | X | H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 85 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

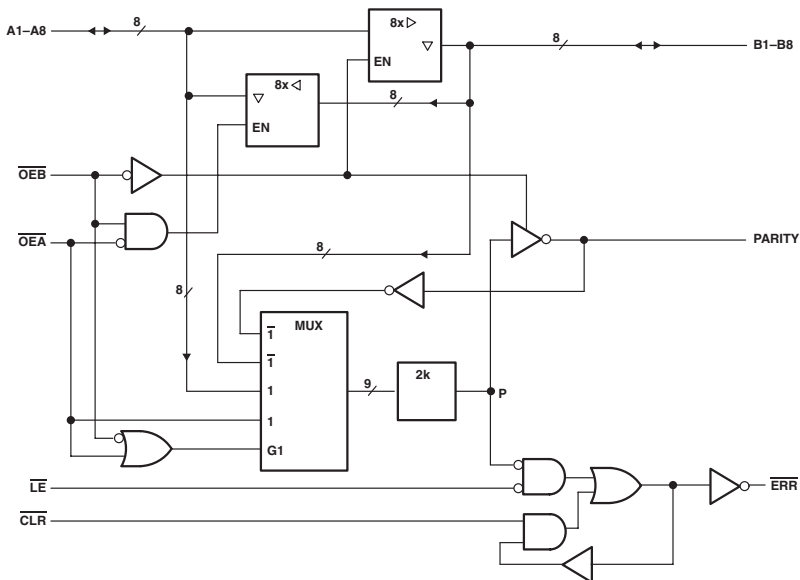
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | |
|-------------------------------|------------------------|--------|------------|-----------------------|-----|
| t _w Pulse duration | CLR low | | MIN | 3.3 | |
| | | | | PRE low | 3.3 |
| | | | | LE high | 3.3 |
| t _{su} Setup time | Data before LE ↓, high | | MIN | 0.9 | |
| | | | | Data before LE ↓, low | 0.6 |
| t _h Hold time | Data after LE ↓, high | | MIN | 1.7 | |
| | | | | Data after LE ↓, low | 1.8 |
| t _{PLH} | D | Q | MAX | 4.8 | |
| t _{PHL} | | | | 4.8 | |
| t _{PLH} | LE | Q | MAX | 5.9 | |
| t _{PHL} | | | | 5.3 | |
| t _{PLH} | PRE | Q | MAX | 6.1 | |
| t _{PHL} | | | | 5 | |
| t _{PLH} | CLR | Q | MAX | 5.4 | |
| t _{PHL} | | | | 6 | |
| t _{PZH} | OE | Q | MAX | 5.4 | |
| t _{PZL} | | | | 5.8 | |
| t _{PHZ} | OE | Q | MAX | 6.3 | |
| t _{PLZ} | | | | 5.2 | |

UNIT: ns

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | OUTPUT AND I/Os | | | | FUNCTION | |
|--------|-----|-----|----|--------------------------|----------------------------|-----------------|----|--------|--------|---|------------------------------|
| OEB | OEA | CLR | LE | A _i Σ OF H | Bi† Σ OF H | A | B | PARITY | ERR‡ | | |
| L | H | X | X | Odd Even | NA | NA | A | L H | NA | A data to B bus and generate parity | |
| H | L | H | L | NA | Odd Even | B | NA | NA | H L | B data to A bus and check parity | |
| H | L | H | H | NA | X | X | NA | NA | NC | Store error flag | |
| X | X | L | H | X | X | X | NA | NA | H | Clear error flag register | |
| H | H | X | X | L L X X | L L Odd H Even | X | Z | Z | Z | NC H H L | Isolation§ (parity check) |
| L | L | X | X | Odd Even | NA | NA | A | H L | NA | A data to B bus and generate inverted parity | |

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

| INPUTS | | INTERNAL TO DEVICE | OUTPUT | OUTPUT ERR | FUNCTION |
|--------|----|-----------------------|----------------------|---------------|----------|
| CLR | LE | POINT P | ERR _{n-1} † | | |
| L | L | L H | X | L H | Pass |
| H | L | X H | L H | L H | Sample |
| L | H | X | X | H | Clear |
| H | H | X | L H | L H | Store |

† State of ERR before changes at CLR, LE, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 40 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

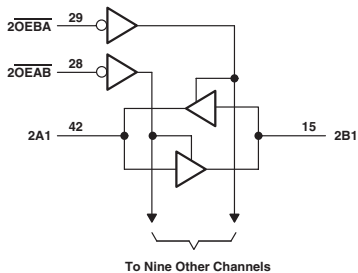
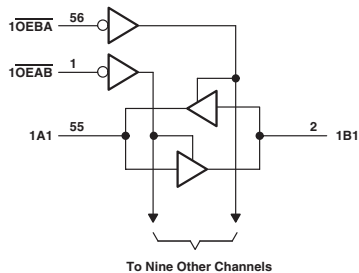
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|-------------------------------|--|------------------|------------|-----|
| t _w Pulse duration | \overline{LE} high or low | | MIN | 8.5 |
| | \overline{CLR} low | | | 4 |
| t _{su} Setup time | A, B and PARITY before $\overline{LE} \downarrow$ | | MIN | 10 |
| | \overline{CLR} before $\overline{LE} \downarrow$ | | | 0 |
| t _h Hold time | A, B and PARITY after $\overline{LE} \downarrow$ | | MIN | 0 |
| | \overline{CLR} after $\overline{LE} \downarrow$ | | | 0 |
| t _{PLH} | A or B | B or A | MAX | 4.1 |
| t _{PHL} | | | | 4.3 |
| t _{PLH} | A or \overline{OE} | PARITY | MAX | 7.1 |
| t _{PHL} | | | | 7.2 |
| t _{PLH} | \overline{CLR} | \overline{ERR} | MAX | 5.7 |
| t _{PZH} | | | | 5.6 |
| t _{PZL} | \overline{OE} | A or B | MAX | 6 |
| t _{PHZ} | | | | 5.4 |
| t _{PLZ} | \overline{OE} | A or B | MAX | 4.3 |
| t _{PZH} | | | | 5.7 |
| t _{PZL} | \overline{OE} | PARITY | MAX | 6.5 |
| t _{PHZ} | | | | 4.7 |
| t _{PLZ} | \overline{OE} | PARITY | MAX | 4.1 |
| t _{PLH} | | | | 4.8 |
| t _{PHL} | \overline{LE} | \overline{ERR} | MAX | 4.9 |
| t _{PLH} | | | | 7.2 |
| t _{PHL} | A, B or PARITY | \overline{ERR} | MAX | 7.4 |

UNIT: ns

20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

| INPUTS | | OPERATION |
|--------|------|--------------------------|
| OEAB | OEBA | |
| L | L | Latch A and B (A = B) |
| L | H | A to B |
| H | L | B to A |
| H | H | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ACT | UNIT |
|-----------|------------|------|------|
| I_{CC} | MAX | 0.08 | mA |
| I_{OH} | MAX | -24 | mA |
| I_{OL} | MAX | 24 | mA |

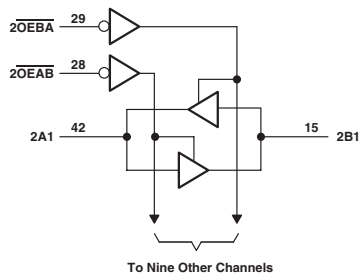
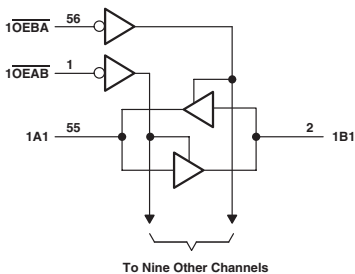
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ACT |
|-----------|--|--------|------------|------|
| t_{PLH} | A or B | B or A | MAX | 10.4 |
| t_{PHL} | | | | 11.1 |
| t_{PZH} | \overline{OEBA} or \overline{OEAB} | A or B | MAX | 10 |
| t_{PZL} | | | | 12.7 |
| t_{PHZ} | \overline{OEBA} or \overline{OEAB} | A or B | MAX | 10.7 |
| t_{PLZ} | | | | 10 |

UNIT: ns

18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

| INPUTS | | OPERATION |
|-------------------|-------------------|-----------------|
| \overline{OEAB} | \overline{OEBA} | |
| H | L | B data to A bus |
| L | H | A data to B bus |
| H | H | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | ALVCH 3V | UNIT |
|-----------|------------|-----|------|-------------|------|
| I_{CC} | MAX | 32 | 0.08 | 0.04 | mA |
| I_{OH} | MAX | -32 | -24 | -24 | mA |
| I_{OL} | MAX | 64 | 24 | 24 | mA |

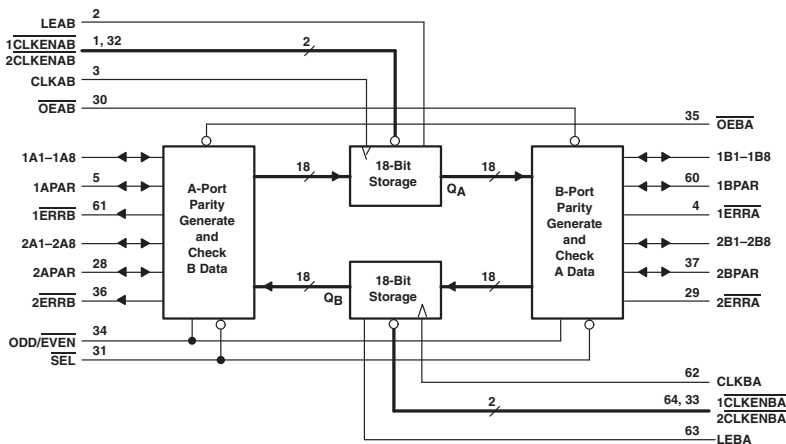
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT | ALVCH 3V |
|-----------|--|--------|------------|-----|------|-------------|
| t_{PLH} | A or B | B or A | MAX | 3.5 | 11.1 | 3.4 |
| t_{PHL} | | | | 3.9 | 11.8 | 3.4 |
| t_{PZH} | \overline{OEBA} or \overline{OEAB} | A or B | MAX | 5.4 | 10.6 | 4.7 |
| t_{PZL} | | | | 4.8 | 13.6 | 4.7 |
| t_{PHZ} | \overline{OEBA} or \overline{OEAB} | A or B | MAX | 6 | 11.6 | 4.2 |
| t_{PLZ} | | | | 5 | 11 | 4.2 |

UNIT: ns

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

Block Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT | |
|---------|------|------|-------|--------|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | B |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B ₀ † |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | B ₀ † |
| L | L | L | H | X | B ₀ ‡ |

† Output level before the indicated steady-state input conditions were established.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PARITY-ENABLE FUNCTION TABLE

| INPUTS | | | OPERATION OR FUNCTION | |
|--------|------|------|---|--|
| SEL | OEBA | OEAB | | |
| L | H | L | Parity is checked on port A and is generated on port B. | |
| L | L | H | Parity is checked on port B and is generated on port A. | |
| L | H | H | Parity is checked on port B and port A. | |
| L | L | L | Parity is generated on port A and B if device is in FF mode. | |
| H | L | L | Parity functions are disabled; device acts as a standard 18-bit registered transceiver. | |
| H | L | H | Q _A data to B, Q _B data to A | |
| H | H | L | Q _B data to A | |
| H | H | H | Q _A data to B | |
| H | H | H | Isolation | |

PARITY FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | | | | | | |
|--------|------|------|----------|--------------------------|--------------------------|------|------|------|------|-----|---|
| SEL | OEBA | OEAB | ODD/EVEN | Σ OF INPUTS A1-A8 = H | Σ OF INPUTS B1-B8 = H | APAR | BPAR | ERRA | ERRB | | |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | H | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | L | N/A | N/A | L | H | Z |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | L | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | H | N/A | N/A | H | H | Z |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | L | L | Z | N/A | H |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | L | H | Z | N/A | L |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | H | L | Z | N/A | L |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | H | H | Z | N/A | H |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | H | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | L | N/A | N/A | L | L | Z |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | H | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | H | N/A | N/A | L | L | Z |
| L | L | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | H | Z | H |
| L | L | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | L | Z | L |
| L | L | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | Z | L | L |
| L | L | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | H | Z | H |
| L | H | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | H | Z | H |
| L | H | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | H | Z | H |
| L | H | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | H | Z | H |
| L | H | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | L | Z | L |
| L | L | L | L | N/A | N/A | N/A | N/A | PE† | Z | PE† | Z |
| L | L | L | H | N/A | N/A | N/A | N/A | PO‡ | Z | PO‡ | Z |

† Parity output is set to the level so that the specific bus side is set to even parity.

‡ Parity output is set to the level so that the specific bus side is set to odd parity.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVCH 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 24 | 24 | mA |

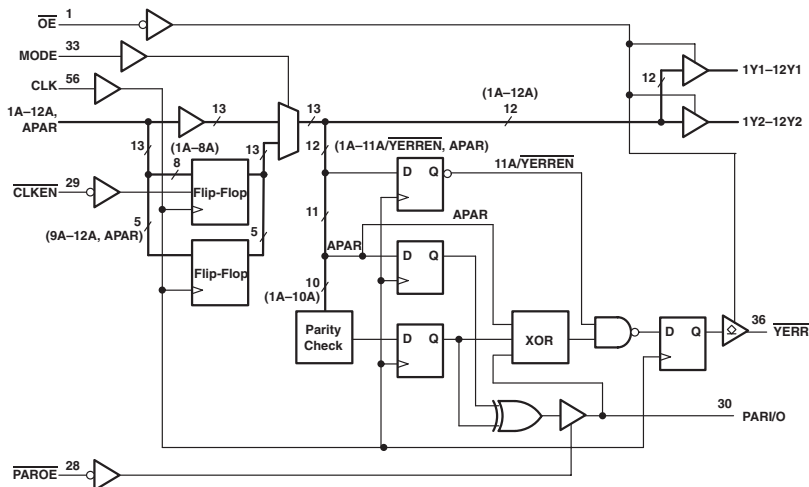
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCH 3V | ALVCH 3V |
|-------------------------------|---------------------------------|------------------------------------|------------|------------|-------------|
| f _{max} | | | MIN | 125 | 125 |
| t _w Pulse duration | CLK ↑ | | MIN | 3 | 3 |
| | LE high | | MIN | 3 | 3 |
| t _{su} Setup time | A, APAR or B, BPAR before CLK ↑ | | MIN | 2.5 | 1.7 |
| | CLKEN before CLK ↑ | | MIN | 2.5 | 1.7 |
| | A, APAR or B, BPAR before LE ↓ | | MIN | 2 | 1.2 |
| t _h Hold time | A, APAR or B, BPAR after CLK ↑ | | MIN | 1.3 | 0.5 |
| | CLKEN after CLK ↑ | | MIN | 1.5 | 0.7 |
| | A, APAR or B, BPAR after LE ↓ | | MIN | 1.7 | 0.9 |
| t _{PLH} | A or B | B or A | MAX | 5.4 | 4.4 |
| t _{PHL} | | | | 5.4 | 4.4 |
| t _{PLH} | A or B | BPAR or APAR | MAX | 7.7 | 6.7 |
| t _{PHL} | | | | 7.7 | 6.7 |
| t _{PLH} | APAR or BPAR | BPAR or APAR | MAX | 5.7 | 4.7 |
| t _{PHL} | | | | 5.7 | 4.7 |
| t _{PLH} | APAR or BPAR | ERRA or ERRB | MAX | 8.5 | 7.5 |
| t _{PHL} | | | | 8.5 | 7.5 |
| t _{PLH} | ODD / EVEN | ERRA or ERRB | MAX | 7.8 | 6.8 |
| t _{PHL} | | | | 7.8 | 6.8 |
| t _{PLH} | ODD / EVEN | BPAR or APAR | MAX | 7.5 | 6.5 |
| t _{PHL} | | | | 7.5 | 6.5 |
| t _{PLH} | SEL | BPAR or APAR | MAX | 6.1 | 5.1 |
| t _{PHL} | | | | 6.1 | 5.1 |
| t _{PLH} | CLKAB or CLKBA | A or B | MAX | 6.1 | 5.1 |
| t _{PHL} | | | | 6.1 | 5.1 |
| t _{PLH} | CLKAB or CLKBA | BPAR or APAR parity feedthrough | MAX | 6.6 | 5.6 |
| t _{PHL} | | | | 6.6 | 5.6 |
| t _{PLH} | CLKAB or CLKBA | BPAR or APAR parity generated | MAX | 8.7 | 7.7 |
| t _{PHL} | | | | 8.7 | 7.7 |
| t _{PLH} | CLKAB or CLKBA | ERRA or ERRB | MAX | 8.9 | 7.9 |
| t _{PHL} | | | | 8.9 | 7.9 |
| t _{PLH} | LEAB or LEBA | A or B | MAX | 5.8 | 4.8 |
| t _{PHL} | | | | 5.8 | 4.8 |
| t _{PLH} | LEAB or LEBA | BPAR or APAR parity feedthrough | MAX | 6.3 | 5.3 |
| t _{PHL} | | | | 6.3 | 5.3 |
| t _{PLH} | LEAB or LEBA | BPAR or APAR parity generated | MAX | 8.4 | 7.4 |
| t _{PHL} | | | | 8.4 | 7.4 |
| t _{PLH} | LEAB or LEBA | ERRA or ERRB | MAX | 8.5 | 7.5 |
| t _{PHL} | | | | 8.5 | 7.5 |
| t _{PZH} | OEAB or OEBA | B, BPAR or A, APAR | MAX | 6.3 | 5.3 |
| t _{PZL} | | | | 6.3 | 5.3 |
| t _{PHZ} | OEAB or OEBA | B, BPAR or A, APAR | MAX | 5.9 | 4.9 |
| t _{P LZ} | | | | 5.9 | 4.9 |
| t _{PZH} | OEAB or OEBA | ERRA or ERRB | MAX | 5.9 | 4.9 |
| t _{PZL} | | | | 5.9 | 4.9 |
| t _{PHZ} | OEAB or OEBA | ERRA or ERRB | MAX | 6.7 | 5.7 |
| t _{P LZ} | | | | 6.7 | 5.7 |
| t _{PZH} | SEL | ERRA or ERRB | MAX | 6.5 | 5.5 |
| t _{PZL} | | | | 6.5 | 5.5 |
| t _{PHZ} | SEL | ERRA or ERRB | MAX | 5.9 | 4.9 |
| t _{PHZ} | | | | 5.9 | 4.9 |

UNIT f_{max} : MHz other : ns

3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | |
|--------|------|-------|-----|---------|-------------------------------|--------------------------------|
| OE | MODE | CLKEN | CLK | A | $1Y_n^\dagger - 8Y_n^\dagger$ | $9Y_n^\dagger - 12Y_n^\dagger$ |
| L | L | L | ↑ | H | H | H |
| L | L | L | ↑ | L | L | L |
| L | L | H | ↑ | H | Y_0 | H |
| L | L | H | ↑ | L | Y_0 | L |
| L | H | X | X | H | H | H |
| L | H | X | X | L | L | L |
| H | X | X | X | X | Z | Z |

† $n=1,2$

PARI/O FUNCTION†

| INPUTS | | | | OUTPUT PARI/O |
|--------|------------------------------------|------|---|------------------|
| PAROE | Σ OF INPUTS 1A - 10A = H | APAR | | |
| L | 0, 2, 4, 6, 8, 10 | L | L | |
| L | 1, 3, 5, 7, 9 | L | H | |
| L | 0, 2, 4, 6, 8, 10 | H | H | |
| L | 1, 3, 5, 7, 9 | H | L | |
| H | X | X | Z | |

† This table applies to the first device of a cascaded pair of ALVCH16903 devices.

PARITY FUNCTION

| INPUTS | | | | | | OUTPUT YERR |
|--------|--------|-------------|--------|------------------------------------|------|----------------|
| OE | PAROE‡ | 11A/YERREN§ | PARI/O | Σ OF INPUTS 1A - 10A = H | APAR | |
| L | H | L | L | 0, 2, 4, 6, 8, 10 | L | H |
| L | H | L | L | 1, 3, 5, 7, 9 | L | L |
| L | H | L | L | 0, 2, 4, 6, 8, 10 | H | L |
| L | H | L | L | 1, 3, 5, 7, 9 | H | H |
| L | H | L | H | 0, 2, 4, 6, 8, 10 | L | L |
| L | H | L | H | 1, 3, 5, 7, 9 | L | H |
| L | H | L | H | 0, 2, 4, 6, 8, 10 | H | H |
| L | H | L | H | 1, 3, 5, 7, 9 | H | L |
| H | X | X | X | X | X | H |
| L | X | H | X | X | X | H |

‡ When used as a single device, PAROE must be tied high.

§ Valid after appropriate number of clock pulses have set internal register.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

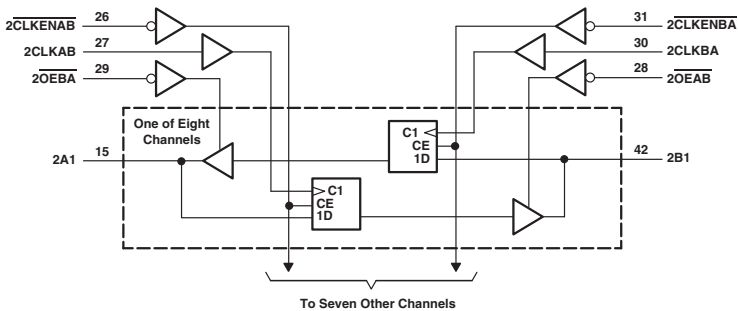
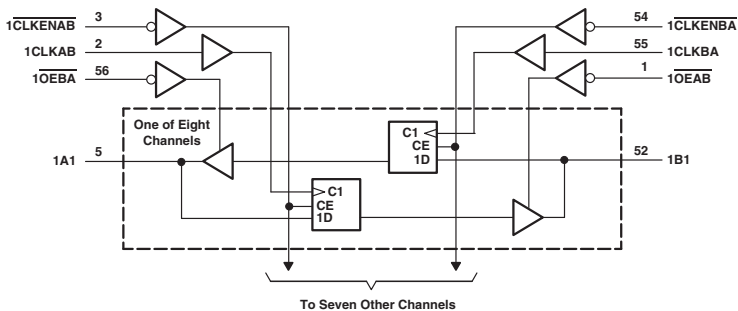
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | |
|--------------------------------------|--------------------------------------|--------|------------|-------------|-----|
| f _{max} | | | MIN | 125 | |
| t _w Pulse duration | CLK ↑ | | MIN | 3 | |
| t _{su} Setup time | 1A-12A before CLK ↑, resistor mode | | MIN | 1.45 | |
| | 1A-10A before CLK ↑, buffer mode | | MIN | 4.4 | |
| | APAR before CLK ↑, resistor mode | | MIN | 1.3 | |
| | APAR before CLK ↑, buffer mode | | MIN | 3.1 | |
| | PARI/O before CLK ↑, both mode | | MIN | 1.7 | |
| | 11A/YERREN before CLK ↑, buffer mode | | MIN | 1.6 | |
| | CLKEN before CLK ↑, resistor mode | | MIN | 2.2 | |
| | CLKEN before CLK ↑, buffer mode | | MIN | 0.55 | |
| t _h Hold time | 1A-12A after CLK ↑, resistor mode | | MIN | 0.25 | |
| | 1A-10A after CLK ↑, buffer mode | | MIN | 0.7 | |
| | APAR after CLK ↑, resistor mode | | MIN | 0.25 | |
| | APAR after CLK ↑, buffer mode | | MIN | 0.4 | |
| | PARI/O before CLK ↑, resistor mode | | MIN | 0.5 | |
| | PARI/O before CLK ↑, buffer mode | | MIN | 0.4 | |
| | 11A/YERREN after CLK ↑, buffer mode | | MIN | 0.4 | |
| | CLKEN after CLK ↑, resistor mode | | MIN | 0.4 | |
| t _{PLH} t _{PHL} | Buffer mode | A | Y | MAX | 3.8 |
| | | | | | 3.8 |
| t _{PLH} t _{PHL} | Both mode | CLK | YERR | MAX | 4.4 |
| | | | | | 4.4 |
| t _{PLH} t _{PHL} | Both mode | CLK | PARI / O | MAX | 6.6 |
| | | | | | 6.6 |
| t _{PLH} t _{PHL} | Both mode | MODE | Y | MAX | 4.9 |
| | | | | | 4.9 |
| t _{PLH} t _{PHL} | Resistor mode | CLK | Y | MAX | 4.8 |
| | | | | | 4.6 |
| t _{PZH} t _{PZL} | Both mode | OE | Y | MAX | 5.4 |
| | | | | | 5.4 |
| t _{PZH} t _{PZL} | Both mode | PAROE | PARI / O | MAX | 4.8 |
| | | | | | 4.8 |
| t _{PHZ} t _{PLZ} | Both mode | OE | Y | MAX | 5 |
| | | | | | 5 |
| t _{PHZ} t _{PLZ} | Both mode | PAROE | PARI / O | MAX | 3.8 |
| | | | | | 3.8 |
| t _{PLH} t _{PHL} | Both mode | OE | YERR | MAX | 4 |
| | | | | | 4.2 |

UNIT f_{max} : MHz other : ns

16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---------|------------|------|---|-----------------|
| CLKENAB | CLKAB | OEAB | A | B |
| H | X | L | X | B_0^{\dagger} |
| X | L | L | X | B_0^{\dagger} |
| L | \uparrow | L | L | L |
| L | \uparrow | L | H | H |
| H | X | H | X | Z |

\dagger A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

\ddagger Level of B before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ACT | LVT 3V | LVTH 3V | LVCH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|------|-----------|------------|------------|-------------|------|
| I _{CC} | MAX | 35 | 0.08 | 5 | 5 | 0.02 | 0.04 | mA |
| I _{OH} | MAX | -32 | -24 | -32 | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | 64 | 64 | 24 | 24 | mA |

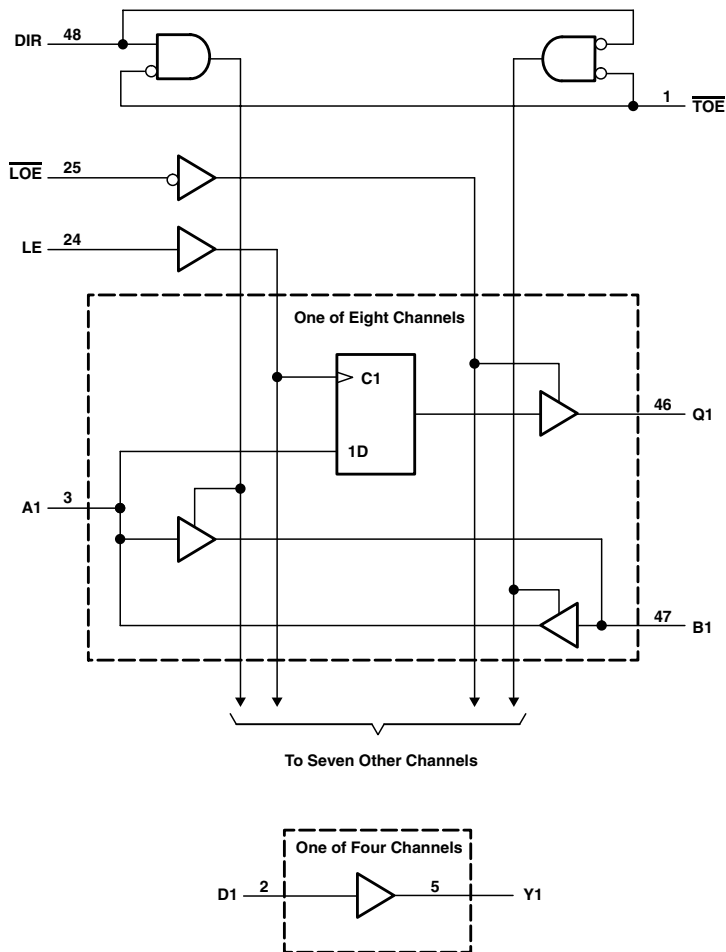
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ACT | LVT 3V | LVTH 3V | LVCH 3V | ALVCH 3V |
|-------------------------------|----------------------------------|--------|------------|-----|------|-----------|------------|------------|-------------|
| f _{max} | | | MIN | 150 | 75 | 150 | 150 | 150 | 150 |
| t _w Pulse duration | CLKEN high (SN74LVT: CLKEN high) | | MIN | - | - | 3.3 | - | - | 3.3 |
| | CLK high or low | | | 3.3 | 6.7 | 3.3 | 3.3 | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK | | MIN | 3.5 | 5 | 2.1 | 1.7 | 2.8 | 1.5 |
| | CLKEN before CLK | | | 3 | 6.5 | 1.2 | 2 | 1.4 | 1 |
| t _h Hold time | Data after CLK | | MIN | 1 | 1 | 0.7 | 0.8 | 0.5 | 0.8 |
| | CLKEN after CLK | | | 1 | 0 | 1.4 | 0.4 | 1.9 | 1.1 |
| t _{PLH} | CLK | A or B | MAX | 4.3 | 11.8 | 5.8 | 4.4 | 6.6 | 3.9 |
| t _{PHL} | | | | 4.5 | 11.7 | 5.8 | 4.4 | 6.6 | 3.9 |
| t _{PZH} | OEBA or OEAB | A or B | MAX | 4.6 | 11.2 | 5.6 | 4.9 | 6.6 | 4.4 |
| t _{PZL} | | | | 6 | 13 | 6.5 | 4.9 | 6.6 | 4.4 |
| t _{PHZ} | OEBA or OEAB | A or B | MAX | 5.5 | 9.4 | 6.3 | 6.2 | 6.7 | 4 |
| t _{PLZ} | | | | 4.2 | 8.7 | 5.1 | 5.3 | 6.7 | 4 |

UNIT f_{max} : MHz other : ns

8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|---------------------------|
| TOE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | A bus and B bus Isolation |

| INPUTS | | | OUTPUT Q |
|--------|----|---|----------------|
| LOE | LE | A | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

| INPUT D | OUTPUT Y |
|------------|-------------|
| L | L |
| H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.03 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|------------------|--------|------------|-------------|
| t _w Pulse duration | LE high | | MIN | 2 |
| t _{su} Setup time | data before LE ↓ | | MIN | 0.9 |
| t _h Hold time | data after LE ↓ | | MIN | 0.9 |
| t _{PLH} | D | Y | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | A | Q | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | LE | Q | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | A or B | B or A | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PZH} | LOE | Q | MAX | 4.7 |
| t _{PZL} | | | | 4.7 |
| t _{PZH} | TOE | A or B | MAX | 4.4 |
| t _{PZL} | | | | 4.4 |
| t _{PZH} | DIR | A or B | MAX | 4.7 |
| t _{PZL} | | | | 4.7 |
| t _{PHZ} | LOE | Q | MAX | 4.1 |
| t _{PLZ} | | | | 4.1 |
| t _{PHZ} | TOE | A or B | MAX | 4.1 |
| t _{PLZ} | | | | 4.1 |
| t _{PHZ} | DIR | A or B | MAX | 4.7 |
| t _{PLZ} | | | | 4.7 |

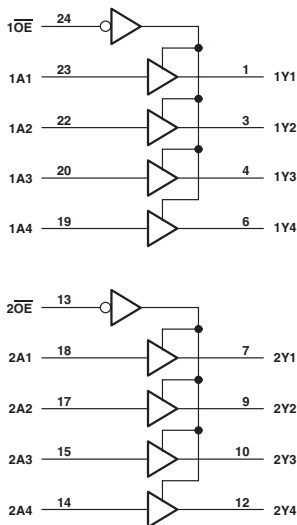
UNIT: ns

25244

25-Ω OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE (each buffer/driver)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | SN64 BCT | UNIT |
|-----------|------------|----------|----------|------|
| I_{CC} | MAX | 119 | 119 | mA |
| I_{OH} | MAX | -80 | -80 | mA |
| I_{OL} | MAX | 188 | 188 | mA |

SWITCHING CHARACTERISTICS

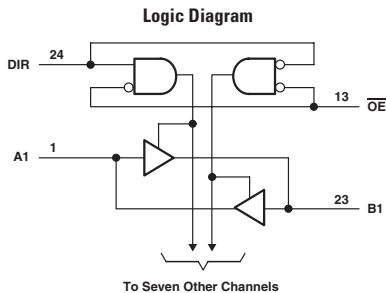
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | SN64 BCT |
|-----------|-----------------|--------|------------|----------|----------|
| t_{PLH} | A | Y | MAX | 5.5 | 5.5 |
| t_{PHL} | | | | 6 | 6.3 |
| t_{PZH} | \overline{OE} | Y | MAX | 9.3 | 9.7 |
| t_{PZL} | | | | 10.2 | 10.4 |
| t_{PHZ} | \overline{OE} | Y | MAX | 6.3 | 6.5 |
| t_{PLZ} | | | | 8.4 | 9.5 |

UNIT: ns

25245

25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | SN64 BCT | ABTH | UNIT |
|-------------------|------------|----------|----------|------|------|
| I_{CC} | MAX | 125 | 125 | 20 | mA |
| I_{OH} (A port) | MAX | -80 | -80 | -80 | mA |
| I_{OH} (B port) | MAX | -3 | -3 | -32 | mA |
| I_{OL} (A port) | MAX | 188 | 188 | 188 | mA |
| I_{OL} (B port) | MAX | 24 | 24 | 64 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT | SN64 BCT | ABTH |
|-----------|-----------------|--------|------------|----------|----------|------|
| t_{PLH} | A | B | MAX | 5.7 | 5.7 | 3.9 |
| t_{PHL} | | | | 7.2 | 7.3 | 4.3 |
| t_{PLH} | B | A | MAX | 5.5 | 5.5 | 3.9 |
| t_{PHL} | | | | 6.2 | 6.3 | 4.3 |
| t_{PZH} | \overline{OE} | A | MAX | 9.6 | 9.7 | 6.5 |
| t_{PZL} | | | | 10.3 | 10.6 | 6.8 |
| t_{PHZ} | \overline{OE} | A | MAX | 6.2 | 6.2 | 7.2 |
| t_{PLZ} | | | | 8.3 | 8.8 | 6.4 |
| t_{PZH} | \overline{OE} | B | MAX | 8.9 | 8.9 | 6.5 |
| t_{PZL} | | | | 9.7 | 9.9 | 6.8 |
| t_{PHZ} | \overline{OE} | B | MAX | 6.9 | 6.9 | 7.2 |
| t_{PLZ} | | | | 7.5 | 7.7 | 6.4 |

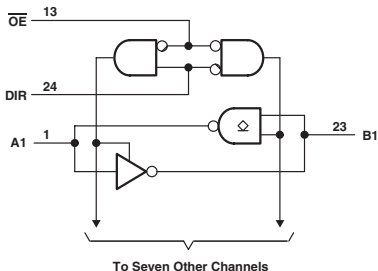
UNIT: ns

25642

25-Ω OCTAL BUS TRANSCEIVER

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|-------------------|------------|----------|------|
| I_{CC} | MAX | 125 | mA |
| I_{OH} (B port) | MAX | -3 | mA |
| I_{OL} (A port) | MAX | 188 | mA |
| I_{OL} (B port) | MAX | 24 | mA |
| V_{OH} (A port) | MAX | 5.5 | V |

SWITCHING CHARACTERISTICS

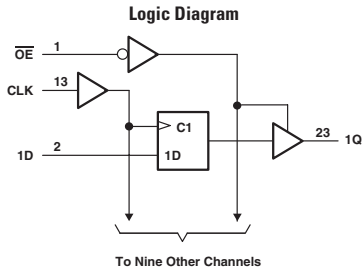
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|-----------|-----------------|--------|------------|----------|
| t_{PLH} | A | B | MAX | 6.2 |
| t_{PHL} | | | | 4 |
| t_{PLH} | B | A | MAX | 6.3 |
| t_{PHL} | | | | 5.9 |
| t_{PLH} | \overline{OE} | A | MAX | 11.6 |
| t_{PHL} | | | | 11.3 |
| t_{PZH} | \overline{OE} | B | MAX | 9.1 |
| t_{PZL} | | | | 9.8 |
| t_{PHZ} | \overline{OE} | B | MAX | 7.3 |
| t_{PLZ} | | | | 7.3 |

UNIT: ns

29821

10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|--------|--------|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | UNIT |
|-----------------|------------|-----|----------|------|
| I _{CC} | MAX | 115 | 35 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 48 | 48 | mA |

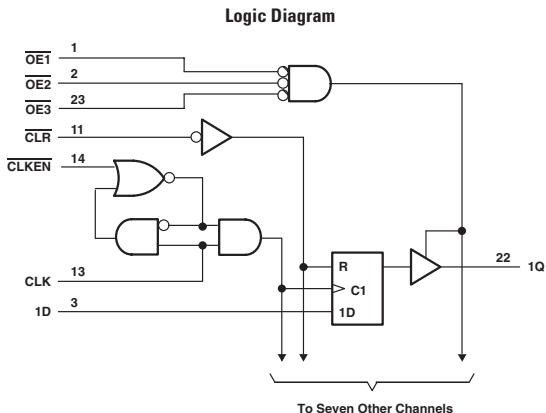
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT |
|-------------------------------|-------------------|--------|------------|-----|----------|
| f _{max} | | | | - | 125 |
| t _w Pulse duration | CLK high or low | | MIN | 7 | 7 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 4 | 7 |
| t _h Hold time | Data after CLK ↑ | | MIN | 2 | 1 |
| t _{PLH} | CLK | Q | MAX | 10 | 12 |
| t _{PHL} | | | | 10 | 10 |
| t _{PZH} | OE | Q | MAX | 14 | 12 |
| t _{PZL} | | | | 14 | 13 |
| t _{PHZ} | OE | Q | MAX | 14 | 8 |
| t _{PLZ} | | | | 12 | 8 |

UNIT f_{max} : MHz other : ns

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

| INPUTS | | | | | OUTPUT Q |
|--------|-----|-------|--------|---|----------------|
| OE† | CLR | CLKEN | CLK | D | |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | H or L | X | Q ₀ |
| H | X | X | X | X | Z |

† OE = H if any of the output-enable inputs is high.
 OE = L if all of the output-enable inputs are low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|-----------------|------------|----------|------|
| I _{CC} | MAX | 40 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

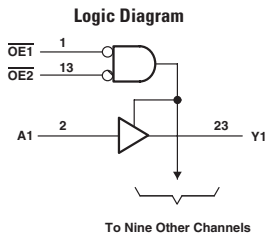
| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|-------------------------------|-------------------------|--------|------------|----------|
| f _{max} | | | MIN | 125 |
| t _w Pulse duration | CLK low | | MIN | 4 |
| | CLK high or low | | MIN | 4 |
| t _{su} Setup time | Before CLK ↑, data high | | MIN | 6 |
| | Before CLK ↑, data low | | MIN | 3.5 |
| | CLR | | MIN | 1 |
| t _h Hold time | CLKEN before CLK ↑ | | MIN | 8 |
| | After CLK ↑, data high | | MIN | 1.5 |
| | After CLK ↑, data low | | MIN | 0 |
| | CLKEN after CLK ↑ | | MIN | 0.5 |
| t _{PLH} | CLK | Q | MAX | 9 |
| t _{PHL} | | | | 8.4 |
| t _{PHL} | CLR | Q | MAX | 9.5 |
| t _{PZH} | OE | Q | MAX | 10.3 |
| t _{PZL} | | | | 10.2 |
| t _{PHZ} | OE | Q | MAX | 9 |
| t _{PLZ} | | | | 8.2 |

UNIT f_{max} : MHz other : ns

29827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| L | X | X | Z |
| H | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | UNIT |
|-----------------|------------|-----|----------|------|
| I _{CC} | MAX | 40 | 40 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 48 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT |
|------------------|-------|--------|------------|-----|----------|
| t _{PLH} | A | Y | MAX | 7 | 5.5 |
| | | | | 7.5 | 7.5 |
| t _{PHL} | OE | Y | MAX | 15 | 9.1 |
| | | | | 15 | 12.8 |
| t _{PHZ} | OE | Y | MAX | 17 | 8.8 |
| | | | | 12 | 8.4 |

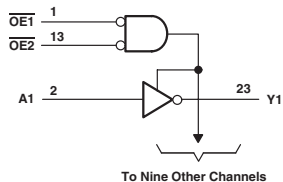
UNIT: ns

29828

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | UNIT |
|-----------|------------|-----|------|
| I_{CC} | MAX | 40 | mA |
| I_{OH} | MAX | -24 | mA |
| I_{OL} | MAX | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS |
|-----------|-----------------|--------|------------|-----|
| t_{PLH} | A | Y | MAX | 7 |
| t_{PHL} | | | | 7.5 |
| t_{PZH} | \overline{OE} | Y | MAX | 15 |
| t_{PZL} | | | | 15 |
| t_{PHZ} | \overline{OE} | Y | MAX | 17 |
| t_{PLZ} | | | | 12 |

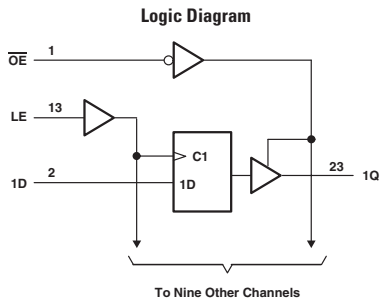
UNIT: ns

NOTICE : ALS IS NOT RECOMMENDED FOR NEW DESIGNS

29841

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|----|---|----------------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | UNIT |
|-----------------|------------|-----|----------|------|
| I _{CC} | MAX | 85 | 35 | mA |
| I _{OH} | MAX | -24 | -24 | mA |
| I _{OL} | MAX | 48 | 48 | mA |

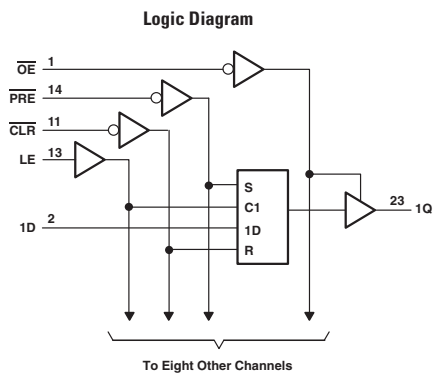
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT |
|-------------------------------|-----------------------|--------|------------|-----|----------|
| t _w Pulse duration | LE high or low | | MIN | 6 | 4 |
| t _{su} Setup time | Data before LE ↓ | | MIN | 2.5 | 2 |
| t _h Hold time | Data after LE ↓, high | | MIN | 4.5 | 1.5 |
| | Data after LE ↓, low | | MIN | 4.5 | 3.5 |
| t _{PLH} | D | Q | MAX | 9.5 | 7.5 |
| t _{PHL} | | | | 9.5 | 8.6 |
| t _{PLH} | LE | Q | MAX | 12 | 8.6 |
| t _{PHL} | | | | 12 | 8.1 |
| t _{PZH} | \overline{OE} | Q | MAX | 14 | 9.2 |
| t _{PZL} | | | | 14 | 12.8 |
| t _{PHZ} | \overline{OE} | Q | MAX | 15 | 6.9 |
| t _{PLZ} | | | | 12 | 6.9 |

UNIT: ns

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

| INPUTS | | | | | OUTPUT Q |
|--------|-----|----|----|---|----------------|
| PRE | CLR | OE | LE | D | |
| L | X | L | X | X | H |
| H | L | L | X | X | L |
| H | H | L | H | L | L |
| H | H | L | H | H | H |
| H | H | L | L | X | Q ₀ |
| X | X | H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

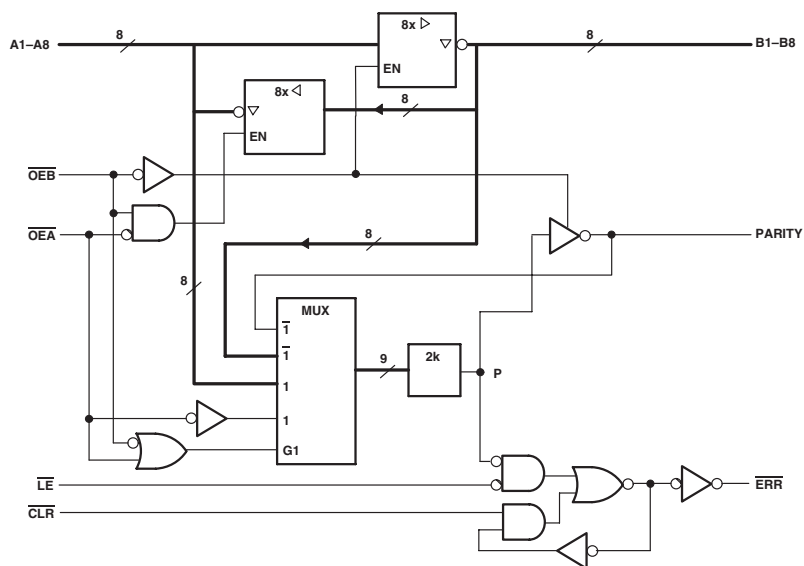
| PARAMETER | MAX or MIN | SN74 BCT | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 35 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | SN74 BCT |
|-------------------------------|-------------------------------|--------|------------|-------------|
| t _w Pulse duration | PRE low | | MIN | 7 |
| | CLR low | | | 5 |
| | LE high | | | 4 |
| t _{su} Setup time | Data before LE ↓, high or low | | MIN | 1.5 |
| | PRE or CLR inactive | | | 2 |
| t _h Hold time | Data after LE ↓, high or low | | MIN | 3.5 |
| t _{PLH} | D | Q | MAX | 8 |
| t _{PHL} | | | | 9 |
| t _{PLH} | LE | Q | MAX | 10 |
| t _{PHL} | | | | 10 |
| t _{PLH} | PRE | Q | MAX | 12 |
| t _{PHL} | | | | 12 |
| t _{PLH} | CLR | Q | MAX | 12 |
| t _{PHL} | | | | 12 |
| t _{PZH} | OE | Q | MAX | 15 |
| t _{PZL} | | | | 15 |
| t _{PHZ} | OE | Q | MAX | 8 |
| t _{PLZ} | | | | 8 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | | | OUTPUT AND I/O | | | | OPERATION |
|--------|-----|-----|----|------------------------------|----------------------|-----------|----------------|--------|--------|--|-----------|
| OEB | OEA | CLR | LE | Ai Σ of Hs Odd Even | Bit Σ of Ls NA | A | B | PARITY | ERR‡ | | |
| L | H | X | X | Odd Even | NA | NA | \bar{A} | H L | NA | \bar{A} data to B bus and generate parity | |
| H | L | X | L | NA | Odd Even | \bar{B} | NA | NA | H L | \bar{B} data to A bus and check parity | |
| H | L | H | H | NA | X | X | NA | NA | N-1 | Store error flag | |
| X | X | L | H | X | X | X | NA | NA | H | Clear error-flag register | |
| H | H | X | X | H L X H | H X L H | X | Z | Z | Z | Isolation§ | |
| L | L | X | X | Odd Even | NA | NA | \bar{A} | L H | NA | \bar{A} data to B bus and generate inverted parity | |

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states Shown assume ERR was previously high.

§ In this mode, ERR, when enabled, shows inverted parity of the A bus.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALS | SN74 BCT | UNIT |
|-----------|------------|-----|-------------|------|
| Icc | MAX | 100 | 80 | mA |
| Ioh | MAX | -24 | -24 | mA |
| Iol | MAX | 48 | 48 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT |
|-------------------|---|------------------|------------|-----|-------------|
| tw Pulse duration | \overline{LE} high | | MIN | 10 | - |
| | \overline{LE} low | | MIN | 10 | 10 |
| | \overline{CLR} low | | MIN | 10 | 10 |
| tsu Setup time | Before \overline{LE} ↓, Bi and PARITY | | MIN | 10 | 18 |
| | Before \overline{LE} ↓, \overline{CLR} high | | MIN | 15 | - |
| th Hold time | Bi and PARITY after \overline{LE} ↓ | | MIN | 3 | 8 |
| tPLH | A or B | B or A | MAX | 8 | 8 |
| tPHL | | | | 8 | 8 |
| tPLH | A | PARITY | MAX | 15 | 15 |
| tPHL | | | | 18 | 15 |
| tPZH | | | | 17 | 17 |
| tPZL | \overline{OEA} or \overline{OEB} | A or B | MAX | 17 | 19 |
| tPHZ | | | | 15 | 15 |
| tPLZ | \overline{OEA} or \overline{OEB} | A or B | MAX | 8 | 17 |
| tPHL | | | | 12 | 9 |
| tPLH | \overline{CLR} | \overline{ERR} | MAX | 12 | 15 |
| tPLH | \overline{OEA} | PARITY | MAX | 17 | 15 |
| tPHL | | | | 19 | 16 |
| tPLH | | | | 20 | 20 |
| tPHL | Bi / PARITY | \overline{ERR} | MAX | 20 | 15 |

UNIT: ns

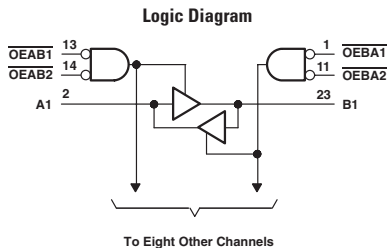
29863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- True Outputs

FUNCTION TABLE

| INPUTS | | | | OPERATION |
|--------------------|--------------------|--------------------|--------------------|---------------|
| $\overline{OEAB1}$ | $\overline{OEAB2}$ | $\overline{OEBA1}$ | $\overline{OEBA2}$ | |
| L | L | L | L | Latch A and B |
| L | L | H | X | A to B |
| L | L | X | H | A to B |
| H | X | L | L | B to A |
| X | H | L | L | B to A |
| H | X | H | X | Isolation |
| H | X | X | H | |
| X | H | X | H | |
| X | H | H | X | |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

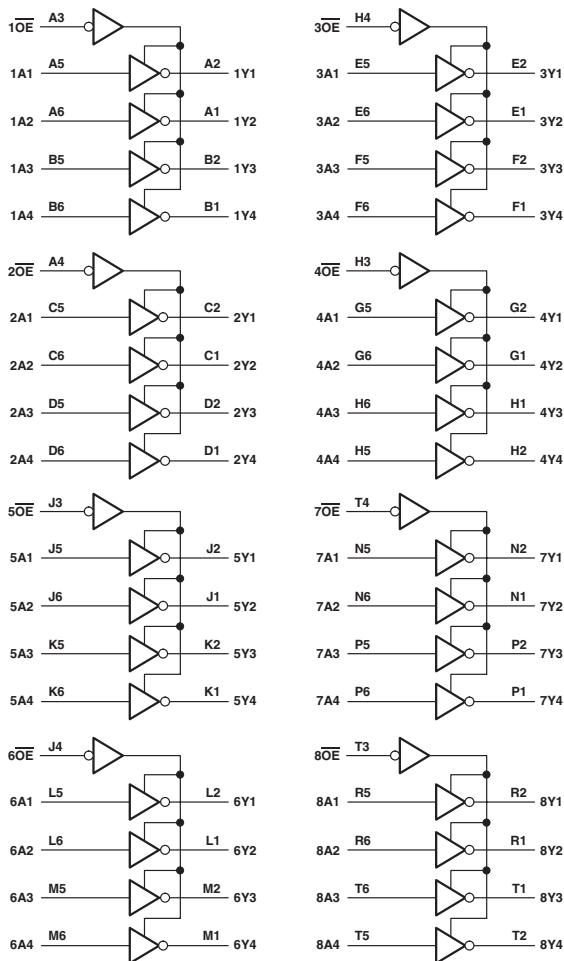
| PARAMETER | MAX or MIN | ALS | SN74 BCT | UNIT |
|-----------|------------|-----|----------|------|
| I_{CC} | MAX | 65 | 45 | mA |
| I_{OH} | MAX | -24 | -24 | mA |
| I_{OL} | MAX | 48 | 48 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALS | SN74 BCT |
|-----------|--|--------|------------|-----|----------|
| t_{PLH} | A or B | B or A | MAX | 8 | 5 |
| t_{PHL} | | | | 8 | 7.5 |
| t_{PZH} | \overline{OEAB} or \overline{OEBA} | A or B | MAX | 15 | 8.4 |
| t_{PZL} | | | | 15 | 12.6 |
| t_{PHZ} | \overline{OEAB} or \overline{OEBA} | A or B | MAX | 17 | 8.8 |
| t_{PLZ} | | | | 12 | 8.1 |

UNIT: ns

Logic Diagram



FUNCTION TABLE

(each 4bit buffer/driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

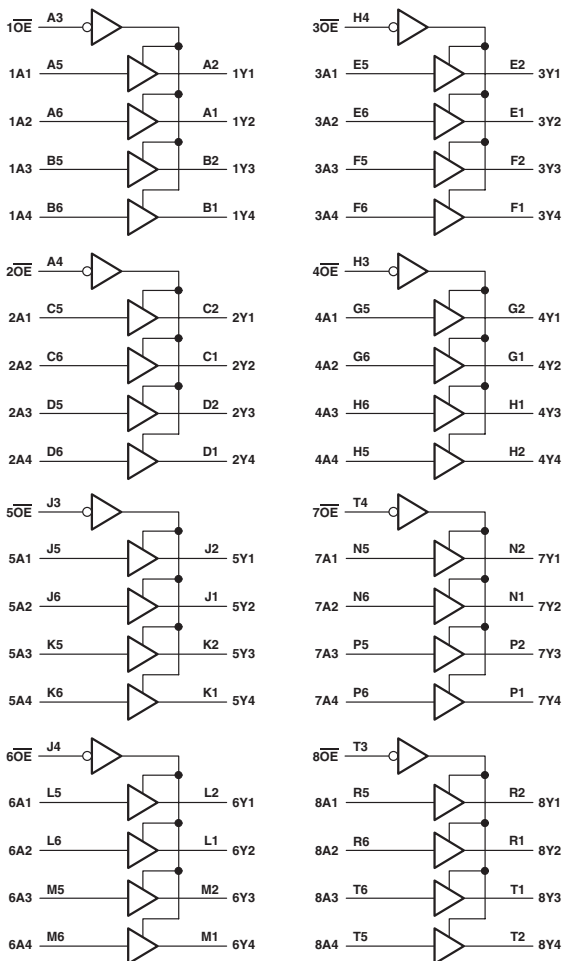
| PARAMETER | MAX or MIN | LVCZ 3V | LVT | UNIT |
|-----------------|------------|------------|-----|------|
| I _{CC} | MAX | 0.2 | 10 | mA |
| I _{OH} | MAX | -24 | -32 | mA |
| I _{OL} | MAX | 24 | 64 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCZ 3V | LVT |
|------------------|------------------------|--------|------------|------------|-----|
| t _{PLH} | A | Y | MAX | 4.2 | 3.5 |
| t _{PHL} | | | MAX | 4.2 | 3.5 |
| t _{PZH} | $\overline{\text{OE}}$ | Y | MAX | 4.7 | 4 |
| t _{PZL} | | | MAX | 4.7 | 4.4 |
| t _{PHZ} | $\overline{\text{OE}}$ | Y | MAX | 5.9 | 4.5 |
| t _{PLZ} | | | MAX | 5.9 | 4.2 |

UNIT:ns

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVT 3V | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | LVCZ 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------------|------------|-----------|------------|-------------|-----------|------------|------------|-------------|-------------|-------------|--------------|--------------|------|
| I _{CC} | MAX | 10 | 10 | 5 | 0.04 | 0.04 | 0.2 | 0.08 | 0.04 | 0.04 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 24 | 24 | 8 | 9 | 8 | 9 | mA |

SWITCHING CHARACTERISTICS

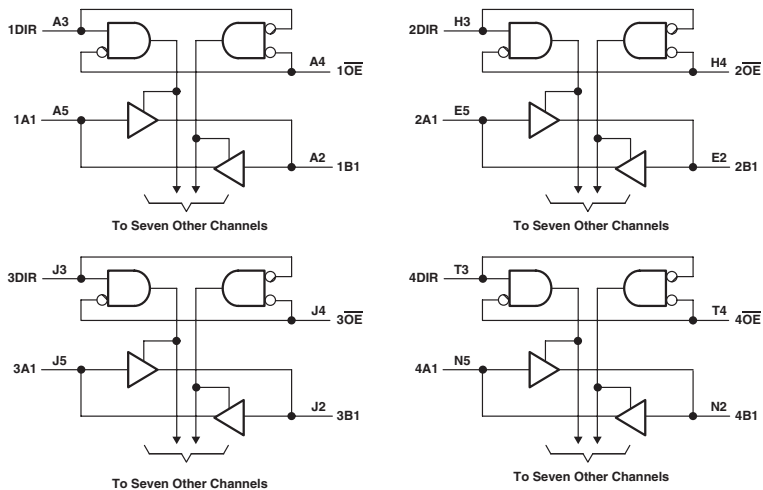
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVT 3V | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | LVCZ 3V | ALVCH 3V | AUC 1.8V |
|------------------|-----------------|--------|------------|-----------|------------|-------------|-----------|------------|------------|-------------|-------------|
| t _{PLH} | A | Y | MAX | 3.2 | 3.2 | 2.4 | 4.1 | 4.1 | 4.1 | 3 | 1.8 |
| t _{PHL} | | | | 3.2 | 3.2 | 2.5 | 4.1 | 4.1 | 4.1 | 3 | 1.8 |
| t _{PZH} | \overline{OE} | Y | MAX | 4 | 4 | 3.8 | 4.6 | 4.6 | 4.6 | 4.4 | 2.5 |
| t _{PZL} | | | | 4 | 4 | 2.9 | 4.6 | 4.6 | 4.6 | 4.4 | 2.5 |
| t _{PHZ} | \overline{OE} | Y | MAX | 4.5 | 4.5 | 4.2 | 5.8 | 5.8 | 5.8 | 4.1 | 4.0 |
| t _{PLZ} | | | | 4.2 | 4.2 | 3.6 | 5.8 | 5.8 | 5.8 | 4.1 | 4.0 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUC 2.3V | AUCH 1.8V | AUCH 2.3V |
|------------------|-----------------|--------|------------|-------------|--------------|--------------|
| t _{PLH} | A | Y | MAX | 1.8 | 1.8 | 1.8 |
| t _{PHL} | | | | 1.8 | 1.8 | 1.8 |
| t _{PZH} | \overline{OE} | Y | MAX | 1.9 | 2.5 | 1.9 |
| t _{PZL} | | | | 1.9 | 2.5 | 1.9 |
| t _{PHZ} | \overline{OE} | Y | MAX | 2 | 4.0 | 2 |
| t _{PLZ} | | | | 2 | 4.0 | 2 |

UNIT: ns

32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE
(each 9-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ABTH | LVTH 3V | LVC 3V | LVCV 3V | LVCHR 3V | LVCR 3V | LVCZ 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | UNIT |
|-----------------|------------|-----|------|------------|-----------|------------|-------------|------------|------------|-------------|-------------|-------------|------|
| I _{CC} | MAX | 20 | 20 | 10 | 0.02 | 0.04 | 0.04 | 0.02 | 0.12 | 0.08 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -32 | -24 | -24 | -12 | -12 | -24 | -24 | -8 | -9 | mA |
| I _{OL} | MAX | 64 | 64 | 64 | 24 | 24 | 12 | 12 | 24 | 24 | 8 | 9 | mA |

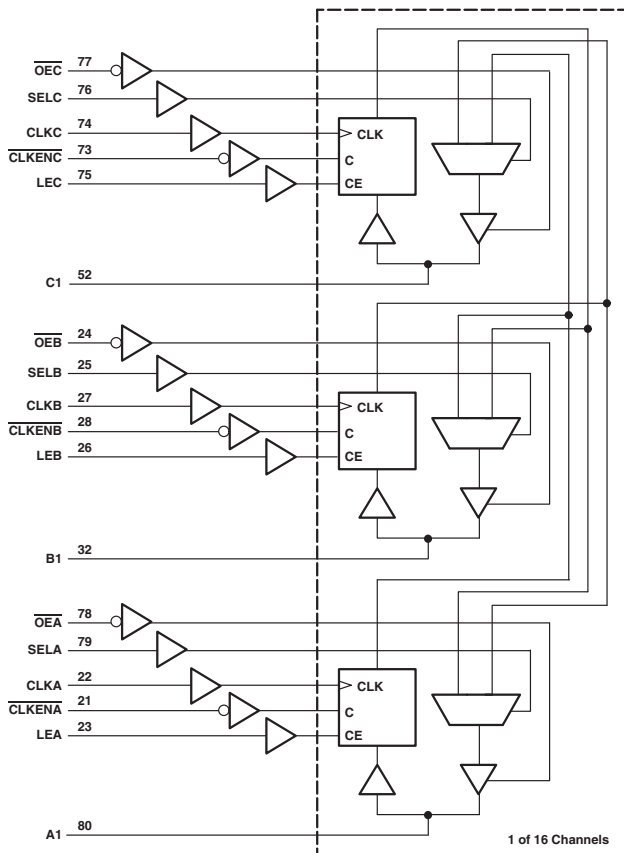
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABTH | LVTH 3V | LVC 3V | LVCV 3V | LVCHR 3V | LVCR 3V | LVCZ 3V | UNIT |
|------------------|-----------------|--------|------------|-----|------|------------|-----------|------------|-------------|------------|------------|------|
| t _{PLH} | A or B | B or A | MAX | 5 | 5 | 3.3 | 4 | 4 | 4.8 | 4.8 | 4.0 | |
| | | | | 5.2 | 5.2 | 3.3 | 4 | 4 | 4.8 | 4.8 | 4.0 | |
| t _{PZH} | \overline{OE} | B or A | MAX | 7.3 | 7.3 | 4.5 | 5.5 | 5.5 | 6.3 | 6.3 | 5.6 | |
| | | | | 8.1 | 8.1 | 4.6 | 5.5 | 5.5 | 6.3 | 6.3 | 5.6 | |
| t _{PZL} | \overline{OE} | B or A | MAX | 6.5 | 6.5 | 5.1 | 6.6 | 6.6 | 7.4 | 7.4 | 6.6 | |
| | | | | 6.9 | 6.9 | 5.1 | 6.6 | 6.6 | 7.4 | 7.4 | 6.6 | |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | AUC 1.8V | AUC 2.3V |
|------------------|-----------------|--------|------------|-------------|-------------|-------------|
| t _{PLH} | A or B | B or A | MAX | 3 | 2.0 | 1.9 |
| | | | | 3 | 2.0 | 1.9 |
| t _{PZH} | \overline{OE} | B or A | MAX | 4.4 | 3.1 | 2.6 |
| | | | | 4.4 | 3.1 | 2.6 |
| t _{PZL} | \overline{OE} | B or A | MAX | 4.1 | 4.8 | 2.9 |
| | | | | 4.1 | 4.8 | 2.9 |

UNIT: ns

Logic Diagram



**FUNCTION TABLE
STORAGE[†]**

| INPUTS | | | | OUTPUT |
|--------|------|-----|---|-----------------------------|
| CLKENA | CLKA | LEA | A | |
| H | X | L | X | Q ₀ [†] |
| L | ↑ | L | L | L |
| L | ↑ | L | H | H |
| X | H | L | X | Q ₀ [†] |
| X | L | L | X | Q ₀ [†] |
| X | X | H | L | L |
| X | X | H | H | H |

[†] A-port register shown, B and C ports are similar but use CLKENB, CLKENC, CLKB, CLKC, LEB, and LEC.

[‡] Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT

| INPUTS | | OUTPUT A |
|--------|------|----------------------|
| OEA | SELA | |
| H | X | Z |
| L | H | Output of C register |
| L | L | Output of B register |

B-PORT OUTPUT

| INPUTS | | OUTPUT B |
|--------|------|----------------------|
| OEB | SELB | |
| H | X | Z |
| L | H | Output of A register |
| L | L | Output of C register |

C-PORT OUTPUT

| INPUTS | | OUTPUT C |
|--------|------|----------------------|
| OEC | SELC | |
| H | X | Z |
| L | H | Output of B register |
| L | L | Output of A register |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

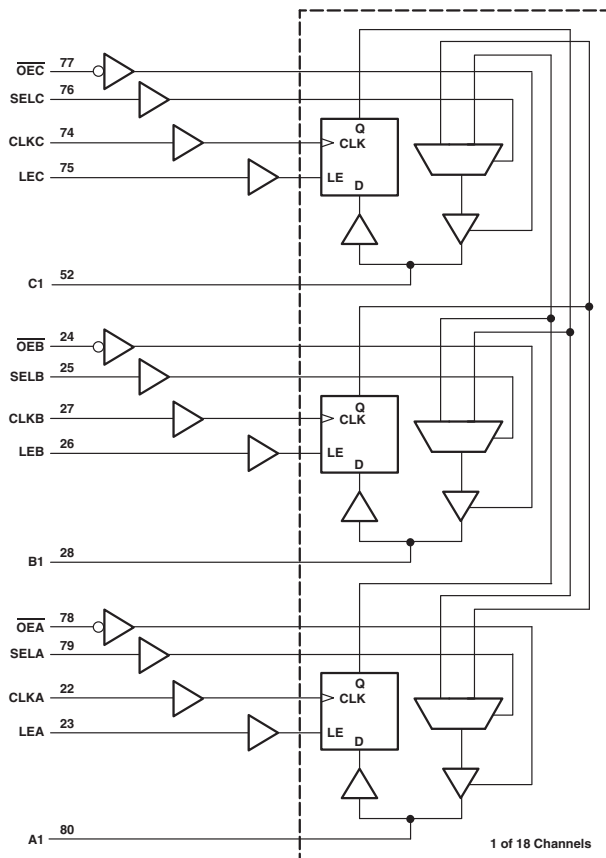
| PARAMETER | MAX or MIN | ABTH | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 40 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH |
|-------------------------------|-------------------------|------------|------------|------|
| t _{max} | | | MIN | 150 |
| t _w Pulse duration | LE high | | MIN | 3.3 |
| | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | A, B, or C before CLK ↑ | | MIN | 2.4 |
| | A or B before LE ↓ | | MIN | 2.1 |
| | CLKEN before CLK ↑ | | MIN | 3.2 |
| t _h Hold time | A, B, or C after CLK ↑ | | MIN | 1.4 |
| | A or B after LE ↓ | | MIN | 2.1 |
| | CLKEN after CLK ↑ | | MIN | 1.1 |
| t _{PLH} | A, B, or C | C, B, or A | MAX | 6.1 |
| t _{PHL} | | | | 6.6 |
| t _{PLH} | SEL | A, B, or C | MAX | 6.5 |
| t _{PHL} | | | | 6.5 |
| t _{PLH} | LE | A, B, or C | MAX | 7.5 |
| t _{PHL} | | | | 6.9 |
| t _{PLH} | CLK | A, B, or C | MAX | 7.5 |
| t _{PHL} | | | | 6.7 |
| t _{PZH} | \overline{OE} | A, B, or C | MAX | 6.4 |
| t _{PZL} | | | | 6.8 |
| t _{PHZ} | \overline{OE} | A, B, or C | MAX | 6 |
| t _{PLZ} | | | | 6.1 |

UNIT f_{max} : MHz other : ns

Logic Diagram



**FUNCTION TABLE
STORAGE**

| INPUTS | | | OUTPUT |
|--------|-----|---|---------------|
| CLKA | LEA | A | |
| ↑ | L | L | L |
| ↑ | L | H | H |
| H | L | X | Q_0^\dagger |
| L | L | X | Q_0^\dagger |
| X | H | L | L |
| X | H | H | H |

† A-port register shown. B and C ports are similar but use CLKB, CLKC, LEB, and LEC.
‡ Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT

| INPUTS | | OUTPUT A |
|--------|------|----------------------|
| OEA | SELA | |
| H | X | Z |
| L | H | Output of C register |
| L | L | Output of B register |

B-PORT OUTPUT

| INPUTS | | OUTPUT B |
|--------|------|----------------------|
| OEB | SELB | |
| H | X | Z |
| L | H | Output of A register |
| L | L | Output of C register |

C-PORT OUTPUT

| INPUTS | | OUTPUT C |
|--------|------|----------------------|
| OEC | SELC | |
| H | X | Z |
| L | H | Output of B register |
| L | L | Output of A register |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | UNIT |
|-----------|------------|------|------|
| ICC | MAX | 45 | mA |
| IDH | MAX | -32 | mA |
| IOL | MAX | 64 | mA |

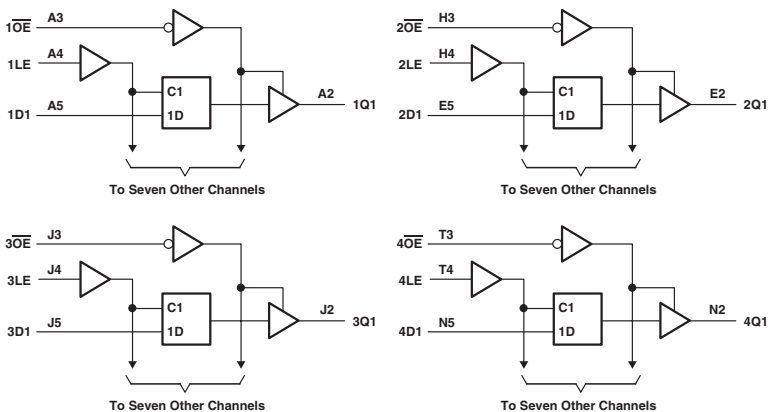
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH |
|----------------------|-------------------------|------------|------------|------|
| f_{max} | | | MIN | 150 |
| t_w Pulse duration | LE high | | MIN | 3.3 |
| | CLK high or low | | MIN | 3.3 |
| t_{su} Setup time | A, B, or C before CLK ↑ | | MIN | 2.4 |
| | A, B, or C before LE ↓ | | MIN | 2.1 |
| t_h Hold time | A, B, or C after CLK ↑ | | MIN | 1.4 |
| | A, B, or C after LE ↓ | | MIN | 2.1 |
| TPLH | A, B, or C | C, B, or A | MAX | 6.1 |
| TPHL | | | 6.6 | |
| TPLH | SEL | A, B, or C | MAX | 6.5 |
| TPHL | | | 6.5 | |
| TPLH | LE | A, B, or C | MAX | 7.5 |
| TPHL | | | 6.9 | |
| TPLH | CLK | A, B, or C | MAX | 7.4 |
| TPHL | | | 6.7 | |
| TPZH | \overline{OE} | A, B, or C | MAX | 6.8 |
| TPZL | | | 7.1 | |
| TPHZ | \overline{OE} | A, B, or C | MAX | 6.2 |
| TPLZ | | | 6 | |

UNIT f_{max} : MHz other: ns

32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | UNIT |
|-----------------|------------|------------|-------------|-----------|------------|------|
| I _{CC} | MAX | 10 | 5 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -32 | -32 | -24 | -24 | mA |
| I _{OL} | MAX | 64 | 64 | 24 | 24 | mA |

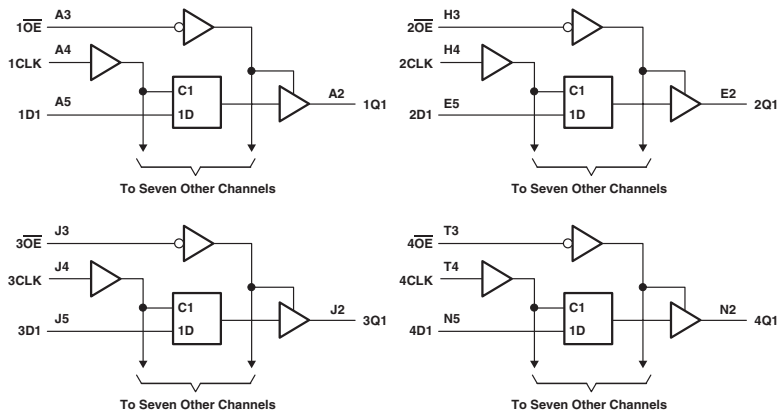
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V |
|---|-----------------------------|--------|------------|------------|-------------|-----------|------------|
| t _w Pulse duration, LE high or low | | | MIN | 3 | 1.5 | 3.3 | 3.3 |
| t _{su} Setup time | Data before LE ↓, data high | | MIN | 1 | 1.4 | 1.7 | 1.7 |
| | Data before LE ↓, data low | | MIN | 1 | 0.9 | 1.7 | 1.7 |
| t _h Hold time | Data after LE ↓, data high | | MIN | 1 | 0.9 | 1.2 | 1.2 |
| | Data after LE ↓, data low | | MIN | 1 | 1.4 | 1.2 | 1.2 |
| t _{PLH} | D | Q | MAX | 3.8 | 3.1 | 4.2 | 4.2 |
| t _{PHL} | | | | 3.6 | 3.3 | 4.2 | 4.2 |
| t _{PLH} | LE | Q | MAX | 4.3 | 3.3 | 4.6 | 4.6 |
| t _{PHL} | | | | 4 | 3.5 | 4.6 | 4.6 |
| t _{PZH} | \overline{OE} | Q | MAX | 4.3 | 4 | 4.7 | 4.7 |
| t _{PZL} | | | | 4.3 | 3.4 | 4.7 | 4.7 |
| t _{PHZ} | \overline{OE} | Q | MAX | 5 | 4.9 | 5.9 | 5.9 |
| t _{P LZ} | | | | 4.7 | 4.5 | 5.9 | 5.9 |

UNIT: ns

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|--------|--------|---|----------------|
| OE | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V | AUCH 1.8V | AUCH 2.3V | UNIT |
|-----------------|------------|------------|-------------|-----------|------------|-------------|-------------|-------------|--------------|--------------|------|
| I _{cc} | MAX | 10 | 5 | 0.04 | 0.04 | 0.08 | 0.04 | 0.04 | 0.04 | 0.04 | mA |
| I _{oh} | MAX | -32 | -32 | -24 | -24 | -24 | -8 | -9 | -8 | -9 | mA |
| I _{ol} | MAX | 64 | 64 | 24 | 24 | 24 | 8 | 9 | 8 | 9 | mA |

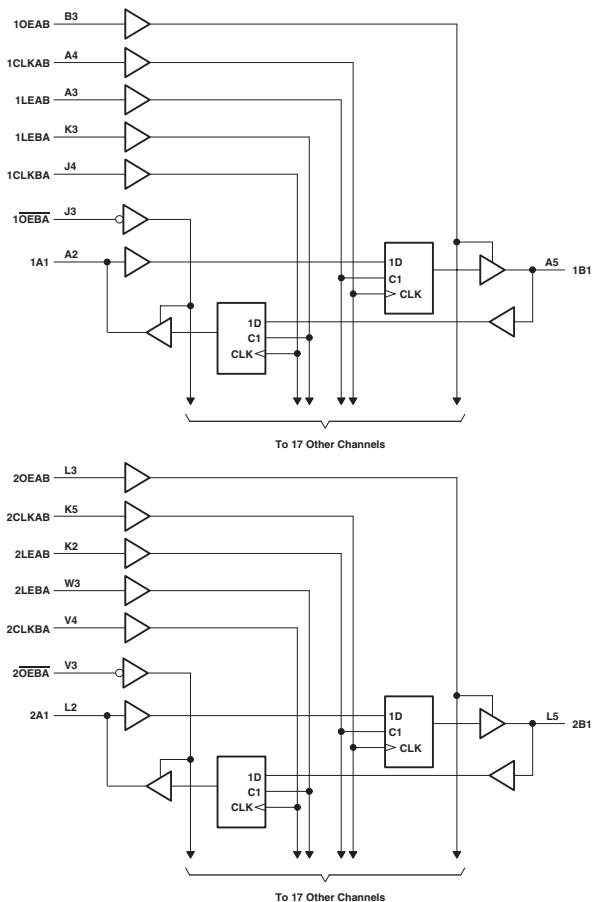
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | ALVCH 3V | AUC 1.8V | AUC 2.3V |
|--|-----------------|------------------------------|------------|------------|-------------|-----------|------------|-------------|-------------|-------------|
| f _{max} | | | | 160 | 250 | 150 | 150 | 150 | 250 | 250 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 | 1.5 | 3.3 | 3.3 | 3.3 | 1.9 | 1.9 |
| t _{su} Setup time | | Data before CLK ↑, data high | MIN | 1.8 | 1 | 1.9 | 1.9 | 1.9 | 0.6 | 0.6 |
| | | Data before CLK ↑, data low | MIN | 1.8 | 1.5 | 1.9 | 1.9 | 1.9 | 0.6 | 0.6 |
| t _h Hold time | | Data after CLK ↑, data high | MIN | 0.8 | 0.5 | 1.9 | 1.1 | 0.5 | 0.4 | 0.4 |
| | | Data after CLK ↑, data low | MIN | 0.8 | 1 | 1.9 | 1.1 | 0.5 | 0.4 | 0.4 |
| t _{PLH} | CLK | Q | MAX | 4.5 | 3.2 | 4.5 | 4.5 | 4.2 | 2.8 | 2.2 |
| t _{PHL} | | | | 4 | 3.2 | 4.5 | 4.5 | 4.2 | 2.8 | 2.2 |
| t _{PZH} | \overline{OE} | Q | MAX | 4.5 | 3.8 | 4.6 | 4.6 | 4.8 | 2.9 | 2.2 |
| t _{PZL} | | | | 4.4 | 3.3 | 4.6 | 4.6 | 4.8 | 2.9 | 2.2 |
| t _{PHZ} | \overline{OE} | Q | MAX | 5 | 4.6 | 5.5 | 5.5 | 4.3 | 4.5 | 2.2 |
| t _{PLZ} | | | | 4.6 | 4.2 | 5.5 | 5.5 | 4.3 | 4.5 | 2.2 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | AUCH 1.8V | AUCH 2.3V |
|--|-----------------|------------------------------|------------|--------------|--------------|
| f _{max} | | | | 250 | 250 |
| t _w Pulse duration, CLK high or low | | | MIN | 1.9 | 1.9 |
| t _{su} Setup time | | Data before CLK ↑, data high | MIN | 0.6 | 0.6 |
| | | Data before CLK ↑, data low | MIN | 0.6 | 0.6 |
| t _h Hold time | | Data after CLK ↑, data high | MIN | 0.4 | 0.4 |
| | | Data after CLK ↑, data low | MIN | 0.4 | 0.4 |
| t _{PLH} | CLK | Q | MAX | 2.8 | 2.2 |
| t _{PHL} | | | | 2.8 | 2.2 |
| t _{PZH} | \overline{OE} | Q | MAX | 2.9 | 2.2 |
| t _{PZL} | | | | 2.9 | 2.2 |
| t _{PHZ} | \overline{OE} | Q | MAX | 4.5 | 2.2 |
| t _{PLZ} | | | | 4.5 | 2.2 |

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE†

| INPUTS | | | | | OUTPUT |
|--------|------|-------|---|---|------------------|
| OEAB | LEAB | CLKAB | A | | B |
| L | X | X | X | X | Z |
| H | H | X | L | L | L |
| H | H | X | H | H | H |
| H | L | ↑ | L | L | L |
| H | L | ↑ | H | H | H |
| H | L | H | X | X | B ₀ ‡ |
| H | L | L | X | X | B ₀ § |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | ALVCH 3V | UNIT |
|-----------------|------------|------|-------------|------|
| I _{CC} | MAX | 90 | 0.08 | mA |
| I _{OH} | MAX | -32 | -24 | mA |
| I _{OL} | MAX | 64 | 24 | mA |

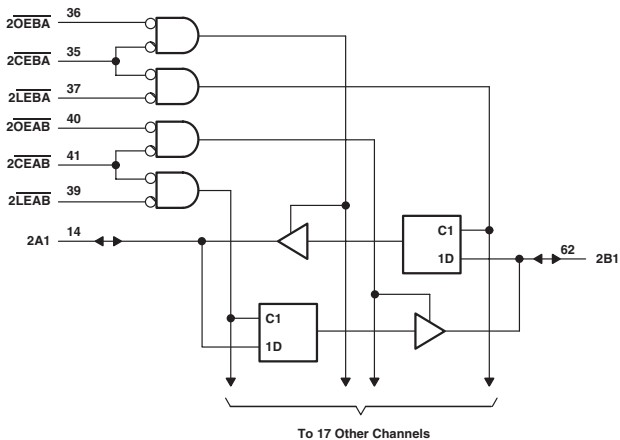
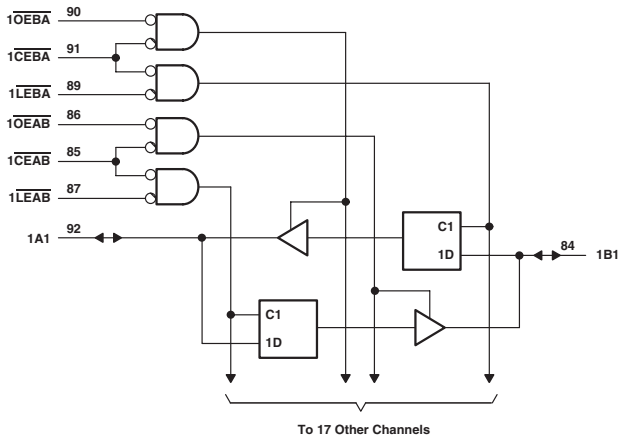
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH | ALVCH 3V |
|-------------------------------|------------------------------------|--------|------------|------|-------------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 3.3 | 3.3 |
| | CLKAB or CLKBA high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | A before CLKAB ↑ | | MIN | 3.5 | 1.7 |
| | B before CLKBA ↑ | | MIN | 3.5 | 1.7 |
| | A before LEAB ↓ or LEBA ↓ CLK high | | MIN | 1.6 | 1.5 |
| | A before LEAB ↓ or LEBA ↓ CLK low | | MIN | 1.6 | 1 |
| t _h Hold time | A after CLKAB ↑ or B after CLKBA ↑ | | MIN | 0 | 0.7 |
| | A after LEAB ↓ or B after LEBA ↓ | | MIN | 1.6 | 1.4 |
| †P _{LH} | A or B | B or A | MAX | 4.8 | 3.9 |
| †P _{HL} | | | | 5.4 | 3.9 |
| †P _{ZH} | LEAB or LEBA | B or A | MAX | 5.3 | 4.6 |
| †P _{ZL} | | | | 5.5 | 4.6 |
| †P _{HZ} | CLKAB or CLKBA | B or A | MAX | 5.3 | 4.9 |
| †P _{LZ} | | | | 5.4 | 4.9 |
| †P _{ZH} | OEAB | B | MAX | 5.6 | 4.6 |
| †P _{ZL} | | | | 6 | 4.6 |
| †P _{HZ} | OEAB | B | MAX | 5.9 | 5 |
| †P _{LZ} | | | | 5.6 | 5 |
| †P _{ZH} | OEBA | A | MAX | 5.6 | 5 |
| †P _{ZL} | | | | 6 | 5 |
| †P _{HZ} | OEBA | A | MAX | 5.9 | 4.2 |
| †P _{LZ} | | | | 5.6 | 4.2 |

UNIT f_{max} : MHz other : ns

36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|------|------|---|---------------|
| CEAB | LEAB | OEAB | A | Y |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B_0^\dagger |
| L | L | L | L | L |
| L | L | L | H | H |

† A-to-B data flow is shown; B-to-A flow conditions is the same that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | UNIT |
|-----------------|------------|------|------|
| I _{CC} | MAX | 20 | mA |
| I _{OH} | MAX | -32 | mA |
| I _{OL} | MAX | 64 | mA |

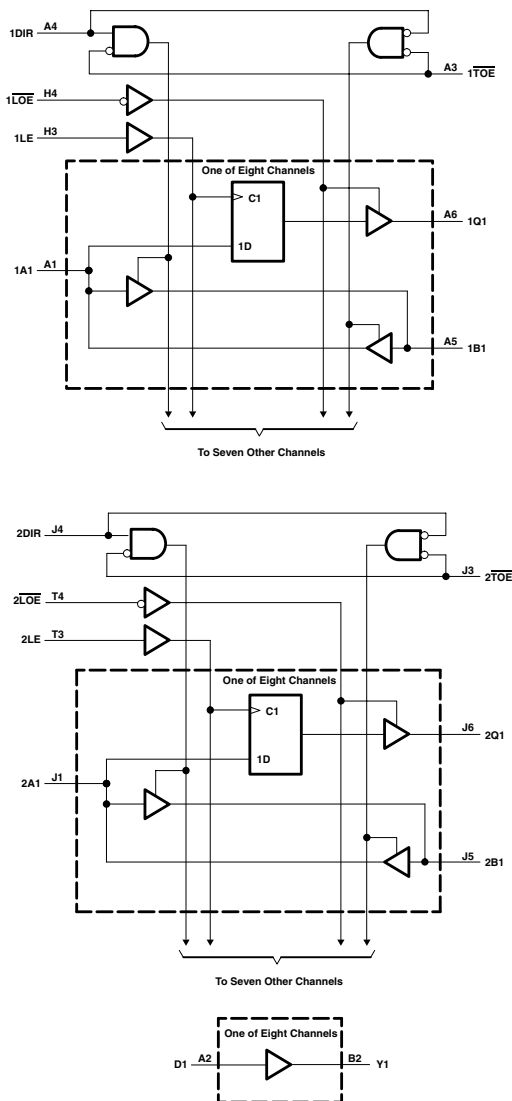
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH |
|---|--|--------|------------|------|
| t _w Pulse duration, \overline{LEAB} or \overline{LEBA} low | | | MIN | 3.3 |
| t _{su} Setup time | Data before $\overline{LEAB} \uparrow$ or $\overline{LEBA} \uparrow$ | | MIN | 2.1 |
| | Data before $\overline{CEAB} \uparrow$ or $\overline{CEBA} \uparrow$ | | MIN | 1.7 |
| t _h Hold time | Data after $\overline{LEAB} \uparrow$ or $\overline{LEBA} \uparrow$ | | MIN | 0.6 |
| | Data after $\overline{CEAB} \uparrow$ or $\overline{CEBA} \uparrow$ | | MIN | 0.9 |
| t _{PLH} | A or B | B or A | MAX | 5.9 |
| t _{PHL} | | | | 5.7 |
| t _{PLH} | \overline{LE} | A or B | MAX | 7.5 |
| t _{PHL} | | | | 6.6 |
| t _{PZH} | \overline{CE} | A or B | MAX | 8 |
| t _{PZL} | | | | 8.8 |
| t _{PHZ} | \overline{CE} | A or B | MAX | 7.1 |
| t _{PLZ} | | | | 7.5 |
| t _{PZH} | \overline{OE} | A or B | MAX | 7.3 |
| t _{PZL} | | | | 8.1 |
| t _{PHZ} | \overline{OE} | A or B | MAX | 6.5 |
| t _{PLZ} | | | | 6.9 |

UNIT: ns

16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH EIGHT INDEPENDENT BUFFERS

Logic Diagram



FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|---------------------------|
| TOE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | A bus and B bus Isolation |

| INPUTS | | | OUTPUT Q |
|--------|----|---|----------------|
| LOE | LE | A | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

| INPUT D | OUTPUT Y |
|---------|----------|
| L | L |
| H | H |

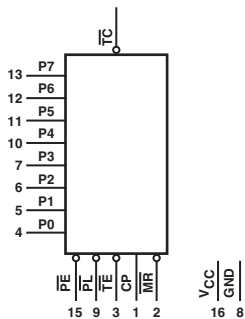
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|----------|------|
| I _{CC} | MAX | 0.06 | mA |
| I _{OH} | MAX | -24 | mA |
| I _{OL} | MAX | 24 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|------------------|--------|------------|----------|
| t _w Pulse duration | LE high | | MIN | 2 |
| t _{su} Setup time | data before LE ↓ | | MIN | 0.9 |
| t _h Hold time | data after LE ↓ | | MIN | 0.9 |
| t _{PLH} | D | Y | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | A | Q | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | LE | Q | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PLH} | A or B | B or A | MAX | 3 |
| t _{PHL} | | | | 3 |
| t _{PZH} | LOE | Q | MAX | 4.7 |
| t _{PZL} | | | | 4.7 |
| t _{PZH} | TOE | A or B | MAX | 4.4 |
| t _{PZL} | | | | 4.4 |
| t _{PZH} | DIR | A or B | MAX | 4.7 |
| t _{PZL} | | | | 4.7 |
| t _{PHZ} | LOE | Q | MAX | 4.1 |
| t _{PLZ} | | | | 4.1 |
| t _{PHZ} | TOE | A or B | MAX | 4.1 |
| t _{PLZ} | | | | 4.1 |
| t _{PHZ} | DIR | A or B | MAX | 4.7 |
| t _{PLZ} | | | | 4.7 |

UNIT: ns



FUNCTION TABLE

| CONTROL INPUTS | | | | PRESET MODE | ACTION |
|----------------|----|----|----|----------------|--|
| MR | PL | PE | TE | | |
| L | X | X | L | Synchronous | Inhibit Counter Count Down |
| X | H | X | L | | |
| X | X | L | L | Asynchronously | Preset On Next Positive Clock Transition |
| H | L | L | L | | Preset Asynchronously |
| H | L | H | L | | Clear to Maximum Count |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | CD74 HC | CD74 HCT | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.16 | 0.16 | mA |
| I _{OH} | MAX | -4 | -4 | mA |
| I _{OL} | MAX | 4 | 4 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | CD74 HC | CD74 HCT |
|------------------|----------|----------------------|------------|---------|----------|
| t _w | CP | | MIN | 50 | 53 |
| | PL | | | 38 | 65 |
| | MR | | | 38 | 53 |
| t _{su} | P to CP | | MIN | 30 | 36 |
| | PE to CP | | | 22 | 30 |
| | TE to CP | | | 45 | 60 |
| t _h | P to CP | | MIN | 5 | 5 |
| | TE to CP | | | 0 | 0 |
| | PE to CP | | | 2 | 2 |
| t _{PLH} | CP | TC (Async Preset) | MAX | 90 | 90 |
| t _{PHL} | | | | 90 | 90 |
| t _{PLH} | CP | TC (Sync Preset) | MAX | 90 | 95 |
| t _{PHL} | | | | 90 | 95 |
| t _{PLH} | TE | TC | MAX | 60 | 75 |
| t _{PHL} | | | | 60 | 75 |
| t _{PLH} | PL | TC | MAX | 83 | 102 |
| t _{PHL} | | | | 83 | 102 |
| t _{PLH} | MR | TC | MAX | 83 | 83 |
| t _{PHL} | | | | 83 | 83 |

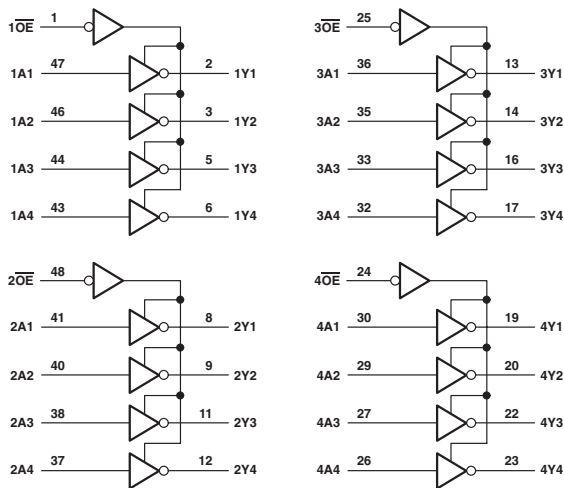
UNIT : ns

162240

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVT162240, SN74LVTH162240: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVT 3V | LVTH 3V | UNIT |
|-----------|------------|-----------|------------|------|
| I_{CC} | MAX | 5 | 5 | mA |
| I_{OH} | MAX | -12 | -12 | mA |
| I_{OL} | MAX | 12 | 12 | mA |

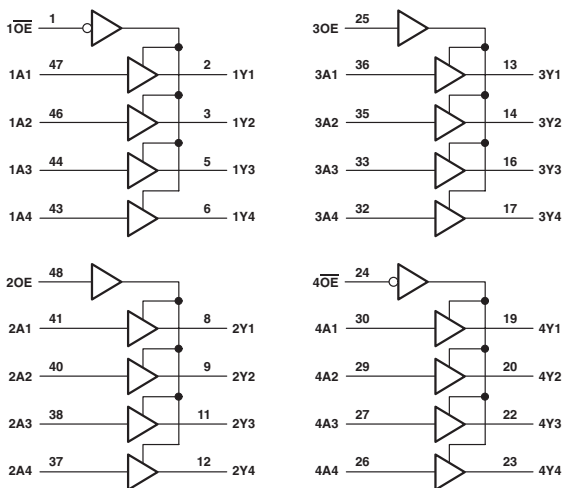
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVT 3V | LVTH 3V |
|-----------|-----------------|--------|------------|-----------|------------|
| t_{PLH} | A | Y | MAX | 4 | 4 |
| t_{PHL} | | | | 4 | 4 |
| t_{PZH} | \overline{OE} | Y | MAX | 4.8 | 4.8 |
| t_{PZL} | | | | 4.7 | 4.7 |
| t_{PHZ} | \overline{OE} | Y | MAX | 4.7 | 4.7 |
| t_{PLZ} | | | | 4.5 | 4.5 |

UNIT: ns

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT | |
|----------|--------|--------|--|
| 1OE, 4OE | 1A, 4A | 1Y, 4Y | |
| L | H | H | |
| L | L | L | |
| H | X | Z | |

| INPUTS | | OUTPUT | |
|----------|--------|--------|--|
| 2OE, 3OE | 2A, 3A | 2Y, 3Y | |
| H | H | H | |
| H | L | L | |
| L | X | Z | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | UNIT |
|-----------|------------|------------|------|
| I_{CC} | MAX | 5 | mA |
| I_{OH} | MAX | -12 | mA |
| I_{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

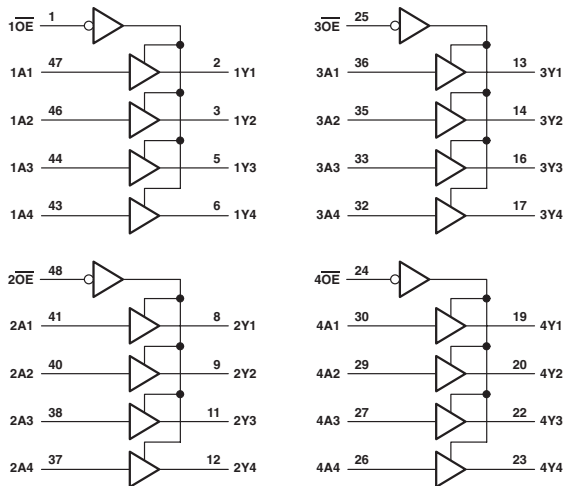
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V |
|-----------|-----------------------|--------|------------|------------|
| t_{PLH} | A | Y | MAX | 4.1 |
| t_{PHL} | | | | 4.1 |
| t_{FZH} | \overline{OE} or OE | Y | MAX | 4.9 |
| t_{FZL} | | | | 4.8 |
| t_{PHZ} | \overline{OE} or OE | Y | MAX | 5.3 |
| t_{PLZ} | | | | 4.9 |

UNIT: ns

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162244: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74LVT162244A, LVTH162244: Output Ports Have Equivalent 22-Ω Series Resistors
- SN74ALVTH162244: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74LVC162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74LVCH162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74ALVCH162244: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | LVT 3V | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | ALVCH 3V | UNIT |
|-----------|------------|-----|--------|---------|----------|--------|---------|----------|------|
| I_{CC} | MAX | 30 | 5 | 5 | 5 | 0.02 | 0.02 | 0.04 | mA |
| I_{OH} | MAX | -12 | -12 | -12 | -12 | -12 | -12 | -12 | mA |
| I_{OL} | MAX | 12 | 12 | 12 | 12 | 12 | 12 | 12 | mA |

SWITCHING CHARACTERISTICS

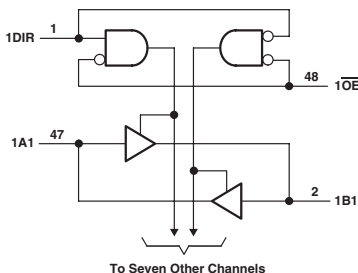
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | LVT 3V | LVTH 3V | ALVTH 3V | LVC 3V | LVCH 3V | ALVCH 3V |
|-----------|-----------------|--------|------------|-----|--------|---------|----------|--------|---------|----------|
| t_{PLH} | A | Y | MAX | 3.9 | 4 | 4 | 3.3 | 4.4 | 4.4 | 4.2 |
| t_{PHL} | | | | 4.8 | 3.6 | 3.6 | 3.3 | 4.4 | 4.4 | 4.2 |
| t_{PZH} | \overline{OE} | Y | MAX | 5.4 | 5.1 | 5.1 | 4.9 | 5.5 | 5.5 | 5.6 |
| t_{PZL} | | | | 5.1 | 4.5 | 4.5 | 3.3 | 5.5 | 5.5 | 5.6 |
| t_{PHZ} | \overline{OE} | Y | MAX | 4.6 | 5 | 5 | 4.9 | 6.3 | 6.3 | 5.5 |
| t_{PLZ} | | | | 4.5 | 5 | 5 | 4.3 | 6.3 | 6.3 | 5.5 |

UNIT: ns

16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162245, SN74ABTH162245: A-Port Outputs Have Equivalent 25- Ω Series Resistors
- SN74LVT162245A, SN74LVTH162245: A-Port Outputs Have Equivalent 22- Ω Series Resistors
- SN74ALVTH162245: A-Port Outputs Have Equivalent 30- Ω Series Resistors
- SN74LVCR162245: All Outputs Have Equivalent 26- Ω Series Resistors

Logic Diagram

FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALVTH 3V | UNIT |
|--------------------------|------------|-----|------|-----------|------------|-------------|------|
| I _{CC} | MAX | 32 | 32 | 5 | 5 | 5 | mA |
| I _{OH} (A port) | MAX | -12 | -12 | -12 | -12 | -12 | mA |
| I _{OH} (B port) | MAX | -32 | -32 | -32 | -32 | -32 | mA |
| I _{OL} (A port) | MAX | 12 | 12 | 12 | 12 | 12 | mA |
| I _{OL} (B port) | MAX | 64 | 64 | 64 | 64 | 64 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ABTH | LVT 3V | LVTH 3V | ALVTH 3V |
|------------------|-----------------|--------|------------|-----|------|-----------|------------|-------------|
| t _{PLH} | A | B | MAX | 3.9 | 3.9 | 3.3 | 3.3 | 3.1 |
| | | | | 4.2 | 4.2 | 3.3 | 3.3 | 3 |
| t _{PHL} | B | A | MAX | 4.6 | 4.6 | 4 | 4 | 3.7 |
| | | | | 5.1 | 5.1 | 3.4 | 3.4 | 3.4 |
| t _{PZH} | \overline{OE} | B | MAX | 6.3 | 6.3 | 4.6 | 4.6 | 3.8 |
| | | | | 6.4 | 6.4 | 4.6 | 4.6 | 3.4 |
| t _{PZL} | \overline{OE} | B | MAX | 6.3 | 6.3 | 5.2 | 5.2 | 4.7 |
| | | | | 5.2 | 5.2 | 5.1 | 5.1 | 4.8 |
| t _{PZH} | \overline{OE} | A | MAX | 7.1 | 7.1 | 5.3 | 5.3 | 4.7 |
| | | | | 7 | 7 | 5.1 | 5.1 | 3.9 |
| t _{PZL} | \overline{OE} | A | MAX | 6.6 | 6.6 | 5.6 | 5.6 | 5 |
| | | | | 5.7 | 5.7 | 5.5 | 5.5 | 4.9 |

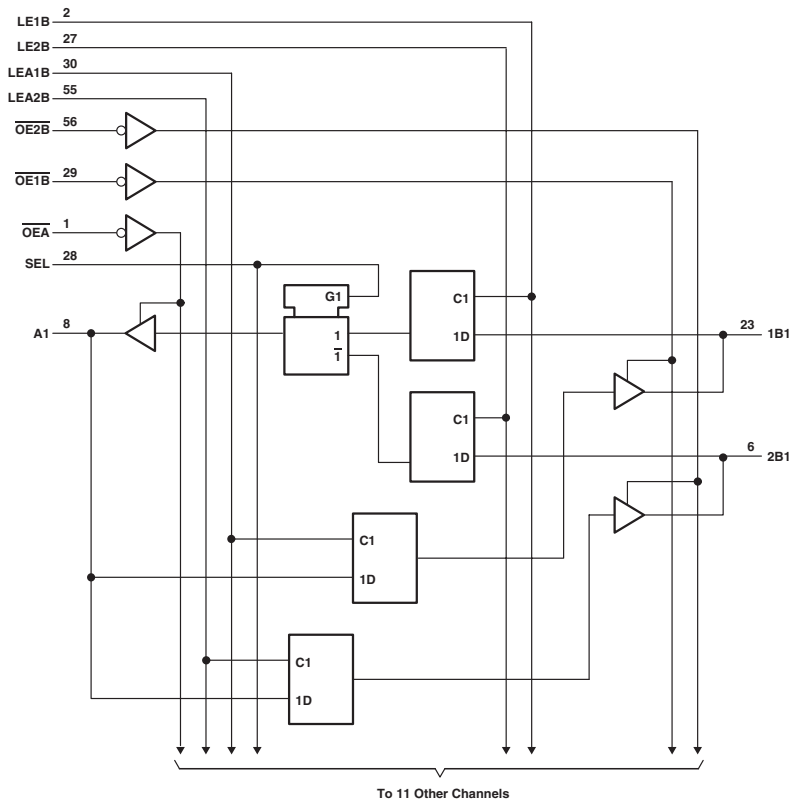
UNIT: ns

162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABTH162260: B-Port Outputs Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162260: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
B TO A ($\overline{OE} = H$)

| INPUTS | | | | | | OUTPUT |
|--------|----|-----|------|------|-----|----------------|
| 1B | 2B | SEL | LE1B | LE2B | OEA | A |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | A ₀ |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | A ₀ |
| X | X | X | X | X | H | Z |

A TO B ($\overline{OE} = H$)

| INPUTS | | | | | | OUTPUTS | |
|--------|-------|-------|-------------------|-------------------|-----------------|-----------------|--|
| A | LEA1B | LEA2B | $\overline{OE}1B$ | $\overline{OE}2B$ | 1B | 2B | |
| H | H | H | L | L | H | H | |
| L | H | H | L | L | L | L | |
| H | H | L | L | L | H | 2B ₀ | |
| L | H | L | L | L | L | 2B ₀ | |
| H | L | H | L | L | 1B ₀ | H | |
| L | L | H | L | L | 1B ₀ | L | |
| X | L | L | L | L | 1B ₀ | 2B ₀ | |
| X | X | X | H | H | Z | Z | |
| X | X | X | L | H | Active | Z | |
| X | X | X | H | L | Z | Active | |
| X | X | X | L | L | Active | Active | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | ALVCH 3V | UNIT |
|--------------------------|------------|------|-------------|------|
| I _{CC} | MAX | 63 | 0.04 | mA |
| I _{OH} (A port) | MAX | -32 | -24 | mA |
| I _{OH} (B port) | MAX | -32 | -12 | mA |
| I _{OL} (A port) | MAX | 64 | 24 | mA |
| I _{OL} (B port) | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH | ALVCH 3V |
|---|-----------------|--------|------------|------|-------------|
| f _{max} | | | | - | 150 |
| t _w Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high | | | MIN | 3.3 | 3.3 |
| t _{su} Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓ | | | MIN | 1.5 | 1.1 |
| t _h Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓ | | | MIN | 1 | 1.5 |
| t _{PLH} | A | B | MAX | 6.1 | 4.9 |
| t _{PHL} | | | | 7.1 | 4.9 |
| t _{PLH} | B | A | MAX | 6 | 4.3 |
| t _{PHL} | | | | 6.2 | 4.3 |
| t _{PLH} | LE | A | MAX | 6.3 | 4.4 |
| t _{PHL} | | | | 5.8 | 4.4 |
| t _{PLH} | LE | B | MAX | 6.1 | 5 |
| t _{PHL} | | | | 7.1 | 5 |
| t _{PLH} | SEL (1B) | A | MAX | 5.6 | 5.6 |
| t _{PHL} | SEL (2B) | | | 6.3 | 5.6 |
| t _{PLH} | SEL (1B) | | | 5 | 5.6 |
| t _{PHL} | SEL (2B) | | | 6.2 | 5.6 |
| t _{PZH} | \overline{OE} | A | MAX | 6.3 | 5.4 |
| t _{PZL} | \overline{OE} | | | 6.5 | 5.4 |
| t _{PZH} | \overline{OE} | B | MAX | 6.3 | 6 |
| t _{PZL} | \overline{OE} | | | 8.2 | 6 |
| t _{PHZ} | \overline{OE} | A | MAX | 6.7 | 4.6 |
| t _{PLZ} | | | | 5.2 | 4.6 |
| t _{PHZ} | \overline{OE} | B | MAX | 7.5 | 5.1 |
| t _{PLZ} | | | | 6.2 | 5.1 |

 UNIT f_{max} : MHz other : ns

FUNCTION TABLE
OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|-----|-----|---------|--------|
| CLK | OEA | OEB | A | 1B, 2B |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

A-TO-B STORAGE ($\overline{OEB} = L$)

| INPUTS | | | | OUTPUTS | |
|---------|---------|-----|---|-------------------|-------------------|
| CLKENA1 | CLKENA2 | CLK | A | 1B | 2B |
| H | H | X | X | 1B ₀ † | 2B ₀ † |
| L | X | ↑ | L | L† | X |
| L | X | ↑ | H | H† | X |
| X | L | ↑ | L | X | L |
| X | L | ↑ | H | X | H |

† Two CLK edges are needed to propagate data.

‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

| INPUTS | | | | | OUTPUT | |
|---------|---------|-----|-----|----|--------|------------------|
| CLKEN1B | CLKEN2B | CLK | SEL | 1B | 2B | A |
| H | X | X | H | X | X | A ₀ † |
| X | H | X | L | X | X | A ₀ † |
| L | X | ↑ | H | H | X | L |
| L | X | ↑ | L | L | X | H |
| X | L | ↑ | L | X | L | L |
| X | L | ↑ | L | X | H | H |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|--------------------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} (A port) | MAX | -24 | mA |
| I _{OH} (B port) | MAX | -12 | mA |
| I _{OL} (A port) | MAX | 24 | mA |
| I _{OL} (B port) | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|--|-------|---------------------------------|------------|-------------|
| t _{max} | | | MIN | 150 |
| t _w Pulse duration, CLK high or low | | | MIN | 3.3 |
| t _{su} Setup time | | A data before CLK ↑ | MIN | 3.4 |
| | | B data before CLK ↑ | MIN | 1 |
| | | SEL before CLK ↑ | MIN | 1.3 |
| | | CLKENA1 or CLKENA2 before CLK ↑ | MIN | 2.8 |
| | | CLKENB1 or CLKENB2 before CLK ↑ | MIN | 2.5 |
| t _h Hold time | | OE before CLK ↑ | MIN | 3.2 |
| | | A data after CLK ↑ | MIN | 0.2 |
| | | B data after CLK ↑ | MIN | 1.3 |
| | | SEL after CLK ↑ | MIN | 1 |
| | | CLKENA1 or CLKENA2 after CLK ↑ | MIN | 0.4 |
| | | CLKENB1 or CLKENB2 after CLK ↑ | MIN | 0.5 |
| | | OE after CLK ↑ | MIN | 0.2 |
| t _{pd} | CLK | B | MAX | 5.4 |
| | | A (1B) | | 4.8 |
| | | A (2B) | | 4.8 |
| | | A (SEL) | | 5.8 |
| t _{en} | CLK | B | MAX | 6.1 |
| | | A | | 5.1 |
| t _{fis} | CLK | B | MAX | 5.9 |
| | | A | | 5 |

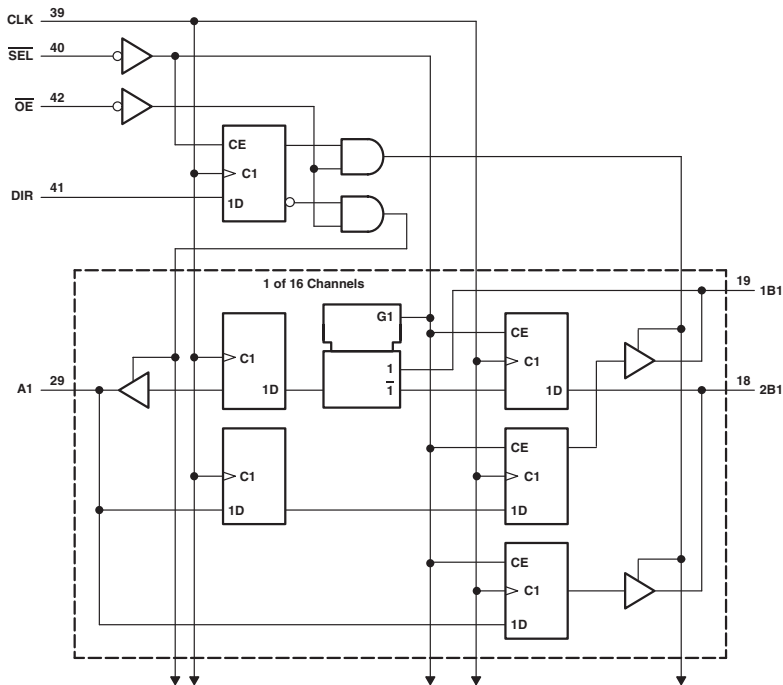
 UNIT f_{max} : MHz other : ns

162280

16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

- SN74ALVCHG162280: A-Port Outputs Have Equivalent 50-Ω Series Resistors
- B-Port Outputs Have Equivalent 20-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

| INPUTS | | | OUTPUTS | |
|--------|-----|---|---------------|---------------|
| SEL | CLK | A | 1B | 2B |
| H | X | X | 1B \uparrow | 2B \uparrow |
| L | X | L | L \uparrow | X |
| L | X | H | H \uparrow | X |

† Output level before indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

| INPUTS | | | OUTPUT | |
|--------|-----|----|--------|--------|
| CLK | SEL | 1B | 2B | A |
| ↑ | H | X | L | L \S |
| ↑ | H | X | H | H \S |
| ↑ | L | L | X | L |
| ↑ | L | H | X | H |

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

C-TO-D STORAGE ($\overline{OE} = L$)

| INPUTS | | | OUTPUT | |
|--------|-----|---|---------------|---------------|
| SEL | CLK | C | 1D | 2D |
| H | X | X | 1B \uparrow | 2B \uparrow |
| L | ↑ | L | L \uparrow | L |
| L | ↑ | H | H \uparrow | H |

† Output level before indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

OUTPUT ENABLE

| INPUTS | | | OUTPUT | | |
|--------|-----------------|-----|--------|--------|--------|
| CLK | \overline{OE} | DIR | A | 1B, 2B | 1D, 2D |
| ↑ | H | X | Z | Z | Z |
| ↑ | L | H | Z | Active | Active |
| ↑ | L | L | Active | Z | Active |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCHG 3V | UNIT |
|--------------------------|------------|-----------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} (A to B) | MAX | 8 | mA |
| I _{OH} (B to A) | MAX | 6 | mA |
| I _{OL} (A to B) | MAX | 8 | mA |
| I _{OL} (B to A) | MAX | 6 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCHG 3V |
|------------------|---------------------------------|----------------------------------|------------|-----------|
| t _{max} | | | MIN | 160 |
| t _w | Pulse duration, CLK high or low | | MIN | 2.3 |
| t _{su} | Setup time | A data before CLK ↑, high or low | MIN | 1.4 |
| | | B data before CLK ↑, high or low | MIN | 2 |
| | | C data before CLK ↑, high or low | MIN | 1.3 |
| | | DIR before CLK ↑, high or low | MIN | 2 |
| | | SEL before CLK ↑, high or low | MIN | 2 |
| t _h | Hold time | A data after CLK ↑, high or low | MIN | 0.3 |
| | | B data after CLK ↑, high or low | MIN | 0.3 |
| | | C data after CLK ↑, high or low | MIN | 0.3 |
| | | DIR after CLK ↑, high or low | MIN | 0.3 |
| | | SEL after CLK ↑, high or low | MIN | 0.3 |
| t _{pd} | CLK | A | MAX | 5 |
| | | B | | 7.4 |
| | | D | | 7.2 |
| t _{en} | CLK | A | MAX | 6.2 |
| | | B | | 9.4 |
| | | A | | 6 |
| | | B | | 9.5 |
| | | D | | 7.9 |
| t _{dis} | CLK | A | MAX | 6.4 |
| | | B | | 7.8 |
| | | A | | 5 |
| | | B | | 7.6 |
| | | D | | 6.7 |

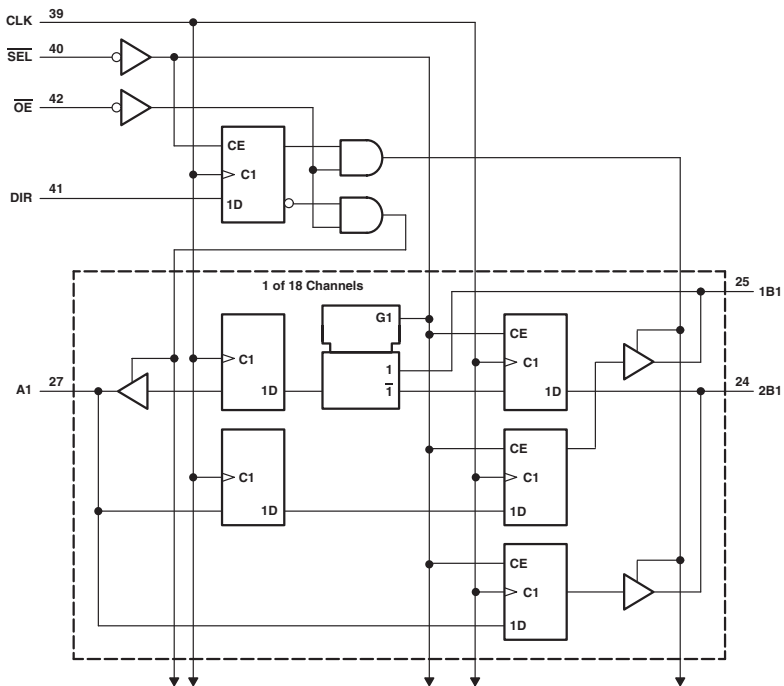
UNIT f_{max}: MHz other: ns

162282

18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCHG162282: A-Port Outputs Have Equivalent 50-Ω Series Resistors
- B-Port Outputs Have Equivalent 20-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
A-TO-B STORAGE
($\overline{OE} = L$, DIR = H)

| INPUTS | | | OUTPUTS | |
|--------|-----|---|-------------------|-------------------|
| SEL | CLK | A | 1B | 2B |
| H | X | X | 1B ₀ † | 2B ₀ † |
| L | ↑ | L | L‡ | L |
| L | ↑ | H | H‡ | H |

† Output level before indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE
($\overline{OE} = L$, DIR = L)

| INPUTS | | | | OUTPUT |
|--------|-----|----|----|--------|
| CLK | SEL | 1B | 2B | A |
| ↑ | H | X | L | L‡ |
| ↑ | H | X | H | H‡ |
| ↑ | L | L | X | L |
| ↑ | L | H | X | H |

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

| INPUTS | | | OUTPUTS | |
|--------|-----------------|-----|---------|--------|
| CLK | \overline{OE} | DIR | A | 1B, 2B |
| ↑ | H | X | Z | Z |
| ↑ | L | H | Z | Active |
| ↑ | L | L | Active | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCHG 3V | UNIT |
|--------------------------|------------|--------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} (A to B) | MAX | 8 | mA |
| I _{OH} (B to A) | MAX | 6 | mA |
| I _{OL} (A to B) | MAX | 8 | mA |
| I _{OL} (B to A) | MAX | 6 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCHG 3V |
|--|---------------------|--------|------------|--------------|
| f _{max} | | | MIN | 160 |
| t _w Pulse duration, CLK high or low | | | MIN | 2.3 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 1.5 |
| | B data before CLK ↑ | | MIN | 2 |
| | DIR before CLK ↑ | | MIN | 2 |
| | SEL before CLK ↑ | | MIN | 2 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.3 |
| | B data after CLK ↑ | | MIN | 0.3 |
| | DIR after CLK ↑ | | MIN | 0.3 |
| | SEL after CLK ↑ | | MIN | 0.3 |
| t _{pd} | CLK | A | MAX | 5 |
| | | B | | 7.4 |
| t _{en} | CLK | A | MAX | 6.3 |
| | | B | | 9.4 |
| | \overline{OE} | A | MAX | 6 |
| | | B | | 9.5 |
| t _{dis} | CLK | A | MAX | 6.4 |
| | | B | | 7.8 |
| | \overline{OE} | A | MAX | 5 |
| | | B | | 7.6 |

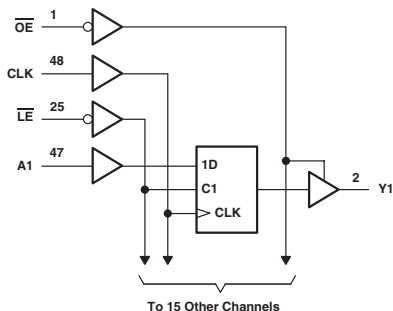
UNIT f_{max} : MHz other : ns

162334

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162334: Output Ports Have Equivalent 26- Ω Series Resistors
- SN74ALVCH162334: Output Port Has Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| OE | INPUTS | | | OUTPUT |
|----|--------|--------|---|------------------|
| | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | Y ₀ ↑ |

↑ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCH 3V |
|-------------------------------|---------------------------|--------|------------|------------|-------------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LE low | | | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.5 | 1.5 |
| | Data before LE ↑ CLK high | | MIN | 1.3 | 1.3 |
| | Data before LE ↑ CLK low | | MIN | 1.2 | 1.2 |
| t _h Hold time | Data after CLK ↑ | | MIN | 0.9 | 0.9 |
| | Data after LE ↑ CLK high | | MIN | 1.1 | 1.1 |
| | Data after LE ↑ CLK low | | MIN | 1.1 | 1.1 |
| t _{pd} | A | Y | MAX | 3.9 | 3.9 |
| | LE | | 5 | 5 | |
| | CLK | | MAX | 4.9 | 4.9 |
| t _{en} | OE | Y | | 5.4 | 5.4 |
| t _{dis} | OE | Y | MAX | 5 | 5 |

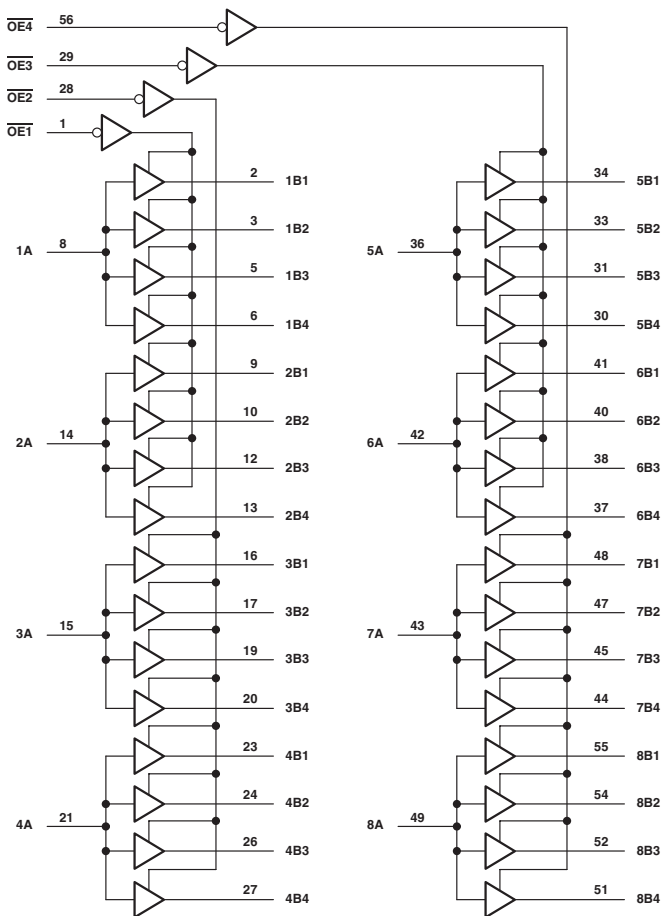
UNIT f_{max} : MHz other : ns

162344

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162344: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Bn |
| L | H | H |
| L | L | L |
| H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

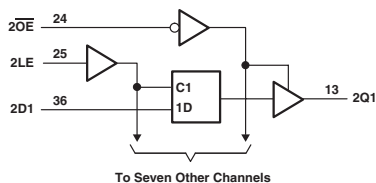
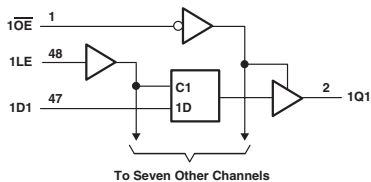
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|------------------|-----------------|--------|------------|-------------|
| T _{PLH} | A | B | MAX | 4.4 |
| T _{PHL} | | | | 4.4 |
| T _{PZH} | \overline{OE} | B | MAX | 5.7 |
| T _{PZL} | | | | 5.7 |
| T _{PHZ} | \overline{OE} | B | MAX | 4.5 |
| T _{PLZ} | | | | 4.5 |

UNIT: ns

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- SN74LVTH162373: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

| INPUTS | | | OUTPUT Q |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 5 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

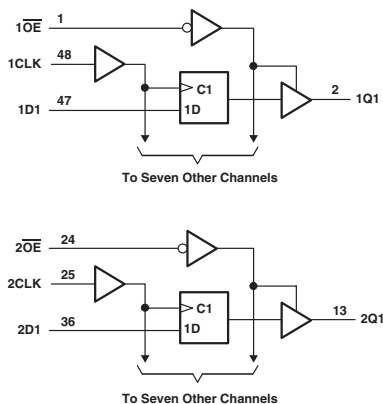
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | ALVC 3V |
|---|-----------------------------|--------|------------|------------|------------|
| t _w Pulse duration, LE high or low | | | MIN | 3 | 3.3 |
| t _{su} Setup time | Data before LE ↓, data high | | MIN | 1 | 1.1 |
| | Data before LE ↓, data low | | MIN | 1 | 1.1 |
| t _h Hold time | Data after LE ↓, data high | | MIN | 1 | 1.1 |
| | Data after LE ↓, data low | | MIN | 1 | 1.1 |
| t _{PLH} | D | Q | MAX | 4.6 | 4 |
| t _{PHL} | | | | 4 | 4 |
| t _{PLH} | LE | Q | MAX | 5.1 | 4.2 |
| t _{PHL} | | | | 4.6 | 4.2 |
| t _{PZH} | OE | Q | MAX | 5.4 | 5 |
| t _{PZL} | | | | 4.9 | 5 |
| t _{PHZ} | OE | Q | MAX | 5.4 | 4.5 |
| t _{PLZ} | | | | 5.1 | 4.5 |

UNIT: ns

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74LVTH162374: Output Ports Have Equivalent 22- Ω Series Resistors
- SN74ALVCH162374: Output Ports Have Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT Q |
|--------|-----|---|----------------|
| OE | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 5 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

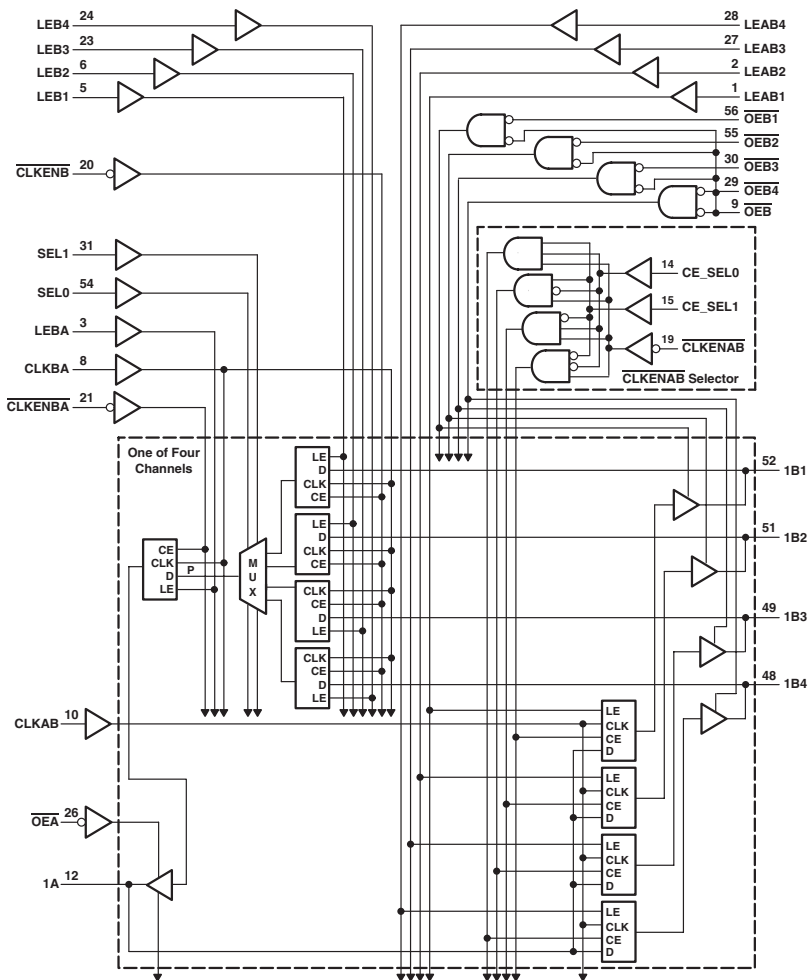
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V | ALVCH 3V |
|--|-------|------------------------------|------------|------------|-------------|
| f _{max} | | | | 160 | 150 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 | 3.3 |
| t _{su} Setup time | | Data before CLK ↑, data high | MIN | 1.8 | 1.9 |
| | | Data before CLK ↑, data low | MIN | 1.8 | 1.9 |
| t _h Hold time | | Data after CLK ↑, data high | MIN | 0.8 | 0.5 |
| | | Data after CLK ↑, data low | MIN | 0.8 | 0.5 |
| t _{PLH} | CLK | Q | MAX | 5.3 | 4.6 |
| t _{PHL} | | | | 4.9 | 4.6 |
| t _{PZH} | OE | Q | MAX | 5.6 | 5.2 |
| t _{PZL} | | | | 4.9 | 5.2 |
| t _{PHZ} | OE | Q | MAX | 5.4 | 4.5 |
| t _{PLZ} | | | | 5 | 4.5 |

UNIT f_{max} : MHz other : ns

4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS

- SN74ABTH162460: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
A-TO-B OUTPUT ENABLE

| INPUTS | | OUTPUT |
|--------|------|--------|
| OEB | OEBn | Bn |
| H | H | Z |
| H | L | Z |
| L | H | Z |
| L | L | Active |

Tn = 1, 2, 3, 4

A-TO-B STORAGE

(assuming OEB = L, OEBn = L)

| INPUTS | | | | | | | | OUTPUTS | | | |
|---------|---------|---------|--------|--------|-------|-------|-------|---------|----|----|----|
| CLKENAB | CE_SEL1 | CE_SEL0 | CLKAB | LEAB1 | LEAB2 | LEAB3 | LEAB4 | B1 | B2 | B3 | B4 |
| X | X | X | X | H or L | H | L | L | A | A0 | A0 | A0 |
| X | X | X | H or L | H | L | L | L | A | A | A | A0 |
| L | X | X | L | L | L | L | L | A0 | A0 | A0 | A0 |
| L | L | L | ↑ | L | L | L | L | A | A0 | A0 | A0 |
| L | L | H | ↑ | L | L | L | L | A0 | A | A0 | A0 |
| L | H | ↑ | L | L | L | L | L | A0 | A0 | A | A0 |
| L | H | H | ↑ | L | L | L | L | A0 | A0 | A0 | A |
| H | X | X | ↑ | L | L | L | L | A0 | A0 | A0 | A0 |

B-TO-A STORAGE

(after point P)

| INPUTS | | | | | | | P | |
|--------|-------|------|------|------|------|------|------|------|
| CLKENB | CLKBA | LEB1 | LEB2 | LEB3 | LEB4 | SEL1 | SEL0 | |
| X | X | H | L | L | L | L | L | B1 |
| X | X | L | H | L | L | L | H | B2 |
| X | X | L | L | H | L | H | L | B3 |
| X | X | L | L | L | H | H | H | B4 |
| L | ↑ | L | L | L | L | L | L | B1 |
| | | | | | | H | L | B2 |
| | | | | | | H | L | B3 |
| | | | | | | H | H | B4 |
| L | L | L | L | L | L | L | L | B10↑ |
| | | | | | | H | H | B20↑ |
| | | | | | | H | L | B30↑ |
| | | | | | | H | H | B40↑ |

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE

(after point P)

| INPUTS | | | | | | OUTPUT |
|---------|-------|------|-----|---|--|--------|
| CLKENBA | CLKBA | LEBA | OEA | B | | A |
| X | X | X | H | X | | X |
| X | X | H | L | L | | L |
| X | X | H | L | H | | H |
| H | X | L | L | X | | A0↑ |
| L | ↑ | L | L | L | | L |
| L | ↑ | L | L | H | | H |
| L | L | L | L | X | | A0↑ |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABTH | UNIT |
|--------------|------------|------|------|
| Icc | MAX | 32 | mA |
| Ioh (A port) | MAX | -32 | mA |
| Ioh (B port) | MAX | -12 | mA |
| Iol (A port) | MAX | 64 | mA |
| Iol (B port) | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | | MAX or MIN | ABTH |
|-------------------|----------------------------|--------------------|------------|
| tmax | | MIN | 160 |
| tw Pulse duration | CLKAB high or low | MIN | 3.8 |
| | CLKBA high or low | MIN | 4.5 |
| | LEAB1, 2, 3 or 4 high | MIN | 2.8 |
| | LEBA high | MIN | 2.8 |
| | LEB1, 2, 3 or 4 high | MIN | 3 |
| tsu Setup time | Before CLKAB ↑ | A bus CE_SEL0/1 | MIN 3.2 |
| | | CLKENAB | MIN 3.2 |
| | Before LEAB1, 2, 3, or 4 ↓ | A bus | MIN 3.6 |
| | | B bus | MIN 3.8 |
| | Before CLKBA ↑ | CLKENB | MIN 2.3 |
| | | CLKENBA | MIN 2.5 |
| | | LEB1, 2, 3 or 4 | MIN 4.3 |
| | | SEL0/1 | MIN 4.5 |
| | Before LEB1, 2, 3, or 4 ↓ | B bus | MIN 3.2 |
| | | B bus | MIN 4 |
| Before CLKBA ↑ | LEB1, 2, 3 or 4 | MIN 4.4 | |
| | SEL0/1 | MIN 4.3 | |
| th Hold time | after CLKAB ↑ | A bus CE_SEL0/1 | MIN 1.1 |
| | | CLKENAB | MIN 0.5 |
| | after LEAB1, 2, 3, or 4 ↓ | A bus | MIN 1.2 |
| | | B bus | MIN 1.3 |
| | after CLKBA ↑ | CLKENB | MIN 1 |
| | | CLKENBA | MIN 1 |
| | | SEL0/1 | MIN 0 |
| | after LEB1, 2, 3, or 4 ↓ | B bus | MIN 1.5 |
| | | B bus | MIN 0.4 |
| | after CLKBA ↑ | SEL0/1 | MIN 0.1 |

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABTH |
|-----------|----------------------------|--------|------------|------|
| trLH | | | | 6.5 |
| trHL | B | A | MAX | 6.5 |
| trZH | | | | 5.6 |
| trZL | \overline{OEA} | A | MAX | 5.5 |
| trHZ | | | | 5.9 |
| trLZ | \overline{OEA} | A | MAX | 6.5 |
| trLH | | | | 6.2 |
| trHL | A | B | MAX | 6.5 |
| trZH | | | | 6.8 |
| trZL | \overline{OEB} | B | MAX | 6.3 |
| trHZ | | | | 6.2 |
| trLZ | \overline{OEB} | B | MAX | 5.8 |
| trZH | | | | 6.6 |
| trZL | $\overline{OEB1}, 2, 3, 4$ | B | MAX | 6.2 |
| trHZ | | | | 5.3 |
| trLZ | $\overline{OEB1}, 2, 3, 4$ | B | MAX | 4.9 |
| trLH | | | | 7.4 |
| trHL | CLKBA | A | MAX | 7.7 |
| trLH | | | | 6.5 |
| trHL | CLKAB | B | MAX | 6.5 |
| trLH | | | | 5.8 |
| trHL | LEBA | A | MAX | 5.8 |
| trLH | | | | 6.2 |
| trHL | LEAB1, 2, 3, 4 | B | MAX | 6.2 |
| trLH | | | | 7.2 |
| trHL | LEBA1, 2, 3, 4 | A | MAX | 6.8 |
| trLH | | | | 7.5 |
| trHL | SEL | A | MAX | 6.9 |

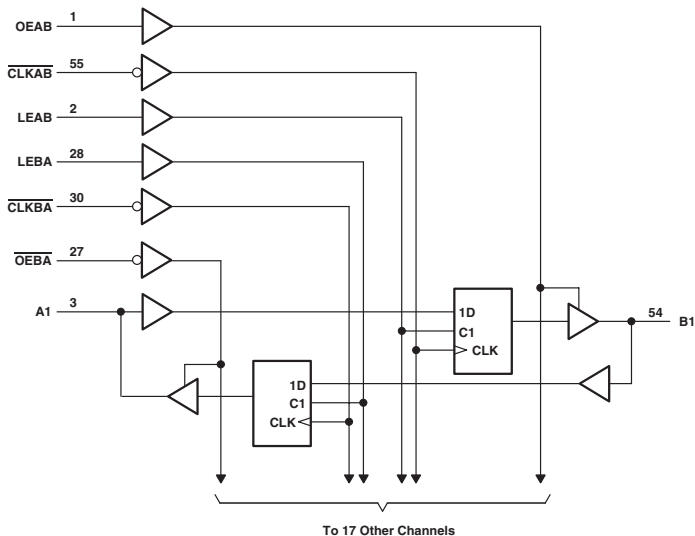
UNIT fmax : MHz other : ns

162500

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162500: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT B |
|--------|------|-------|---|-----------------------------|
| OEAB | LEAB | CLKAB | A | |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↓ | L | L |
| H | L | ↓ | H | H |
| H | L | H | X | B ₀ [‡] |
| H | L | L | X | B ₀ [§] |

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|--------------------------|------------|-----|------|
| I _{CC} | MAX | 36 | mA |
| I _{OH} (A port) | MAX | -32 | mA |
| I _{OH} (B port) | MAX | -12 | mA |
| I _{OL} (A port) | MAX | 64 | mA |
| I _{OL} (B port) | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|-------------------------------|------------------------------------|--------|------------|-----|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 2.5 |
| | CLKAB or CLKBA high or low | | MIN | 3 |
| t _{su} Setup time | A before CLKAB ↓ | | MIN | 3.3 |
| | B before CLKBA ↓ | | MIN | 3.3 |
| | A before LEAB ↓ or LEBA ↓ CLK high | | MIN | 1 |
| | A before LEAB ↓ or LEBA ↓ CLK low | | MIN | 2.5 |
| t _h Hold time | A after CLKAB ↓ or B after CLKBA ↓ | | MIN | 0 |
| | A after LEAB ↓ or B after LEBA ↓ | | MIN | 2 |
| t _{PLH} | A or B | B or A | MAX | 4.8 |
| t _{PHL} | | | | 5.7 |
| t _{PZH} | LEAB or LEBA | B or A | MAX | 5.6 |
| t _{PZL} | | | | 5.9 |
| t _{PHZ} | CLKAB or CLKBA | B or A | MAX | 5.9 |
| t _{PLZ} | | | | 6 |
| t _{PZH} | OEAB | B | MAX | 5.3 |
| t _{PZL} | | | | 5.4 |
| t _{PHZ} | OEAB | B | MAX | 6.5 |
| t _{PLZ} | | | | 5.8 |
| t _{PZH} | OEBA | A | MAX | 5.3 |
| t _{PZL} | | | | 5.4 |
| t _{PHZ} | OEBA | A | MAX | 6.5 |
| t _{PLZ} | | | | 5.8 |

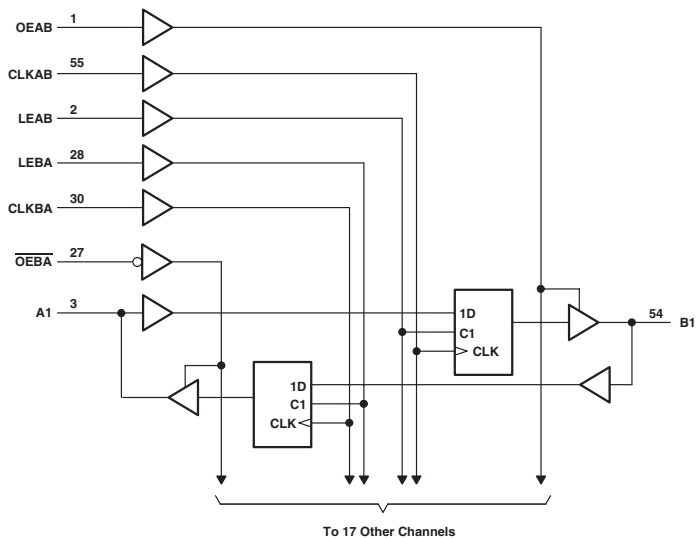
UNIT f_{max} : MHz other : ns

162501

18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- SN74ABT162501: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE[†]

| INPUTS | | | | OUTPUT |
|--------|------|-------|---|-----------------------------|
| OEAB | LEAB | CLKAB | A | Y |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | H | X | B ₀ [‡] |
| H | L | L | X | B ₀ [§] |

[†] A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|--------------------------|------------|-----|------|
| I _{CC} | MAX | 36 | mA |
| I _{OH} (A port) | MAX | -32 | mA |
| I _{OL} (B port) | MAX | -12 | mA |
| I _{OL} (A port) | MAX | 64 | mA |
| I _{OL} (B port) | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|-------------------------------|------------------------------------|--------|------------|-----|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 3 |
| | CLKAB or CLKBA high or low | | MIN | 3.3 |
| t _{su} Setup time | A before CLKAB ↑ | | MIN | 4.3 |
| | B before CLKBA ↑ | | MIN | 4.3 |
| | A before LEAB ↓ or LEBA ↓ CLK high | | MIN | 2.5 |
| | A before LEAB ↓ or LEBA ↓ CLK low | | MIN | 1 |
| t _h Hold time | A after CLKAB ↑ or B after CLKBA ↑ | | MIN | 0 |
| | A after LEAB ↓ or B after LEBA ↓ | | MIN | 2 |
| t _{PLH} | A or B | B or A | MAX | 4.8 |
| t _{PHL} | | | | 5.7 |
| t _{PZH} | LEAB or LEBA | B or A | MAX | 5.6 |
| t _{PZL} | | | | 5.9 |
| t _{PHZ} | CLKAB or CLKBA | B or A | MAX | 5.5 |
| t _{PLZ} | | | | 5.3 |
| t _{PZH} | OEAB | B | MAX | 5.3 |
| t _{PZL} | | | | 5.4 |
| t _{PHZ} | OEAB | B | MAX | 6.5 |
| t _{PLZ} | | | | 5.8 |
| t _{PZH} | OEBA | A | MAX | 5.3 |
| t _{PZL} | | | | 5.4 |
| t _{PHZ} | OEBA | A | MAX | 6.5 |
| t _{PLZ} | | | | 5.8 |

UNIT f_{max} : MHz other : ns

FUNCTION TABLE

A-TO-B STORAGE (OEAB = L)

| INPUTS | | | OUTPUT |
|--------|-------|---|------------------|
| CLKNAB | OLKAB | A | B |
| H | X | X | B ₀ † |
| L | ↑ | L | L |
| L | ↑ | H | H |

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEBA = L)

| INPUTS | | | | | OUTPUT |
|---------|--------|--------|-----|---|------------------|
| CLKENBA | CLK2BA | CLK1BA | SEL | B | A |
| H | X | X | X | X | A ₀ † |
| L | ↑ | X | H | L | L |
| L | ↑ | X | H | H | H |
| L | ↑ | ↑ | L | L | L‡ |
| L | ↑ | ↑ | L | H | H‡ |

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|--------------------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} (A port) | MAX | -24 | mA |
| I _{OH} (B port) | MAX | -12 | mA |
| I _{OL} (A port) | MAX | 24 | mA |
| I _{OL} (B port) | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|--|-------------------------|--------|------------|-------------|
| t _{max} | | | MIN | 150 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 |
| t _{su} Setup time | A data before CLKAB ↑ | | MIN | 1.3 |
| | B data before CLK2BA ↑ | | MIN | 1.7 |
| | B data before CLK1BA ↑ | | MIN | 1.1 |
| | SEL before CLK2BA ↑ | | MIN | 3.3 |
| | CLKENAB before CLKAB ↑ | | MIN | 1.6 |
| | CLKENBA before CLK1BA ↑ | | MIN | 2.1 |
| t _h Hold time | CLKENBA before CLK2BA ↑ | | MIN | 2.2 |
| | A data after CLKAB ↑ | | MIN | 0.9 |
| | B data after CLK2BA ↑ | | MIN | 0.6 |
| | B data after CLK1BA ↑ | | MIN | 1 |
| | SEL after CLK2BA ↑ | | MIN | 0.1 |
| | CLKENAB after CLKAB ↑ | | MIN | 0.3 |
| t _{pd} | CLKENBA after CLK1BA ↑ | | MIN | 0.1 |
| | CLKENBA after CLK2BA ↑ | | MIN | 0 |
| t _{pd} | CLKAB | B | MAX | 4.7 |
| | CLK2BA | A | | 4.2 |
| t _{en} | OEBA | A | MAX | 5.1 |
| | OEAB | B | | 5.7 |
| t _{dis} | OEBA | A | MAX | 4.9 |
| | OEAB | B | | 4.9 |

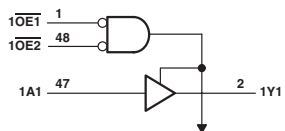
UNIT f_{max} : MHz other : ns

162541

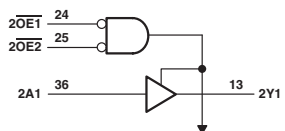
3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVTH162541: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



To Seven Other Channels



To Seven Other Channels

FUNCTION TABLE
(each 8-bit section)

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | UNIT |
|-----------------|------------|------------|------|
| I _{CC} | MAX | 5 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V |
|------------------|-----------------|--------|------------|------------|
| t _{PLH} | A | Y | MAX | 4.1 |
| | | | | 4.1 |
| t _{PZH} | \overline{OE} | Y | MAX | 5 |
| | | | | 4.8 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.9 |
| | | | | 5.4 |

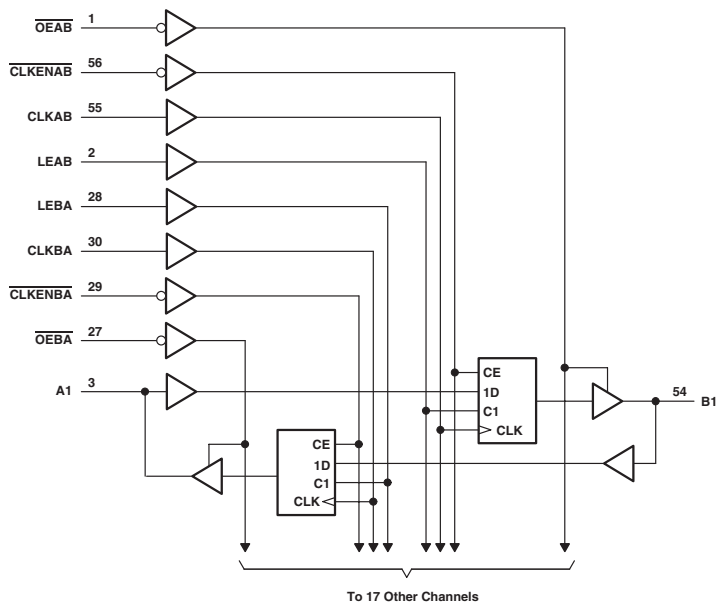
UNIT: ns

162601

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162601: B-Port Outputs Have Equivalent 25- Ω Series Resistors
- SN74ALVCH162601: B-Port Outputs Have Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | | OUTPUT B |
|---------|------|------|-------|---|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B ₀ † |
| H | L | L | X | X | B ₀ † |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | B ₀ † |
| L | L | L | H | X | B ₀ ‡ |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ALVCH 3V | UNIT |
|--------------------------|------------|-----|-------------|------|
| I _{cc} | MAX | 36 | 0.04 | mA |
| I _{OH} (A port) | MAX | -32 | -24 | mA |
| I _{OH} (B port) | MAX | -12 | -12 | mA |
| I _{OL} (A port) | MAX | 64 | 24 | mA |
| I _{OL} (B port) | MAX | 12 | 12 | mA |

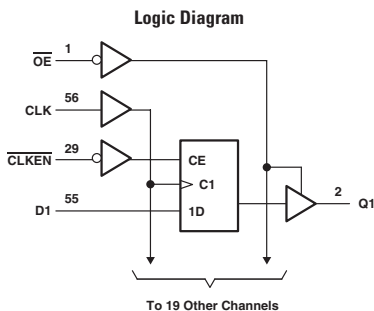
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVCH 3V |
|-------------------------------|--|--------|------------|-----|-------------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LEAB or LEBA high | | MIN | 2.5 | 3.3 |
| | CLKAB or CLKBA high or low | | MIN | 3 | 3.3 |
| | Data before CLK ↑ | | MIN | 4.3 | 2.1 |
| t _{su} Setup time | A before LEAB ↓ or B before LEBA ↓, CLK high | | MIN | 2.5 | 1.6 |
| | A before LEAB ↓ or B before LEBA ↓, CLK low | | MIN | 1 | 1.1 |
| | CLKEN before ↑ | | MIN | 2.7 | 1.7 |
| | Data after CLK ↑ | | MIN | 0 | 0.8 |
| t _h Hold time | A after LEAB ↓ or B after LEBA ↓, CLK high | | MIN | 0.5 | 1.4 |
| | A after LEAB ↓ or B after LEBA ↓, CLK low | | MIN | 0.5 | 1.7 |
| | CLKEN after ↑ | | MIN | 0 | 0.6 |
| †P _{LH} | A | B | MAX | 4.8 | 4.5 |
| †P _{HL} | | | | 5.7 | 4.5 |
| †P _{LH} | B | A | MAX | 4 | 4.1 |
| †P _{HL} | | | | 4.9 | 4.1 |
| †P _{LH} | LEBA | A | MAX | 5 | 4.7 |
| †P _{HL} | | | | 5 | 4.7 |
| †P _{LH} | LEAB | B | MAX | 5.6 | 5.1 |
| †P _{HL} | | | | 5.9 | 5.1 |
| †P _{LH} | CLKBA | A | MAX | 5.3 | 5 |
| †P _{HL} | | | | 5 | 5 |
| †P _{LH} | CLKAB | B | MAX | 5.5 | 5.5 |
| †P _{HL} | | | | 5.3 | 5.5 |
| †P _{ZH} | OEBA | A | MAX | 5.1 | 5.2 |
| †P _{ZL} | | | | 5.4 | 5.2 |
| †P _{ZH} | OEAB | B | MAX | 6.1 | 5.7 |
| †P _{ZL} | | | | 5.7 | 5.7 |
| †P _{HZ} | OEBA | A | MAX | 6.2 | 4.4 |
| †P _{LZ} | | | | 5.4 | 4.4 |
| †P _{HZ} | OEAB | B | MAX | 5.4 | 4.8 |
| †P _{LZ} | | | | 5.2 | 4.8 |

UNIT f_{max}: MHz other: ns

3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

- SN74ALVCH162721: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUT |
|--------|-------|--------|---|----------------|
| OE | CLKEN | CLK | D | Q |
| L | H | X | X | Q ₀ |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | L or H | X | Q ₀ |
| H | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

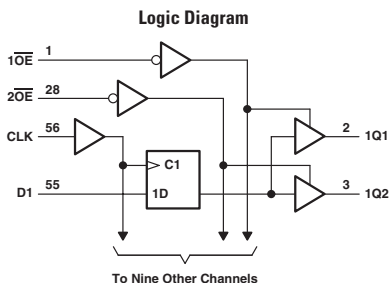
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|--------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 3.1 |
| | CLKEN before CLK ↑ | | MIN | 2.7 |
| t _h Hold time | Data after CLK ↑ | | MIN | 0 |
| | CLKEN after CLK ↑ | | MIN | 0 |
| t _{PLH} | CLK | Q | MAX | 5.3 |
| t _{PHL} | | | | 5.3 |
| t _{PZH} | OE | Q | MAX | 5.8 |
| t _{PZL} | | | | 5.8 |
| t _{PHZ} | OE | Q | MAX | 5 |
| t _{PLZ} | | | | 5 |

UNIT f_{max}: MHz other: ns

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

- SN74ALVCH162820: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE
(each flip flop)

| INPUTS | | | OUTPUT |
|------------------------------|-----|---|----------------|
| OE _n [†] | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

[†]n = 1,2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{cc} | MAX | 0.04 | mA |
| I _{oh} | MAX | -12 | mA |
| I _{ol} | MAX | 12 | mA |

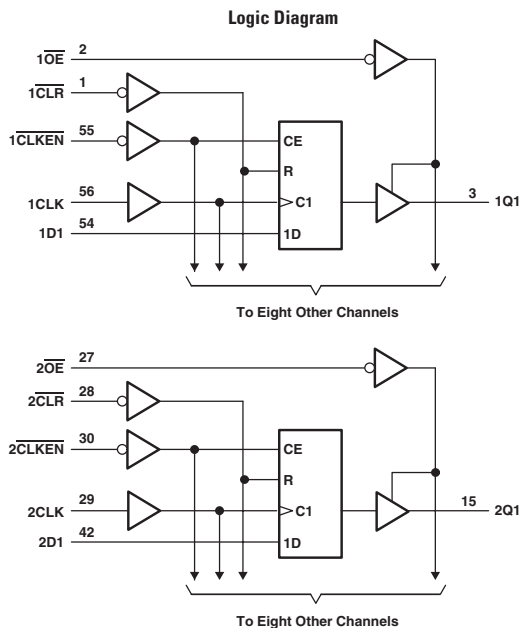
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|-------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.4 |
| t _h Hold time | Data after CLK ↑ | | MIN | 1 |
| TP _{LH} | CLK | Q | MAX | 5.4 |
| TP _{HL} | | | | 5.4 |
| TP _{ZH} | OE | Q | MAX | 5.6 |
| TP _{ZL} | | | | 5.6 |
| TP _{HZ} | OE | Q | MAX | 5 |
| TP _{LZ} | | | | 5 |

UNIT f_{max} : MHz other : ns

18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74ABT162823A: Output Ports Have Equivalent 25-Ω Series Resistors



FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|--------|-----|-------|-----|---|----------------|
| OE | CLR | CLENK | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | L | L | X | Q ₀ |
| L | H | H | X | X | Q ₀ |
| H | X | X | X | X | Z |

ELECTRICAL CHARACTERISTICS AND
RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 80 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|-------------------------------|------------------------|--------|------------|-----|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLR low | | MIN | 3.3 |
| | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | CLR inactive | | MIN | 1.6 |
| | Data before CLK ↑ | | MIN | 2 |
| | CLKEN low before CLK ↑ | | MIN | 2.8 |
| t _h Hold time | Data after CLK ↑ | | MIN | 1.2 |
| | CLKEN low after CLK ↑ | | MIN | 0.6 |
| t _{PLH} | CLK | Q | MAX | 7.5 |
| t _{PHL} | | | | 6.7 |
| t _{PHL} | CLR | Q | MAX | 7 |
| t _{PZH} | OE | Q | MAX | 5.9 |
| t _{PZL} | | | | 7 |
| t _{PHZ} | OE | Q | MAX | 6.6 |
| t _{PLZ} | | | | 9 |

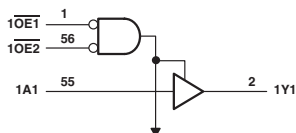
UNIT f_{max}: MHz other : ns

162825

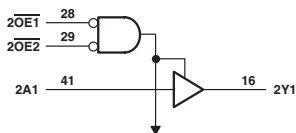
18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162825: Output Ports Have Equivalent 25-Ω Series Resistors

Logic Diagram



To Eight Other Channels



To Eight Other Channels

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|-----|---|--------|
| OE1 | OE2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | UNIT |
|-----------------|------------|-----|------|
| I _{CC} | MAX | 32 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

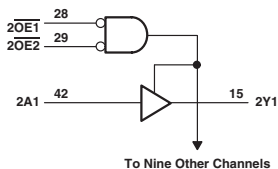
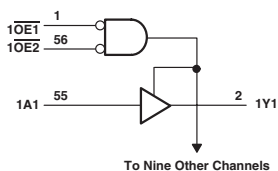
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT |
|------------------|-----------------|--------|------------|-----|
| t _{PLH} | A | Y | MAX | 3.9 |
| t _{PHL} | | | | 4.7 |
| t _{PZH} | \overline{OE} | Y | MAX | 6.9 |
| t _{PZL} | | | | 6.3 |
| t _{PHZ} | \overline{OE} | Y | MAX | 6.6 |
| t _{PLZ} | | | | 6.3 |

UNIT: ns

20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162827A: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVTH162827: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74ALVCH162827: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip flop)

| INPUTS | | | OUTPUT | |
|--------|-----|---|--------|--|
| OE1 | OE2 | A | Y | |
| L | L | L | L | |
| L | L | H | H | |
| H | X | X | Z | |
| X | H | X | Z | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ALVTH 3V | ALVCH 3V | UNIT |
|-----------------|------------|-----|-------------|-------------|------|
| I _{CC} | MAX | 32 | 5.5 | 0.04 | mA |
| I _{DH} | MAX | -12 | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | 12 | mA |

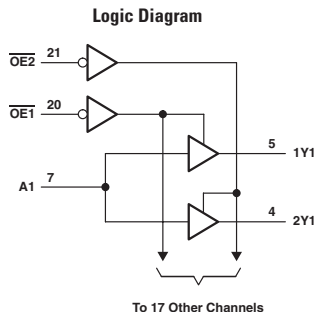
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVTH 3V | ALVCH 3V |
|------------------|-----------------|--------|------------|-----|-------------|-------------|
| t _{PLH} | A | Y | MAX | 3.9 | 3.9 | 3.8 |
| t _{PHL} | | | | 4.7 | 3.7 | 3.8 |
| t _{PZH} | \overline{OE} | Y | MAX | 6.9 | 5.6 | 5.1 |
| t _{PZL} | | | | 6.3 | 4.1 | 5.1 |
| t _{PHZ} | \overline{OE} | Y | MAX | 6.6 | 6.3 | 4.7 |
| t _{PLZ} | | | | 6.3 | 5.1 | 4.7 |

UNIT: ns

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162830, SN74ALVCHS162830: Output Ports Have Equivalent 26- Ω Series Resistors



FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------|-----|---|---------|-----|
| OE1 | OE2 | A | 1Yn | 2Yn |
| L | H | H | H | Z |
| L | H | L | L | Z |
| H | L | H | Z | H |
| H | L | L | Z | L |
| L | L | H | H | H |
| L | L | L | L | L |
| H | H | X | Z | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | ALVCHS 3V | UNIT |
|-----------------|------------|-------------|--------------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

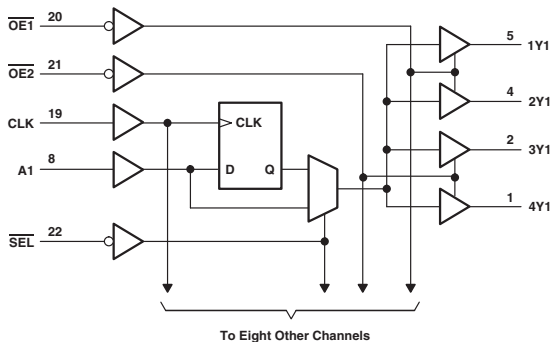
SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V | ALVCHS 3V |
|------------------|-----------------|--------|------------|-------------|--------------|
| t _{PLH} | A | Y | MAX | 3.5 | 3.5 |
| t _{PHL} | | | | 3.5 | 3.5 |
| t _{PZH} | \overline{OE} | Y | MAX | 4.8 | 4.8 |
| t _{PZL} | | | | 4.8 | 4.8 |
| t _{PHZ} | \overline{OE} | Y | MAX | 5.2 | 5.2 |
| t _{PLZ} | | | | 5.2 | 5.2 |

UNIT: ns

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162831, SN74ALVCH162831: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE

| INPUTS | | | | OUTPUT | |
|--------|-----|-----|---|--------|---|
| OE | SEL | CLK | A | Y | Z |
| H | X | X | X | L | L |
| L | H | X | L | H | L |
| L | H | X | H | L | H |
| L | L | ↑ | L | L | L |
| L | L | ↑ | H | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCH 3V | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

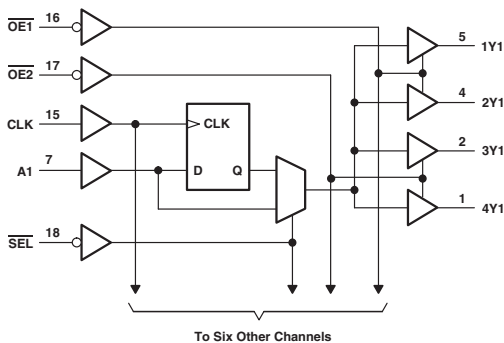
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCH 3V |
|-------------------------------|---------------------|--------|------------|---------|----------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 1.6 | 1.6 |
| t _h Hold time | A data after CLK ↑ | | MIN | 1.1 | 1.1 |
| t _{PLH} | A | Y | MAX | 4.3 | 4.3 |
| t _{PHL} | A | Y | MAX | 4.3 | 4.3 |
| t _{PLH} | CLK | Y | MAX | 4.7 | 4.7 |
| t _{PHL} | CLK | Y | MAX | 4.7 | 4.7 |
| t _{PLH} | SEL | Y | MAX | 4.8 | 4.8 |
| t _{PHL} | SEL | Y | MAX | 4.8 | 4.8 |
| t _{PZH} | OE | Y | MAX | 5.1 | 5.1 |
| t _{PZL} | OE | Y | MAX | 5.1 | 5.1 |
| t _{PHZ} | OE | Y | MAX | 5.1 | 5.1 |
| t _{PLZ} | OE | Y | MAX | 5.1 | 5.1 |

UNIT f_{max}: MHz other: ns

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162832: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|-----|-----|---|--------|
| OE | SEL | CLK | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVCH 3V | UNIT |
|-----------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

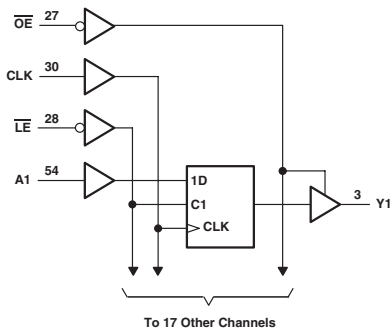
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVCH 3V |
|-------------------------------|---------------------|--------|------------|-------------|
| f _{max} | | | MIN | 150 |
| t _w Pulse duration | CLK high or low | | MIN | 3.3 |
| t _{su} Setup time | A data before CLK ↑ | | MIN | 1.6 |
| t _h Hold time | A data after CLK ↑ | | MIN | 1.1 |
| t _{PLH} | A | Y | MAX | 4.3 |
| t _{PHL} | | | 4.3 | |
| t _{PLH} | CLK | Y | MAX | 4.7 |
| t _{PHL} | | | 4.7 | |
| t _{PLH} | SEL | Y | MAX | 4.8 |
| t _{PHL} | | | 4.8 | |
| t _{PZH} | OE | Y | MAX | 5.1 |
| t _{PZL} | | | 5.1 | |
| t _{PHZ} | OE | Y | MAX | 5.1 |
| t _{PLZ} | | | 5.1 | |

UNIT f_{max}: MHz other: ns

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162834: Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|-----|---|-----------------|
| OE | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | H | X | Y _{0†} |
| L | H | L | X | Y _{0‡} |

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high.

‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCF 3V | UNIT |
|-----------------|------------|---------|----------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -18 | mA |
| I _{OL} | MAX | 12 | 18 | mA |

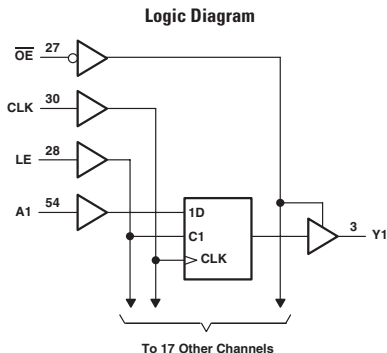
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCF 3V |
|-------------------------------|----------------------------|--------|------------|---------|----------|
| f _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LE low | | MIN | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | Data before LE ↑, CLK high | | MIN | 1.7 | 1.0 |
| | Data before LE ↑, CLK low | | MIN | 1.9 | 1.5 |
| | Data before LE ↓, CLK high | | MIN | 1.5 | 1.0 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.7 | 0.6 |
| | Data after LE ↑, CLK high | | MIN | 0.9 | 1.4 |
| | Data after LE ↓, CLK low | | MIN | 0.9 | 1.4 |
| t _{PLH} | A | Y | MAX | 4.2 | 3.5 |
| | | | | 4.2 | 3.5 |
| t _{PHL} | LE | Y | MAX | 5.8 | 4.6 |
| | | | | 5.8 | 4.6 |
| t _{PLH} | CLK | Y | MAX | 5.4 | 3.5 |
| | | | | 5.4 | 3.5 |
| t _{PHL} | OE | Y | MAX | 5.9 | 5.0 |
| | | | | 5.9 | 5.0 |
| t _{PHZ} | OE | Y | MAX | 5 | 4.2 |
| | | | | 5 | 4.2 |

UNIT f_{max}: MHz other: ns

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162835, SN74ALVCH162835: Output Port Has Equivalent 26-Ω Series Resistors



FUNCTION TABLE

| INPUTS | | | | OUTPUT Y |
|--------|----|--------|---|------------------|
| OE | LE | CLK | A | |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | L | L or H | X | Y ₀ † |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCF 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|-------------|------|
| I _{CC} | MAX | 0.04 | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -18 | -12 | mA |
| I _{OL} | MAX | 12 | 18 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCF 3V | ALVCH 3V |
|-------------------------------|----------------------------|--------|------------|------------|-------------|-------------|
| f _{max} | | | MIN | 150 | 150 | 150 |
| t _w Pulse duration | LE low | | MIN | 3.3 | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.7 | 1.0 | 1.7 |
| | Data before LE ↓, CLK high | | MIN | 1.5 | 1.5 | 1.5 |
| | Data before LE ↓, CLK low | | MIN | 1 | 1.0 | 1 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.7 | 0.6 | 0.7 |
| | Data after LE ↓, CLK high | | MIN | 1.4 | 1.4 | 1.4 |
| | Data after LE ↓, CLK low | | MIN | 1.4 | 1.4 | 1.4 |
| †P _{LH} | A | Y | MAX | 4.2 | 3.5 | 4.2 |
| †P _{HL} | | | | 4.2 | 3.5 | 4.2 |
| †P _{LH} | LE | Y | MAX | 5.1 | 4.6 | 5.1 |
| †P _{HL} | | | | 5.1 | 4.6 | 5.1 |
| †P _{LH} | CLK | Y | MAX | 5.4 | 3.5 | 5.4 |
| †P _{HL} | | | | 5.4 | 3.5 | 5.4 |
| †P _{ZH} | OE | Y | MAX | 5.5 | 5.0 | 5.5 |
| †P _{ZL} | | | | 5.5 | 5.0 | 5.5 |
| †P _{HZ} | OE | Y | MAX | 4.5 | 4.2 | 4.5 |
| †P _{LZ} | | | | 4.5 | 4.2 | 4.5 |

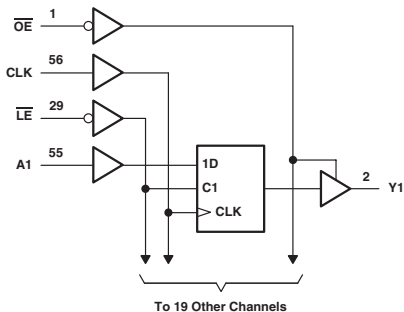
UNIT f_{max}: MHz other: ns

162836

20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162836, SN74ALVCH162836: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|--------|---|------------------|
| OE | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | Y ₀ † |

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ALVC 3V | ALVCH 3V | UNIT |
|-----------------|------------|------------|-------------|------|
| I _{CC} | MAX | 0.04 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

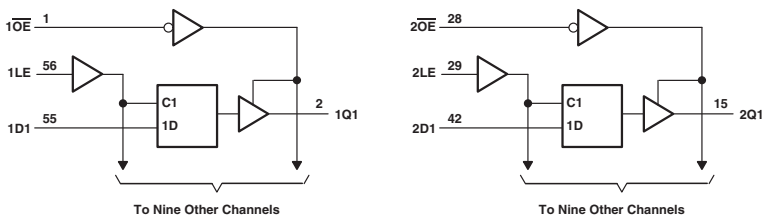
| PARAMETER | INPUT | OUTPUT | MAX or MIN | ALVC 3V | ALVCH 3V |
|-------------------------------|----------------------------|--------|------------|------------|-------------|
| t _{max} | | | MIN | 150 | 150 |
| t _w Pulse duration | LE low | | MIN | 3.3 | 3.3 |
| | CLK high or low | | MIN | 3.3 | 3.3 |
| t _{su} Setup time | Data before CLK ↑ | | MIN | 1.5 | 1.5 |
| | Data before LE ↓, CLK high | | MIN | 1.3 | 1.3 |
| | Data before LE ↓, CLK low | | MIN | 1.2 | 1.2 |
| t _h Hold time | A data after CLK ↑ | | MIN | 0.9 | 0.9 |
| | Data after LE ↓, CLK high | | MIN | 1.1 | 1.1 |
| | Data after LE ↓, CLK low | | MIN | 1.1 | 1.1 |
| t _{PLH} | A | Y | MAX | 4 | 4 |
| | | | | 4 | 4 |
| t _{PHL} | LE | Y | MAX | 5.1 | 5.1 |
| | | | | 5.1 | 5.1 |
| t _{PLH} | CLK | Y | MAX | 5 | 5 |
| | | | | 5 | 5 |
| t _{PHL} | OE | Y | MAX | 5.5 | 5.5 |
| | | | | 5.5 | 5.5 |
| t _{PHZ} | OE | Y | MAX | 5.1 | 5.1 |
| | | | | 5.1 | 5.1 |

UNIT f_{max}: MHz other: ns

20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162841: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162841: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 10-bit latch)

| INPUTS | | | OUTPUT |
|--------|----|---|----------------|
| OE | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | ABT | ALVCH 3V | UNIT |
|-----------------|------------|-----|-------------|------|
| I _{CC} | MAX | 89 | 0.04 | mA |
| I _{OH} | MAX | -12 | -12 | mA |
| I _{OL} | MAX | 12 | 12 | mA |

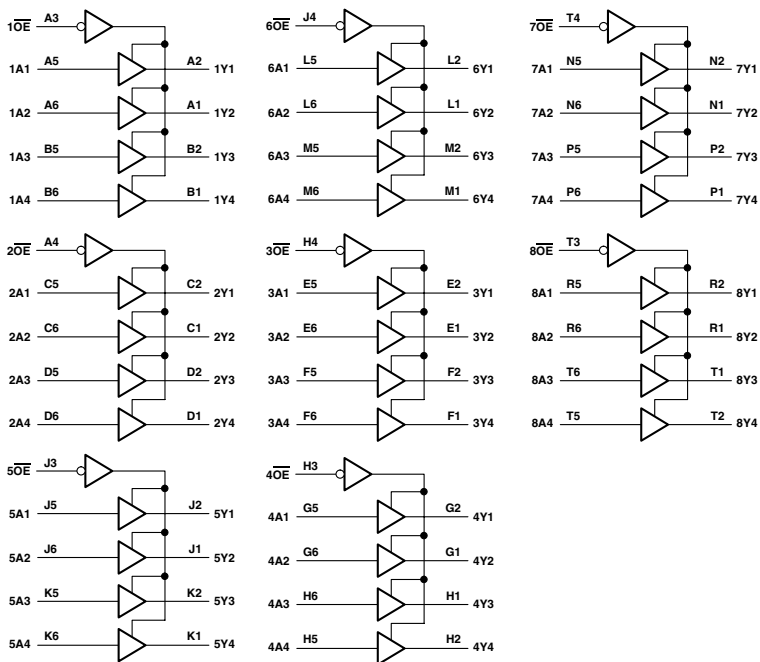
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | ABT | ALVCH 3V |
|------------------|----------------|------------------|------------|-----|-------------|
| t _{sw} | Pulse duration | LE high or low | MIN | 4 | 3.3 |
| t _{su} | Setup time | Data before LE ↓ | MIN | 0.8 | - |
| | | Data before LE ↑ | | - | 1.1 |
| t _h | Hold time | Data after LE ↓ | MIN | 1.8 | - |
| | | Data after LE ↑ | | - | 1.1 |
| t _{PLH} | D | Q | MAX | 5.2 | 4.3 |
| t _{PHL} | | | | 6 | 4.3 |
| t _{PLH} | LE | Q | MAX | 5.4 | 4.7 |
| t _{PHL} | | | | 5.8 | 4.7 |
| t _{PZH} | OE | Q | MAX | 5.7 | 5.3 |
| t _{PZL} | | | | 6.5 | 5.3 |
| t _{PHZ} | OE | Q | MAX | 6.5 | 4.4 |
| t _{PLZ} | | | | 7.1 | 4.4 |

UNIT : ns

32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVCH 3V | UNIT |
|-----------|------------|------------|------|
| I_{CC} | MAX | 0.04 | mA |
| I_{OH} | MAX | -12 | mA |
| I_{OL} | MAX | 12 | mA |

SWITCHING CHARACTERISTICS

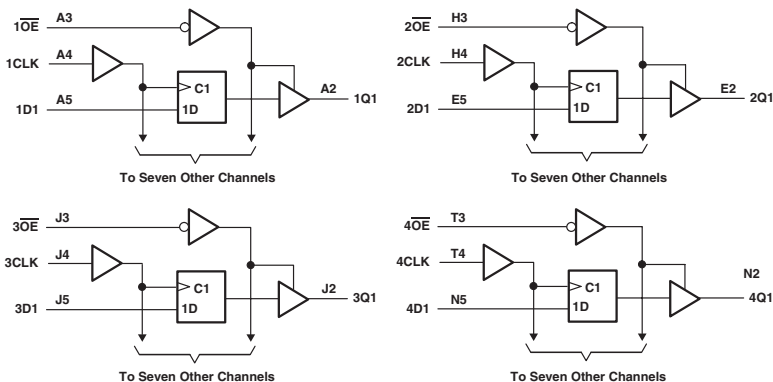
| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVCH 3V |
|-----------|-----------------|--------|------------|------------|
| t_{PLH} | A | Y | MAX | 4.4 |
| t_{PHL} | | | | 4.4 |
| t_{PZH} | \overline{OE} | Y | MAX | 5.5 |
| t_{PZL} | | | | 5.5 |
| t_{PHZ} | \overline{OE} | Y | MAX | 6.3 |
| t_{PLZ} | | | | 6.3 |

UNIT: ns

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

- Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

(each 8bit flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|----------------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

ELECTRICAL CHARACTERISTICS AND
RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MAX or MIN | LVTH 3V | UNIT |
|-----------------|------------|------------|------|
| I _{CC} | MAX | 10 | mA |
| I _{OH} | MAX | -12 | mA |
| I _{OL} | MAX | 12 | mA |

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

| PARAMETER | INPUT | OUTPUT | MAX or MIN | LVTH 3V |
|--|------------------------------|--------|------------|------------|
| f _{max} | | | | 160 |
| t _w Pulse duration, CLK high or low | | | MIN | 3 |
| t _{su} Setup time | Data before CLK ↑, data high | | MIN | 1.8 |
| | Data before CLK ↑, data low | | MIN | 1.8 |
| t _h Hold time | Data after CLK ↑, data high | | MIN | 0.8 |
| | Data after CLK ↑, data low | | MIN | 0.8 |
| t _{PLH} | CLK | Q | MAX | 5.3 |
| t _{PHL} | | | | 4.9 |
| t _{FZH} | \overline{OE} | Q | MAX | 5.6 |
| t _{FZL} | | | | 4.9 |
| t _{PHZ} | \overline{OE} | Q | MAX | 5.4 |
| t _{PLZ} | | | | 5 |

UNIT f_{max}: MHz other : ns

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