

**AT91SAM7X-EK
Evaluation Board
for AT91SAM7X and AT91SAM7XC**

User Guide





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Section 1

Overview

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|------------|--|--|
| 1.1 | Scope | <p>The AT91SAM7X-EK and the AT91SAM7XC-EK evaluation kits enable evaluation capabilities and code development of applications running on the AT91SAM7X or the AT91SAM7XC microcontroller.</p> <p>This guide focuses on the AT91SAM7X-EK board as a common evaluation platform for the AT91SAM7X and AT91SAM7XC devices in a 100-lead LQFP package.</p> |
| <hr/> | | |
| 1.2 | Deliverables | <p>The package contains the following items:</p> <ul style="list-style-type: none">■ a board marked AT91SAM7X-EK■ one A/B-type USB cable■ one crossed serial RS232 cable■ one RJ45 crossed Ethernet cable■ universal input AC/DC power supply with US and EU plug adapter■ one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly. |
| <hr/> | | |
| 1.3 | The AT91SAM7X-EK Evaluation Board | <p>Depending on the model of the kit, the board is equipped with either an AT91SAM7X256 or an AT91SAM7XC256 (100-pin LQFP Green package) together with the following interfaces:</p> <ul style="list-style-type: none">■ USB device port■ DBGU serial communication port■ RS232 serial communication port with RTS/CTS■ JTAG/ICE debug interface connector■ serial CAN communication ports■ MII Ethernet 100-base TX with auto MDIX capability■ buffered analog input and PWM output |

- Power LED and general-purpose LEDs
- DataFlash® card slot
- expansion connector
- Atmel® serial DataFlash
- One footprint for Atmel Serial EEPROM (MN11)



Section 2

Setting Up the AT91SAM7X-EK Evaluation Board

-
- | | | |
|------------|------------------------------|---|
| 2.1 | Electrostatic Warning | The AT91SAM7X-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element. |
|------------|------------------------------|---|
-
- | | | |
|------------|---------------------|--|
| 2.2 | Requirements | <p>In order to set up the AT91SAM7X-EK evaluation board, the following items are required:</p> <ul style="list-style-type: none">■ the AT91SAM7X-EK evaluation board itself■ an A/B-type USB cable <p>or</p> <ul style="list-style-type: none">■ a DC USB power adapter (5V at 0.5 A) with USB A/B cable <p>Note: The kit is not delivered with a JTAG/ICE interface which is required to start evaluating the device.</p> |
|------------|---------------------|--|
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2.3 Layout

Figure 2-1. Layout - Top View

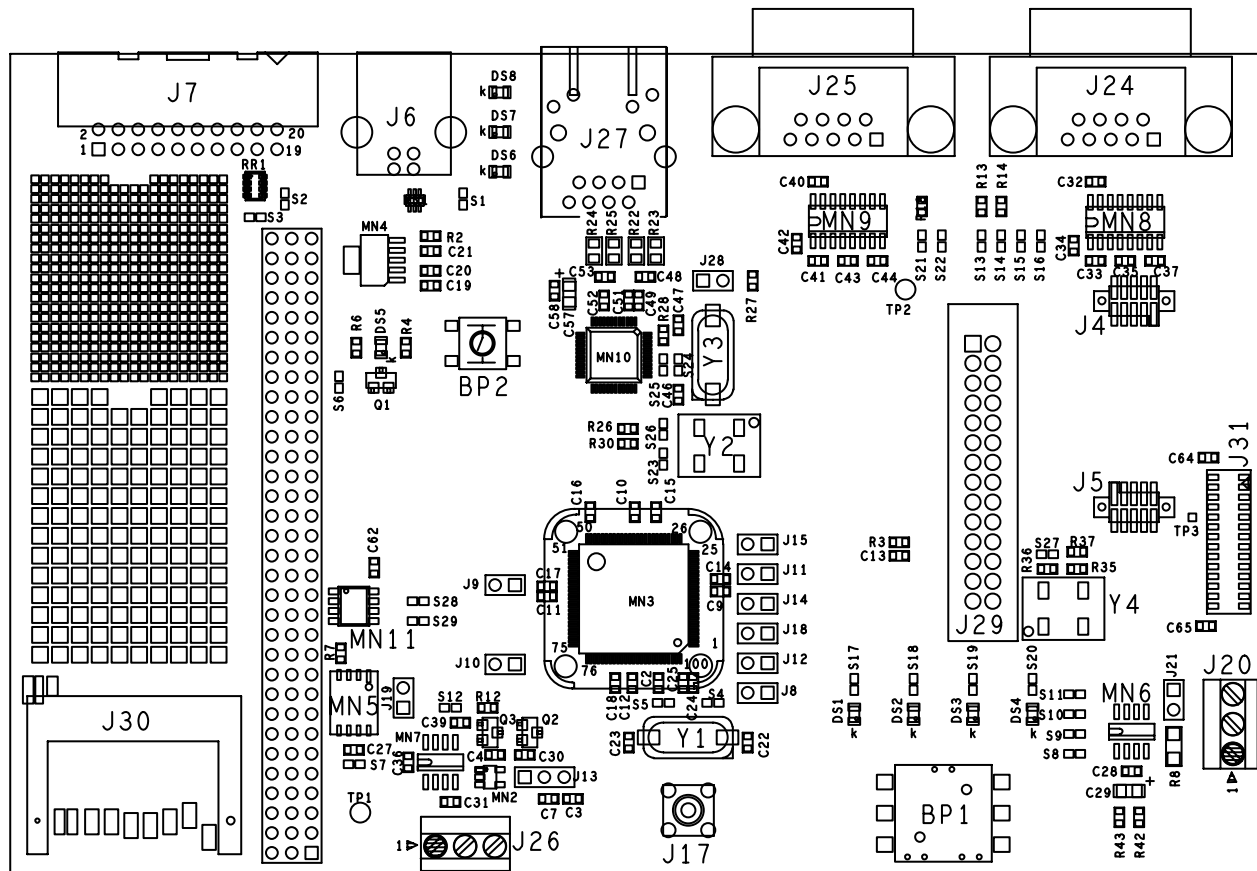
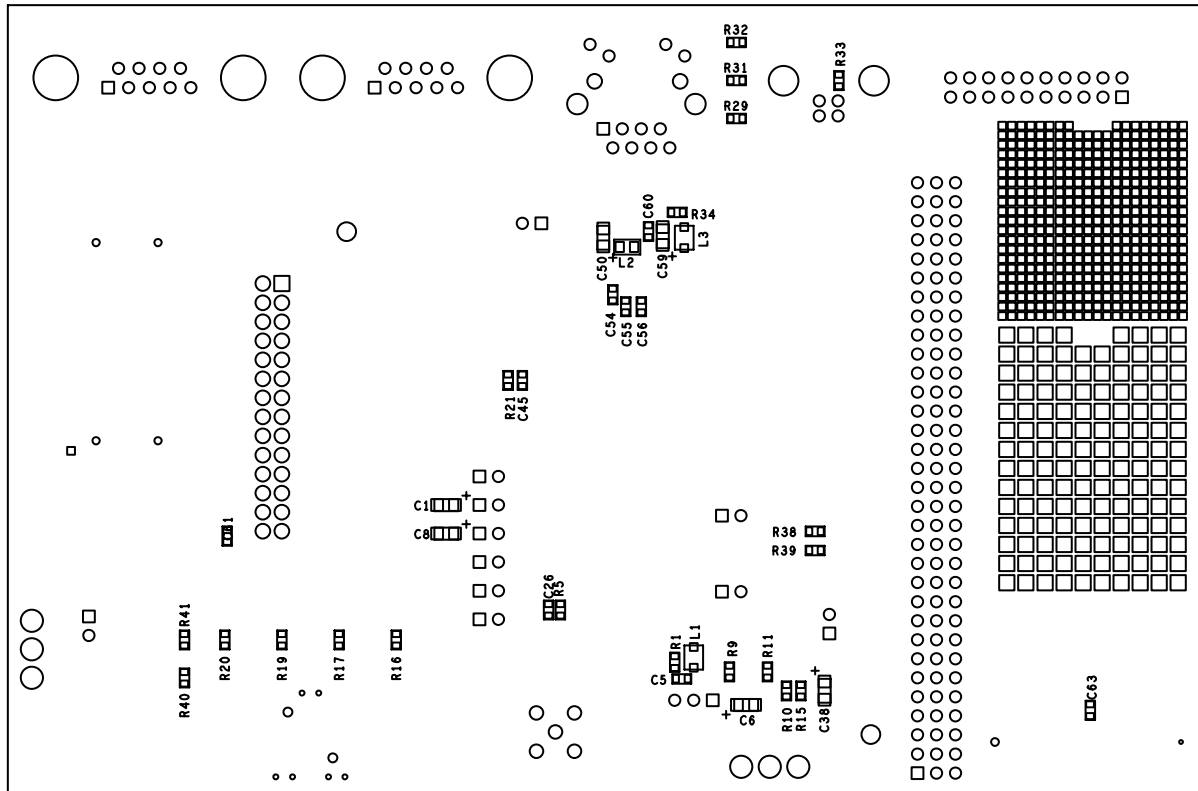


Figure 2-2. Layout - Bottom View

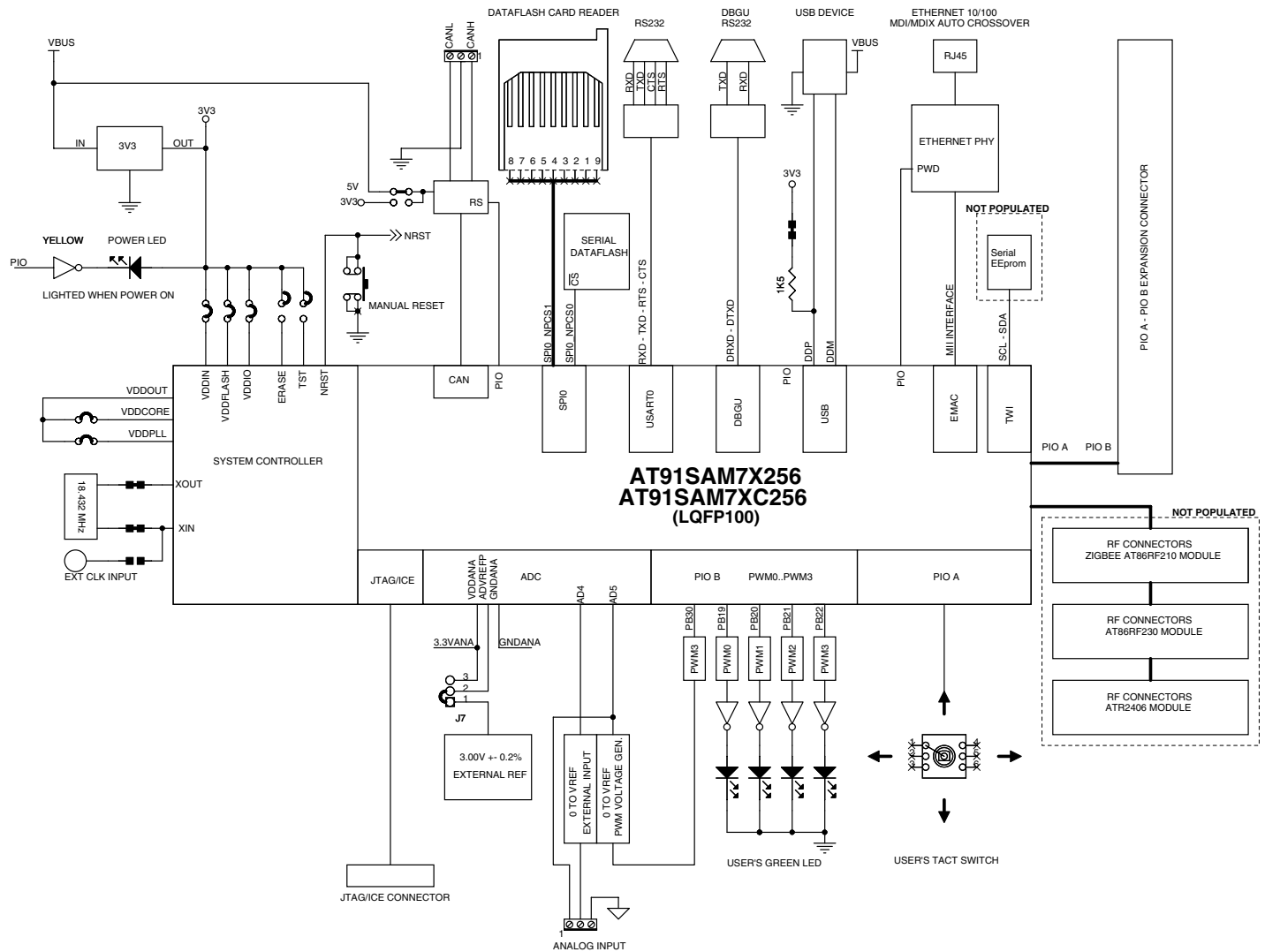


2.4 Powering Up the Board The AT91SAM7X-EK board is self-powered by the USB port or by a USB power adapter.

2.5 Getting Started The AT91SAM7X-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the evaluation kit.

2.6 AT91SAM7X-EK Block Diagram

Figure 2-3. Block Diagram





Section 3

Board Description

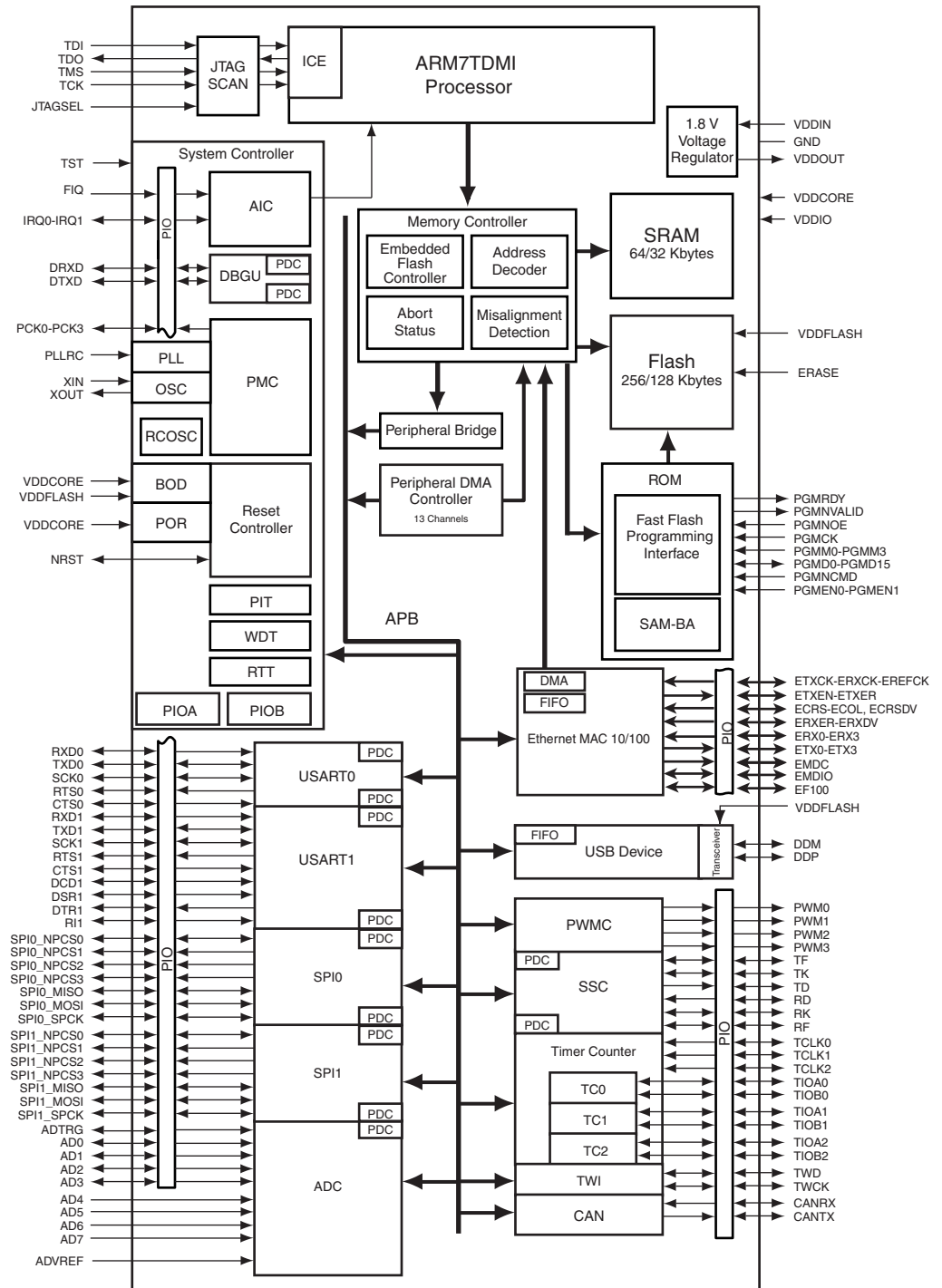
- 3.1 AT91SAM7X Microcontroller**
- Incorporates the ARM7TDMI® ARM® Thumb® Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - EmbeddedICE™, Debug Communication Channel Support
 - Internal High-speed Flash
 - 256 Kbytes (AT91SAM7X256) Organized in 1024 Pages of 256 Bytes
 - 128 Kbytes (AT91SAM7X128) Organized in 512 Pages of 256 Bytes
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
 - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
 - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
 - Fast Flash Programming Interface for High Volume Production
 - Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - 64 Kbytes (AT91SAM7X256)
 - 32 Kbytes (AT91SAM7X128)
 - Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
 - Reset Controller (RSTC)
 - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
 - Provides External Reset Signal Shaping and Reset Source Status
 - Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
 - Power Management Controller (PMC)

- Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
- Four Programmable External Clock Signals
- **Advanced Interrupt Controller (AIC)**
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- **Debug Unit (DBGU)**
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- **Periodic Interval Timer (PIT)**
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- **Windowed Watchdog (WDT)**
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- **Real-time Timer (RTT)**
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- **Two Parallel Input/Output Controllers (PIO)**
 - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- **Thirteen Peripheral DMA Controller (PDC) Channels**
- **One USB 2.0 Full Speed (12 Mbps per second) Device Port**
 - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- **One Ethernet MAC 10/100 base-T**
 - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
 - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- **One Part 2.0A and Part 2.0B Compliant CAN Controller**
 - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- **One Synchronous Serial Controller (SSC)**
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer

- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
 - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1
- Two Master/Slave Serial Peripheral Interfaces (SPI)
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
 - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit Power Width Modulation Controller (PWMC)
- One Two-wire Interface (TWI)
 - Master Mode Support Only, All Two-wire Atmel EEPROMs Supported
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™ Boot Assistance
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, Including Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.2 AT91SAM7X Block Diagram

Figure 3-1. Block Diagram



3.3 AT91SAM7XC Microcontroller

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - EmbeddedICE™, Debug Communication Channel Support
- Internal High-speed Flash
 - 256 Kbytes (AT91SAM7XC256) Organized in 1024 Pages of 256 Bytes
 - 128 Kbytes (AT91SAM7XC128) Organized in 512 Pages of 256 Bytes
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
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 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
 - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - 64 Kbytes (AT91SAM7XC256)
 - 32 Kbytes (AT91SAM7XC128)
- Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
 - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
 - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
 - Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
 - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)

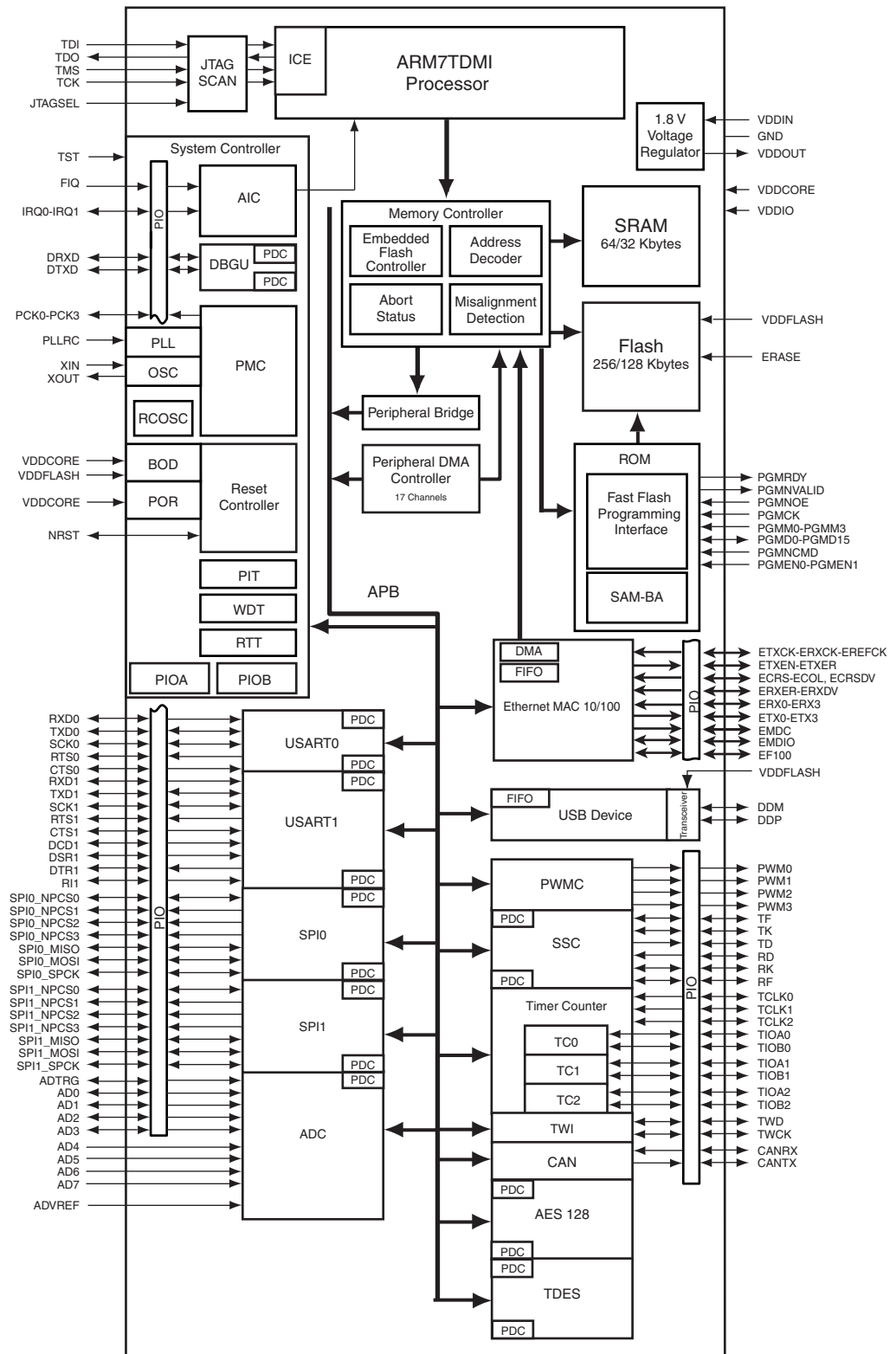
- 12-bit key-protected Programmable Counter
- Provides Reset or Interrupt Signals to the System
- Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- Two Parallel Input/Output Controllers (PIO)
 - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Seventeen Peripheral DMA Controller (PDC) Channels
- One Advanced Encryption System (AES)
 - 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications
 - Buffer Encryption/Decryption Capabilities with PDC
- One Triple Data Encryption System (TDES)
 - Two-key or Three-key Algorithms, Compliant with FIPS PUB 46-3 Specifications
 - Optimized for Triple Data Encryption Capability
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
 - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- One Ethernet MAC 10/100 base-T
 - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
 - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- One Part 2.0A and Part 2.0B Compliant CAN Controller
 - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- One Synchronous Serial Controller (SSC)
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 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
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 - Full Modem Line Support on USART1
- Two Master/Slave Serial Peripheral Interfaces (SPI)

- 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
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 - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.4 AT91SAM7XC Export Regulations Statement

These commodities, technology or software will be exported from France and the applicable Export Administration Regulations will apply. French, United States and other relevant laws, regulations and requirements regarding the export of products may restrict sale, export and re-export of these products; please assure you conduct your activities in accordance with the applicable relevant export regulations.

Figure 3-2. Block Diagram



-
- 3.6 Memory**
- 256 Kbytes of Internal High-speed Flash
 - 64 Kbytes of Internal High-speed SRAM
 - Atmel serial DataFlash®
 - One footprint for Atmel Serial EEPROM memory. The user can fit an AT24C128AN or AT24C256AN or AT24C512AN in 8S1 package as well as a cryptomemory AT88C25616C-SI
-
- 3.7 Clock Circuitry**
- 18.432 MHz standard crystal for the embedded oscillator
 - 32 KHz internal RC oscillator
-
- 3.8 Reset Circuitry**
- Internal reset controller with a bidirectional reset pin
 - External reset pushbutton
-
- 3.9 Power Supply Circuitry**
- USB powered, the dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. The total current at power-up is less than 100 mA.
 - External power can be applied via USB Power adapter 5V 0.5A with USB A/B cable
 - On-chip embedded VDDCORE 1.8V regulator
 - On-board 3.3V 400 mA linear regulator
-
- 3.10 Remote Communication**
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
 - One Serial interface (RS232 COM Port) via RS-232 DB9 male socket
 - USB V2.0 Full-speed compliant, 12 Mbits per second (UDP)
 - One CAN 2.0B communication port via the 3-position printed circuit terminal block
 - One MII Ethernet 100-base TX (auto MDI/MDI-X crossover cable)
-
- 3.11 Analog Interface**
- One selectable 0.2% 3.00V Vref or 3.3V ANA
 - One 3-position printed circuit terminal block
 - Two analog up to Vref inputs. One external user input and one back-looped with buffered PWM3 output.
 - One buffered PWM3 analog output (up to Vref)
-
- 3.12 User Interface**
- One 5-way joystick (4 directions and push for confirmation)
 - Four general-purpose buffered green user LEDs (PWM controlled)
-

- One yellow power LED (can also be software controlled)

3.13 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU serial RS232 COM Port

3.14 Expansion Slot

- One DataFlash card slot
- All I/Os of the AT91SAM7X and the AT91SAM7XC are routed to peripheral extension connectors (J16). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.



Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J8	Opened	Erases all internal Flash memory when the board is powered. To do that, the user will have to close the J8 at least 200 ms.
J9	Opened	Do not use: Factory test mode. J9 is not populated
J10	Opened	Selects ICE mode or JTAG mode (Closed). J10 is not populated.
J11	Closed	VDDIN Jumper ⁽¹⁾
J12	Closed	VDDFLASH Jumper ⁽¹⁾
J13	1-2	ADVREF Jumper select 1-2: 3.00V Voltage reference 2-3: VDDANA
J14	Closed	VDDCORE Jumper ⁽¹⁾
J15	Closed	VDDIO Jumper ⁽¹⁾
J17	Opened	External XIN clock input. S4 and S5 must be open. J17 is not populated.
J18	Closed	VDDPLL Jumper ⁽¹⁾
J19	Closed	Enables the use of the NPCS00 (PA12).
J21	Closed	Enables 120 ohms CAN bus resistance termination.
J28	Closed	Enables Ethernet Auto MDIX control.
S1	Closed	Enables permanent pull up on USB DP.
S2	Closed	The System Reset signal (NRST) is connected to the ICE/JTAG socket (J7, pin 15).
S3	Opened	Disables 5V (VUSB) power supply on J16 extension connector.

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S4 - S5	Closed	Enables the use of 18.432MHz crystal. Must be open if an external clock is used.
S6	Closed	Enables the Power Led control (PB25).
S7	Opened	Disables Serial DataFlash write protect.
S8	Closed	Enables the use of the TXD CAN transceiver (PA20)
S9	Closed	Enables the use of the RXD CAN transceiver (PA19)
S10	Closed	Enables control of the Standby/Normal mode for CAN transceivers (PA2)
S11	Opened	Enables control of the Standby/Normal mode for CAN transceivers (PA2). If S11 is closed, S10 must be open.
S12	Closed	Enables the use of PWM3 Analog Output (PB30)
S13	Closed	Enables the use of the TXD0 signal (PA1)
S14	Closed	Enables the use of the RTS0 signal (PA3)
S15	Closed	Enables the use of the RXD0 signal (PA0)
S16	Closed	Enables the use of the CTS0 signal (PA4)
S17	Closed	Enables the use of the User LED DS1 (PB19)
S18	Closed	Enables the use of the User LED DS2 (PB20)
S19	Closed	Enables the use of the User LED DS3 (PB21)
S20	Closed	Enables the use of the User LED DS4 (PB22)
S21	Closed	Enables the use of the DBGU TXD signal (PA28)
S22	Closed	Enables the use of the DBGU RXD signal (PA27)
S23	Opened	ETHERNET MII is the default mode. To evaluate the RMII mode, the user change S23 to S26 configuration in the following way: S23 Closed, S24 Opened, S25 Closed, S26 Opened
S24	Closed	
S25	Opened	
S26	Closed	
S27	Opened	Reserved
S28	Closed	Enables the use of the SCL of MN11 (PA11)
S29	Closed	Enables the use of the SDA of MN11 (PA10)
TP1	N.A	GND Test point.
TP2	N.A	GND Test point.

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.



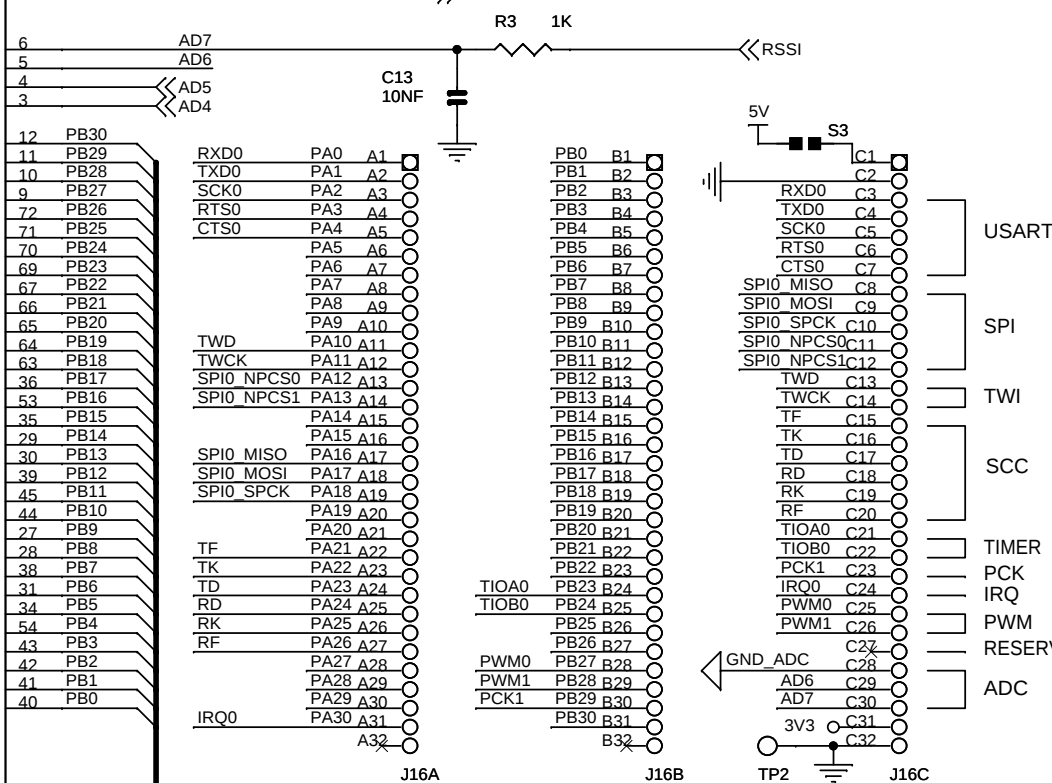
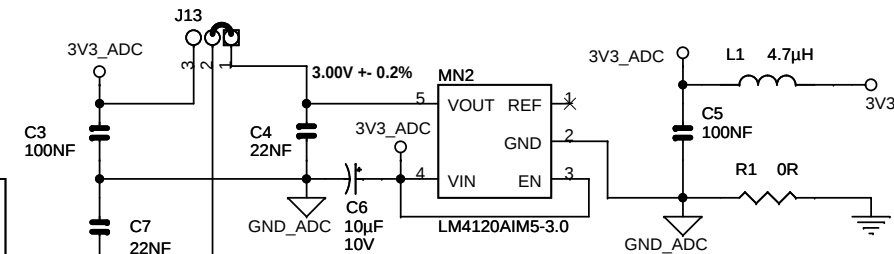
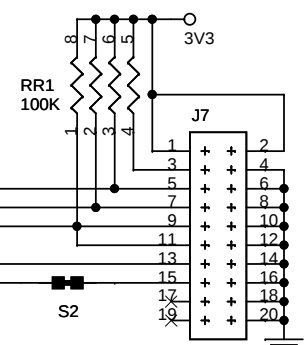
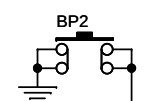
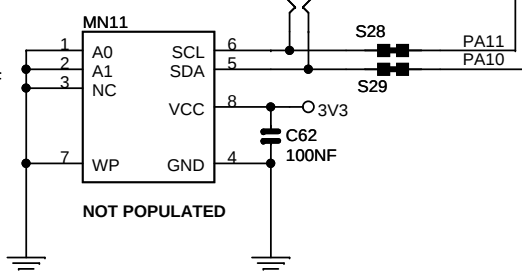
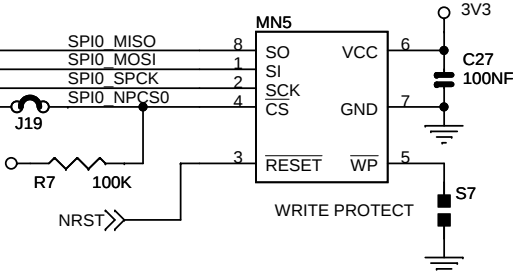
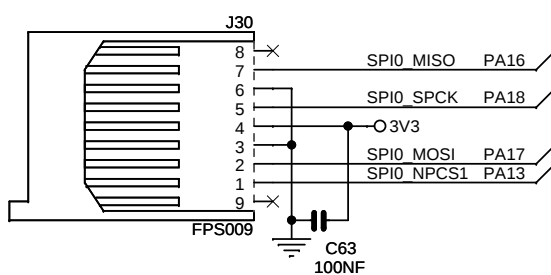
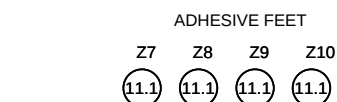
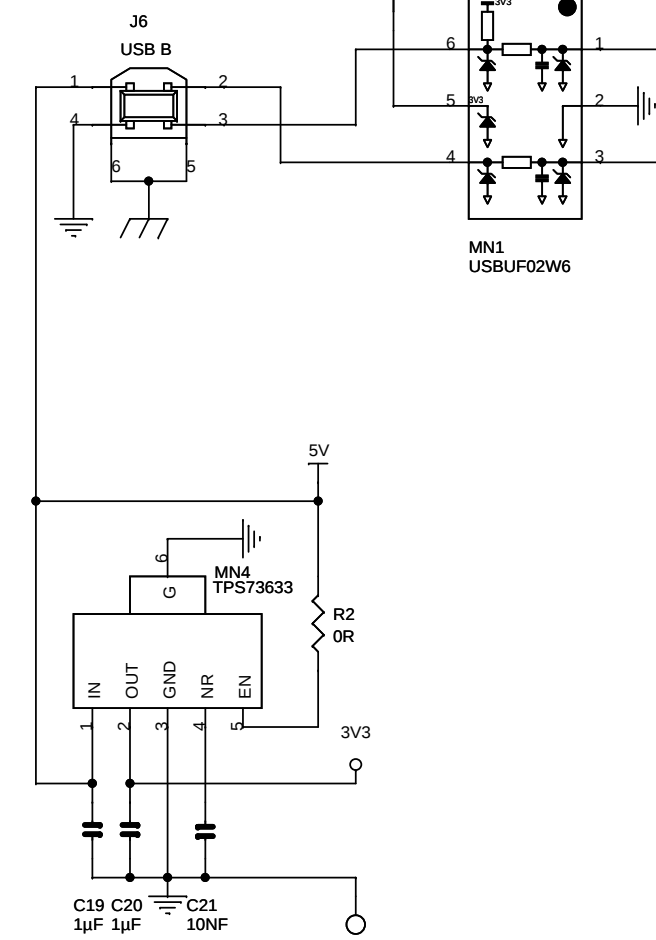
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Processor Board
- I/O
- Ethernet
- RF modules

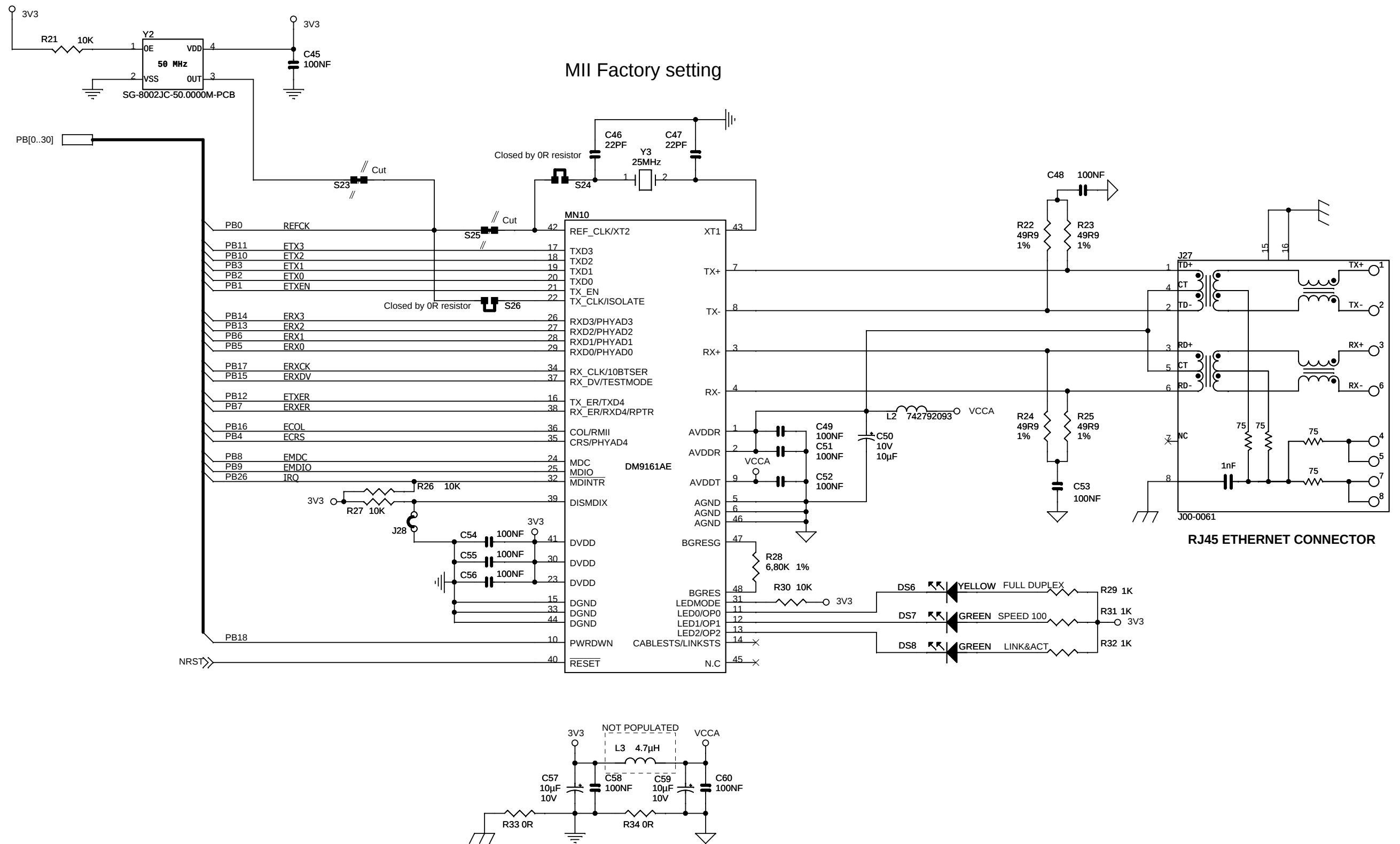


PA0	81	PA07XDX0	PA07XCK1	PA07XSP0	PA07XSP1	PA07XSP2	PA07XSP3	PA07XSP4	PA07XSP5	PA07XSP6	PA07XSP7	PA07XSP8	PA07XSP9	PA07XSP10	PA07XSP11	PA07XSP12	PA07XSP13	PA07XSP14	PA07XSP15	PA07XSP16	PA07XSP17	PA07XSP18	PA07XSP19	PA07XSP20	PA07XSP21	PA07XSP22	PA07XSP23	PA07XSP24	PA07XSP25	PA07XSP26	PA07XSP27	PA07XSP28	PA07XSP29	PA07XSP30	PA07XSP31	PA07XSP32	PA07XSP33	PA07XSP34	PA07XSP35	PA07XSP36	PA07XSP37	PA07XSP38	PA07XSP39	PA07XSP40	PA07XSP41	PA07XSP42	PA07XSP43	PA07XSP44	PA07XSP45	PA07XSP46	PA07XSP47	PA07XSP48	PA07XSP49	PA07XSP50	PA07XSP51	PA07XSP52	PA07XSP53	PA07XSP54	PA07XSP55	PA07XSP56	PA07XSP57	PA07XSP58	PA07XSP59	PA07XSP60	PA07XSP61	PA07XSP62	PA07XSP63	PA07XSP64	PA07XSP65	PA07XSP66	PA07XSP67	PA07XSP68	PA07XSP69	PA07XSP70	PA07XSP71	PA07XSP72	PA07XSP73	PA07XSP74	PA07XSP75	PA07XSP76	PA07XSP77	PA07XSP78	PA07XSP79	PA07XSP80	PA07XSP81	PA07XSP82	PA07XSP83	PA07XSP84	PA07XSP85	PA07XSP86	PA07XSP87	PA07XSP88	PA07XSP89	PA07XSP90	PA07XSP91	PA07XSP92	PA07XSP93	PA07XSP94	PA07XSP95	PA07XSP96	PA07XSP97	PA07XSP98	PA07XSP99	PA07XSP100	PA07XSP101	PA07XSP102	PA07XSP103	PA07XSP104	PA07XSP105	PA07XSP106	PA07XSP107	PA07XSP108	PA07XSP109	PA07XSP110	PA07XSP111	PA07XSP112	PA07XSP113	PA07XSP114	PA07XSP115	PA07XSP116	PA07XSP117	PA07XSP118	PA07XSP119	PA07XSP120	PA07XSP121	PA07XSP122	PA07XSP123	PA07XSP124	PA07XSP125	PA07XSP126	PA07XSP127	PA07XSP128	PA07XSP129	PA07XSP130	PA07XSP131	PA07XSP132	PA07XSP133	PA07XSP134	PA07XSP135	PA07XSP136	PA07XSP137	PA07XSP138	PA07XSP139	PA07XSP140	PA07XSP141	PA07XSP142	PA07XSP143	PA07XSP144	PA07XSP145	PA07XSP146	PA07XSP147	PA07XSP148	PA07XSP149	PA07XSP150	PA07XSP151	PA07XSP152	PA07XSP153	PA07XSP154	PA07XSP155	PA07XSP156	PA07XSP157	PA07XSP158	PA07XSP159	PA07XSP160	PA07XSP161	PA07XSP162	PA07XSP163	PA07XSP164	PA07XSP165	PA07XSP166	PA07XSP167	PA07XSP168	PA07XSP169	PA07XSP170	PA07XSP171	PA07XSP172	PA07XSP173	PA07XSP174	PA07XSP175	PA07XSP176	PA07XSP177	PA07XSP178	PA07XSP179	PA07XSP180	PA07XSP181	PA07XSP182	PA07XSP183	PA07XSP184	PA07XSP185	PA07XSP186	PA07XSP187	PA07XSP188	PA07XSP189	PA07XSP190	PA07XSP191	PA07XSP192	PA07XSP193	PA07XSP194	PA07XSP195	PA07XSP196	PA07XSP197	PA07XSP198	PA07XSP199	PA07XSP200	PA07XSP201	PA07XSP202	PA07XSP203	PA07XSP204	PA07XSP205	PA07XSP206	PA07XSP207	PA07XSP208	PA07XSP209	PA07XSP210	PA07XSP211	PA07XSP212	PA07XSP213	PA07XSP214	PA07XSP215	PA07XSP216	PA07XSP217	PA07XSP218	PA07XSP219	PA07XSP220	PA07XSP221	PA07XSP222	PA07XSP223	PA07XSP224	PA07XSP225	PA07XSP226	PA07XSP227	PA07XSP228	PA07XSP229	PA07XSP230	PA07XSP231	PA07XSP232	PA07XSP233	PA07XSP234	PA07XSP235	PA07XSP236	PA07XSP237	PA07XSP238	PA07XSP239	PA07XSP240	PA07XSP241	PA07XSP242	PA07XSP243	PA07XSP244	PA07XSP245	PA07XSP246	PA07XSP247	PA07XSP248	PA07XSP249	PA07XSP250	PA07XSP251	PA07XSP252	PA07XSP253	PA07XSP254	PA07XSP255	PA07XSP256	PA07XSP257	PA07XSP258	PA07XSP259	PA07XSP260	PA07XSP261	PA07XSP262	PA07XSP263	PA07XSP264	PA07XSP265	PA07XSP266	PA07XSP267	PA07XSP268	PA07XSP269	PA07XSP270	PA07XSP271	PA07XSP272	PA07XSP273	PA07XSP274	PA07XSP275	PA07XSP276	PA07XSP277	PA07XSP278	PA07XSP279	PA07XSP280	PA07XSP281	PA07XSP282	PA07XSP283	PA07XSP284	PA07XSP285	PA07XSP286	PA07XSP287	PA07XSP288	PA07XSP289	PA07XSP290	PA07XSP291	PA07XSP292	PA07XSP293	PA07XSP294	PA07XSP295	PA07XSP296	PA07XSP297	PA07XSP298	PA07XSP299	PA07XSP300	PA07XSP301	PA07XSP302	PA07XSP303	PA07XSP304	PA07XSP305	PA07XSP306	PA07XSP307	PA07XSP308	PA07XSP309	PA07XSP310	PA07XSP311	PA07XSP312	PA07XSP313	PA07XSP314	PA07XSP315	PA07XSP316	PA07XSP317	PA07XSP318	PA07XSP319	PA0
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RXD0	PA0	A1		PB0	B1
TXD0	PA1	A2		PB1	B2
SCK0	PA2	A3		PB2	B3
RTS0	PA3	A4		PB3	B4
CTS0	PA4	A5		PB4	B5
	PA5	A6		PB5	B6
	PA6	A7		PB6	B7
	PA7	A8		PB7	B8
	PA8	A9		PB8	B9
	PA9	A10		PB9	B10
TWD	PA10	A11	PB10	B11	
TWCK	PA11	A12	PB11	B12	
SPI0_NPCS0	PA12	A13	PB12	B13	
SPI0_NPCS1	PA13	A14	PB13	B14	
	PA14	A15	PB14	B15	
	PA15	A16	PB15	B16	
SPI0_MISO	PA16	A17	PB16	B17	
SPI0_MOSI	PA17	A18	PB17	B18	
SPI0_SPCK	PA18	A19	PB18	B19	
	PA19	A20	PB19	B20	
	PA20	A21	PB20	B21	
TF	PA21	A22	PB21	B22	
TK	PA22	A23	PB22	B23	
TD	PA23	A24	TIOA0	PB23 B24	
RD	PA24	A25	TIOB0	PB24 B25	
RK	PA25	A26	PB25	B26	
RF	PA26	A27	PB26	B27	
	PA27	A28	PB27	B28	
	PA28	A29	PWM0	PB28 B29	
	PA29	A30	PWM1	PB29 B30	
IRQ0	PA30	A31	CK1	PB30 B31	

Pinout diagram of the STM32F103C8T6 microcontroller. The diagram shows a 40-pin package with pins numbered C1 to C40. Functions are assigned to pins: C1 (blank), C2 (GND), C3 (RXD0), C4 (TXD0), C5 (SCK0), C6 (RTS0), C7 (CTS0), C8 (SPI0 MISO), C9 (SPI0 MOSI), C10 (SPI0 SPCK), C11 (SPI0 NPCS0), C12 (SPI0 NPCS1), C13 (TWD), C14 (TWCK), C15 (TF), C16 (TK), C17 (TD), C18 (RD), C19 (RK), C20 (RF), C21 (TIOA0), C22 (TIOB0), C23 (PCK1), C24 (IRQ0), C25 (PWM0), C26 (PWM1), C27 (blank), C28 (GND_ADC), C29 (AD6), C30 (AD7), C31 (3V3), C32 (blank), C33 (blank), C34 (blank), C35 (blank), C36 (blank), C37 (blank), C38 (blank), C39 (blank), C40 (blank). Functions are grouped by brackets: USART (C3-C7), SPI (C8-C12), TWI (C13-C14), SCC (C15-C20), TIMER (C21-C22), PCK (C23), IRQ (C24), PWM (C25), RESERVED (C27-C31), and ADC (C28-C30).

 AT91SAM7X-EK AT91SAM7XC-EK PROCESSOR BOARD							
	C		JPG	14/12/05			
	B		JPG	30/09/05			
	A	INIT EDIT	JPG	13/09/05			
	REV	MODIF.	DES.	DATE	VER.	DATE	
	SCALE	1/1			REV.	SHEET	
					C	1/4	
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PA[0..30]

RX PA26 GPIO PA14 PA15 PA18 PA17 PA16

J4

1 GPIO PA14
3 SPI0 NPCS PA15
5 SPI0 SPCK PA18
7 SPI0 MOSI PA17
9 SPI0 MISO PA16

TX SEL
CHIP_READY
RX_DATA_CLK
RX_DATA
TX_DATA

PA9 GPIO PA29
PA7 SCK1 PA8
PA5 RXD1
PA6 TXD1

J5

9
8 GPIO PA29
6 GPIO PA8
4
2

3V3

CCA START

NOT POPULATED

[illegible]

1.27 PITCH

2.54 PITCH



Section 6

Errata

-
- | | | |
|------------|---|---|
| 6.1 | DM9161A Ethernet Phy Connections | <p>The Ethernet interface works as presented in the schematics, but the connections are not in compliance with Davicom recommendations.</p> <p>To comply with Davicom recommendations on connecting this device, J27-4 and J27-5 (RJ45 connector, CT) should be connected to the VCCA side of L2. In the current schematics (ETHERNET, Sheet 3/4), the VCCA side of L2 is connected to MN10-1 and MN10-2 (DM9161A, AVDDR).</p> <p>For additional information, refer to the Davicom datasheet for DM9161A and associated Application Notes available on http://www.davicom.com.tw/.</p> |
| <hr/> | | |
| 6.2 | TWI line pullups for Fast Mode operation | <p>In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R38 and R39 should be replaced by smaller values (e.g., 2.2 KΩ).</p> <p>Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).</p> |



Section 7

Revision History

7.1 Revision History

Table 7-1. Change History

Document	Comments	Change Request Ref.
6195A	First issue.	
6195B	Updated Figure 2-3 with new signal names. Updated document to show new product functionalities. New board block diagram and schematics issued.	05-430
6195C	Updated document to contain new product AT91SAM7XC. Added new section with Errata.	
6195D	Removed references to 32 Mbit serial DataFlash (AT45DB321C-CNC) in Section 1.3 and in Section 3.6 . Inserted new Figure 2-3 and new schematics in Section 5 .	2862
6195E	Added Errata Section 6.2 "TWI line pullups for Fast Mode operation"	4084



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