4Mbyte(1Mx32) Fast Page Mode, 1K Refresh, 72Pin SIMM, 5V Design
Part No. HMD1M32M2G

DESCRIPTION

The HMD1M32M2G is an 1M x 32 bits Dynamic RAM MODULE which is assembled 2 pieces of 1M x 16bit DRAMs in 42 pin SOJ package on single sides the printed circuit board with decoupling capacitors. The HMD1M32M2G is optimized for application to the systems, which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others, which are, requested compact size.

The HMD1M32M2G provides common data and outputs.

Features

- w 72 pins Single In-Line Package
- w Fast Page Mode Capability
- w Single +5V± 0.5V power supply
- w Fast Access Time & Cycle Time

	tRAC	tCAC	tRC	tPC
HMD1M32M2G-6	60	15	110	40
HMD1M32M2G-7	70	18	130	45

- w Low Power

  Active: 1,870/1,650/1,430 mW(MAX)

  Standby: 11mW(CMOS level : MAX)
- w /RAS Only Refresh, /CAS before /RAS Refresh,

  Hidden Refresh Capability
- w All inputs and outputs TTL Compatible
- w 1,024 Refresh Cycles/16ms

PRESENCE DETECT PINS (Optional)

PIN	60NS	70NS
PD1	Vss	Vss
PD2	Vss	Vss
PD3	NC	Vss
PD4	NC	NC

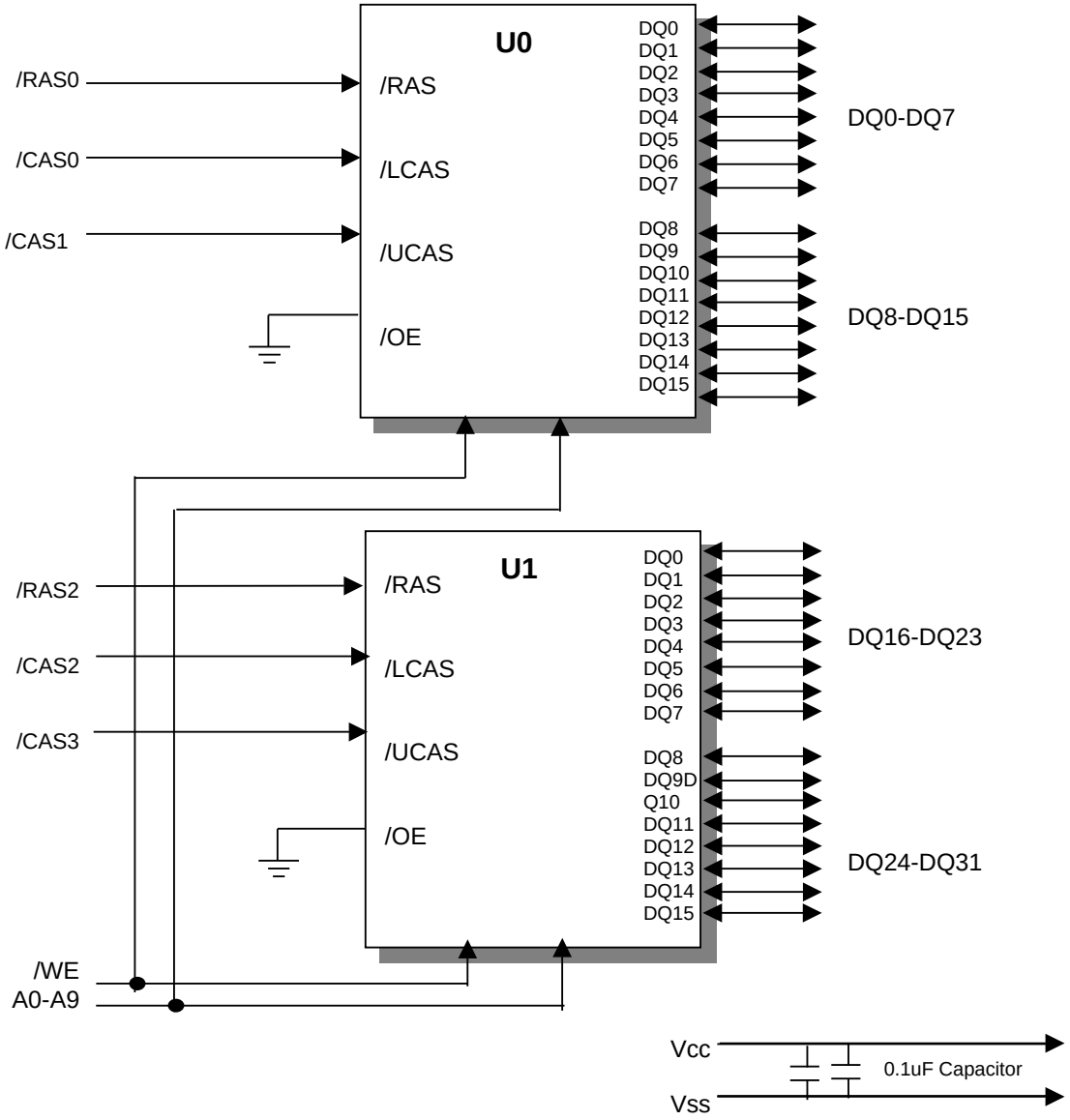
PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ22	49	DQ8
2	DQ0	26	DQ7	50	DQ24
3	DQ16	27	DQ23	51	DQ9
4	DQ1	28	A7	52	DQ25
5	DQ17	29	NC	53	DQ10
6	DQ2	30	Vcc	54	DQ26
7	DQ18	31	A8	55	DQ11
8	DQ3	32	A9	56	DQ27
9	DQ19	33	NC	57	DQ12
10	Vcc	34	/RAS2	58	DQ28
11	NC	35	NC	59	Vcc
12	A0	36	NC	60	DQ29
13	A1	37	NC	61	DQ13
14	A2	38	NC	62	DQ30
15	A3	39	Vss	63	DQ14
16	A4	40	/CAS0	64	DQ31
17	A5	41	/CAS2	65	DQ15
18	A6	42	/CAS3	66	NC
19	NC	43	/CAS1	67	PD1
20	DQ4	44	/RAS0	68	PD2
21	DQ20	45	NC	69	PD3
22	DQ5	46	NC	70	PD4
23	DQ21	47	/WE	71	NC
24	DQ6	48	NC	72	Vss

PIN DESCRIPTION

PIN	FUNCTION	PIN	FUNCTION
A0 – A9	Address Inputs	PD1 – PD4	Presence Detect
DQ0 – DQ31	Data Input/Output	Vcc	Power (+5V)
/RAS0, /RAS2	Row Address Strobe	Vss	Ground
/CAS0 - /CAS3	Column Address Strobe	NC	No Connection
/WE	Read/Write Enable	-	-

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature under Bias	**0 ~ 70**	C
TSTG	Storage Temperature (Plastic)	**-55 ~ 125**	C
VIN/VOUT	Voltage on any Pin Relative to Vss	**-1.0 ~ 7.0**	V
VCC	Power Supply Voltage	**-1.0 ~ 7.0**	V
IOUT	Short Circuit Output Current	**50**	mA
PD	Power Dissipation	**2**	W

***NOTE**: 1. Stress greater than above absolute Maximum Ratings? May cause permanent damage to the device.

RECOMMENDED DC OPERATING CONDITIONS (TA = 0 ~ 70C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

***NOTE**: All voltages referenced to Vcc

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTE
VOH	Output Level Output High Level Voltage (**I**OUT = -5mA)		2.4	Vcc	V	
VOL	Output Level Output Low Level Voltage (**I**OUT = 4.2mA)		0	0.4	V	
ICC1	Operating Current Average Power Supply Operating Current (/RAS,/CAS,Address Cycling : **t**RC = **t**RC min)	60ns	-	340	mA	1,2
		70ns	-	300		
		-	-	-		
ICC2	Standby Current (TTL) Power Supply Standby Current (/RAS,/CAS = VIH)		-	4	mA	
ICC3	/RAS Only Refresh Current Average Power Supply Current /RAS Only Mode (/RAS Cycling, /CAS = VIH,: **t**RC = **t**RC min)	60ns	-	340	mA	2
		70ns		300		
ICC ICC4	Fast Page Mode Current Average Power Supply Current Fast Page Mode (/RAS = VIL, /CAS, Address Cycling : tPC = tPC min)	60ns	-	340	mA	1,3
		70ns	-	300	mA	1,3
ICC5	Standby Current (CMOS) Power Supply Standby Current (/RAS,/CAS >= Vcc –0.2V)		-	2	mA	
ICC6	/CAS before /RAS Refresh Current (**t**RC = **t**RC min)	60ns	-	340	mA	
		70ns	-	300		

ICC7	Standby Current /RAS = VIH /CAS = VIL DOUT = Enable	-	10	mA	1
II(L)	Input Leakage Current Any Input (0V<=VIN<=7V) All Other Pins Not Under Test = 0V	-10	10	uA	
IO(L)	Output Leakage Current (DOUT is Disabled, 0V<=VOUT<=7V)	-10	10	uA	

Note: 1.Icc depends on output load condition when the device is selected.

Icc (max) is specified at the output open condition.

2. Address can be changed once or less while /RAS = VIL.

3. Address can be changed once or less while /CAS = VIH

CAPACITANCE (T_A=25°C, Vcc = 5V+/- 10%, f = 1Mhz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTE
Input Capacitance (A0-A9)	C_{I1}	-	35	pF	1
Input Capacitance (/WE)	C_{I2}	-	34	pF	1,2
Input Capacitance (/RAS0,/RAS2)	C_{I3}	-	27	pF	1,2
Input Capacitance (/CAS0-/CAS3)	C_{I4}	-	27	pF	1,2
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	20	pF	1,2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. /CAS = VIH to disable DOUT.

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,15.)

The GMM731000CNS/SG writes data only in early write cycle (twcs>=twcs(min))
Delayed write cycle is not available because of I/O common.

READ, WRITE AND REFRESH CYCLE (Common Parameters)

SYMBOL	PARAMETER	-6		-7		UNIT	NOTE
		MIN	MAX	MIN	MAX		
tRC	Random Read or Write Cycle Time	110	-	130	-	ns	
tPR	/RAS Precharge Time	40	-	50	-	ns	
tRAS	/RAS Pulse Width	60	10K	70	10K	ns	
tCAS	/CAS Pulse Width	15	10K	18	10K	ns	
tASR	Row Address Setup Time	0	-	0	-	ns	
tRAH	Row Address Hold Time	10	-	10	-	ns	
tASC	Column Address Setup Time	0	-	0	-	ns	

tCAH	Column Address Hold Time	10	-	15	-	ns	9
tRCD	/RAS to /CAS Delay Time	20	45	20	52	ns	10
tRAD	/RAS to Column Address Delay Time	15	30	15	35	ns	
tRSH	/RAS Hold Time	15	-	18	-	ns	
tCSH	/CAS Hold Time	60	-	70	-	ns	
tCRP	/CAS to /RAS Precharge Time	5	-	5	-	ns	
tT	Transition Time (Rise and Fall)	3	50	3	50	ns	8
tREF	Refresh Period (1024 Cycle)	-	16	-	16	ms	

READ CYCLE

SYMBOL	PARAMETER	-6		-7		UNIT	NOTE
		MIN	MAX	MIN	MAX		
tRAC	Access Time from /RAS	-	60	-	70	ns	2,3
tCAC	Access Time from /CAS	-	15	-	18	ns	3,4
tAA	Access Time from Column Address	-	30	-	35	ns	3,5,14
tRCS	Read Command Setup Time	0	-	0	-	ns	
tRCH	Read Command Hold Time to /CAS	0	-	0	-	ns	6
tRRH	Read Command Hold Time to /RAS	0	-	0	-	ns	6
tRAL	Column Address to /RAS Lead Time	30	-	35	-	ns	
tOFF	Output Buffer Turn-off Time	-	15	-	15	ns	7

WRITE CYCLE

SYMBOL	PARAMETER	-6		-7		UNIT	NOTE
		MIN	MAX	MIN	MAX		
twcs	Write Command Setup Time	0	-	0	-	ns	11
tWCH	Write Command Hold Time	10	-	15	-	ns	
tWP	Write Command Pulse Width	10	-	10	-	ns	
tRWL	Write Command to /RAS Lead Time	15	-	18	-	ns	
tCWL	Write Command to /CAS Lead Time	15	-	18	-	ns	
tDS	Data-in Setup Time	0	-	0	-	ns	12
tDH	Data-in Hold Time	10	-	15	-	ns	12

REFRESH CYCLE

SYMBOL	PARAMETER	-6		-7		UNIT	NOTE
		MIN	MAX	MIN	MAX		
tCRS	/CAS Setup Time (/CAS-before-/RAS Refresh Cycle)	10	-	10	-	ns	
tCHR	/CAS Hold Time (/CAS-before-/RAS Refresh Cycle)	10	-	10	-	ns	

tRPC	/RAS Precharge to /CAS Hold Time	5	-	5	-	ns	

FAST PAGE MODE CYCLE

SYMBOL	PARAMETER	-6		-7		UNIT	NOTE
		MIN	MAX	MIN	MAX		
tPC	Fast Page Mode Cycle Time	40	-	45	-	ns	
tCP	Fast Page Mode /RAS Precharge Time	10	-	10	-	ns	
tRASP	Fast Page Mode /CAS Pulse Time	60	100K	70	100K	ns	13
tACP	Access Time from /CAS Precharge	-	35	-	40	ns	14
tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	ns	

Note: 1. AC measurements assume **t**T = 5ns.

2. Assumes that **t**RCD<=**t**RCD(max) and **t**RCD<=**t**RCD(max). If **t**RCD or **t**RCD is greater than the maximum recommended value shown in this table, **t**RCD exceeds the value shown.

3. Measured with a load circuit equivalent to 2TTL loads and 100PpF.

4. Assumes that **t**RCD >= **t**RCD (max) and **t**RCD<= **t**RCD (max).

5.Assumes that tRCD <= **t**RCD (max) and **t**RCD>= **t**RCD (max).

6.Either **t**RCH or **t**RRH must be satisfied for a read cycles.

7. **t**OFF(max) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

8. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.

9. Operation with the **t**RCD (max) limit insures that **t**RAC (max) can be met, **t**RCD (max) is specified as a reference point only, if **t**RCD is greater than the specified **t**RCD (max) limit, then access time is controlled exclusively by **t**CAC .

10. Operation with the **t**RAD (max) limit insures that **t**RAC (max) can be met, **t**RAD (max) is specified as a reference point only, if **t**RAD is greater than the specified **t**RAD (max) limit, then access time is controlled exclusively by **t**AA.

11. TWCS is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If **t**wcs >= **t**wcs (min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.

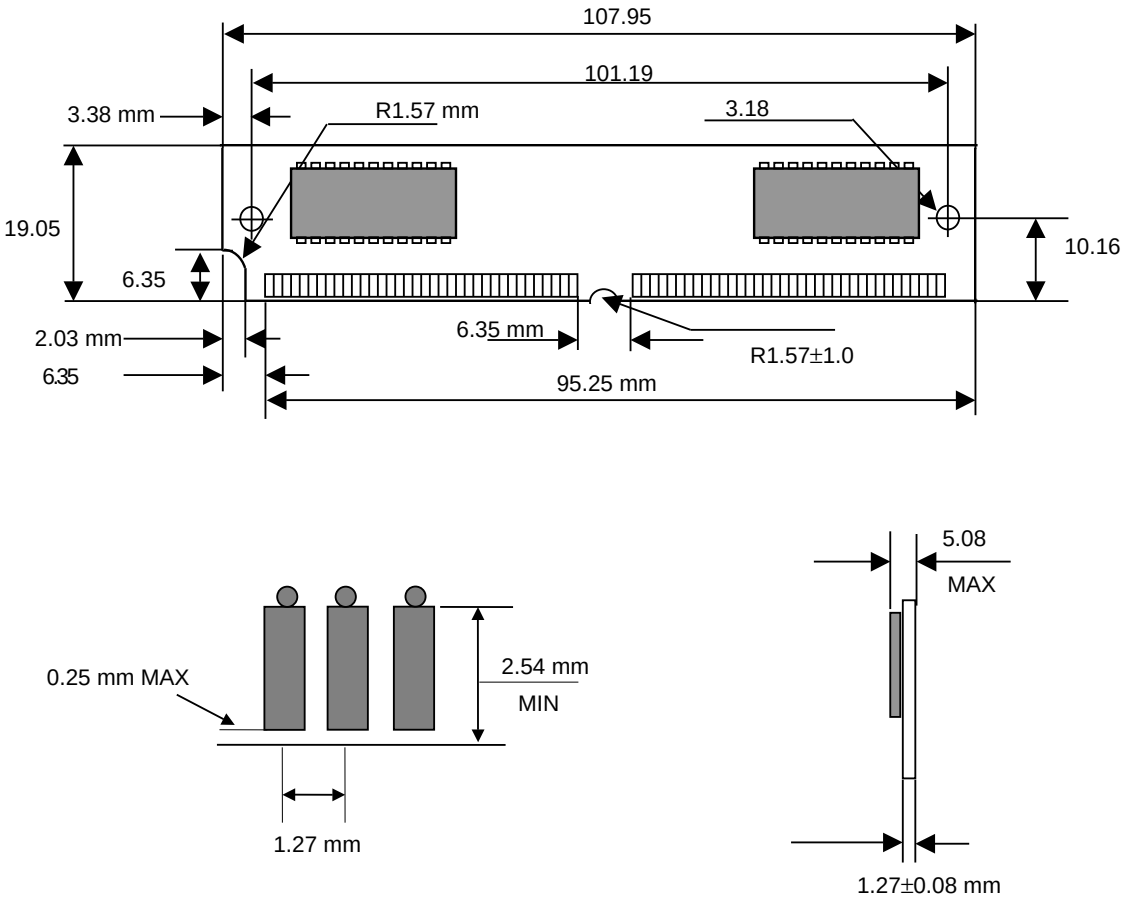
12. These parameters are referenced to /CAS leading edge in early write cycles.

13. **t**RASP is defines /RAS pulse width in Fast Page Mode cycles.

14. Access time is determined by the longer of **t**AA or **t**CAC or **t**ACP .

15. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycle (eny combination of cycles containing /RAS clock such as /RAS only refresh). If the internal refresh count is used, a mnimum of eight /CAS before /RAS refresh cycle are required.

PACKAGING INFORMATION



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD1M32M2G-6	4MByte	X32	72 Pin-SIMM	2EA	5V	FP	60ns

HMD1M32M2G-7	4MByte	x 32	72 Pin-SIMM	2EA	5V	FP	70ns

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