CY7C4281
CY7C4291

64K/128K x 9 Deep Sync FIFOs

Features

- **High-speed, low-power, first-in first-out (FIFO) memories**
- **64K × 9 (CY7C4281)**
- **128K × 9 (CY7C4291)**
- **0.5-micron CMOS for optimum speed/power**
- **High-speed 100-MHz operation (10-ns read/write cycle times)**
- **Low power**
  - **— I_{CC} = 40 mA**
  - **— I_{SB} = 2 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, and programmable Almost Empty and Almost Full status flags**
- **TTL compatible**
- **Output Enable (OE) pin**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion Capability**
- **Pin-compatible density upgrade to CY7C42X1 family**
- **Pin-compatible density upgrade to IDT72201/11/21/31/41/51**
- **Pb-Free Packages Available**

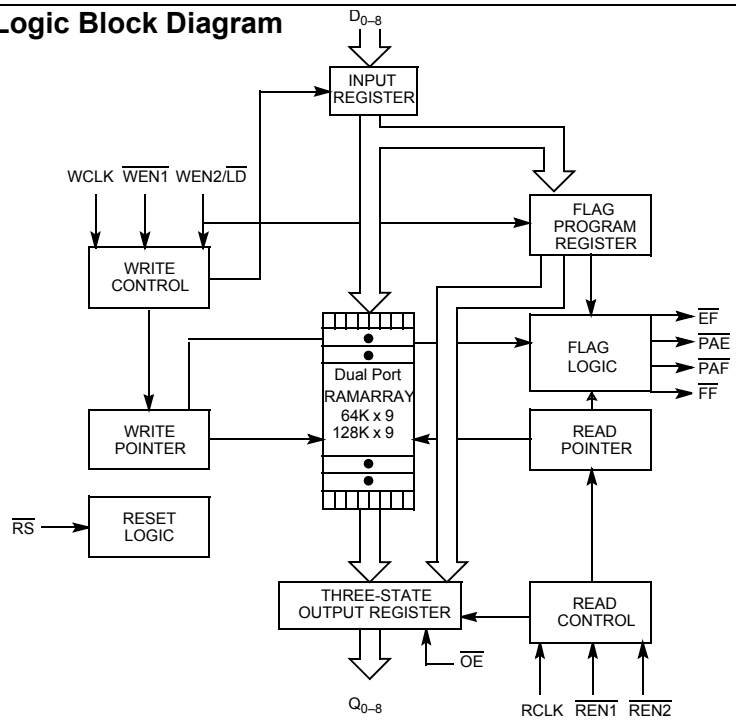
Functional Description

The CY7C4281/91 are high-speed, low-power FIFO memories with clocked read and write interfaces. All are nine bits wide. The CY7C4281/91 are pin-compatible to the CY7C42X1 Synchronous FIFO family. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

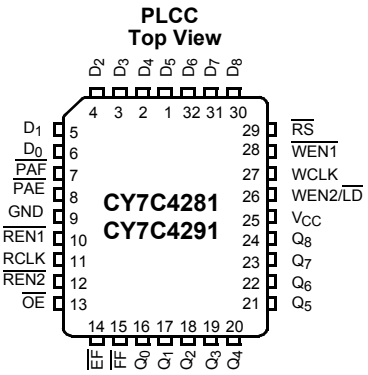
These FIFOs have nine-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C4281/91 has an output enable pin ($\overline{OE}$). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable. Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pin Configuration



Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	**Data Inputs for 9-bit bus**.
Q_{0-8}	Data Outputs	O	**Data Outputs for 9-bit bus**.
$\overline{WEN1}$	Write Enable 1	I	**The only write enable when device is configured to have programmable flags**. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2 Load	I	**If HIGH at reset, this pin operates as a second write enable**. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	**Enables the device for Read operation**. Both $\overline{REN1}$ and $\overline{REN2}$ must be asserted to allow a read operation.
WCLK	Write Clock	I	**The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full**. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	**The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty**. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	**When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK**.
$\overline{FF}$	Full Flag	O	**When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK**.
$\overline{PAE}$	Programmable Almost Empty	O	**When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO**. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost Full	O	**When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO**. $\overline{PAF}$ is synchronized to WCLK.
$\overline{RS}$	Reset	I	**Resets device to empty condition**. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	**When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected**. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

	CY7C4281	CY7C4291
Density	64k x 9	128k x 9
Package	32-pin PLCC	32-pin PLCC

Selection Guide

		7C4281/91-10	7C4281/91-15	7C4281/91-25	Unit
Maximum Frequency		100	66.7	40	MHz
Maximum Access Time		8	10	15	ns
Minimum Cycle Time		10	15	25	ns
Minimum Data or Enable Set-up		3	4	6	ns
Minimum Data or Enable Hold		0.5	1	1	ns
Maximum Flag Delay		8	10	15	ns
Active Power Supply Current (I_{CC1})	Commercial	40	40	40	mA
	Industrial	45			

Functional Description (continued)

The CY7C4281/91 provides four status pins: Empty, Full, Programmable Almost Empty, and Programmable Almost Full. The Almost Empty/Almost Full flags are programmable to single-word granularity. The programmable flags default to Empty+7 and Full-7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

All configurations are fabricated using an advanced 0.5μ CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Architecture

The CY7C4281/91 consists of an array of 64K to 128K words of nine bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, $\overline{\text{WEN1}}$, $\overline{\text{WEN2}}$, $\overline{\text{RS}}$), and flags ($\overline{\text{EF}}$, $\overline{\text{PAE}}$, $\overline{\text{PAF}}$, $\overline{\text{FF}}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{\text{RS}}$) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{\text{RS}}$. In order for the FIFO to reset to its default state, the user must not read or write while $\overline{\text{RS}}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{\text{RS}}$ is taken LOW.

FIFO Operation

When the $\overline{\text{WEN1}}$ signal is active LOW, WEN2 is active HIGH, and $\overline{\text{FF}}$ is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ signals are active LOW and $\overline{\text{EF}}$ is active HIGH, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are active. $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{\text{WEN1}}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{\text{OE}}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{\text{OE}}$ is asserted. When $\overline{\text{OE}}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{\text{OE}}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 ($\overline{\text{WEN1}}$) — If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{\text{WEN1}}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{\text{WEN1}}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{\text{LD}}$) — This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{\text{LD}}$) is set active HIGH at Reset ($\overline{\text{RS}}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{\text{WEN1}}$) is LOW and Write Enable 2/Load (WEN2/$\overline{\text{LD}}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{\text{LD}}$ is held LOW during Reset, this pin is the load ($\overline{\text{LD}}$) enable for flag offset programming. In this configuration, WEN2/$\overline{\text{LD}}$ can be used to access the four nine-bit offset registers contained in the CY7C4281/4291 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

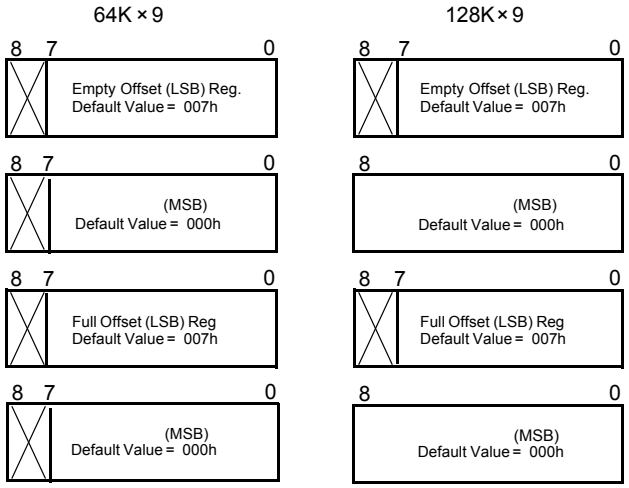


Figure 1. Offset Register Location and Default Values

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/LD input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/LD is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/LD is LOW and both REN1 and REN2 are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

Programmable Flag (PAE, PAF) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag (PAE) and programmable almost-full flag (PAF) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

LD	WEN	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as n and determines the operation of PAE. PAF is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. PAE is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n + 1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as m and determines the operation of PAF. PAE is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4281 (64K-m) and CY7C4291 (128K-m). PAF is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO					
CY7C4281	CY7C4291	FF	PAF	PAE	EF
0	0	H	H	L	L
1 to n[2]	1 to n[2]	H	H	L	H
(n+1) to (65536 – (m+1))	(n+1) to (131072–(m+1))	H	H	H	H
(65536 – m)[3] to 65535	131072 – m)[3] to 131071	H	L	H	H
65536	131072	L	L	H	H

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags (EF and FF). The partial status flags (PAE and PAF) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable (REN2) control input can be grounded (see *Figure 2*). In this configuration, the Write Enable 2/Load (WEN2/LD) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C4281/91 devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

Full Flag

The Full Flag (FF) will go LOW when the device is full. Write operations are inhibited whenever FF is LOW regardless of the state of WEN1 and WEN2/LD. FF is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag (EF) will go LOW when the device is empty. Read operations are inhibited whenever EF is LOW, regardless of the state of REN1 and REN2. EF is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Note:
1. The same selection sequence applies to reading from the registers. REN1 and REN2 are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n = 7 default value).
3. m = Full Offset (m = 7 default value).

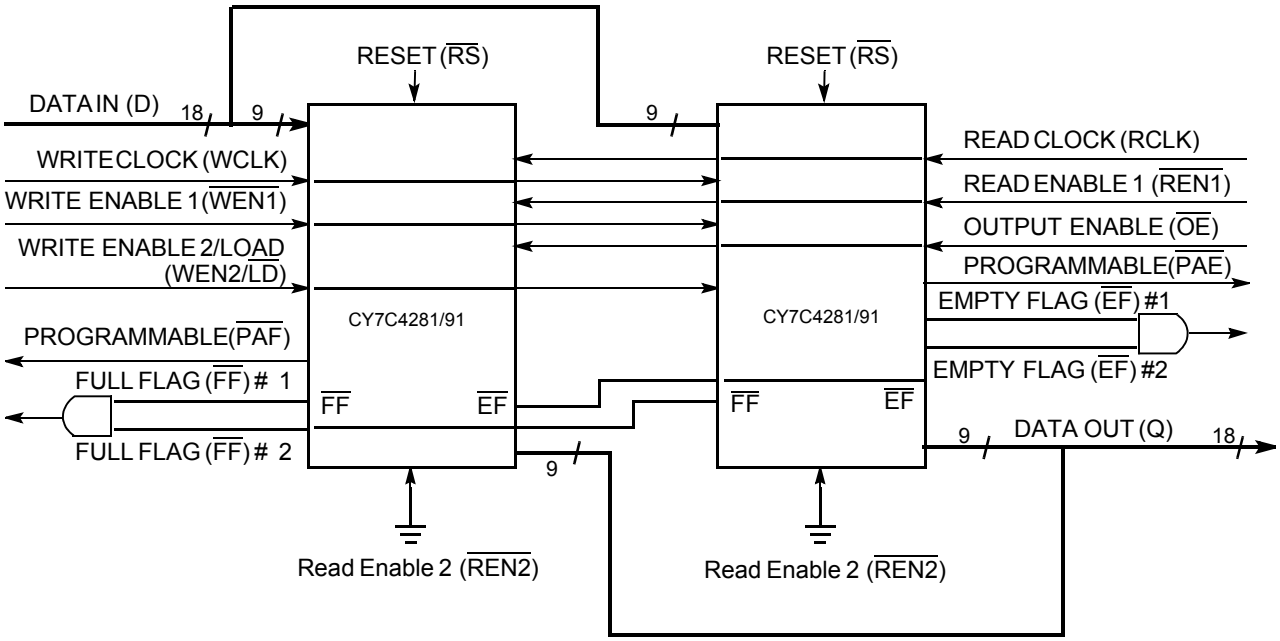


Figure 2. Block Diagram of 64k x 9/128k x 9 Deep Sync FIFO Memory Used in a Width Expansion Configuration

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range[4]

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[5]	–40°C to +85°C	5V ± 10%

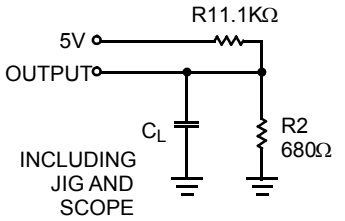
Electrical Characteristics Over the Operating Range

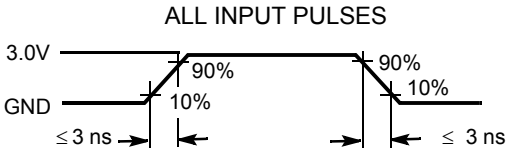
Parameter	Description	Test Conditions		7C42X1–10		7C42X1–15		7C42X1–25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	μA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	μA
I_{CC1}[6]	Active Power Supply Current		Com'l		40		40		40	mA
			Ind		45		45		45	mA
I_{SB}[7]	Average Standby Current		Com'l		2		2		2	mA
			Ind		2					mA

Capacitance[8]

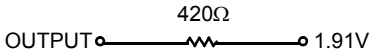
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[9, 10]





Equivalent to: THÉVENIN EQUIVALENT



Notes:

4. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
5. T_A is the "instant on" case temperature.
6. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded. Icc1(typical) = (20 mA + (freq – 20 MHz)*(0.7 mA/MHz)).
7. All inputs = V_{CC} – 0.2V, except WCLK and RCLK (which are at frequency = 0 MHz). All outputs are unloaded.
8. Tested initially and after any design or process changes that may affect these parameters.
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.

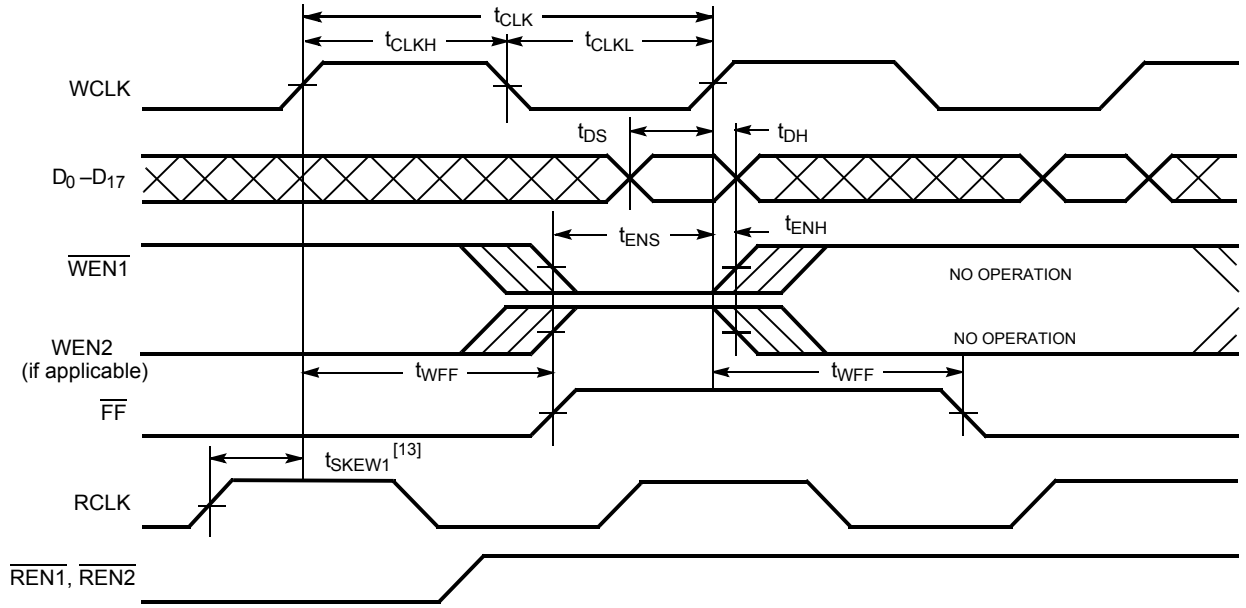
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1-10		7C42X1-15		7C42X1-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40	MHz
t_A	Data Access Time	2	8	2	10	2	15	ns
t_{CLK}	Clock Cycle Time	10		15		25		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		ns
t_{DS}	Data Set-up Time	3		4		6		ns
t_{DH}	Data Hold Time	0.5		1		1		ns
t_{ENS}	Enable Set-up Time	3		4		6		ns
t_{ENH}	Enable Hold Time	0.5		1		1		ns
t_{RS}	Reset Pulse Width[11]	10		15		25		ns
t_{RSS}	Reset Set-up Time	8		10		15		ns
t_{RSR}	Reset Recovery Time	8		10		15		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25	ns
t_{OLZ}	Output Enable to Output in Low Z[12]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	ns
t_{OHZ}	Output Enable to Output in High Z[12]	3	7	3	8	3	12	ns
t_{WFF}	Write Clock to Full Flag		8		10		15	ns
t_{REF}	Read Clock to Empty Flag		8		10		15	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	10		15		18		ns

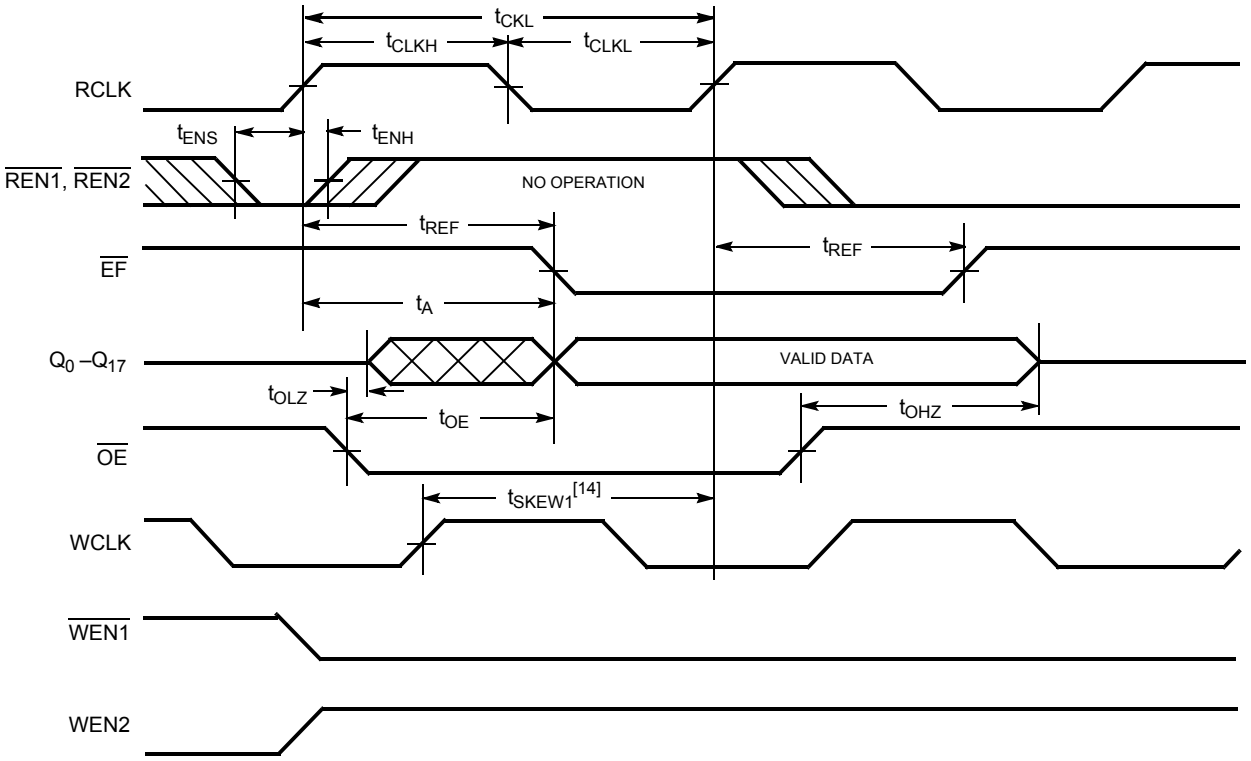
Notes:
11. Pulse widths less than minimum values are not allowed.
12. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

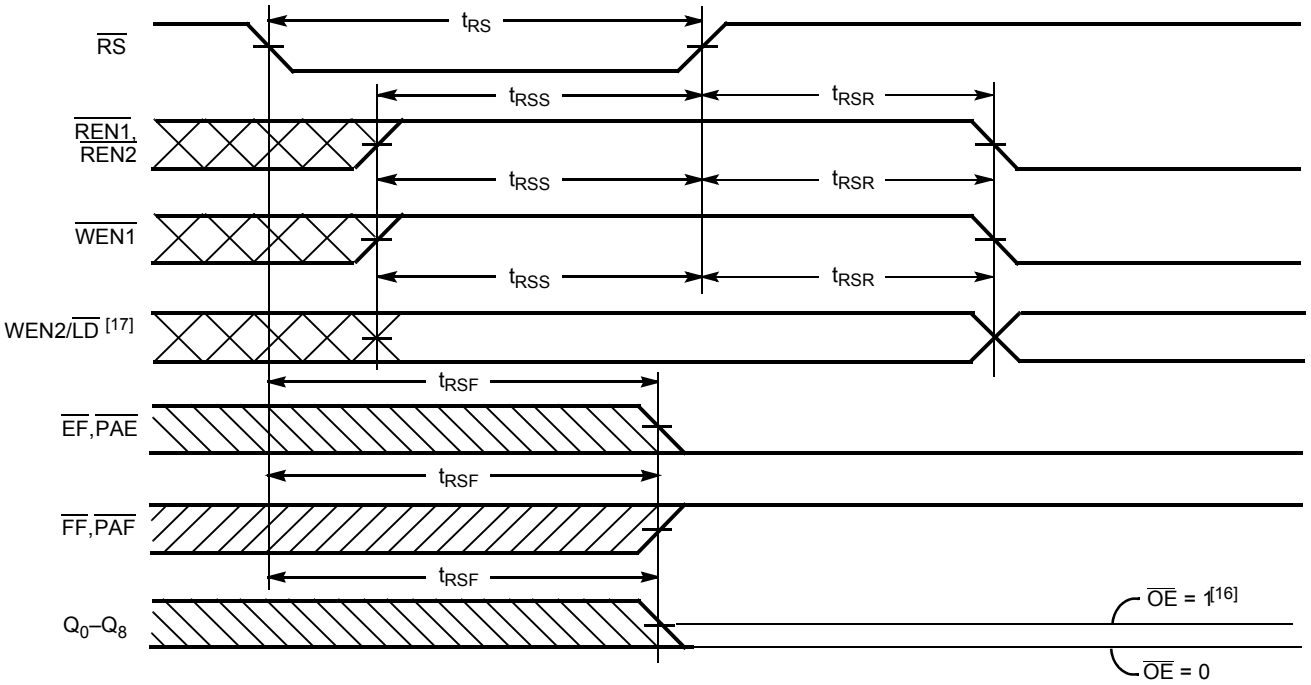


Notes:

13. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
14. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

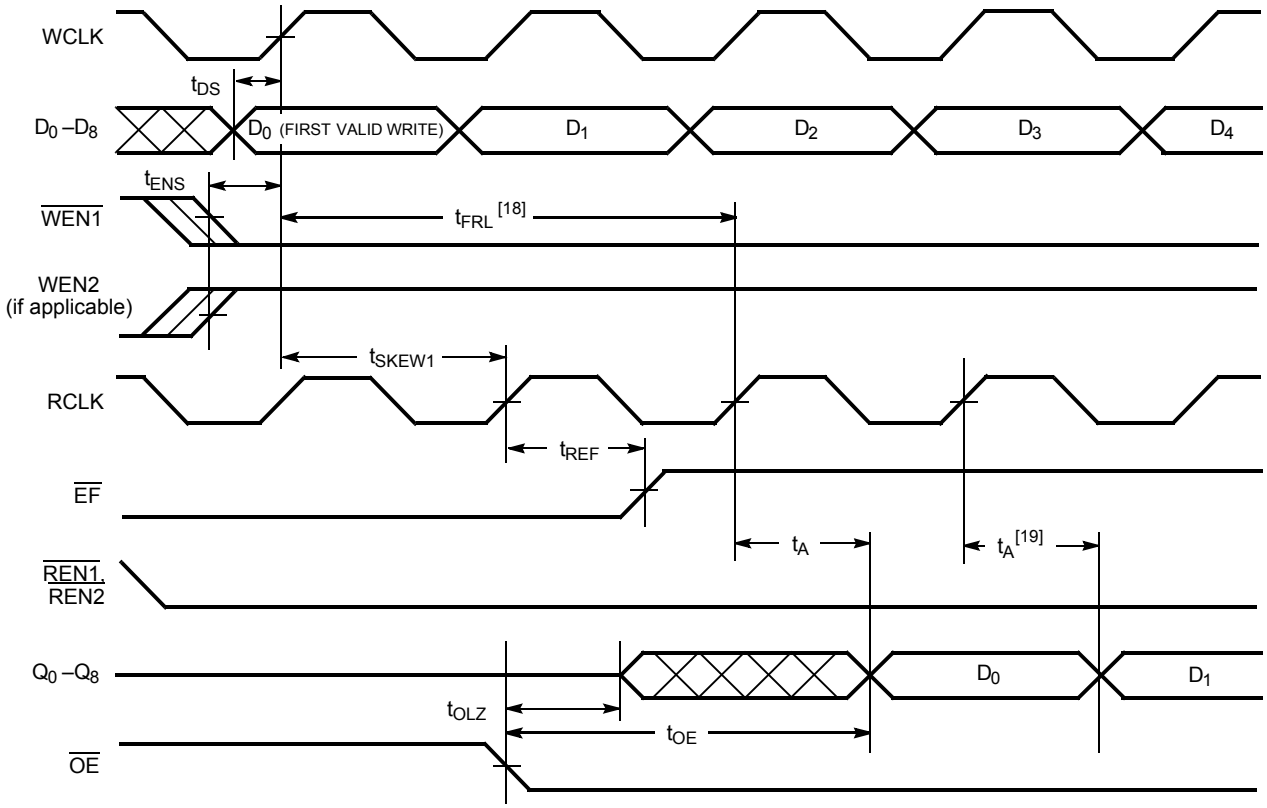
Reset Timing[15]



Notes:
15. The clocks (RCLK, WCLK) can be free-running during reset.
16. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
17. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)

First Data Word Latency after Reset with Read and Write

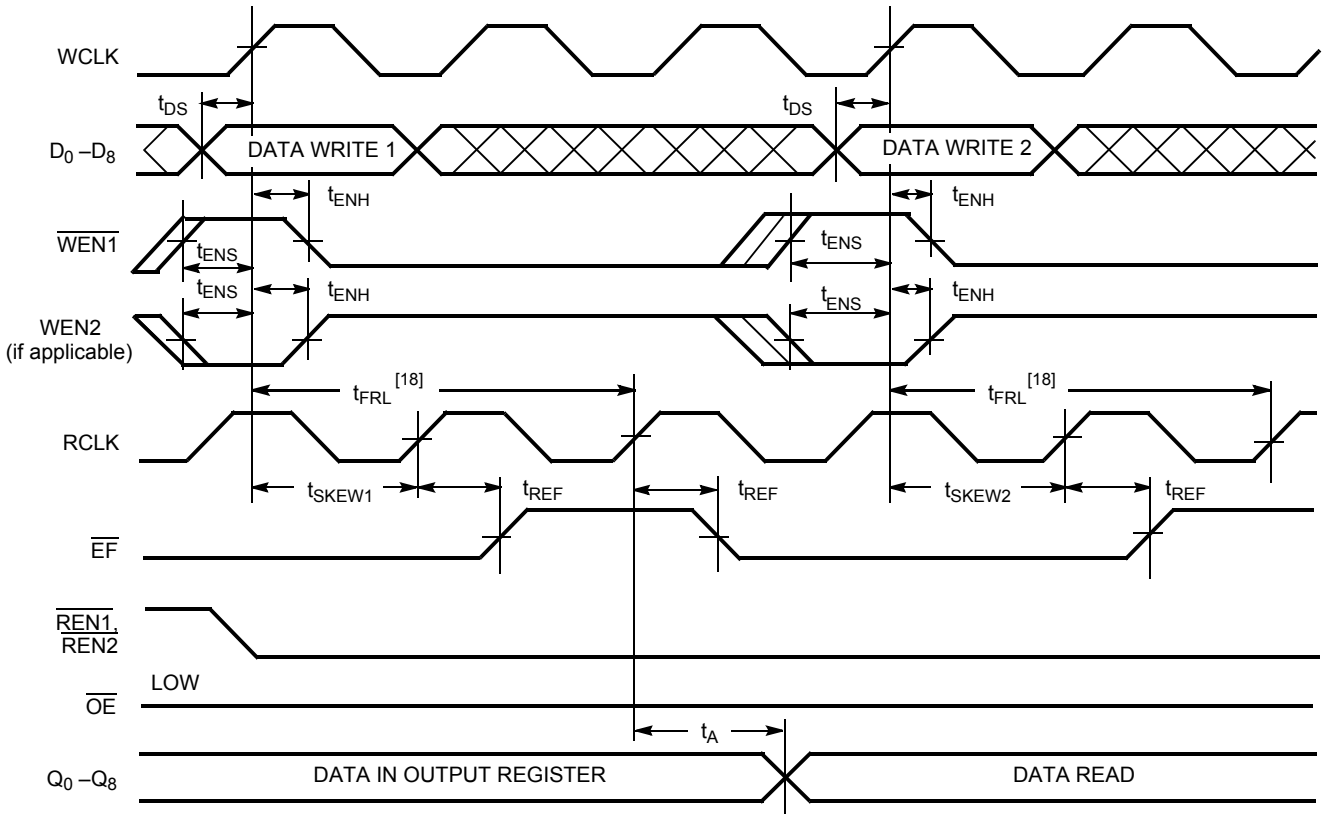


Notes:

18. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
19. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

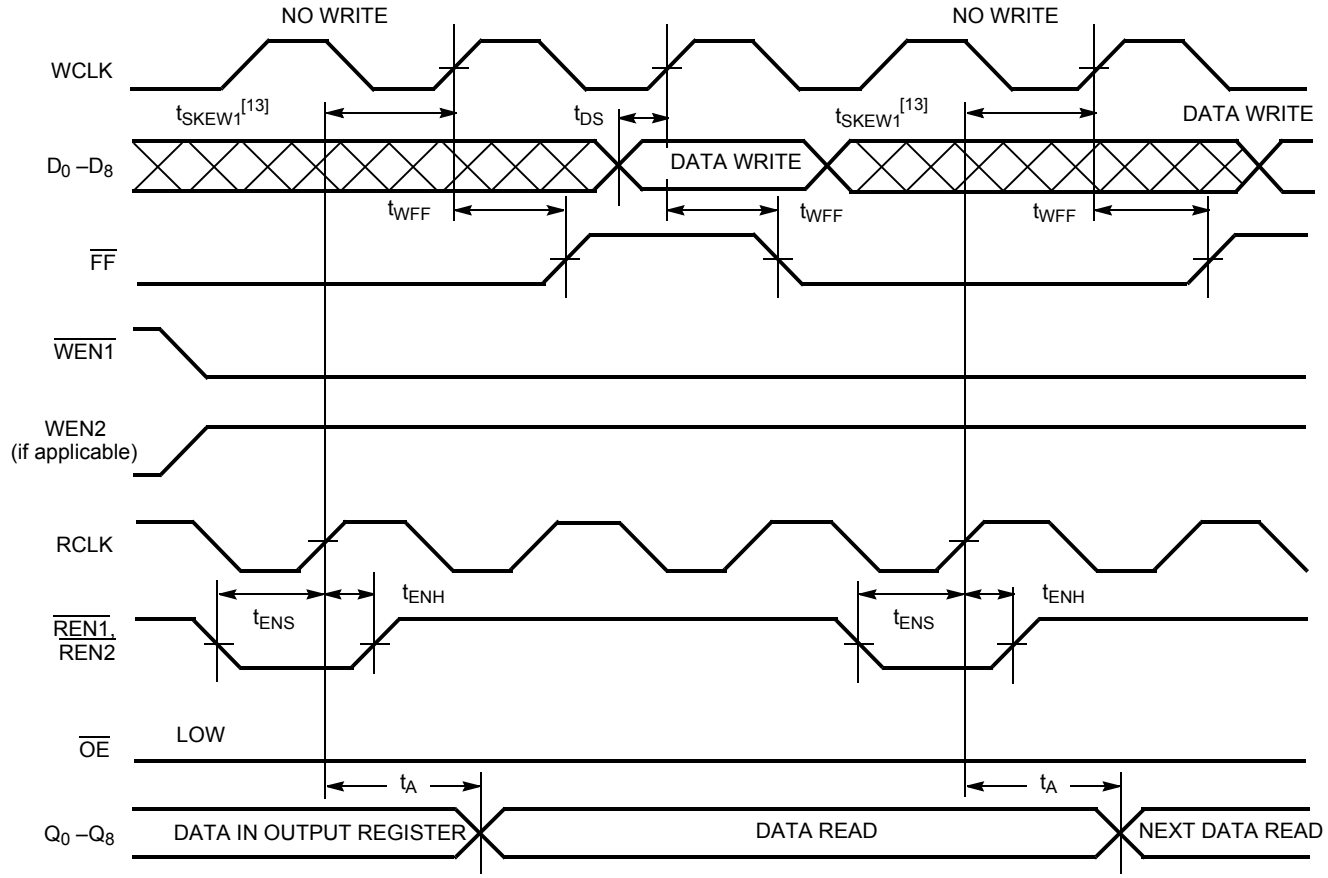
Switching Waveforms (continued)

Empty Flag Timing

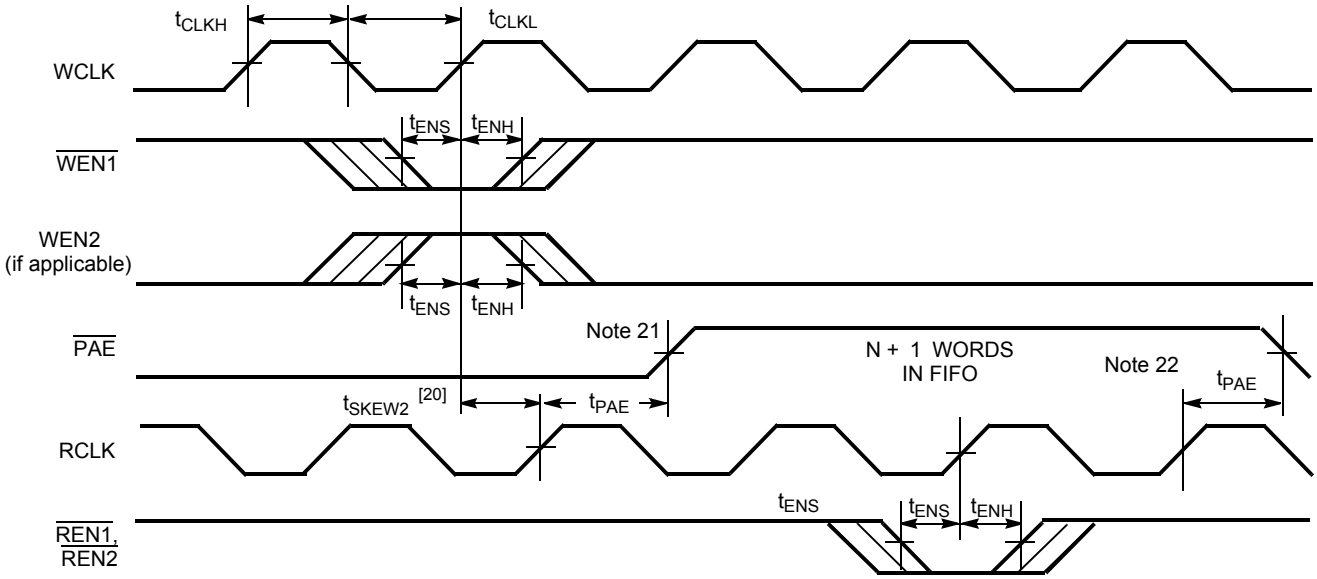


Switching Waveforms (continued)

Full Flag Timing



Programmable Almost Empty Flag Timing

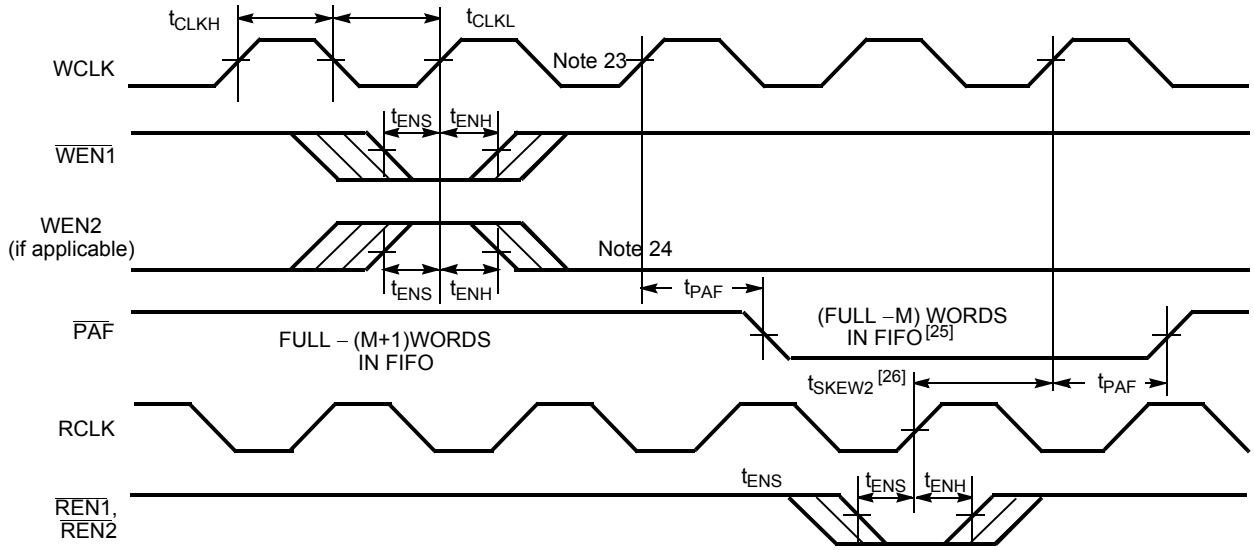


Notes:

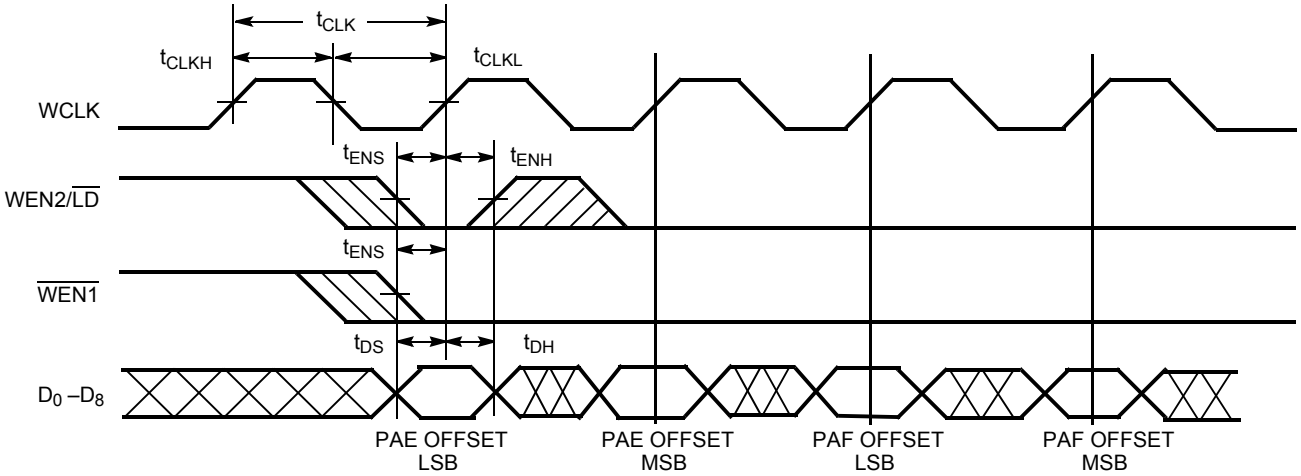
20. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
21. PAE offset = n.
22. If a read is performed on this rising edge of the read clock, there will be Empty + (n –1) words in the FIFO when $\overline{PAE}$ goes LOW.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing



Write Programmable Registers

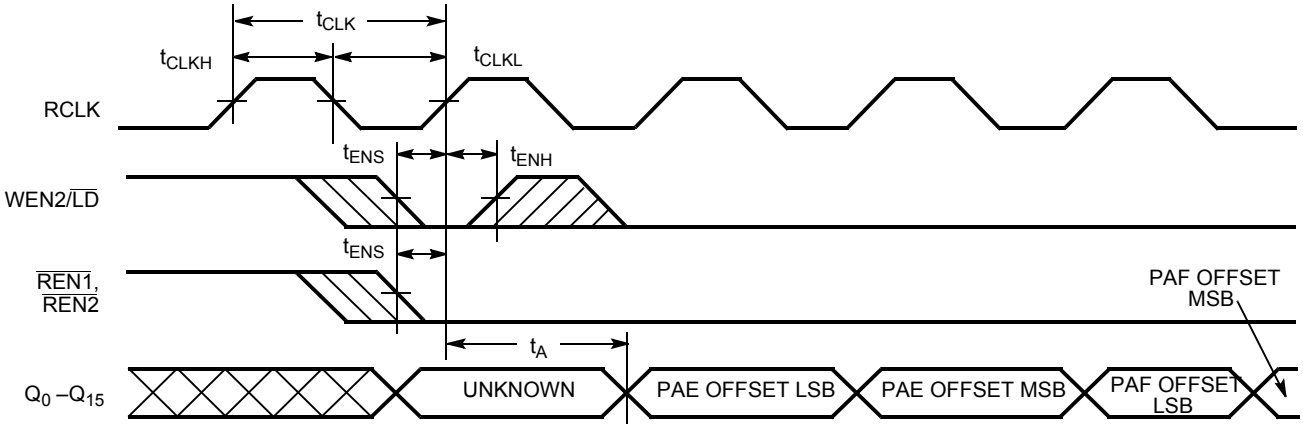


Notes:

23. If a write is performed on this rising edge of the write clock, there will be Full – (m – 1) words of the FIFO when $\overline{PAF}$ goes LOW.
24. PAF offset = m.
25. 16,384 – m words for CY7C4281, 32,768 – m words for CY4291.
26. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

Read Programmable Registers



Ordering Information

64K x 9 Deep Sync FIFO

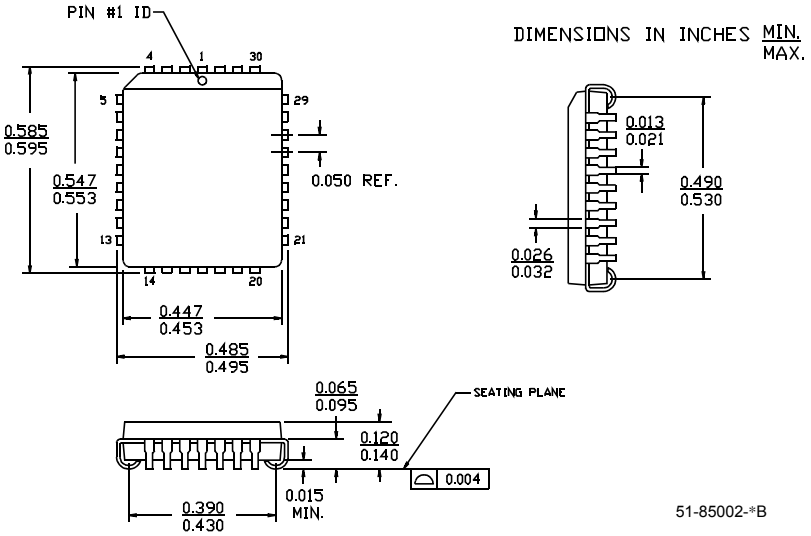
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4281-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4281-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C4281-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7C4281-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

128K x 9 Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4291-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4291-10JXC	J65	32-Lead Pb-Free Plastic Leaded Chip Carrier	Commercial
	CY7C4291-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C4291-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4291-15JXC	J65	32-Lead Pb-Free Plastic Leaded Chip Carrier	Commercial
25	CY7C4291-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

Package Diagrams

32-Lead Plastic Leaded Chip Carrier J65
32-Lead Pb-Free Plastic Leaded Chip Carrier J65



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Document History Page

Document Title: CY7C4281, CY7C4291 64K/128K X 9 Deep Sync FIFOs Document Number: 38-06007				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106468	07/12/01	SZV	Change from Spec number: 38-00587 to 38-06007
*A	122259	12/26/02	RBI	Power up requirements added to Operating Range Information
*B	127854	08/22/03	FSG	Removed Preliminary Fixed empty flag timing diagram Switching waveform diagram typo fixed
*C	386004	See ECN	ESH	Added Pb-Free logo to top of front page Added CY7C4291-10JXC, CY7C4291-15JXC to ordering information

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