

Features

- ☐ High-performance CMOS non-volatile static RAM 32768 x 8 bits
- ☐ 25, 35 and 45 ns Access Times
- ☐ 10, 15 and 20 ns Output Enable Access Times
- ☐ $I_{CC} = 15 \text{ mA}$ at 200 ns Cycle Time
- ☐ Automatic STORE to EEPROM on Power Down using system capacitance
- ☐ Software initiated STORE
- ☐ Automatic STORE Timing
- ☐ 10^5 STORE cycles to EEPROM
- ☐ 10 years data retention in EEPROM
- ☐ Automatic RECALL on Power Up
- ☐ Software RECALL Initiation
- ☐ Unlimited RECALL cycles from EEPROM
- ☐ Single $5 \text{ V} \pm 10 \%$ Operation
- ☐ Operating temperature range:
0 to 70 °C
-40 to 85 °C
- ☐ CECC 90000 Quality Standard
- ☐ ESD characterization according MIL STD 883C M3015.7-HB (classification see IC Code Numbers)
- ☐ Packages: PDIP28 (300 mil)
PDIP28 (600 mil)
SOP28 (330 mil)

Description

The U635H256 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U635H256 is a fast static RAM (25, 35, 45 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in system capacitance. Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on power up. The U635H256 combines the high per-

formance and ease of use of a fast SRAM with nonvolatile data integrity.

STORE cycles also may be initiated under user control via a software sequence.

Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted.

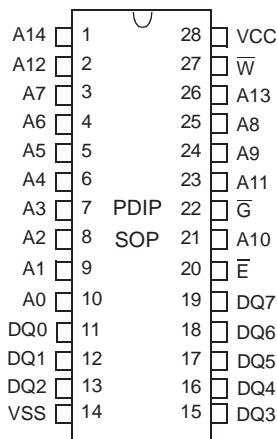
RECALL cycles may also be initiated by a software sequence.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

The U635H256 is pin compatible with standard SRAMs.

Pin Configuration



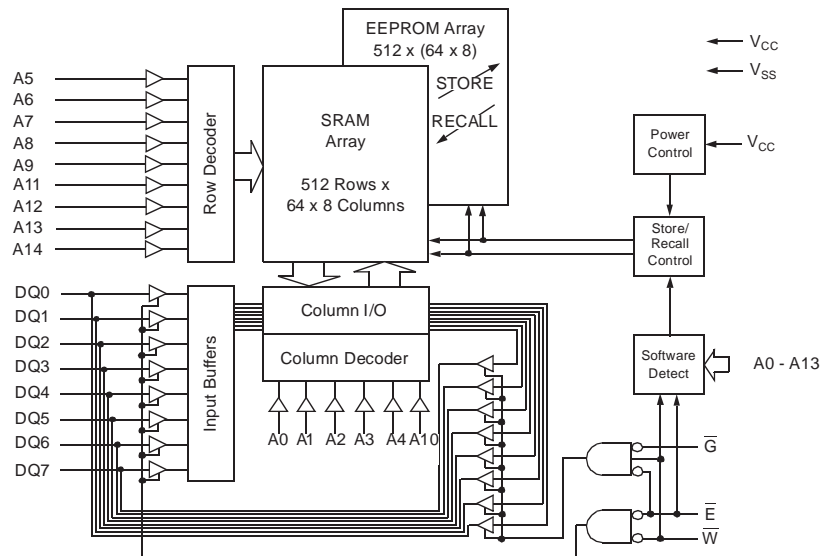
Top View

Pin Description

| Signal Name | Signal Description |
|-------------|----------------------|
| A0 - A14 | Address Inputs |
| DQ0 - DQ7 | Data In/Out |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{W} | Write Enable |
| VCC | Power Supply Voltage |
| VSS | Ground |

U635H256

Block Diagram



Truth Table for SRAM Operations

| Operating Mode | \bar{E} | \bar{W} | \bar{G} | DQ0 - DQ7 |
|----------------------|-----------|-----------|-----------|--------------------|
| Standby/not selected | H | * | * | High-Z |
| Internal Read | L | H | H | High-Z |
| Read | L | H | L | Data Outputs Low-Z |
| Write | L | L | * | Data Inputs High-Z |

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0$ V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I , as well as input levels of $V_{IL} = 0$ V and $V_{IH} = 3$ V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis} -times and t_{en} -times, in which cases transition is measured ± 200 mV from steady-state voltage.

| Absolute Maximum Ratings ^a | Symbol | Min. | Max. | Unit |
|---------------------------------------|-----------|----------|--------------|----------|
| Power Supply Voltage | V_{CC} | -0.5 | 7 | V |
| Input Voltage | V_I | -0.3 | $V_{CC}+0.5$ | V |
| Output Voltage | V_O | -0.3 | $V_{CC}+0.5$ | V |
| Power Dissipation | P_D | | 1 | W |
| Operating Temperature | T_a | 0 -40 | 70 85 | °C °C |
| Storage Temperature | T_{stg} | -65 | 150 | °C |

a: Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Recommended Operating Conditions | Symbol | Conditions | Min. | Max. | Unit |
|----------------------------------|----------|--|------|--------------|------|
| Power Supply Voltage | V_{CC} | | 4.5 | 5.5 | V |
| Input Low Voltage | V_{IL} | -2 V at Pulse Width 10 ns permitted | -0.3 | 0.8 | V |
| Input High Voltage | V_{IH} | | 2.2 | $V_{CC}+0.3$ | V |

| DC Characteristics | Symbol | Conditions | C-Type | | K-Type | | Unit |
|--|---------------|--|--------|----------------|--------|-----------------|----------------|
| | | | Min. | Max. | Min. | Max. | |
| Operating Supply Current ^b | I_{CC1} | $V_{CC} = 5.5 \text{ V}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2.2 \text{ V}$ $t_c = 25 \text{ ns}$ $t_c = 35 \text{ ns}$ $t_c = 45 \text{ ns}$ | | 95 75 65 | | 100 80 70 | mA mA mA |
| Average Supply Current during ^c STORE | I_{CC2} | $V_{CC} = 5.5 \text{ V}$ $\overline{E} \leq 0.2 \text{ V}$ $\overline{W} \geq V_{CC}-0.2 \text{ V}$ $V_{IL} \leq 0.2 \text{ V}$ $V_{IH} \geq V_{CC}-0.2 \text{ V}$ | | 6 | | 7 | mA |
| Operating Supply Current ^b at $t_{CR} = 200 \text{ ns}$ (Cycling CMOS Input Levels) | I_{CC3} | $V_{CC} = 5.5 \text{ V}$ $\overline{W} \geq V_{CC}-0.2 \text{ V}$ $V_{IL} \leq 0.2 \text{ V}$ $V_{IH} \geq V_{CC}-0.2 \text{ V}$ | | 15 | | 15 | mA |
| Average Supply Current during ^c PowerStore Cycle | I_{CC4} | $V_{CC} = 4.5 \text{ V}$ $V_{IL} = 0.2 \text{ V}$ $V_{IH} \geq V_{CC}-0.2 \text{ V}$ | | 4 | | 4 | mA |
| Standby Supply Current ^d (Cycling TTL Input Levels) | $I_{CC(SB)1}$ | $V_{CC} = 5.5 \text{ V}$ $\overline{E} = V_{IH}$ $t_c = 25 \text{ ns}$ $t_c = 35 \text{ ns}$ $t_c = 45 \text{ ns}$ | | 40 36 33 | | 42 38 35 | mA mA mA |
| Standby Supply Current ^d (Stable CMOS Input Levels) | $I_{CC(SB)}$ | $V_{CC} = 5.5 \text{ V}$ $\overline{E} \geq V_{CC}-0.2 \text{ V}$ $V_{IL} \leq 0.2 \text{ V}$ $V_{IH} \geq V_{CC}-0.2 \text{ V}$ | | 3 | | 3 | mA |

b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
The current I_{CC1} is measured for WRITE/READ - ratio of 1/2.

c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective STORE cycles.

d: Bringing $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table. The current $I_{CC(SB)1}$ is measured for WRITE/READ - ratio of 1/2.

| DC Characteristics | Symbol | Conditions | C-Type | | K-Type | | Unit |
|---|------------------------|---|--------|------|--------|------|--------------------------------|
| | | | Min. | Max. | Min. | Max. | |
| Output High Voltage Output Low Voltage | V_{OH} V_{OL} | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -4\text{ mA}$ $I_{OL} = 8\text{ mA}$ | 2.4 | 0.4 | 2.4 | 0.4 | V V |
| Output High Current Output Low Current | I_{OH} I_{OL} | $V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$ $V_{OL} = 0.4\text{ V}$ | 8 | -4 | 8 | -4 | mA mA |
| Input Leakage Current High Low | I_{IH} I_{IL} | $V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$ | -1 | 1 | -1 | 1 | μA μA |
| Output Leakage Current High at Three-State- Output Low at Three-State- Output | I_{OHZ} I_{OLZ} | $V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$ | -1 | 1 | -1 | 1 | μA μA |

SRAM MEMORY OPERATIONS

| No. | Switching Characteristics Read Cycle | Symbol | | 25 | | 35 | | 45 | | Unit |
|-----|--|--------------|--------------|------|------|------|------|------|------|------|
| | | Alt. | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | Read Cycle Time ^f | t_{AVAV} | t_{cR} | 25 | | 35 | | 45 | | ns |
| 2 | Address Access Time to Data Valid ^g | t_{AVQV} | $t_{a(A)}$ | | 25 | | 35 | | 45 | ns |
| 3 | Chip Enable Access Time to Data Valid | t_{ELQV} | $t_{a(E)}$ | | 25 | | 35 | | 45 | ns |
| 4 | Output Enable Access Time to Data Valid | t_{GLQV} | $t_{a(G)}$ | | 10 | | 15 | | 20 | ns |
| 5 | \overline{E} HIGH to Output in High-Z ^h | t_{EHQZ} | $t_{dis(E)}$ | | 10 | | 13 | | 15 | ns |
| 6 | \overline{G} HIGH to Output in High-Z ^h | t_{GHQZ} | $t_{dis(G)}$ | | 10 | | 13 | | 15 | ns |
| 7 | \overline{E} LOW to Output in Low-Z | t_{ELQX} | $t_{en(E)}$ | 5 | | 5 | | 5 | | ns |
| 8 | \overline{G} LOW to Output in Low-Z | t_{GLQX} | $t_{en(G)}$ | 0 | | 0 | | 0 | | ns |
| 9 | Output Hold Time after Address Change | t_{AXQX} | $t_{v(A)}$ | 3 | | 3 | | 3 | | ns |
| 10 | Chip Enable to Power Active ^e | t_{ELICCH} | t_{PU} | 0 | | 0 | | 0 | | ns |
| 11 | Chip Disable to Power Standby ^{d, e} | t_{EHICCL} | t_{PD} | | 25 | | 35 | | 45 | ns |

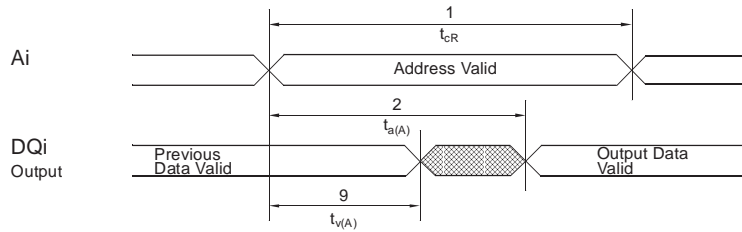
e: Parameter guaranteed but not tested.

f: Device is continuously selected with \overline{E} and \overline{G} both Low.

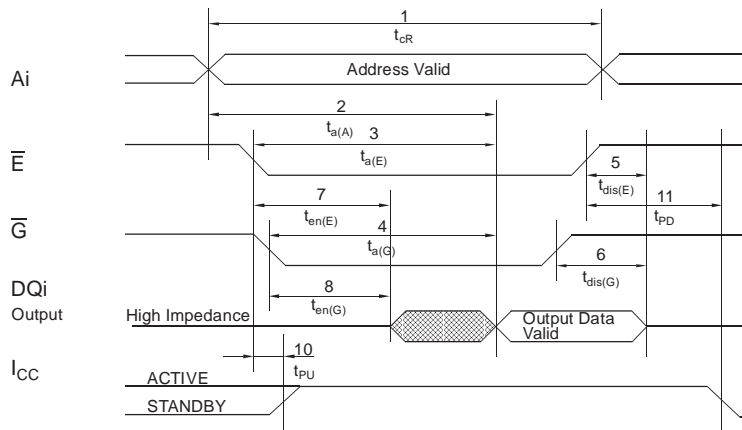
g: Address valid prior to or coincident with \overline{E} transition LOW.

h: Measured $\pm 200\text{ mV}$ from steady state output voltage.

Read Cycle 1: Ai-controlled (during Read cycle: $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)^f

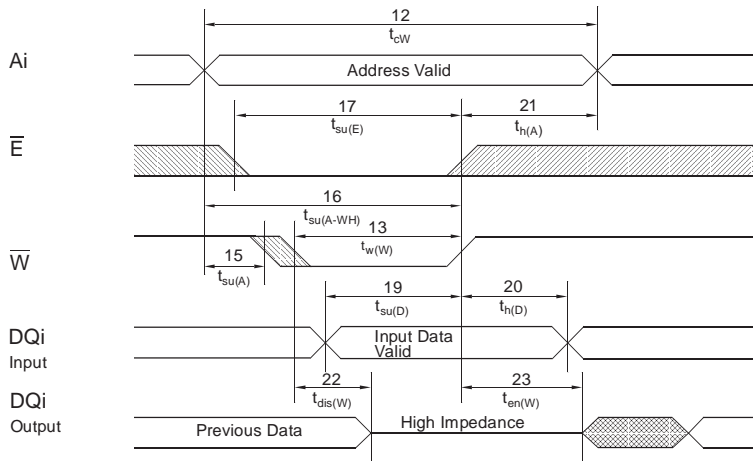


Read Cycle 2: \overline{G} -, \overline{E} -controlled (during Read cycle: $\overline{W} = V_{IH}$)^g

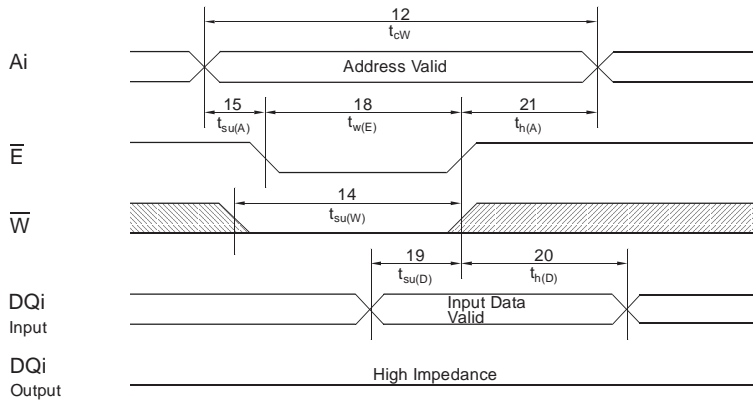


| No. | Switching Characteristics Write Cycle | Symbol | | | 25 | | 35 | | 45 | | Unit |
|-----|--|------------|------------|----------------|------|------|------|------|------|------|------|
| | | Alt. #1 | Alt. #2 | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 12 | Write Cycle Time | t_{AVAV} | t_{AVAV} | t_{cW} | 25 | | 35 | | 45 | | ns |
| 13 | Write Pulse Width | t_{WLWH} | | $t_{w(W)}$ | 20 | | 25 | | 30 | | ns |
| 14 | Write Pulse Width Setup Time | | t_{WLEH} | $t_{su(W)}$ | 20 | | 25 | | 30 | | ns |
| 15 | Address Setup Time | t_{AVWL} | t_{AVEL} | $t_{su(A)}$ | 0 | | 0 | | 0 | | ns |
| 16 | Address Valid to End of Write | t_{AVWH} | t_{AVEH} | $t_{su(A-WH)}$ | 20 | | 25 | | 30 | | ns |
| 17 | Chip Enable Setup Time | t_{ELWH} | | $t_{su(E)}$ | 20 | | 25 | | 30 | | ns |
| 18 | Chip Enable to End of Write | | t_{ELEH} | $t_{w(E)}$ | 20 | | 25 | | 30 | | ns |
| 19 | Data Setup Time to End of Write | t_{DVWH} | t_{DVEH} | $t_{su(D)}$ | 10 | | 12 | | 15 | | ns |
| 20 | Data Hold Time after End of Write | t_{WHDx} | t_{EHDx} | $t_{h(D)}$ | 0 | | 0 | | 0 | | ns |
| 21 | Address Hold after End of Write | t_{WHAX} | t_{EHAX} | $t_{h(A)}$ | 0 | | 0 | | 0 | | ns |
| 22 | \overline{W} LOW to Output in High-Z ^{h, i} | t_{WLQZ} | | $t_{dis(W)}$ | | 10 | | 13 | | 15 | ns |
| 23 | \overline{W} HIGH to Output in Low-Z | t_{WHQX} | | $t_{en(W)}$ | 5 | | 5 | | 5 | | ns |

Write Cycle #1: \overline{W} -controlled^j



Write Cycle #2: \overline{E} -controlled^j



undefined  L- to H-level  H- to L-level 

i: If \overline{W} is low and when \overline{E} goes low, the outputs remain in the high impedance state.

j: \overline{E} or \overline{W} must be V_{IH} during address transition.

NONVOLATILE MEMORY OPERATIONS

MODE SELECTION

| \bar{E} | \bar{W} | A13 - A0 (hex) | Mode | I/O | Power | Notes |
|-----------|-----------|--|---|--|---------|--|
| H | X | X | Not Selected | Output High Z | Standby | |
| L | H | X | Read SRAM | Output Data | Active | m |
| L | L | X | Write SRAM | Input Data | Active | |
| L | H | 0E38 31C7 03E0 3C1F 303F 0FC0 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE | Output Data Output Data Output Data Output Data Output Data Output High Z | Active | k, l k, l k, l k, l k, l k, l |
| L | H | 0E38 31C7 03E0 3C1F 303F 0C63 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL | Output Data Output Data Output Data Output Data Output Data Output High Z | Active | k, l k, l k, l k, l k, l k, l |

k: The six consecutive addresses must be in order listed. \bar{W} must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.

The following six-address sequence is used for testing purposes and should not be used: 0E38, 31C7, 03E0, 3C1F, 303F, 339C.

l: While there are 15 addresses on the U635H256, only the lower 14 are used to control software modes.

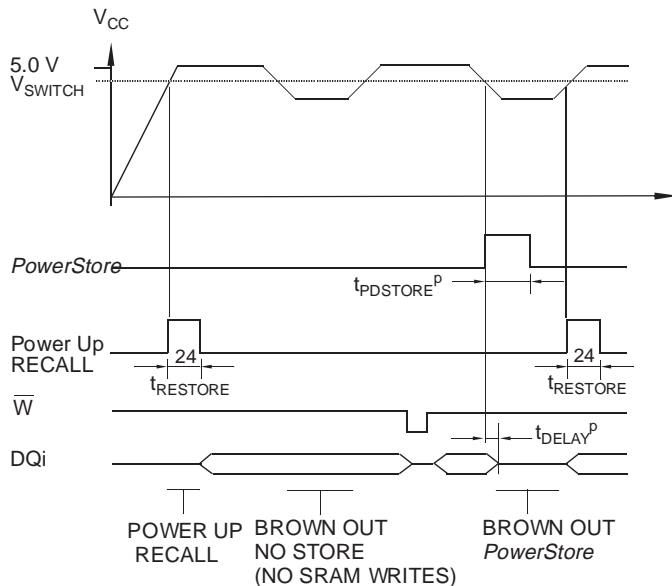
Activation of nonvolatile cycles does not depend on the state of \bar{G} .

m: I/O state assumes that $\bar{G} \leq V_{IL}$.

| No. | PowerStore Power Up RECALL | Symbol | | Conditions | Min. | Max. | Unit |
|-----|--|----------------------|-----|---|------|------|---------------|
| | | Alt. | IEC | | | | |
| 24 | Power Up RECALL Duration ⁿ | t_{RESTORE} | | | | 650 | μs |
| 25 | STORE Cycle Duration ^{f, e} | t_{PDSTORE} | | the power supply voltage must be stay above 3.6 V for at least 10 ms after the start of the STORE operation | | 10 | ms |
| 26 | Time allowed to Complete SRAM Cycle ^f | t_{DELAY} | | | 1 | | μs |
| | Low Voltage Trigger Level | V_{SWITCH} | | | 4.0 | 4.5 | V |

n: t_{RESTORE} starts from the time V_{CC} rises above V_{SWITCH} .

PowerStore and automatic Power Up RECALL



| No. | Software Controlled STORE/RECALL Cycle ^{k, o} | Symbol | | 25 | | 35 | | 45 | | Unit |
|-----|--|--------------------|-----------------------|------|------|------|------|------|------|------|
| | | Alt. | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 27 | STORE/RECALL Initiation Time | t _{AVAV} | t _{cR} | 25 | | 35 | | 45 | | ns |
| 28 | Chip Enable to Output Inactive ^p | t _{ELQZ} | t _{dis(E)SR} | | 600 | | 600 | | 600 | ns |
| 29 | STORE Cycle Time ^q | t _{ELQXS} | t _{d(E)S} | | 10 | | 10 | | 10 | ms |
| 30 | RECALL Cycle Time ^r | t _{ELQXR} | t _{d(E)R} | | 20 | | 20 | | 20 | μs |
| 31 | Address Setup to Chip Enable ^s | t _{AVELN} | t _{su(A)SR} | 0 | | 0 | | 0 | | ns |
| 32 | Chip Enable Pulse Width ^{s, t} | t _{ELEHN} | t _{w(E)SR} | 20 | | 25 | | 30 | | ns |
| 33 | Chip Disable to Address Change ^s | t _{EHAXN} | t _{h(A)SR} | 0 | | 0 | | 0 | | ns |

o: The software sequence is clocked with E controlled READs.

p: Once the software controlled STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

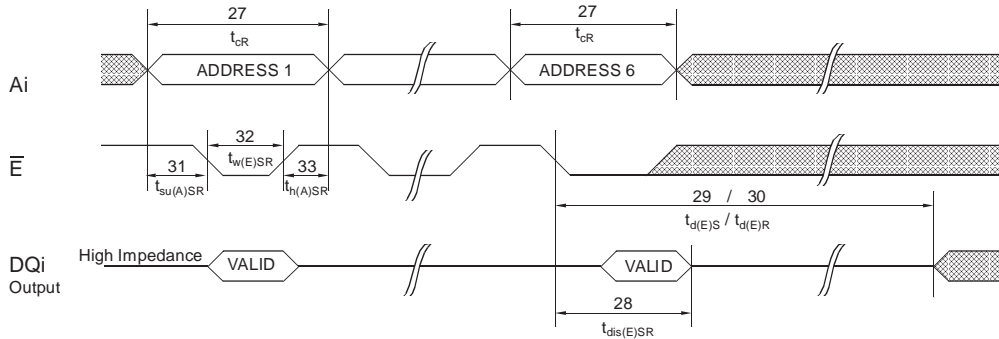
q: Note that STORE cycles (but not RECALL) are aborted by V_{CC} < V_{SWITCH} (STORE inhibit).

r: An automatic RECALL also takes place at power up, starting when V_{CC} exceeds V_{SWITCH} and takes t_{RESTORE}. V_{CC} must not drop below V_{SWITCH} once it has been exceeded for the RECALL to function properly.

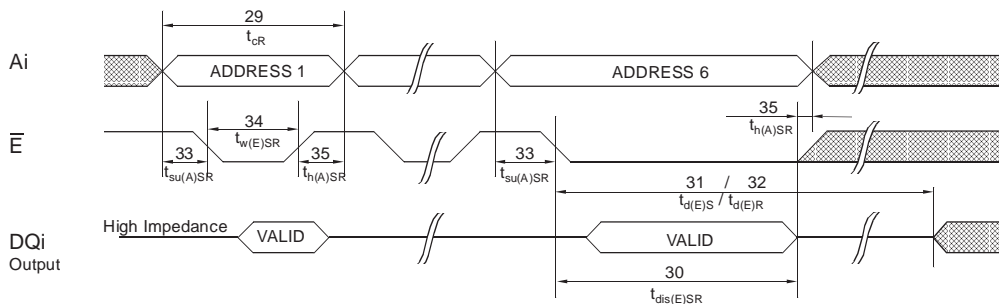
s: Noise on the E pin may trigger multiple READ cycles from the same address and abort the address sequence.

t: If the Chip Enable Pulse Width is less than t_{b(E)} (see Read Cycle) but greater than or equal t_{w(E)SR}, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

SOFTWARE CONTROLLED STORE/RECALL CYCLE^{t, u, v} (\bar{E} = HIGH after STORE initiation)



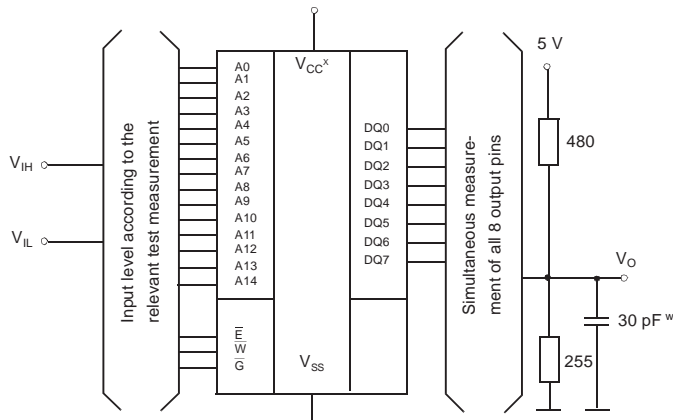
SOFTWARE CONTROLLED STORE/RECALL CYCLE^{t, u, v, w} (\bar{E} = LOW after STORE initiation)



u: \bar{W} must be HIGH when \bar{E} is LOW during the address sequence in order to initiate a nonvolatile cycle. \bar{G} may be either HIGH or LOW throughout. Addresses 1 through 6 are found in the mode selection table. Address 6 determines whether the U635H256 performs a STORE or RECALL.

v: \bar{E} must be used to clock in the address sequence for the Software controlled STORE and RECALL cycles.

Test Configuration for Functional Check



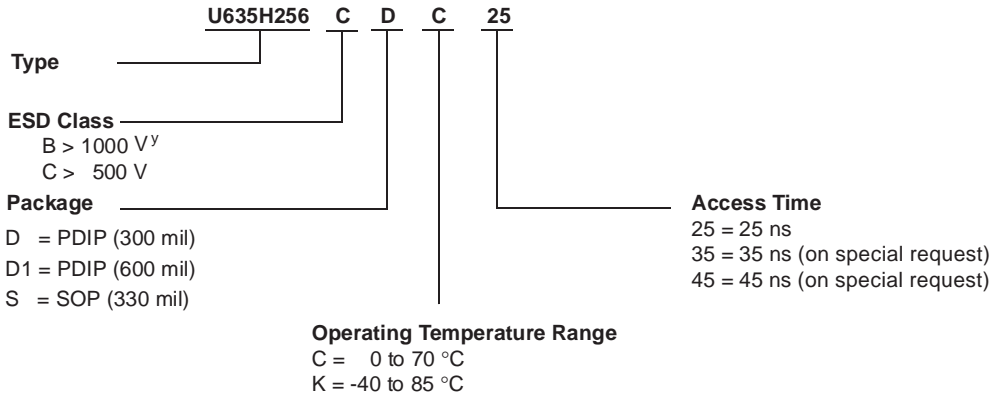
w: In measurement of t_{dls} -times and t_{en} -times the capacitance is 5 pF.
x: Between V_{CC} and V_{SS} must be connected a high frequency bypass capacitor 0.1 μ F to avoid disturbances.

| Capacitance ^e | Conditions | Symbol | Min. | Max. | Unit |
|--------------------------|--|--------|------|------|------|
| Input Capacitance | $V_{CC} = 5.0 \text{ V}$ $V_I = V_{SS}$ | C_I | | 8 | pF |
| Output Capacitance | $f = 1 \text{ MHz}$ $T_a = 25 \text{ }^\circ\text{C}$ | C_O | | 7 | pF |

All Pins not under test must be connected with ground by capacitors.

IC Code Numbers

Example



The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

y: ESD protection > 1000 V and 2000 V under development

Device Operation

The U635H256 has two separate modes of operation: SRAM mode and nonvolatile mode. The memory operates in SRAM mode as a standard fast static RAM. Data is transferred in nonvolatile mode from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH} . RECALL operations are automatically initiated upon power up and may also occur when the V_{CC} rises above V_{SWITCH} , after a low power condition. RECALL cycles may also be initiated by a software sequence.

SRAM READ

The U635H256 performs a READ cycle whenever \bar{E} and \bar{G} are LOW and \bar{W} is HIGH. The address specified on pins A0 - A14 determines which of the 32768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{CR} . If the READ is initiated by \bar{E} or \bar{G} , the outputs will be valid at $t_{\text{a(E)}}$ or at $t_{\text{a(G)}}$, whichever is later. The data outputs will repeatedly respond to address changes within the t_{CR} access time without the need for transition on any control input pins, and will remain valid until another address change or until \bar{E} or \bar{G} is brought HIGH or \bar{W} is brought LOW.

SRAM WRITE

A WRITE cycle is performed whenever \bar{E} and \bar{W} are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either \bar{E} or \bar{W} goes HIGH at the end of the cycle. The data on pins DQ0 - 7 will be written into the memory if it is valid $t_{\text{su(D)}}$ before the end of a \bar{W} controlled WRITE or $t_{\text{su(D)}}$ before the end of an \bar{E} controlled WRITE.

It is recommended that \bar{G} is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If \bar{G} is left LOW, internal circuitry will turn off the output buffers $t_{\text{dis(W)}}$ after \bar{W} goes LOW.

AUTOMATIC STORE

The U635H256 uses the intrinsic system capacitance to perform an automatic STORE on power down. As long as the system power supply take at least t_{PDSTORE} to decay from V_{SWITCH} down to 3.6 V the U635H256 will safely and automatically STORE the SRAM data in EEPROM on power down.

In order to prevent unneeded STORE operations, automatic STORE will be ignored unless at least one

WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

AUTOMATIC RECALL

During power up, an automatic RECALL takes place. At a low power condition (power supply voltage $< V_{\text{SWITCH}}$) an internal RECALL request may be latched. As soon as power supply voltage exceeds the sense voltage of V_{SWITCH} , a requested RECALL cycle will automatically be initiated and will take t_{RESTORE} to complete.

If the U635H256 is in a WRITE state at the end of power up RECALL, the SRAM data will be corrupted.

To help avoid this situation, a 10 k Ω resistor should be connected between \bar{W} and power supply voltage.

SOFTWARE NONVOLATILE STORE

The U635H256 software controlled STORE cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the U635H256 implements nonvolatile operation while remaining compatible with standard 32K x 8 SRAMs. During the STORE cycle, an erase of the previous nonvolatile data is performed first, followed by a parallel programming of all the nonvolatile elements. Once a STORE cycle is initiated, further inputs and outputs are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted.

To initiate the STORE cycle the following READ sequence must be performed:

1. Read addresses 0E38 (hex) Valid READ
2. Read addresses 31C7 (hex) Valid READ
3. Read addresses 03E0 (hex) Valid READ
4. Read addresses 3C1F (hex) Valid READ
5. Read addresses 303F (hex) Valid READ
6. Read addresses 0FC0 (hex) Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that \bar{G} be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A RECALL cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1. Read addresses 0E38 (hex) Valid READ
2. Read addresses 31C7 (hex) Valid READ
3. Read addresses 03E0 (hex) Valid READ
4. Read addresses 3C1F (hex) Valid READ
5. Read addresses 303F (hex) Valid READ
6. Read addresses 0C63 (hex) Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After $t_{d(E)R}$ cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

HARDWARE PROTECTION

The U635H256 offers hardware protection against inadvertent STORE operation through V_{CC} Sense. When $V_{CC} < V_{SWITCH}$ all software STORE operations will be inhibited.

LOW AVERAGE ACTIVE POWER

The U635H256 has been designed to draw significantly less power when \bar{E} is LOW (chip enabled) but the access cycle time is longer than 55 ns.

When \bar{E} is HIGH the chip consumes only standby current.

The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. the time during which the chip is disabled (\bar{E} HIGH)
3. the cycle time for accesses (\bar{E} LOW)
4. the ratio of READs to WRITEs
5. the operating temperature
6. the V_{CC} level



Zentrum Mikroelektronik Dresden

Memory Products 1998

PowerStore 32K x 8 nvSRAM U635H256

LIFE SUPPORT POLICY

ZMD products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the ZMD product could create a situation where personal injury or death may occur.

Components used in life-support devices or systems must be expressly authorized by ZMD for such purpose.

The information describes the type of component and shall not be considered as assured characteristics.

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