High Performance Video Op Amp

AD811

FEATURES

High speed
- **140 MHz bandwidth (3 dB, G = +1)**
- **120 MHz bandwidth (3 dB, G = +2)**
- **35 MHz bandwidth (0.1 dB, G = +2)**
- **2500 V/µs slew rate**
- **25 ns settling time to 0.1% (for a 2 V step)**
- **65 ns settling time to 0.01% (for a 10 V step)**

Excellent video performance (R_L =150 Ω)
- **0.01% differential gain, 0.01° differential phase**
- **Voltage noise of 1.9 nV/$\sqrt{Hz}$**

Low distortion: THD = −74 dB @ 10 MHz

Excellent dc precision: 3 mV max input offset voltage

Flexible operation
- **Specified for ±5 V and ±15 V operation**
- **±2.3 V output swing into a 75 Ω load (V_S = ±5 V)**

APPLICATIONS

Video crosspoint switchers, multimedia broadcast systems

HDTV compatible systems

Video line drivers, distribution amplifiers

ADC/DAC buffers

DC restoration circuits

Medical
- **Ultrasound**
- **PET**
- **Gamma**
- **Counter applications**

GENERAL DESCRIPTION

A wideband current feedback operational amplifier, the AD811 is optimized for broadcast-quality video systems. The −3 dB bandwidth of 120 MHz at a gain of +2 and the differential gain and phase of 0.01% and 0.01° (R_L = 150 Ω) make the AD811 an excellent choice for all video systems. The AD811 is designed to meet a stringent 0.1 dB gain flatness specification to a bandwidth of 35 MHz (G = +2) in addition to low differential gain and phase errors. This performance is achieved whether driving one or two back-terminated 75 Ω cables, with a low power supply current of 16.5 mA. Furthermore, the AD811 is specified over a power supply range of ±4.5 V to ±18 V.

(Continued on page 3)

CONNECTION DIAGRAMS

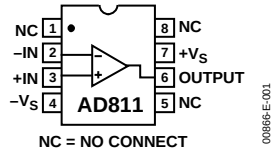


Figure 1. 8-Lead Plastic (N-8), CERDIP (Q-8), SOIC (R-8)

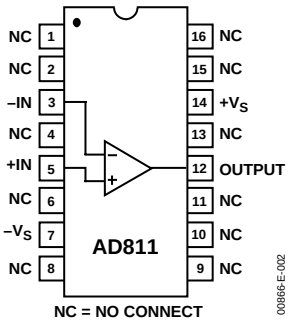


Figure 2. 16-Lead SOIC (R-16)

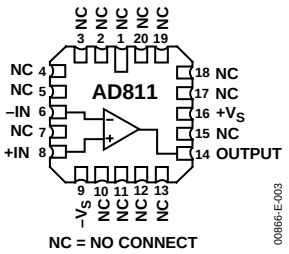


Figure 3. 20-Terminal LCC (E-20A)

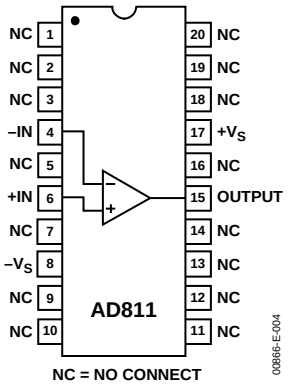


Figure 4. 20-Lead SOIC (R-20)

Rev. E

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REVISION HISTORY

7/04—Data Sheet Changed from Rev. D to Rev. E

Updated Format ..... Universal
Change to Maximum Power Dissipation Section 7
Changes to Ordering Guide 20
Updated Outline Dimensions 20

GENERAL DESCRIPTION (continued)

The AD811 is also excellent for pulsed applications where transient response is critical. It can achieve a maximum slew rate of greater than 2500 V/µs with a settling time of less than 25 ns to 0.1% on a 2 V step and 65 ns to 0.01% on a 10 V step.

The AD811 is ideal as an ADC or DAC buffer in data acquisition systems due to its low distortion up to 10 MHz and its wide unity gain bandwidth. Because the AD811 is a current feedback amplifier, this bandwidth can be maintained over a wide range of gains. The AD811 also offers low voltage and current noise of 1.9 nV/$\sqrt{\text{Hz}}$ and 20 pA/$\sqrt{\text{Hz}}$, respectively, and excellent dc accuracy for wide dynamic range applications.

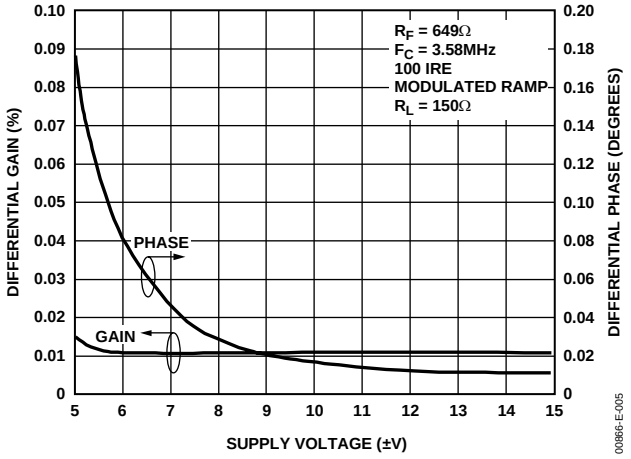


Figure 5. Differential Gain and Phase

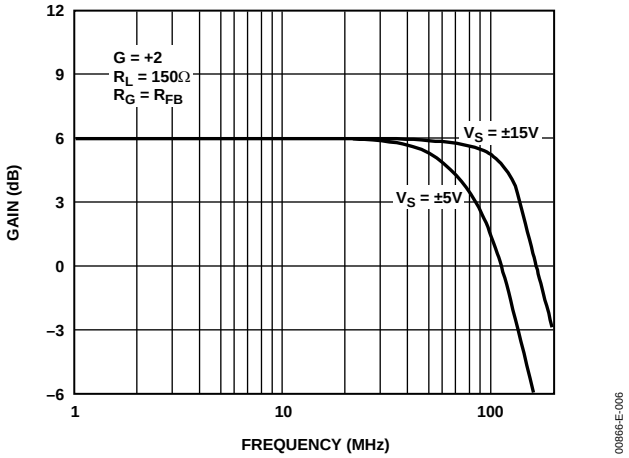


Figure 6. Frequency Response

SPECIFICATIONS

@ T_A = +25°C, V_S = ±15 V dc, R_{LOAD} = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	V_S	AD811J/A[1] Min	AD811J/A[1] Typ	AD811J/A[1] Max	AD811S[2] Min	AD811S[2] Typ	AD811S[2] Max	Unit
DYNAMIC PERFORMANCE									
Small Signal Bandwidth (No Peaking)									
−3 dB									
G = +1	R_{FB} = 562 Ω	±15 V		140			140		MHz
G = +2	R_{FB} = 649 Ω	±15 V		120			120		MHz
G = +2	R_{FB} = 562 Ω	±15 V		80			80		MHz
G = +10	R_{FB} = 511 Ω	±15 V		100			100		MHz
0.1 dB Flat									
G = +2	R_{FB} = 562 Ω	±15		25			25		MHz
	R_{FB} = 649 Ω	±15		35			35		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p	±15		40			40		MHz
Slew Rate	V_{OUT} = 4 V p-p	±15		400			400		V/µs
	V_{OUT} = 20 V p-p	±15		2500			2500		V/µs
Settling Time to 0.1%	10 V Step, A_V = − 1	±15		50			50		ns
Settling Time to 0.01%	10 V Step, A_V = − 1	±15		65			65		ns
Settling Time to 0.1%	2 V Step, A_V = − 1	±15		25			25		ns
Rise Time, Fall Time	R_{FB} = 649, A_V = +2	±15		3.5			3.5		ns
Differential Gain	f = 3.58 MHz	±15		0.01			0.01		%
Differential Phase	f = 3.58 MHz	±15		0.01			0.01		Degree
THD @ f_C = 10 MHz	V_{OUT} = 2 V p-p, A_V = +2	±15		−74			−74		dBc
Third-Order Intercept[4]	@ f_C = 10 MHz	±15		36			36		dBm
		±15		43			43		dBm
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.5	3		0.5	3	mV
	T_{MIN} to T_{MAX}				5			5	mV
Offset Voltage Drift				5			5		µV/°C
INPUT BIAS CURRENT									
−Input		±5 V, ±15 V		2	5		2	5	µA
	T_{MIN} to T_{MAX}				15			30	µA
+Input		±5 V, ±1 5 V		2	10		2	10	µA
	T_{MIN} to T_{MAX}				20			25	µA
TRANSRESISTANCE	T_{MIN} to T_{MAX}								
	V_{OUT} = ±10 V								
	R_L = ∞	±15 V	0.75	1.5		0.75	1.5		MΩ
	R_L = 200 Ω	±15 V	0.5	0.75		0.5	0.75		MΩ
	V_{OUT} = ±2.5 V								
	R_L = 150 Ω	±5 V	0.25	0.4		0.125	0.4		MΩ

[1] The AD811JR is specified with ±5 V power supplies only, with operation up to ±12 V.
[2] See the Analog Devices military data sheet for 883B tested specifications.
[3] FPBW = slew rate/(2 π V_{PEAK}).
[4] Output power level, tested at a closed-loop gain of two.

Parameter	Conditions	V_s	AD811J/A[1] Min	Typ	Max	AD811S[2] Min	Typ	Max	Unit
COMMON-MODE REJECTION									
V_{OS} (vs. Common Mode)									
T_{MIN} to T_{MAX}	V_{CM} = ±2.5 V	±5 V	56	60		50	60		dB
T_{MIN} to T_{MAX}	V_{CM} = ±10 V	±15 V	60	66		56	66		dB
Input Current (vs. Common Mode)	T_{MIN} to T_{MAX}			1	3		1	3	µA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V								
V_{OS}	T_{MIN} to T_{MAX}		60	70		60	70		dB
+Input Current	T_{MIN} to T_{MAX}			0.3	2		0.3	2	µA/V
−Input Current	T_{MIN} to T_{MAX}			0.4	2		0.4	2	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz			1.9			1.9		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz			20			20		pA/$\sqrt{Hz}$
OUTPUT CHARACTERISTICS									
Voltage Swing, Useful Operating Range[3]		±5 V		±2.9			±2.9		V
		±15 V		±12			±12		V
Output Current	T_J = 25°C			100			100		mA
Short-Circuit Current				150			150		mA
Output Resistance	(Open Loop @ 5 MHz)			9			9		Ω
INPUT CHARACTERISTIC									
+Input Resistance				1.5			1.5		MΩ
−Input Resistance				14			14		Ω
Input Capacitance	+Input			7.5			7.5		pF
Common-Mode Voltage Range		±5 V		±3			±3		V
		±15 V		±13			±13		V
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		14.5	16.0		14.5	16.0	mA
		±15 V		16.5	18.0		16.5	18.0	mA
TRANSISTOR COUNT	Number of Transistors			40			40		

[1] The AD811JR is specified with ±5 V power supplies only, with operation up to ±12 V.
[2] See the Analog Devices military data sheet for 883B tested specifications.
[3] Useful operating range is defined as the output voltage at which linearity begins to degrade.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
AD811JR Grade Only	±12 V
Internal Power Dissipation	Observe Derating Curves
8-Lead PDIP Package	θ_{JA} = 90°C/ W
8-Lead CERDIP Package	θ_{JA} = 110°C/W
8-Lead SOIC Package	θ_{JA} = 155°C/W
16-Lead SOIC Package	θ_{JA} = 85°C/W
20-Lead SOIC Package	θ_{JA} = 80°C/W
20-Lead LCC Package	θ_{JA} = 70°C/W
Output Short-Circuit Duration	Observe Derating Curves
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range (Q, E)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD811J	0°C to +70°C
AD811A	−40°C to +85°C
AD811S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD811 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the CERDIP and LCC packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation is restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves in Figure 22 and Figure 25.

While the AD811 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. An important example is when the amplifier is driving a reverse-terminated 75 Ω cable and the cable's far end is shorted to a power supply. With power supplies of ±12 V (or less) at an ambient temperature of +25°C or less, and the cable shorted to a supply rail, the amplifier is not destroyed, even if this condition persists for an extended period.

METALIZATION PHOTOGRAPH

Contact the factory for the latest dimensions.

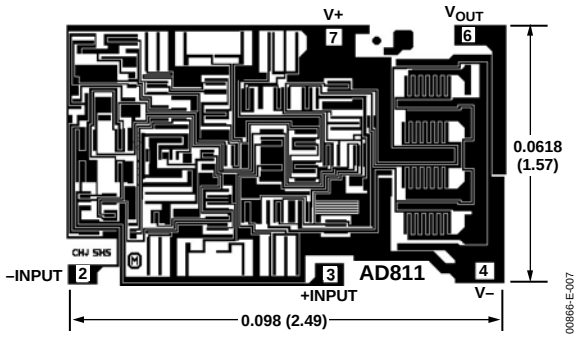


Figure 7. Metalization Photograph
Dimensions Shown in Inches and (Millimeters)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

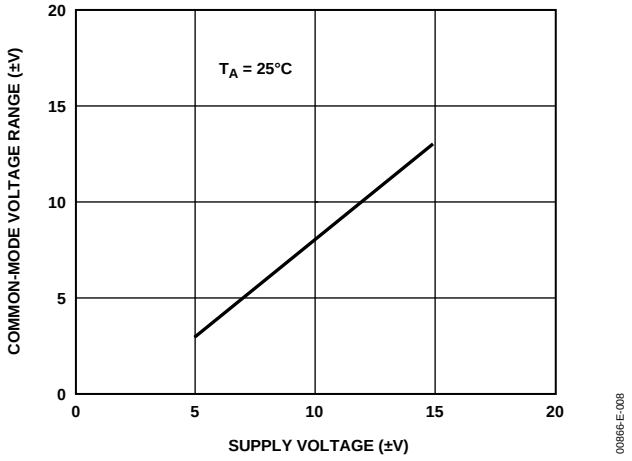


Figure 8. Input Common-Mode Voltage Range vs. Supply Voltage

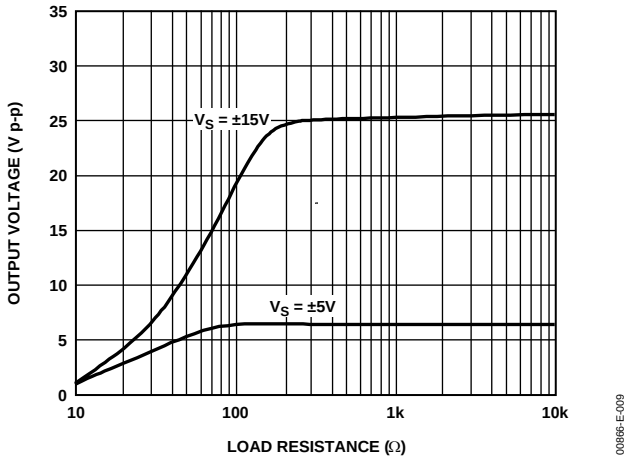


Figure 9. Output Voltage Swing vs. Resistive Load

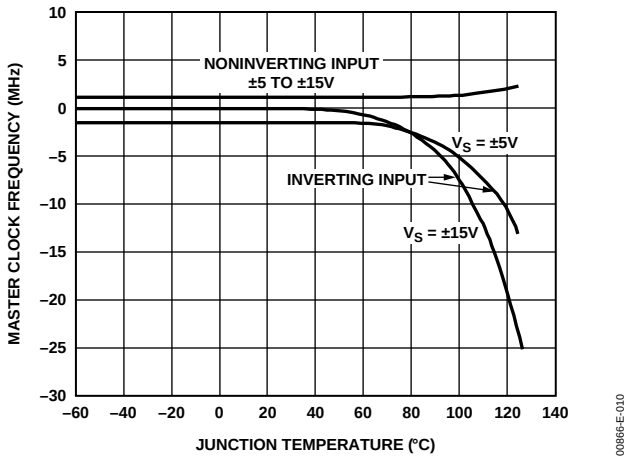


Figure 10. Input Bias Current vs. Junction Temperature

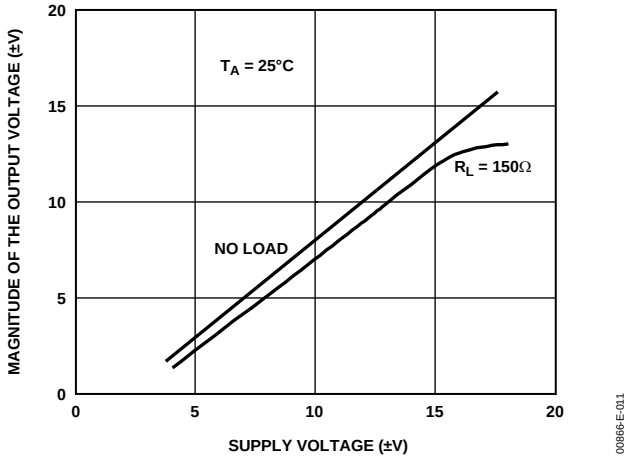


Figure 11. Output Voltage Swing vs. Supply Voltage

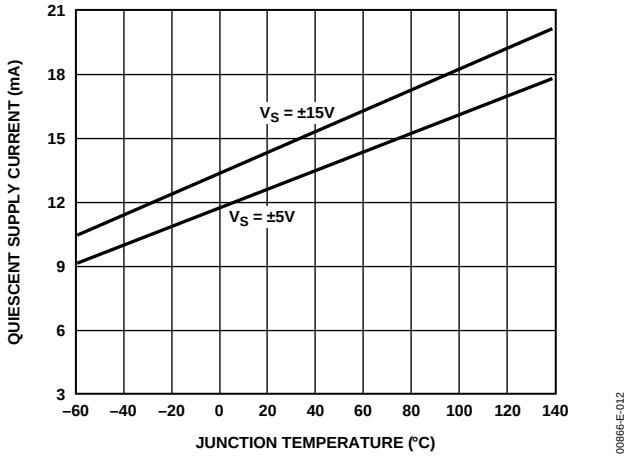


Figure 12. Quiescent Supply Current vs. Junction Temperature

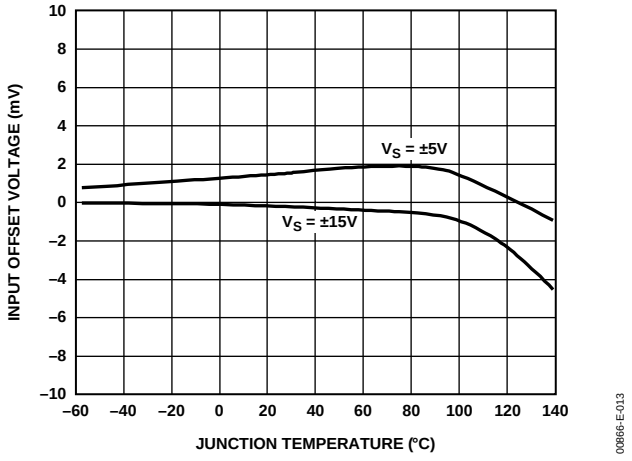


Figure 13. Input Offset Voltage vs. Junction Temperature

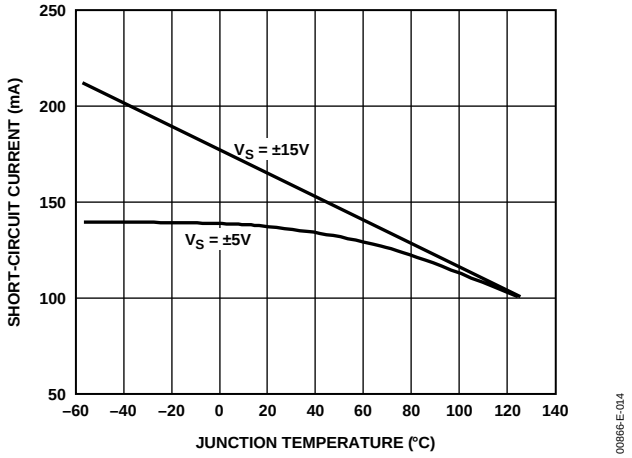


Figure 14. Short-Circuit Current vs. Junction Temperature

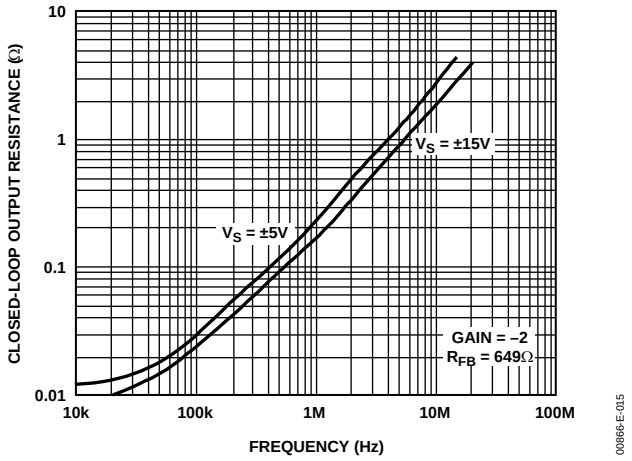


Figure 15. Closed-Loop Output Resistance vs. Frequency

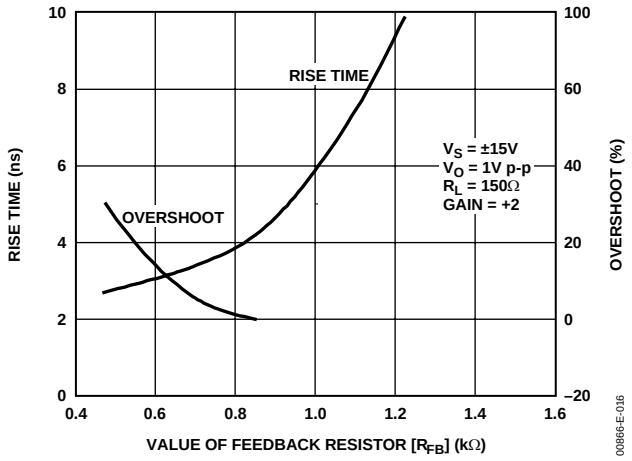


Figure 16. Rise Time and Overshoot vs. Value of Feedback Resistor, R_{FB}

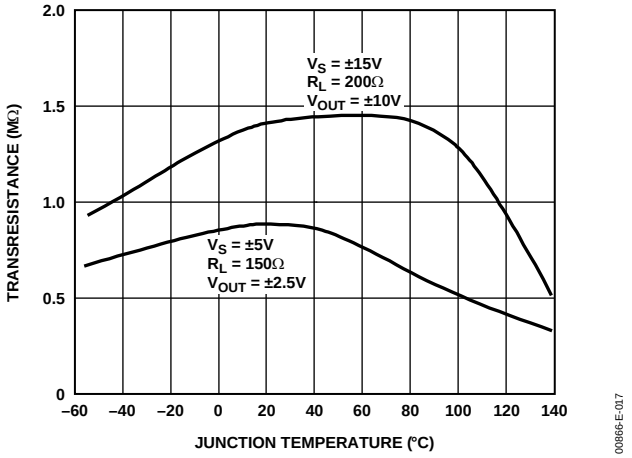


Figure 17. Transresistance vs. Junction Temperature

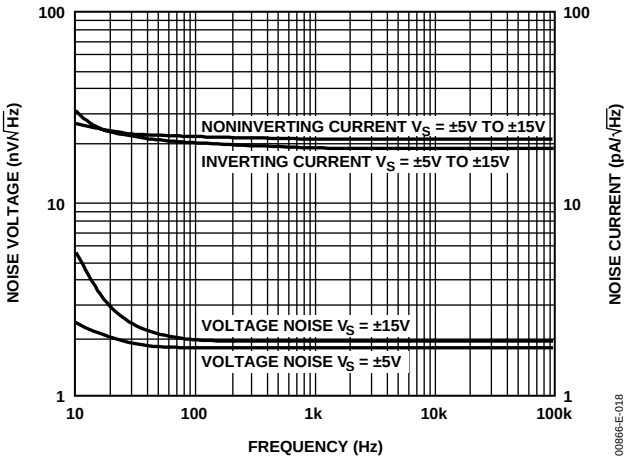


Figure 18. Input Noise vs. Frequency

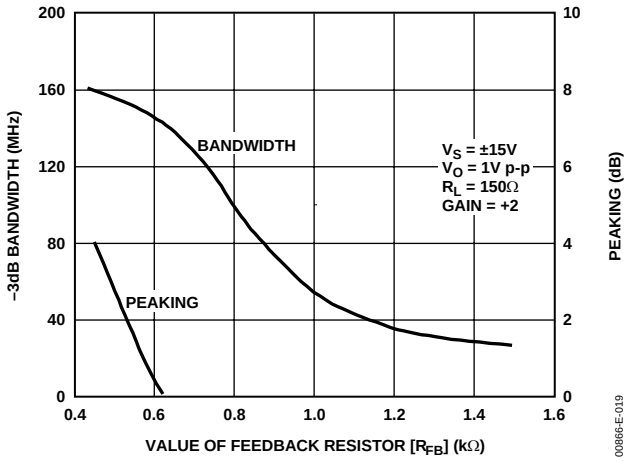


Figure 19. –3 dB Bandwidth and Peaking vs. Value of R_{FB}

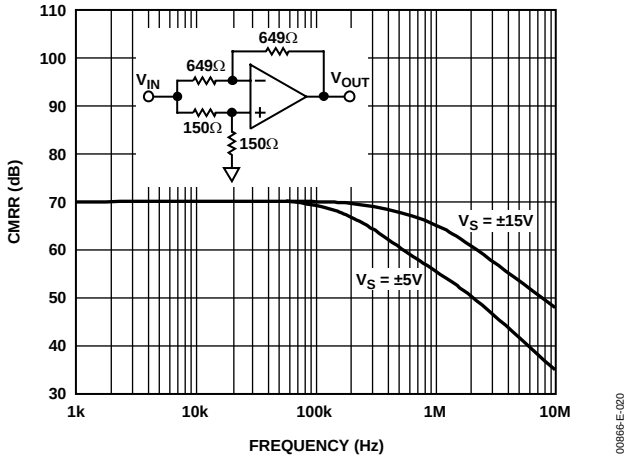


Figure 20. Common-Mode Rejection Ratio vs. Frequency

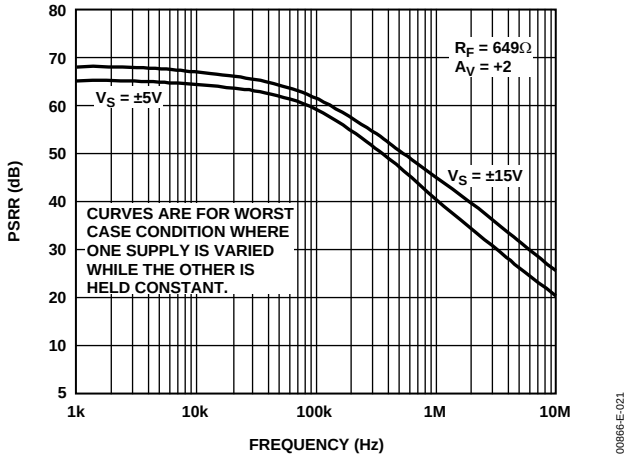


Figure 21. Power Supply Rejection Ration vs. Frequency

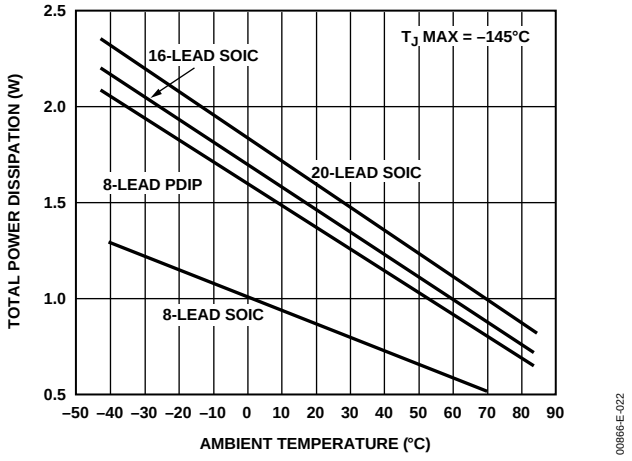


Figure 22. Maximum Power Dissipation vs. Temperature for Plastic Packages

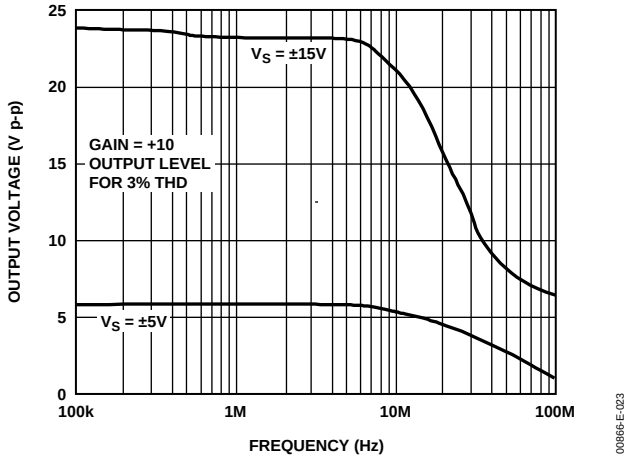


Figure 23. Large Signal Frequency Response

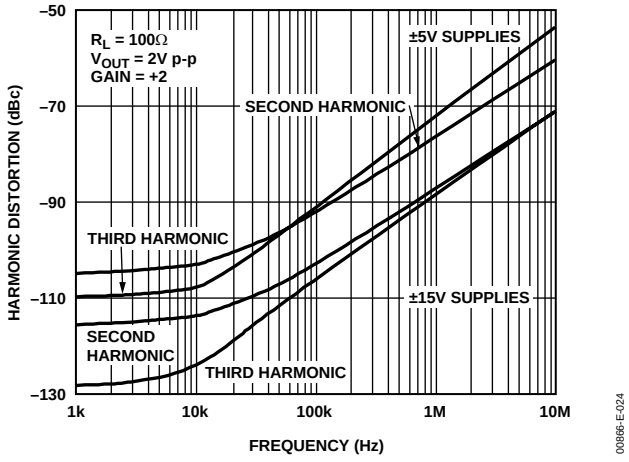


Figure 24. Harmonic Distortion vs. Frequency

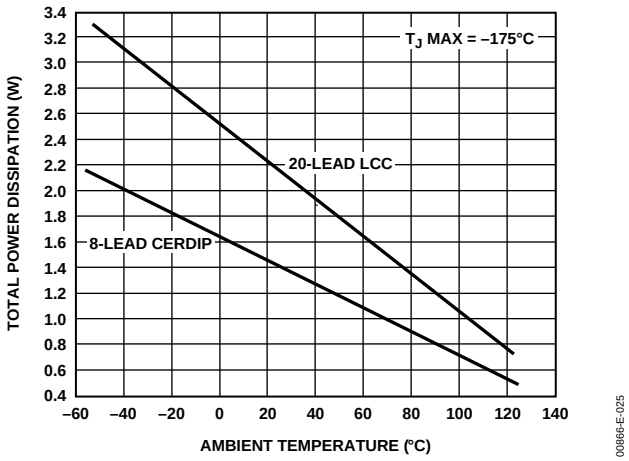


Figure 25. Maximum Power Dissipation vs. Temperature for Hermetic Packages

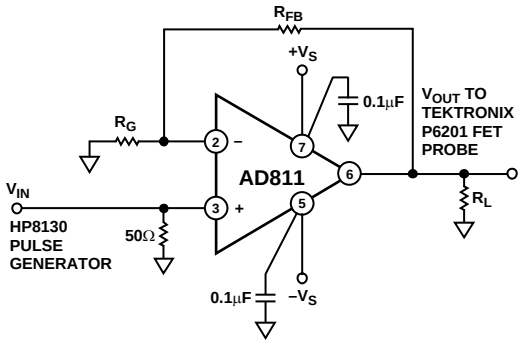


Figure 26. Noninverting Amplifier Connection

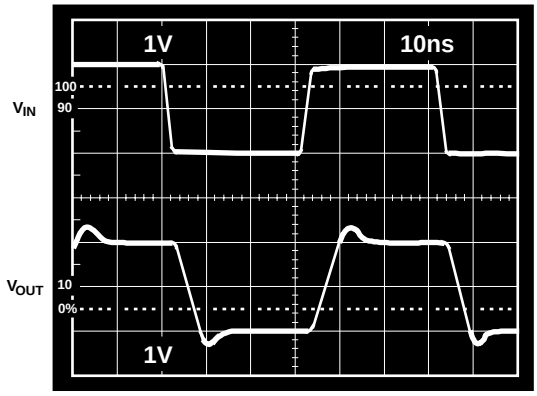


Figure 27. Small Signal Pulse Response, Gain = +1

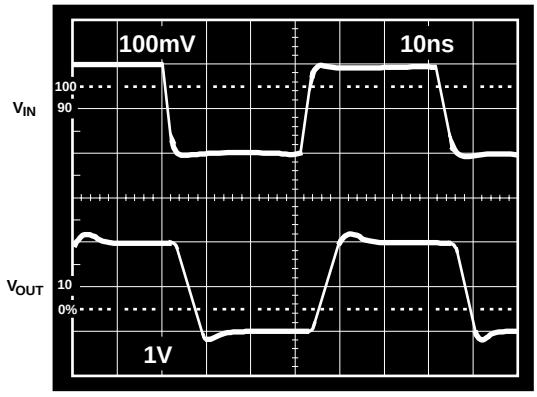


Figure 28. Small Signal Pulse Response, Gain = +10

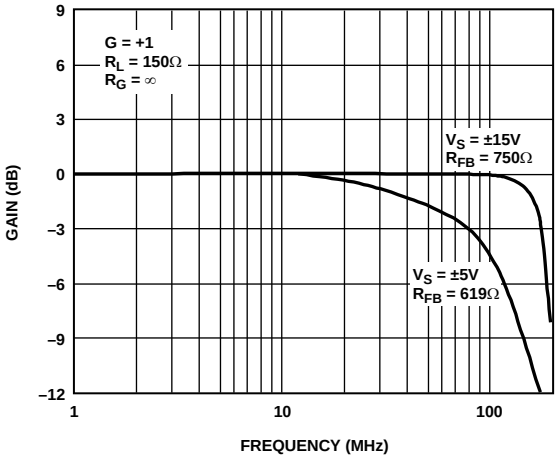


Figure 29. Closed-Loop Gain vs. Frequency, Gain = +1

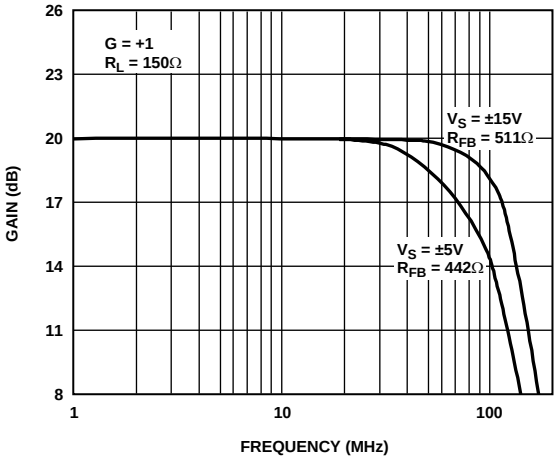


Figure 30. Closed-Loop Gain vs. Frequency, Gain = +10

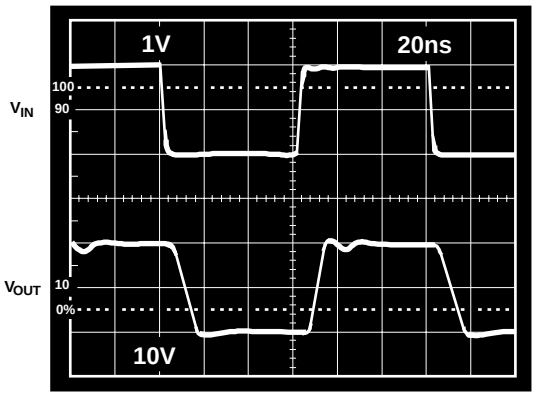


Figure 31. Large Signal Pulse Response, Gain = +10

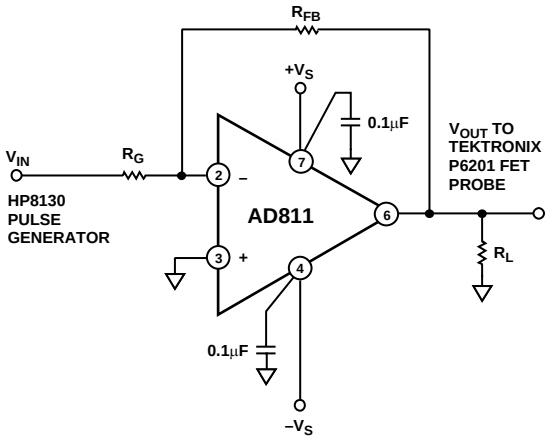


Figure 32. Inverting Amplifier Connection

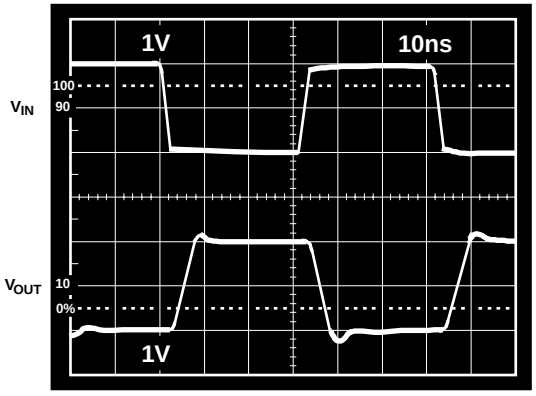


Figure 33. Small Signal Pulse Response, Gain = −1

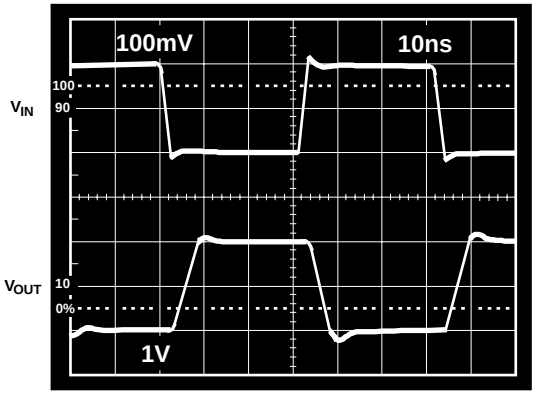


Figure 34. Small Signal Pulse Response, Gain = −10

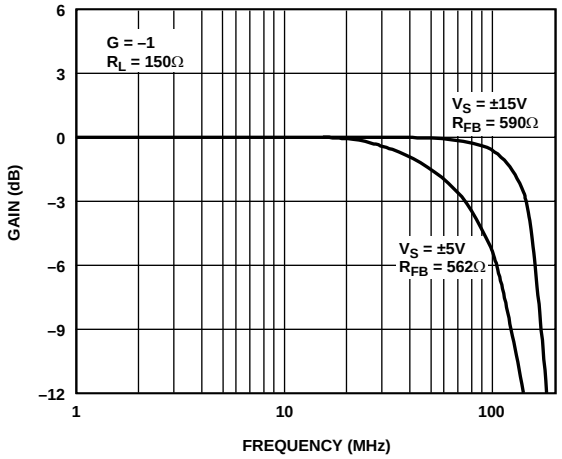


Figure 35. Closed-Loop Gain vs. Frequency, Gain = −1

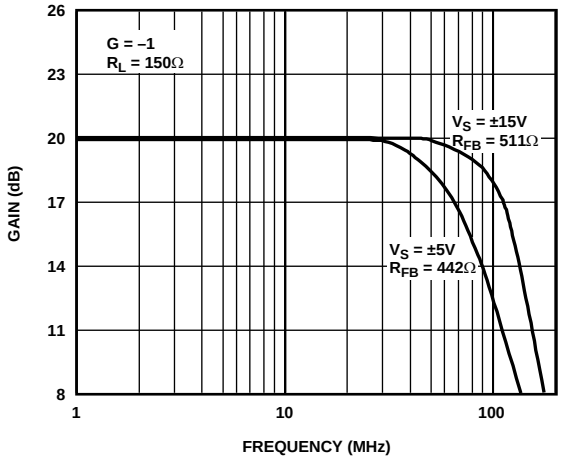


Figure 36. Closed-Loop Gain vs. Frequency, Gain = −10

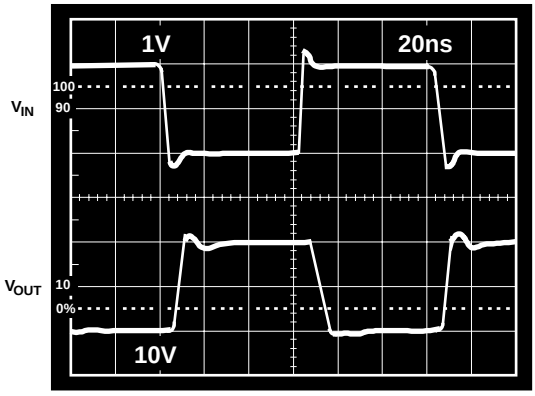


Figure 37. Large Signal Pulse Response, Gain = −10

APPLICATIONS

GENERAL DESIGN CONSIDERATIONS

The AD811 is a current feedback amplifier optimized for use in high performance video and data acquisition applications. Because it uses a current feedback architecture, its closed-loop −3 dB bandwidth is dependent on the magnitude of the feedback resistor. The desired closed-loop gain and bandwidth are obtained by varying the feedback resistor (R_{FB}) to tune the bandwidth and by varying the gain resistor (R_G) to obtain the correct gain. Table 3 contains recommended resistor values for a variety of useful closed-loop gains and supply voltages.

Table 3. −3 dB Bandwidth vs. Closed-Loop Gain and Resistance Values

V_S = ±15 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	750 Ω		140
+2	649 Ω	649 Ω	120
+10	511 Ω	56.2 Ω	100
−1	590 Ω	590 Ω	115
−10	511 Ω	51.1 Ω	95
V_S = ±5 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	619 Ω		80
+2	562 Ω	562 Ω	80
+10	442 Ω	48.7 Ω	65
−1	562 Ω	562 Ω	75
−10	442 Ω	44.2 Ω	65
V_S = ±10 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	649 Ω		105
+2	590 Ω	590 Ω	105
+10	499 Ω	49.9 Ω	80
−1	590 Ω	590 Ω	105
−10	499 Ω	49.9 Ω	80

Figure 18 and Figure 19 illustrate the relationship between the feedback resistor and the frequency and time domain response characteristics for a closed-loop gain of +2. (The response at other gains is similar.)

The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, for example, the magnitude of the internal junction capacitances is increased, causing a reduction in closed-loop bandwidth. To compensate for this, smaller values of feedback resistor are used at lower supply voltages.

ACHIEVING THE FLATTEST GAIN RESPONSE AT HIGH FREQUENCY

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

Choice of Feedback and Gain Resistors

Because of the previously mentioned relationship between the 3 dB bandwidth and the feedback resistor, the fine scale gain flatness varies, to some extent, with feedback resistor tolerance. Therefore, it is recommended that resistors with a 1% tolerance be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Metal film resistors were used for the bulk of the characterization for this data sheet. It is possible that values other than those indicated are optimal for other resistor types.

Printed Circuit Board Layout Considerations

As is expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is used on the same side of the board as the signal traces, a space (3/16" is plenty) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4" are recommended.

Quality of Coaxial Cable

Optimum flatness when driving a coax cable is possible only when the driven cable is terminated at each end with a resistor matching its characteristic impedance. If the coax is ideal, then the resulting flatness is not affected by the length of the cable. While outstanding results can be achieved using inexpensive cables, note that some variation in flatness due to varying cable lengths may occur.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) are required to provide the best settling time and lowest distortion. Although the recommended 0.1 μF power supply bypass capacitors are sufficient in many applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases.

Driving Capacitive Loads

The feedback and gain resistor values in Table 3 result in very flat closed-loop responses in applications where the load capacitances are below 10 pF. Capacitances greater than this result in increased peaking and overshoot, although not necessarily in a sustained oscillation.

There are at least two very effective ways to compensate for this effect. One way is to increase the magnitude of the feedback resistor, which lowers the 3 dB frequency. The other method is to include a small resistor in series with the output of the amplifier to isolate it from the load capacitance. The results of these two techniques are illustrated in Figure 39. Using a 1.5 kΩ feedback resistor, the output ripple is less than 0.5 dB when driving 100 pF. The main disadvantage of this method is that it sacrifices a little bit of gain flatness for increased capacitive load drive capability. With the second method, using a series resistor, the loss of flatness does not occur.

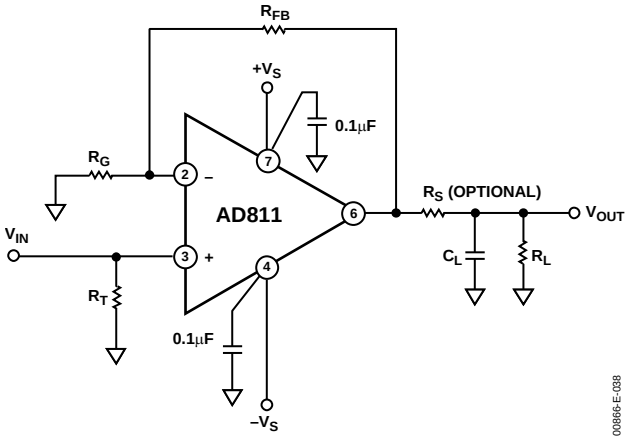


Figure 38. Recommended Connection for Driving a Large Capacitive Load

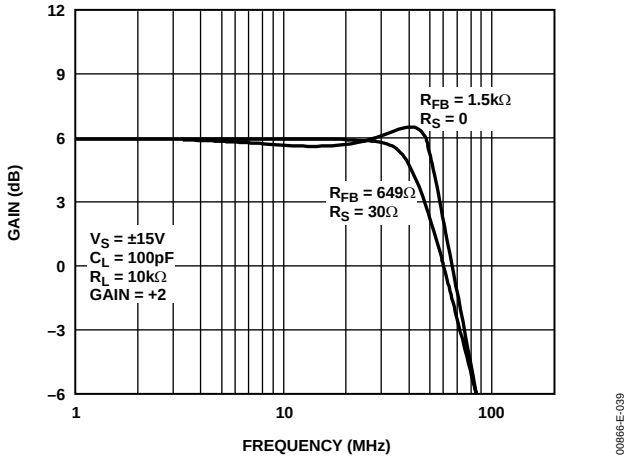


Figure 39. Performance Comparison of Two Methods for Driving a Capacitive Load

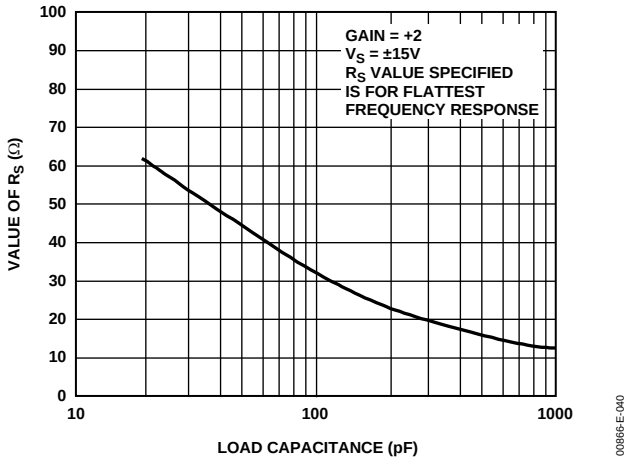


Figure 40. Recommended Value of Series Resistor vs. the Amount of Capacitive Load

Figure 40 shows recommended resistor values for different load capacitances. Refer again to Figure 39 for an example of the results of this method. Note that it may be necessary to adjust the gain setting resistor, R_G, to correct for the attenuation which results due to the divider formed by the series resistor, R_S, and the load resistance.

Applications that require driving a large load capacitance at a high slew rate are often limited by the output current available from the driving amplifier. For example, an amplifier limited to 25 mA output current cannot drive a 500 pF load at a slew rate greater than 50 V/μs. However, because of the AD811's 100 mA output current, a slew rate of 200 V/μs is achievable when driving the same 500 pF capacitor, as shown in Figure 41.

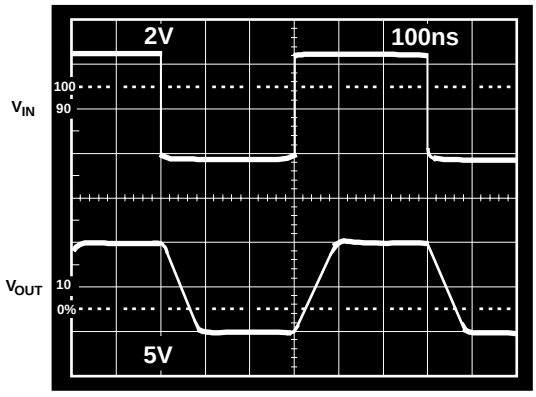


Figure 41. Output Waveform of an AD811 Driving a 500 pF Load. Gain = +2, R_{FB} = 649 Ω, R_S = 15 Ω, R_S = 10 kΩ

OPERATION AS A VIDEO LINE DRIVER

The AD811 has been designed to offer outstanding performance at closed-loop gains of +1 or greater, while driving multiple reverse-terminated video loads. The lowest differential gain and phase errors are obtained when using ±15 V power supplies. With ±12 V supplies, there is an insignificant increase in these errors and a slight improvement in gain flatness. Due to power dissipation considerations, ±12 V supplies are recommended for optimum video performance. Excellent performance can be achieved at much lower supplies as well.

The closed-loop gain versus the frequency at different supply voltages is shown in Figure 43. Figure 44 is an oscilloscope photograph of an AD811 line driver's pulse response with ±15 V supplies. The differential gain and phase error versus the supply are plotted in Figure 45 and Figure 46, respectively.

Another important consideration when driving multiple cables is the high frequency isolation between the outputs of the cables. Due to its low output impedance, the AD811 achieves better than 40 dB of output-to-output isolation at 5 MHz driving back-terminated 75 Ω cables.

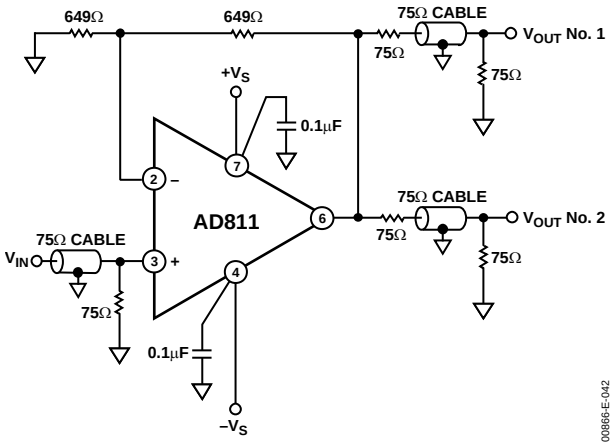


Figure 42. A Video Line Driver Operating at a Gain of +2

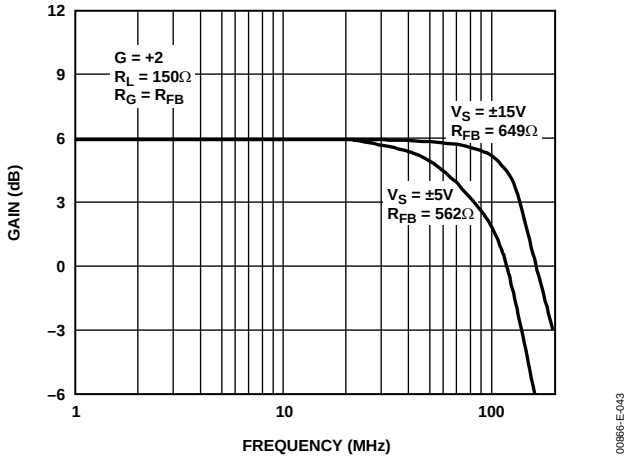


Figure 43. Closed-Loop Gain vs. Frequency, Gain = +2

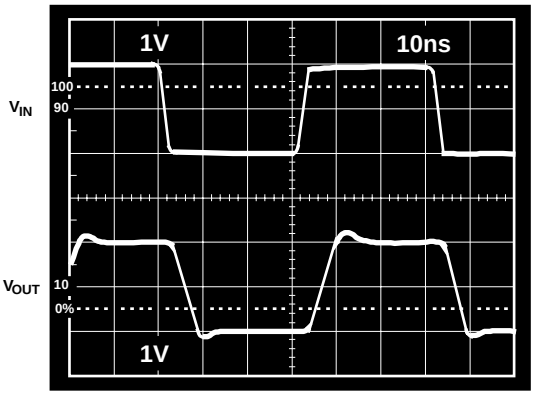


Figure 44. Small Signal Pulse Response, Gain = +2, V_S = ±15 V

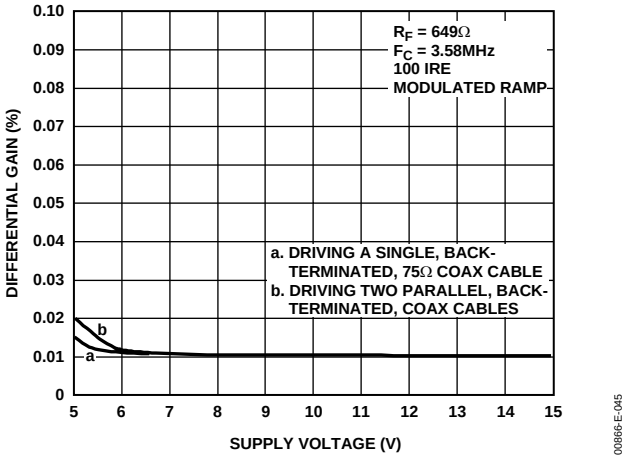


Figure 45. Differential Gain Error vs. Supply Voltage for the Video Line Driver of Figure 42

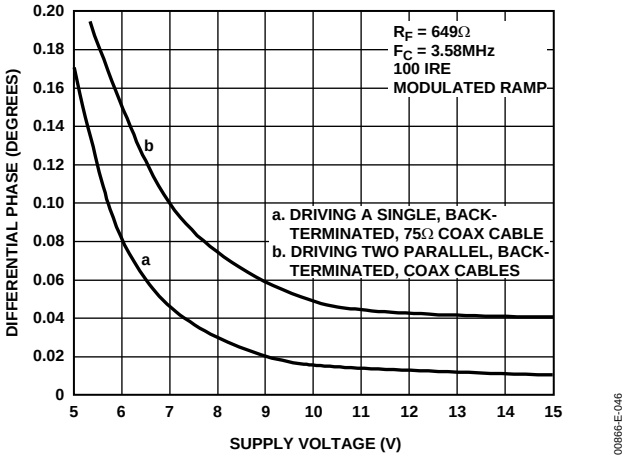


Figure 46. Differential Phase Error vs. Supply Voltage for the Video Line Driver of Figure 42

AN 80 MHZ VOLTAGE-CONTROLLED AMPLIFIER CIRCUIT

The voltage-controlled amplifier (VCA) circuit of Figure 48 shows the AD811 being used with the AD834, a 500 MHz, 4-quadrant multiplier. The AD834 multiplies the signal input by the dc control voltage, V_G. The AD834 outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available for certain applications. Here, the AD811 op amp provides a buffered, single-ended, ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω, the overall gain ranges from −70 dB for V_G = 0 dB to +12 dB (a numerical gain of +4) when V_G = 1 V. The overall transfer function of the VCA is $V_{OUT} = 4 (X1 - X2)(Y1 - Y2)$, which reduces to $V_{OUT} = 4 V_G V_{IN}$ using the labeling conventions shown in Figure 47. The circuit's −3 dB bandwidth of 80 MHz is maintained essentially constant—that is, independent of gain. The response can be maintained flat to within ±0.1 dB from dc to 40 MHz at full gain with the addition of an optional capacitor of about 0.3 pF across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V.

The gain can be increased to 20 dB (×10) by raising R8 and R9 to 1.27 kΩ, with a corresponding decrease in −3 dB bandwidth to approximately 25 MHz. The maximum output voltage under these conditions is increased to ±9 V using ±12 V supplies.

The gain-control input voltage, V_G, may be a positive or negative ground-referenced voltage, or fully differential, depending on the choice of connections at Pins 7 and 8. A positive value of V_G results in an overall noninverting response. Reversing the sign of V_G simply causes the sign of the overall response to invert. In fact, although this circuit has been classified as a voltage-controlled amplifier, it is also quite useful as a general-purpose, four-quadrant multiplier, with good load driving capabilities and fully symmetrical responses from the X and Y inputs.

The AD811 and AD834 can both be operated from power supply voltages of ±5 V. While it is not necessary to power them from the same supplies, the common-mode voltage at W1 and W2 must be biased within the common-mode range of the AD811's input stage. To achieve the lowest differential gain and phase errors, it is recommended that the AD811 be operated from power supply voltages of ±10 V or greater. This VCA circuit operates from a ±12 V dual power supply.

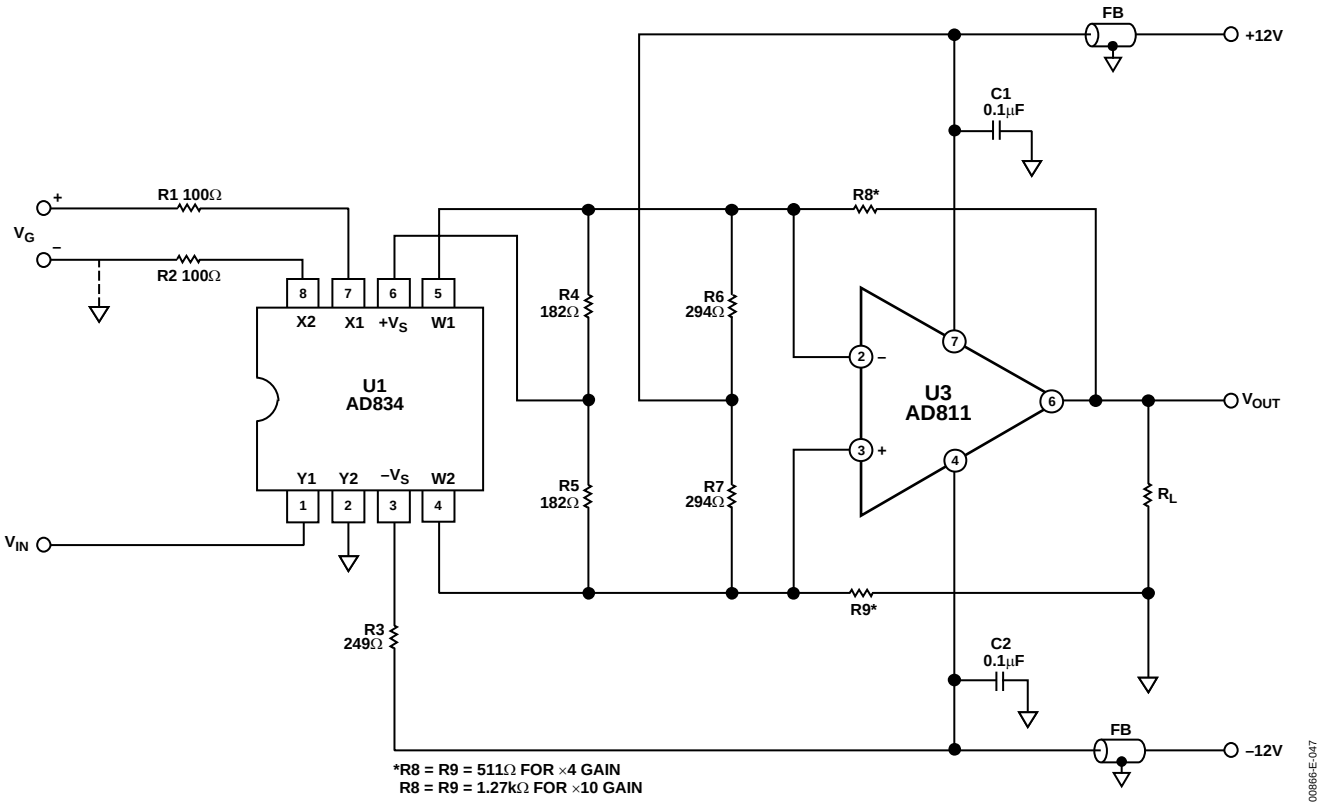


Figure 47. An 80 MHz Voltage-Controlled Amplifier

A VIDEO KEYER CIRCUIT

By using two AD834 multipliers, an AD811, and a 1 V dc source, a special form of a two-input VCA circuit called a video keyer can be assembled. Keying is the term used in reference to blending two or more video sources under the control of a third signal or signals to create such special effects as dissolves and overlays. The circuit shown in Figure 48 is a two-input keyer, with video inputs V_A and V_B, and a control input V_G. The transfer function (with V_{OUT} at the load) is given by

$$V_{OUT} = GV_A + (1-G)V_B$$

where G is a dimensionless variable (actually, just the gain of the A signal path) that ranges from 0 when V_G = 0 to 1 when V_G = 1 V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

Circuit operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is clearly 0 when V_G = 0, and the scaling chosen ensures that it has a unity value when V_G = 1 V; this takes care of the first term of the transfer function. On the other hand, the V_G input to U2 is taken to the inverting input X2 while X1 is biased at an accurate 1 V. Thus, when V_G = 0, the response to video input V_B is already at its full-scale value of unity, whereas when V_G = 1 V, the differential input X1–X2 is 0. This generates the second term.

The bias currents required at the output of the multipliers are provided by R8 and R9. A dc level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned at a voltage within its common-mode range. At high frequencies, C1 and C2 bypass R10 and R11, respectively. R14 is included to lower the HF loop gain and is needed because the voltage-to-current conversion in the AD834s, via the Y2 inputs, results in an effective value of the feedback resistance of 250 Ω; this is only about half the value required for optimum flatness in the AD811's response. (Note that this resistance is unaffected by G: when G = +1, all the feedback is via U1, while when G = 0 it is all via U2). R14 reduces the fractional amount of output current from the multipliers into the current-summing inverting input of the AD811 by sharing it with R8. This resistor can be used to adjust the bandwidth and damping factor to best suit the application.

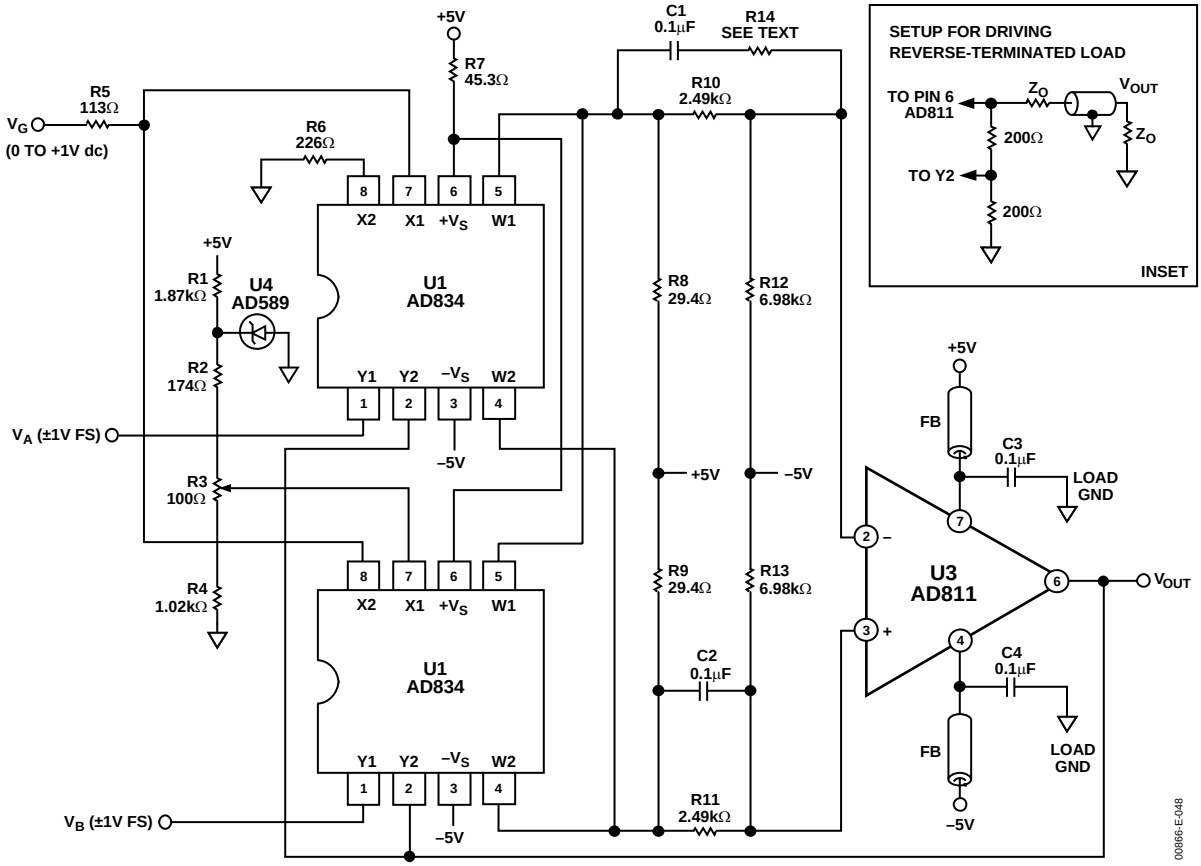


Figure 48. A Practical Video Keyer Circuit

To generate the 1 V dc needed for the 1−G term, an AD589 reference supplies 1.225 V ± 25 mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide exactly 1 V at the X1 input.

In this case, an arrangement is shown using dual supplies of ±5 V for both the AD834 and the AD811. Also, the overall gain is arranged to be unity at the load when it is driven from a reverse-terminated 75 Ω line. This means that the dual VCA has to operate at a maximum gain of +2, rather than +4 as in the VCA circuit of Figure 47. However, this cannot be achieved by lowering the feedback resistor because below a critical value (not much less than 500 Ω) the AD811's peaking may be unacceptable. This is because the dominant pole in the open-loop ac response of a current feedback amplifier is controlled by this feedback resistor. It would be possible to operate at a gain of ×4 and then attenuate the signal at the output. Instead, the signals have been attenuated by 6 dB at the input to the AD811; this is the function of R8 through R11.

Figure 49 is a plot of the ac response of the feedback keyer when driving a reverse-terminated 50 Ω cable. Output noise and adjacent channel feedthrough, with either channel fully off and the other fully on, is about −50 dB to 10 MHz. The feedthrough at 100 MHz is limited primarily by board layout. For V_G = 1 V, the −3 dB bandwidth is 15 MHz when using a 137 Ω resistor for R14 and 70 MHz with R14 = 49.9 Ω. For more information on the design and operation of the VCA and video keyer circuits, refer to the application note "Video VCAs and Keyers: Using the AD834 and AD811" by Brunner, Clarke, and Gilbert, available on the Analog Devices, Inc. website at www.analog.com.

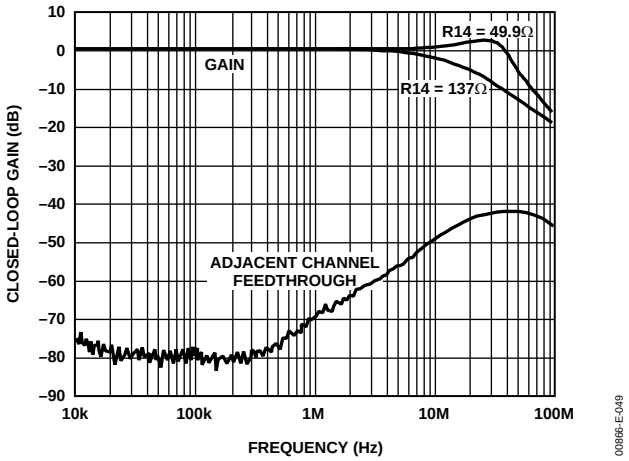
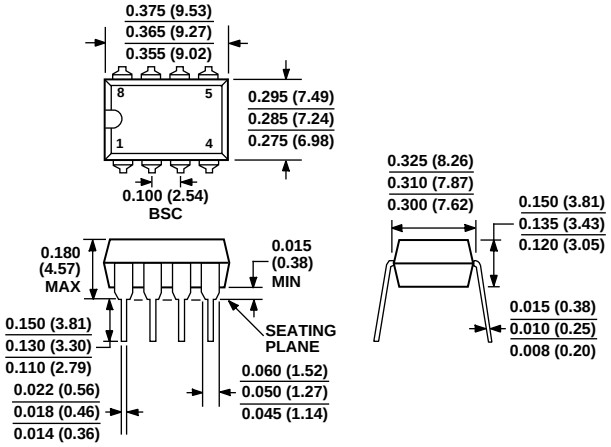


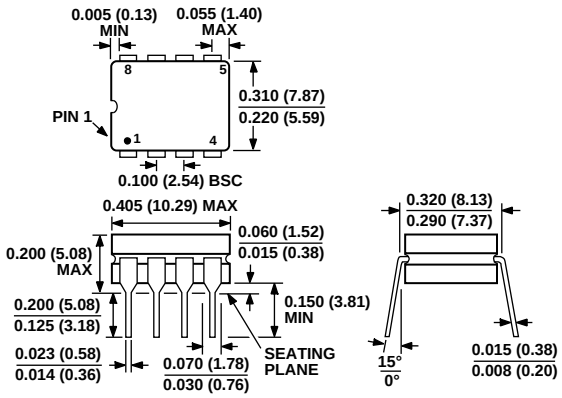
Figure 49. A Plot of the AC Response of the Video Keyer

OUTLINE DIMENSIONS



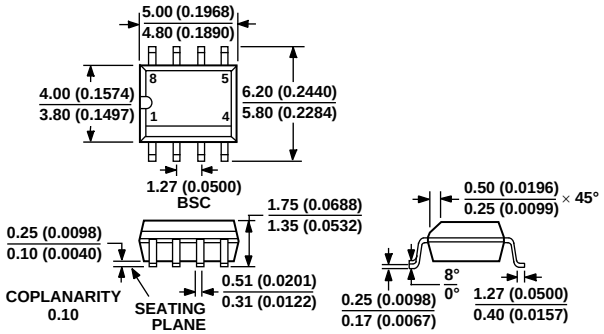
COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



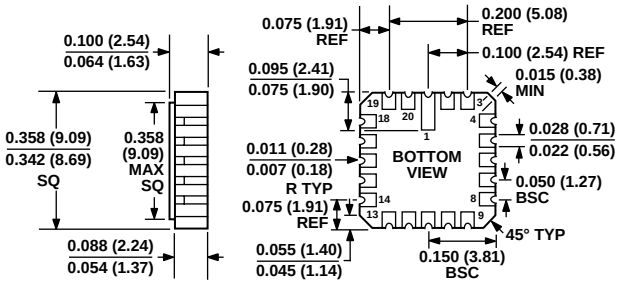
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Figure 51. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



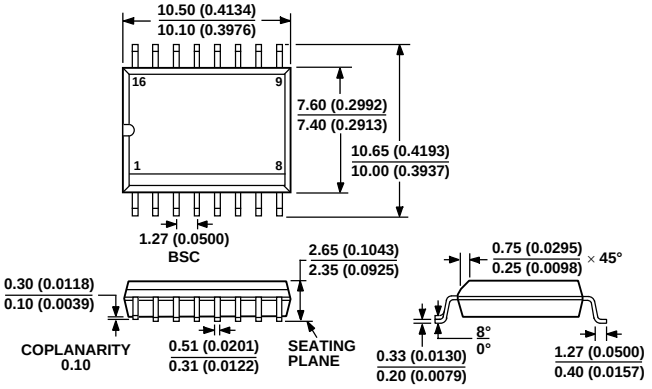
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CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 52. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



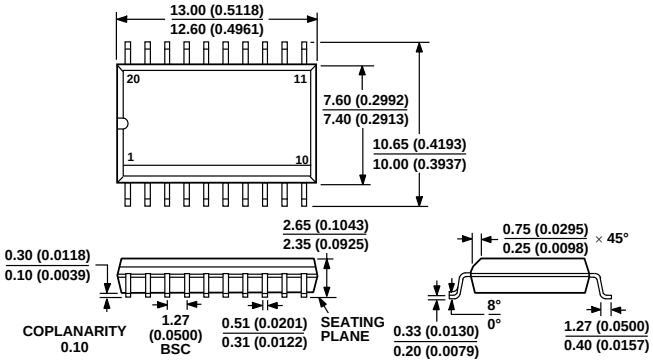
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 53. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20A)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 54. 16-Lead Standard Small Outline Package [SOIC]
Wide Body (R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 55. 20-LeadStandard Small Outline Package [SOIC]
Wide Body (R-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD811AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package (PDIP)	N-8
AD811ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package (PDIP)	N-8
AD811AR-16	−40°C to +85°C	16-LeadStandard Small Outline Package (SOIC)	R-16
AD811AR-16-REEL	−40°C to +85°C	16-LeadStandard Small Outline Package (SOIC)	R-16
AD811AR-16-REEL7	−40°C to +85°C	16-LeadStandard Small Outline Package (SOIC)	R-16
AD811AR-20	−40°C to +85°C	20-LeadStandard Small Outline Package (SOIC)	R-20
AD811AR-20-REEL	−40°C to +85°C	20-LeadStandard Small Outline Package (SOIC)	R-20
AD811JR	0°C to +70°C	8-LeadStandard Small Outline Package (SOIC)	R-8
AD811JR-REEL	0°C to +70°C	8-LeadStandard Small Outline Package (SOIC)	R-8
AD811JR-REEL7	0°C to +70°C	8-LeadStandard Small Outline Package (SOIC)	R-8
AD811JRZ[1]	0°C to +70°C	8-LeadStandard Small Outline Package (SOIC)	R-8
AD811SQ/883B	−55°C to +125°C	8-Lead Ceramic Dual In-Line Package (CERDIP)	Q-8
5962-9313101MPA	−55°C to +125°C	8-Lead Ceramic Dual In-Line Package (CERDIP)	Q-8
AD811SE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier (LCC)	E-20A
5962-9313101M2A	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier (LCC)	E-20A
AD811ACHIPS	−40°C to +85°C		DIE
AD811SCHIPS	−55°C to +125°C		DIE

[1] Z = Pb-free part.

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