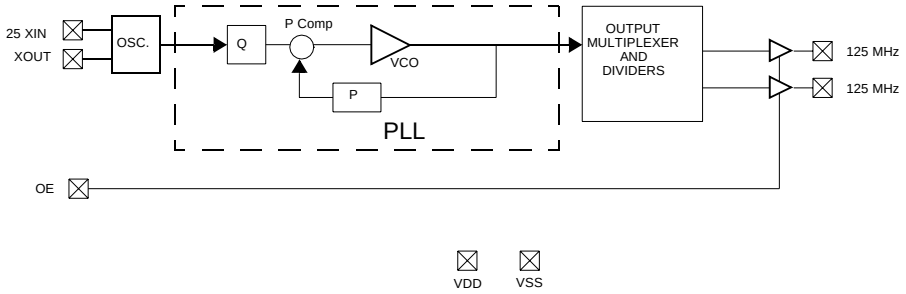
# Dual Output 125-MHz Clock Generator

| Features | Benefits |
|---|---|
| • **Integrated phase-locked loop** | Highest-performance PLL tailored for multimedia applications |
| • **Low skew, low jitter, high accuracy outputs** | Meets critical timing requirements in complex system designs |
| • **3.3V Operation** | |

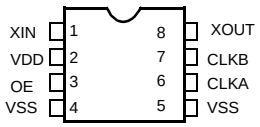
| Part Number | Outputs | Input Frequency Range | Output Frequencies |
|---|---|---|---|
| CY26126 | 2 | 25 MHz | 2 copies of 125 MHz (3.3V) |

## Logic Block Diagram




## Pin Configurations

**CY26126**
**8-pin SOIC**



## Pin Summary

| Name | Pin Number | Description |
|---|---|---|
| XIN | 1 | Reference Input |
| VDD | 2 | 3.3V Voltage Supply |
| OE | 3 | Output Enable |
| VSS | 4 | Ground |
| VSS | 5 | Ground |
| CLKA | 6 | 125-MHz Clock Output A |
| CLKB | 7 | 125-MHz Clock Output B |
| XOUT[1] | 8 | Reference Output |

## Absolute Maximum Conditions

| Parameter | Description | Min. | Max. | Unit. |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | –0.5 | 7.0 | V |
| $T_S$ | Storage Temperature[2] | –65 | 125 | °C |
| $T_J$ | Junction Temperature | | 125 | °C |
| | Digital Inputs | $V_{SS}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| | Digital Outputs referred to $V_{DD}$ | $V_{SS}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| | Electro-Static Discharge | 2 | | kV |

## Recommended Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | 3.14 | 3.3 | 3.47 | V |
| $T_A$ | Ambient Temperature | 0 | | 70 | °C |
| $C_{LOAD}$ | Max. Load Capacitance | | | 15 | pF |
| $P_{max}$ | Max. Output Power Dissipation | | | 150 | mW |
| $f_{REF}$ | Reference Frequency | | 25 | | MHz |
| $t_{PU}$ | Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | | 500 | ms |

## DC Electrical Characteristics

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ | 12 | 24 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL} = 0.5$, $V_{DD} = 3.3V$ | 12 | 24 | | mA |
| $V_{IH}$ | Input High Voltage | CMOS Levels 70% of $V_{DD}$ | 0.7 | | | $V_{DD}$ |
| $V_{IL}$ | Input Low Voltage | CMOS Levels 30% of $V_{DD}$ | | | 0.3 | $V_{DD}$ |
| $C_{IN}$ | Input Capacitance | | | | 7 | pF |
| $I_{IZ}$ | Input Leakage Current | | | 5 | | µA |
| $I_{DD}$ | Supply Current | Sum of Core and Output Current | | | 35 | mA |

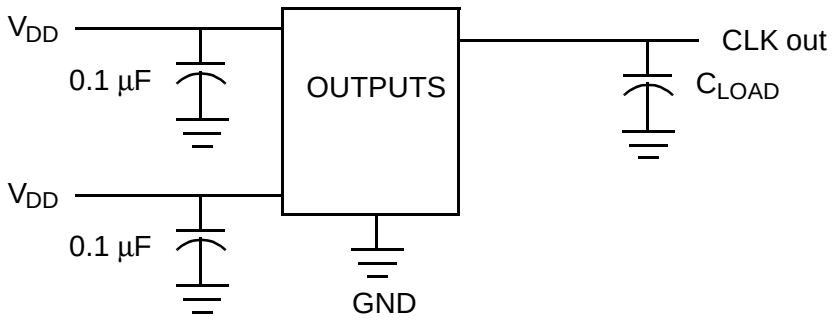
**Notes:**
1. Float XOUT pin if XIN is driven by reference clock (as opposed to crystal).
2. Rated for 10 years.

## AC Electrical Characteristics ($V_{DD}$ = 3.3V)[3]

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Output Duty Cycle | Duty Cycle is defined in *Figure 1*, 50% of $V_{DD}$ | 45 | 50 | 55 | % |
| t3 | Rising Edge Slew Rate | Output Clock Rise Time, 20% - 80% of $V_{DD}$ | 0.8 | 1.4 | | V/ns |
| t4 | Falling Edge Slew Rate | Output Clock Fall Time, 80% - 20% of $V_{DD}$ | 0.8 | 1.4 | | V/ns |
| t9 | Clock Jitter | Peak to Peak period jitter | | | 200 | ps |
| t10 | PLL Lock Time | | | | 3 | ms |

**Note:**
3. Not 100% tested.

## Test Circuit



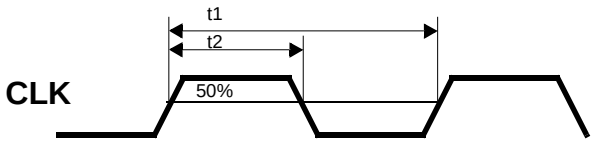




**Figure 1. Duty Cycle Definition; DC = t2/t1**

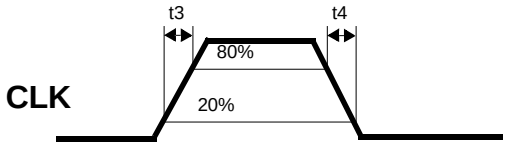


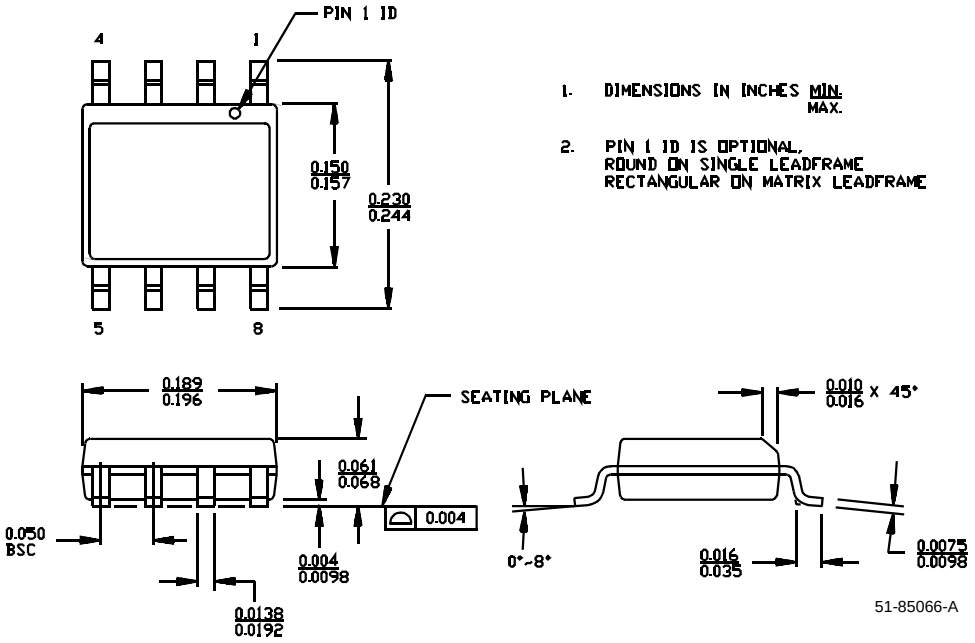

**Figure 2. Rise and Fall Time Definitions**

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage |
|---|---|---|---|---|
| CY26126SC | S8 | 8-Pin SOIC | Commercial | 3.3V |

## Package Diagram

**8-Lead (150-Mil) SOIC S8**



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| Document Title: CY26126 Dual Output 125-MHz Clock Generator<br>Document Number: 38-07351 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 112233 | 03/01/02 | CKN | New data sheet |
| *A | 121891 | 12/14/02 | RBI | Power up requirements added to Operating Conditions Information |

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