FAN2510, FAN2511

100 mA CMOS LDO Regulators with Fast Start Enable

Features

- Ultra Low Power Consumption
- Enable optimized for CDMA time slices
- 100 mV dropout voltage at 100 mA
- 25 µA ground current at 100 mA
- Enable/Shutdown Control
- SOT23-5 package
- Thermal limiting
- 300 mA peak current

Applications

- Cellular Phones and accessories
- PDAs
- Portable cameras and video recorders
- Laptop, notebook and palmtop computers

Description

The FAN2510/11 family of micropower low-dropout voltage regulators utilize CMOS technology to offer a new level of cost-effective performance in GSM, TDMA, and CDMA cellular handsets, Laptop and Notebook portable computers, and other portable devices. Features include extremely low power consumption and low shutdown current, low dropout voltage, exceptional loop stability able to accommodate a wide variety of external capacitors, and the compact SOT23-5 surface-mount package. In addition, the FAN2510/11 family offer the fast power-cycle time required in CDMA handset applications. These products offer significant improvements over older BiCMOS designs and are pin-compatible with many popular devices. The output is thermally protected against overload.

The FAN2510 and FAN2511 devices are distinguished by the assignment of pin 4:

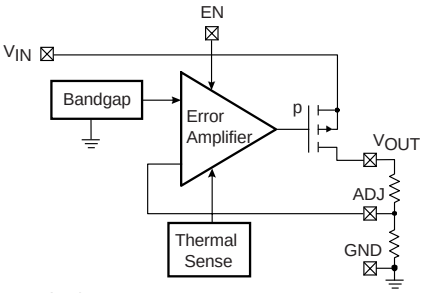
FAN2510: pin 4 – ADJ, allowing the user to adjust the output voltage over a wide range using an external voltage divider.

FAN2510-XX: pin 4 – BYP, to which a bypass capacitor may be connected for optimal noise performance. Output voltage is fixed, indicated by the suffix XX.

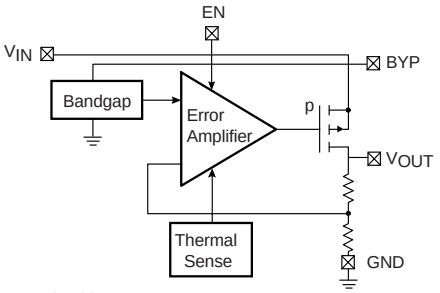
FAN2511-XX: pin 4 – $\overline{ERR}$, a flag which indicates that the output voltage has dropped below the specified minimum due to a fault condition.

The standard fixed output voltages available are 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 3.0V, and 3.3V. Custom output voltage are also available: please contact your local Fairchild Sales Office for information.

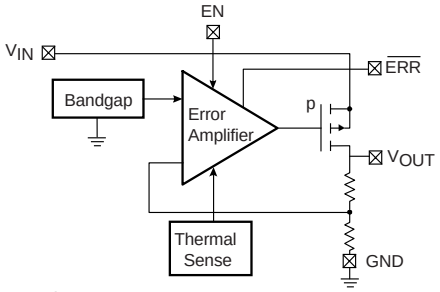
Block Diagrams



FAN2510

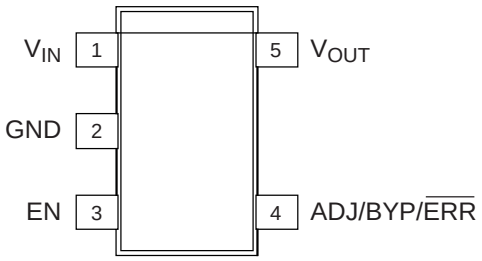


FAN25100-XX



FAN2511-XX

Pin Assignments



Pin No.	FAN2510	FAN2510-XX	FAN2511-XX
1.	V_{IN}	V_{IN}	V_{IN}
2.	GND	GND	GND
3.	EN	EN	EN
4.	ADJ	BYP	$\overline{ERR}$
5.	V_{OUT}	V_{OUT}	V_{OUT}

Pin Descriptions

Pin Name	Pin No.	Type	Pin Function Description
ADJ	4	Input	**FAN2510 Adjust.** Ratio of potential divider from VOUT to ADJ determines output voltage.
BYP	4	Passive	**FAN2510-XX Bypass.** Connect 470 pF capacitor for noise reduction.
$\overline{ERR}$	4	Open drain	**FAN2511-XX Error.** Error flag output. **0:** Output voltage < 95% of nominal. **1:** Output voltage > 95% of nominal.
EN	3	Digital Input	**Enable.** **0:** Shutdown V_{OUT}. **1:** Enable V_{OUT}.
V_{IN}	1	Power in	**Voltage Input.** Supply voltage input.
V_{OUT}	5	Power out	**Voltage Output.** Regulated output voltage.
GND	2	Power	**Ground.**

Functional Description

Designed utilizing CMOS process technology, the FAN2510/11 family of products are carefully optimized for use in compact battery-powered devices, offering a unique combination of low power consumption, extremely low dropout voltages, high tolerance for a variety of output capacitors, and the ability to disable the output to less than 1µA under user control. In the circuit, a difference amplifier controls the current through a series-pass P-Channel MOSFET, comparing the load voltage at the output with an onboard low-drift bandgap reference. The series resistance of the pass P-Channel MOSFET is approximately 1Ω, resulting in an unusually low dropout voltage under load when compared to older bipolar pass-transistor designs.

Protection circuitry is provided onboard for overload conditions. In conditions where the device reaches temperatures exceeding the specified maximums, an onboard circuit shuts down the output, where it remains suspended until it has cooled before re-enabling. The user is also free to shut down the device using the Enable control pin at any time.

Careful design of the output regulator amplifier assures loop stability over a wide range of ESR values in the external output capacitor. A wide range of values and types can be accommodated, allowing the user to select a capacitor meeting his space, cost, and performance requirements, and enjoy reliable operation over temperature, load, and tolerance variations.

An Enable pin, available on all devices, allows the user to shut down the regulator output to conserve power, reducing supply current to less than 1µA. The output can then be re-Enabled within 500µSec, fulfilling the fast power-cycling needs of CDMA applications. Depending on the model selected, other control and status functions are available at pin 4 to enhance the operation of the device. The adjustable-voltage versions utilize pin 4 to connect to an external voltage divider which feeds back to the regulator error amplifier, thereby setting the voltage as desired. Two other functions are available in the fixed-voltage versions: in noise-sensitive applications, an external Bypass capacitor connection is provided that allows the user to achieve optimal noise performance at the output, while the Error output functions as a diagnostic flag to indicate that the output voltage has dropped more than 5% below the nominal fixed voltage.

Applications Information

External Capacitors – Selection

The FAN2510/11 allows the user to utilize a wide variety of capacitors compared to other LDO products. An innovative design approach offers significantly reduced sensitivity to ESR (Effective Series Resistance), which degrades regulator loop stability in older designs. While the improvements featured in the FAN2510/11 family greatly simplify the design task, capacitor quality still must be considered if the designer is to achieve optimal circuit performance. In general, ceramic capacitors offer superior ESR performance, at a lower cost and a smaller case size than tantalums. Those with X7R or Y5Vdielectric offer the best temperature coefficient characteristics. The combination of tolerance and variation over temperature in some capacitor types can result in significant variations, resulting in unstable performance over rated conditions.

Input Capacitor

An input capacitor of 2.2µF (nominal value) or greater, connected between the Input pin and Ground, located in close proximity to the device, will improve transient response and noise rejection. Higher values will offer superior input ripple rejection and transient response. An input capacitor is recommended when the input source, either a battery or a regulated AC voltage, is located far from the device. Any good quality ceramic, tantalum, or metal film capacitor will give acceptable performance, however tantalum capacitors with a surge current rating appropriate to the application must be selected to avoid catastrophic failure.

Output Capacitor

An output capacitor is required to maintain regulator loop stability. Unlike many other LDO regulators, the FAN2510/11 family of products are nearly insensitive to output capacitor ESR. Stable operation will be achieved with a wide variety of capacitors with ESR values ranging from 10mΩ to 10Ω or more. Tantalum or aluminum electrolytic, or multilayer ceramic types can all be used. A nominal value of at least 1µF is recommended.

Bypass Capacitor (FAN2510 Only)

In the fixed-voltage configuration, connecting a capacitor between the bypass pin and ground can significantly reduce noise on the output. Values ranging from 470pF to 10nF can be used, depending on the sensitivity to output noise in the application.

At the high-impedance Bypass pin, care must be taken in the circuit layout to minimize noise pickup, and capacitors must be selected to minimize current loading (leakage). Noise pickup from external sources can be considerable. Leakage currents into the Bypass pin will directly affect regulator accuracy and should be kept as low as possible; thus, high-quality ceramic and film types are recommended for their low leakage characteristics. Cost-sensitive applications not concerned with noise can omit this capacitor.

Control Functions

Enable Pin

Applying a voltage of 0.4V or less at the Enable pin will disable the output, reducing the quiescent output current to less than 1µA, while a voltage of 2.0V or greater will enable the device. If this shutdown function is not needed, the pin can simply be connected to the V_{IN} pin. Allowing this pin to float will cause erratic operation.

Error Flag (FAN2511 Only)

To indicate conditions such as input voltage dropout (low V_{IN}), overheating, or overloading (excessive output current), the $\overline{ERR}$ pin indicates a fault condition. It is an open-drain output which is HIGH when the voltage at V_{OUT} is greater than 95% of the nominal rated output voltage and LOW when V_{OUT} is less than 95% or the rated output voltage, as specified in the error trip level characteristics.

A logic pullup resistor of 100KΩ is recommended at this output. The pin can be left disconnected if unused.

Thermal Protection

The FAN2510/11 is designed to supply high peak output currents of up to 1A for brief periods, however this output load will cause the device temperature to increase and exceed maximum ratings due to power dissipation. During output overload conditions, when the die temperature exceeds the shutdown limit temperature of 150°C, onboard thermal protection will disable the output until the temperature drops below this limit, at which point the output is then re-enabled. During a thermal shutdown situation the user may assert the power-down function at the Enable pin, reducing power consumption to the minimum level $I_{GND} \cdot V_{IN}$.

Thermal Characteristics

The FAN2510/11 is designed to supply 100mA at the specified output voltage with an operating die (junction) temperature of up to 125°C. Once the power dissipation and thermal resistance is known, the maximum junction temperature of the device can be calculated. While the power dissipation is calculated from known electrical parameters, the thermal resistance is a result of the thermal characteristics of the compact SOT23-5 surface-mount package and the surrounding PC Board copper to which it is mounted.

The power dissipation is equal to the product of the input-to-output voltage differential and the output current plus the ground current multiplied by the input voltage, or:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN}I_{GND}$$

The ground pin current I_{GND} can be found in the charts provided in the Electrical Characteristics section.

The relationship describing the thermal behavior of the package is:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die, which is 125°C, and T_A is the ambient operating temperature. θ_{JA} is dependent on the surrounding PC board layout and can be empirically obtained. While the θ_{JC} (junction-to-case) of the SOT23-5 package is specified at 130°C /W, the θ_{JA} of the minimum PWB footprint will be at least 235°C /W. This can be improved upon by providing a heat sink of surrounding copper ground on the PWB. Depending on the size of the copper area, the resulting θ_{JA} can range from approximately 180°C /W for one square inch to nearly 130°C /W for 4 square inches. The addition of backside copper with through-holes, stiffeners, and other enhancements can also aid in reducing this value. The heat contributed by the dissipation of other devices located nearby must be included in design considerations.

Once the limiting parameters in these two relationships have been determined, the design can be modified to ensure that the device remains within specified operating conditions. If overload conditions are not considered, it is possible for the device to enter a thermal cycling loop, in which the circuit enters a shutdown condition, cools, re-enables, and then again overheats and shuts down repeatedly due to an unmanaged fault condition.

Operation of Adjustable Version

The adjustable version of the FAN2510/11 includes an input pin ADJ which allows the user to select an output voltage ranging from 1.8V to near V_{IN}, using an external resistor divider. The voltage V_{ADJ} presented to the ADJ pin is fed to the onboard error amplifier which adjusts the output voltage until V_{ADJ} is equal to the onboard bandgap reference voltage of 1.32V(typ). The equation is:

$$V_{OUT} = 1.32V \times \left[1 + \frac{R_{upper}}{R_{lower}} \right]$$

The total value of the resistor chain should not exceed 250KΩ total to keep the error amplifier biased during no-load conditions. Programming output voltages very near V_{IN} need to allow for the magnitude and variation of the dropout voltage V_{DO} over load, supply, and temperature variations. Note that the low-leakage FET input to the CMOS Error Amplifier induces no bias current error to the calculation.

General PWB Layout Considerations

To achieve the full performance of the device, careful circuit layout and grounding technique must be observed. Establishing a small local ground, to which the GND pin, the output and bypass capacitors are connected, is recommended, while the input capacitor should be grounded to the main ground plane. The quiet local ground is then routed back to the main ground plane using feedthrough vias. In general, the high-frequency compensation components (input, bypass, and output capacitors) should be located as close to the device as possible. The proximity of the output capacitor is especially important to achieve optimal noise compensation from the onboard error amplifier, especially during high load conditions. A large copper area in the local ground will provide the heat sinking discussed above when high power dissipation significantly increases the temperature of the device. Component-side copper provides significantly better thermal performance for this surface-mount device, compared to that obtained when using only copper planes on the underside.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{IN} (Measured to GND)	0		7	V
Enable Input (EN)				
Applied voltage (Measured to GND)[2]	0		7	V
$\overline{ERR}$ Output				
Applied voltage (Measured to GND)[2]	0		7	V
Power				
Dissipation[3]	Internally limited			
Temperature				
Junction	-65		150	°C
Lead Soldering (5 seconds)			260	°C
Storage	-65		150	°C
Electrostatic Discharge[4]	4			kV

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Based upon thermally limited junction temperature:

$$P_D = \frac{T_{J(max)} - T_A}{\Theta_{JA}}$$

4. Human Body Model is 4kV minimum using Mil Std. 883E, method 3015.7. Machine Model is 400V minimum using JEDEC method A115-A.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Units
V_{IN}	Input Voltage Range	2.7		6.5	V
V_{OUT}	Output Voltage Range, Adjustable	V_{REF}		V_{IN}-V_{DO}	V
V_{EN}	Enable Input Voltage	0		V_{IN}	V
V_{ERR}	$\overline{ERR}$ Flag Voltage			V_{IN}	V
T_J	Junction Temperature	-40		+125	°C
θ_{JA}	Thermal resistance		220		°C/W
θ_{JC}	Thermal resistance		130		°C/W

Electrical Characteristics (Notes 1, 2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Regulator						
V_{DO}	Drop Out Voltage	I_{OUT} = 100 µA		2.5	4	mV
		I_{OUT} = 50 mA		50	75	mV
		I_{OUT} = 100 mA		100	140	mV
ΔV_O	Output Voltage Accuracy		**-2**		**2**	%
V_{DO}	Reference Voltage Accuracy, Adjustable Mode		1.24	1.32	1.40	V
ΔV_O[3]	Output Voltage Accuracy, Adjustable Mode		-6		6	%
I_{GND}	Ground Pin Current	I_{OUT} = 100 mA			50	µA
Protection						
	Current Limit	Thermally Protected				
I_{GSD}	Shut-Down Current	EN = 0V			1	µA
T_{SH}	Thermal Protection Shutdown Temperature		150			°C
E_{TL}	$\overline{ERR}$ Trip Level	FAN2511 only	90	95	99	%
Enable Input						
V_{IL}	Logic Low Voltage			1.2	**0.4**	V
V_{IH}	Logic High Voltage		**2.0**	1.4		V
I_{IH}	Input Current High				1	µA
I_I	Input Current Low				1	µA

Switching Characteristics (Notes 1, 2)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Enable Input[4]					
Response time				500	µsec
Error Flag (FAN2511-XX)					
Response time				3	msec

Performance Characteristics (Notes 1, 2)

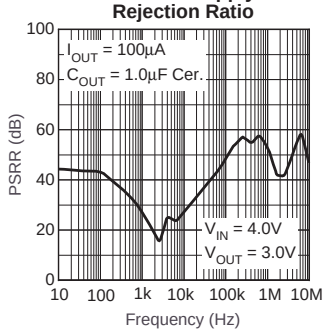
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{IN} = (V_{OUT} + 1) to 6.5V		0.3		%/V
$\Delta V_{OUT}/V_{OUT}$	Load regulation	I_{OUT} = 0.1 to 100mA		1.0	2.0	%
e_N	Output noise	10Hz–1KHz C_{OUT} = 10µF, C_{BYP} = 0.01µF		<7		µV/$\sqrt{Hz}$
		>10KHz, C_{OUT} = 10µF, C_{BYP} = 0.01µF		<0.01		
PSRR	Power Supply Rejection	120 Hz, C_{OUT} = 10µF, C_{BYP} = 0.01µF		43		dB

Notes:

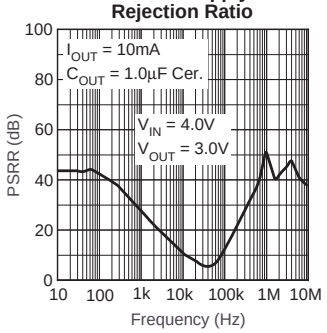
1. Unless otherwise stated, T_A = 25°C, V_{IN} = V_{OUT} + 1V, I_{OUT} = 100µA, V_{IH} > 2.0 V.
2. Bold values indicate -40 ≤ T_J ≤ 125°C.
3. The adjustable version, has a bandgap voltage range of 1.24V to 1.40V with a nominal value of 1.32V.
4. When using repeated cycling.

Typical Performance Characteristics

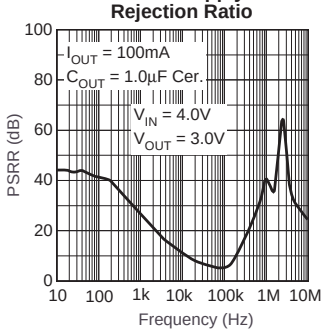
Power Supply Rejection Ratio



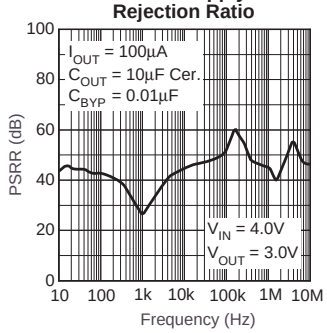
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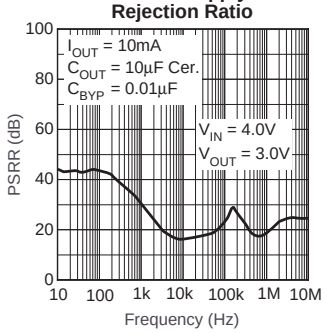
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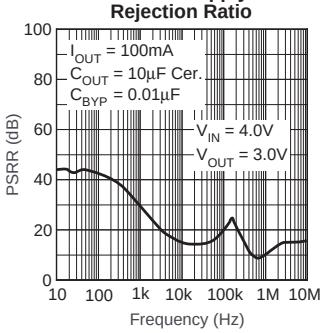
Power Supply Rejection Ratio



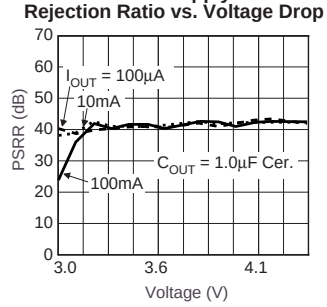
Power Supply Rejection Ratio



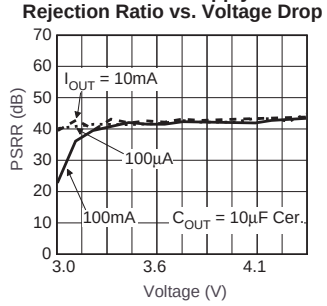
Power Supply Rejection Ratio



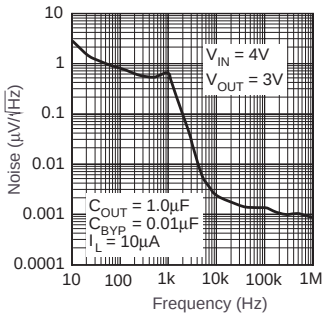
Power Supply Rejection Ratio vs. Voltage Drop



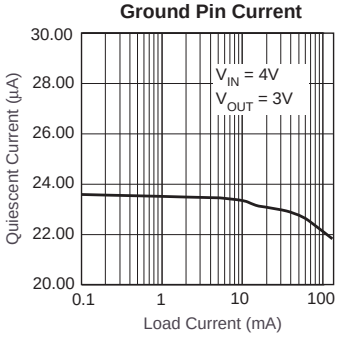
Power Supply Rejection Ratio vs. Voltage Drop



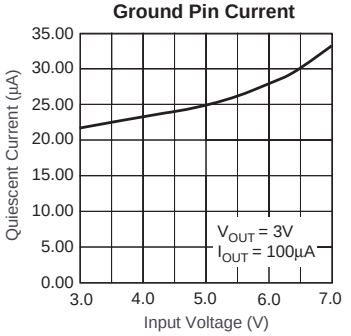
Noise Performance



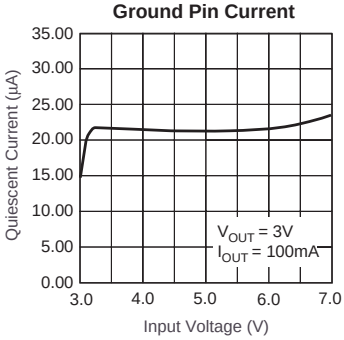
Ground Pin Current



Ground Pin Current



Ground Pin Current



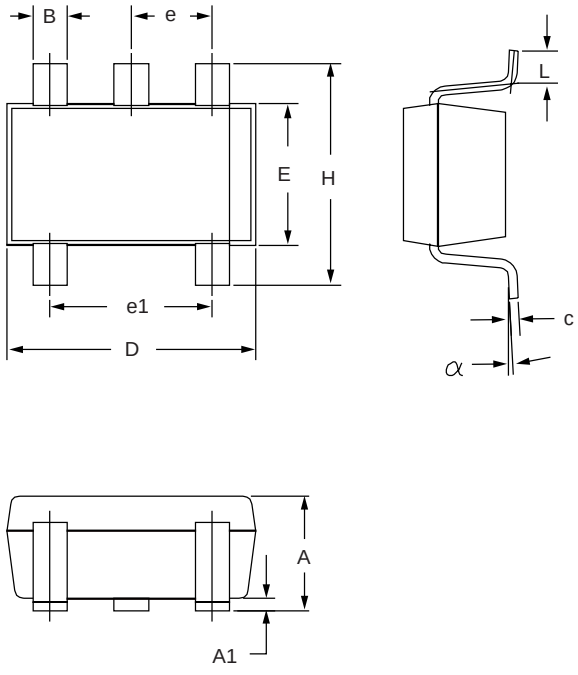
Mechanical Dimensions

5-Lead SOT-23-5 (S) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.035	.057	.90	1.45	
A1	.000	.006	.00	.15	
B	.008	.020	.20	.50	
c	.003	.010	.08	.25	
D	.106	.122	2.70	3.10	
E	.059	.071	1.50	1.80	
e	.037 BSC		.95 BSC		
e1	.075 BSC		1.90 BSC		
H	.087	.126	2.20	3.20	
L	.004	.024	.10	.60	
α	0°	10°	0°	10°	

Notes:

1. Package outline exclusive of mold flash & metal burr.
2. Package outline exclusive of solder plating.
3. EIAJ Ref Number SC-74A.



Ordering Information

Product Number	V_{OUT}	Pin 4 Function	Package Marking
FAN2510SX	Adj.	Adjust	ANA

Tape and Reel Information

Quantity	Reel Size	Width
3000	7"	8mm

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