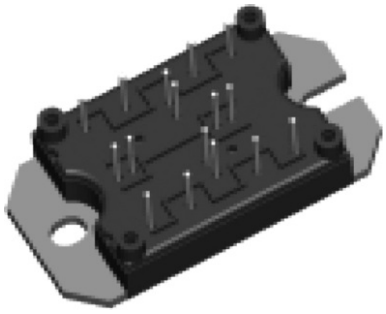
"Full Bridge" FREDFET MTP (Power MOSFET), 31 A



MTP

FEATURES

- Low on-resistance
- High performance optimized built-in fast recovery diodes
- Fully characterized capacitance and avalanche voltage and current
- Al_2O_3 DBC
- Very low stray inductance design for high speed operation
- UL approved file E78996
- Compliant to RoHS directive 2002/95/EC

Pb-free
RoHS COMPLIANT

BENEFITS

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Low t_{rr} and soft diode reverse recovery
- Optimized for welding, UPS and SMPS applications
- Outstanding ZVS and high frequency operation
- Direct mounting to heatsink
- PCB solderable terminals
- Very low junction to case thermal resistance

PRODUCT SUMMARY	
V_{DSS}	500 V
$R_{DS(on)}$	0.25 Ω
I_D	31 A
Type	Modules - MOSFET
Package	MTP

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at V_{GS} 10 V	I_D	T_C = 25 °C	31	A
		T_C = 100 °C	19	
Pulsed drain current	I_{DM} (1)		124	
Maximum power dissipation	P_D	T_C = 25 °C	1140	W
		T_C = 100 °C	456	
Gate to source voltage	V_{GS}		± 30	V
RMS isolation voltage	V_{ISOL}	Any terminal to case, t = 1 min	2500	
Peak diode recovery dV/dt	dV/dt (2)		15	V/ns
Operating junction temperature range	T_J		- 55 to + 150	°C
Operating storage temperature range	T_{Stg}		- 55 to + 125	°C

Notes

(1) Repetitive rating; pulse width limited by maximum junction temperature

(2) $I_{SD} \leq 31$ A, dI/dt ≤ 340 A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150$ °C

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DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
Temperature coefficient of breakdown voltage	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 4 mA, reference to T_J = 25 °C	-	0.48	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}$ (1)	V_{GS} = 10 V, I_D = 19 A	-	0.19	0.22	Ω
		V_{GS} = 10 V, I_D = 31 A	-	0.21	0.25	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3.0	-	6.0	V
Drain to source leakage current	I_{DSS} (2)	V_{DS} = 500 V, V_{GS} = 0 V	-	-	50	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	2	mA
Gate to source forward leakage	I_{GSS}	V_{GS} = 30 V	-	-	150	nA
Gate to source reverse leakage		V_{GS} = - 30 V	-	-	- 150	

Notes

(1) Pulse width ≤ 400 µs, duty cycle ≤ 2 %

(2) I_{CES} includes also opposite leg overall leakage

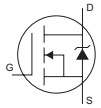
DYNAMIC CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 19 A	-	26	-	S
Total gate charge	Q_g (1)	I_D = 31 A V_{DS} = 400 V V_{GS} = 10 V	-	105	160	nC
Gate to source charge	Q_{gs} (1)		-	36	55	
Gate to drain ("Miller") charge	Q_{gd} (1)		-	46	70	
Turn-on delay time	$t_{d(on)}$	I_D = 31 A V_{DS} = 250 V V_{GS} = 10 V R_g = 4.3 Ω	-	49	74	ns
Turn-off delay time	$t_{d(off)}$		-	80	120	
Rise time	t_r		-	165	250	
Fall time	t_f		-	76	115	
Input capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1.0 MHz	-	4808	7210	pF
Output capacitance	C_{oss}		-	1165	1750	
Reverse transfer capacitance	C_{rss}		-	40	60	

Note

(1) Pulse width ≤ 400 µs, duty cycle ≤ 2 %

DIODE CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	31	A
Pulsed source current (body diode)	I_{SM} (1)		-	-	124	
Diode forward voltage	V_{SD} (2)	T_J = 25 °C, I_S = 31 A, V_{GS} = 0 V	-	1.01	1.1	V
Reverse recovery time	t_{rr}	T_J = 125 °C, I_F = 31 A; dI/dt = 100 A/µs (2)	-	252	378	ns
Reverse recovery charge	Q_{rr}		-	1619	2428	nC

Notes

(1) Repetitive rating; pulse width limited by maximum junction temperature

(2) Pulse width ≤ 400 µs, duty cycle ≤ 2 %

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Document Number: 94546
Revision: 12-May-10

AVALANCHE CHARACTERISTICS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Single pulse avalanche energy	E_{AS} (1)	-	-	493	mJ
Avalanche current	I_{AR} (2)	-	-	31	A
Repetitive avalanche energy	E_{AR} (2)	-	-	114	mJ

Notes

(1) Starting T_J = 25 °C, L = 1.0 mH, R_g = 25 Ω, I_{AS} = 31 A

(2) Repetitive rating; pulse width limited by maximum junction temperature

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Operating junction temperature range	T_J		- 40	-	150	°C
Storage temperature range	T_{Stg}		- 40	-	125	
Junction to case per MOSFET	R_{thJC}		-	-	0.44	°C/W
Case to sink	R_{thCS}	Heatsink compound thermal conductivity = 1 W/mK	-	0.06	-	
Clearance (1)		External shortest distance in air between 2 terminals	5.5	-	-	mm
Creepage (1)		Shortest distance along external surface of the insulating material between 2 terminals	8	-	-	
Weight			-	66	-	g

Note

(1) Standard version only i.e. without optional thermistor

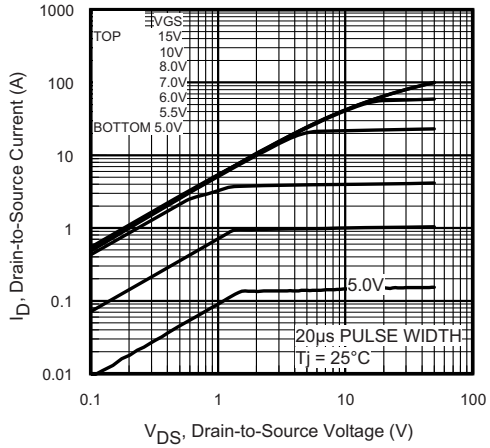


Fig. 1 - Typical Output Characteristics

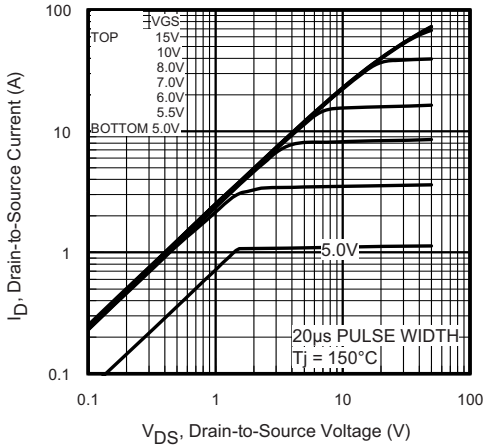


Fig. 2 - Typical Output Characteristics

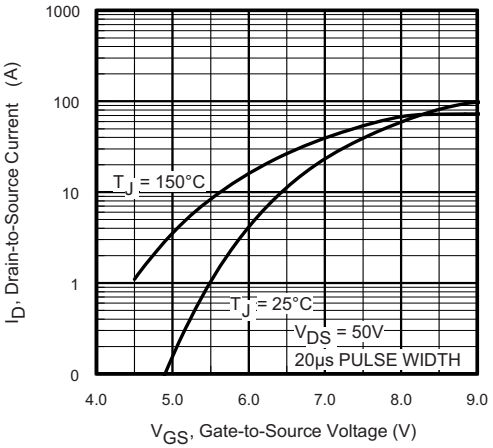


Fig. 3 - Typical Transfer Characteristics

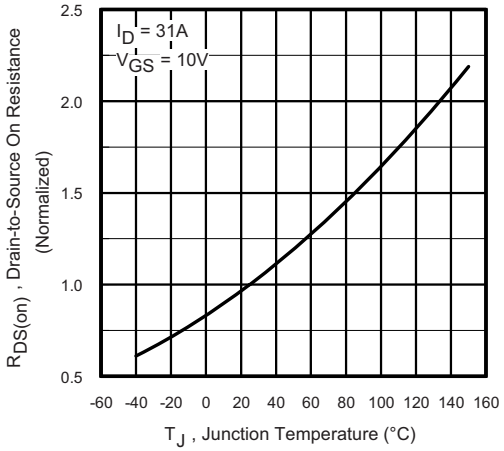


Fig. 4 - Normalized On-Resistance vs. Temperature

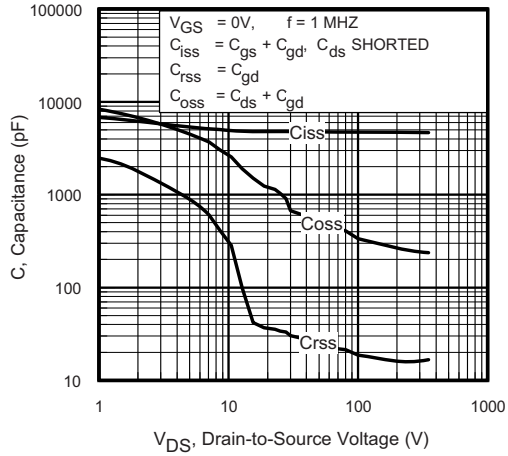


Fig. 5 - Typical Capacitance vs.
Drain to Source Voltage

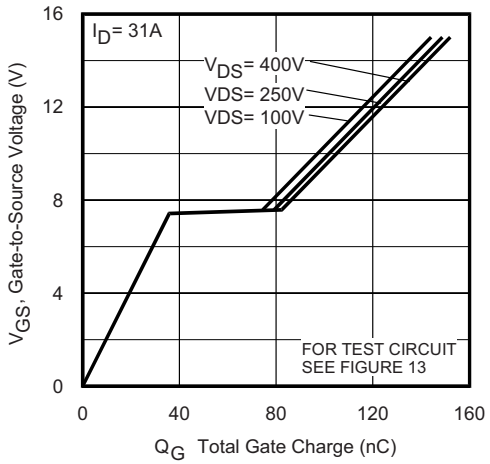


Fig. 6 - Typical Gate Charge vs.
Gate to Source Voltage

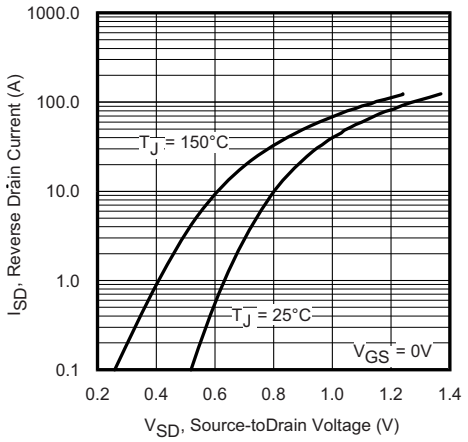


Fig. 7 - Typical Source Drain Diode Forward Voltage

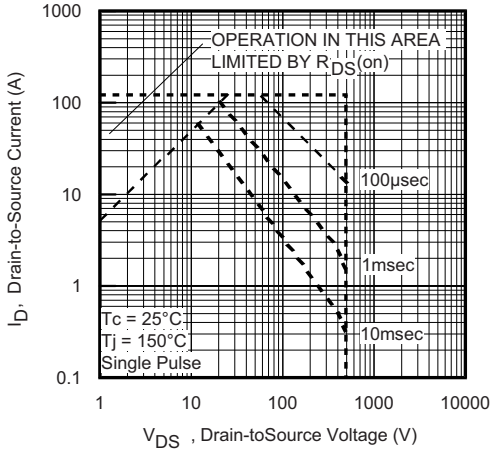


Fig. 8 - Maximum Safe Operating Area

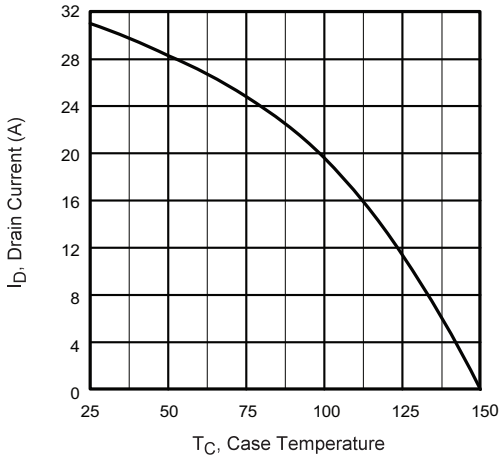


Fig. 9 - Maximum Drain Current vs. Case Temperature

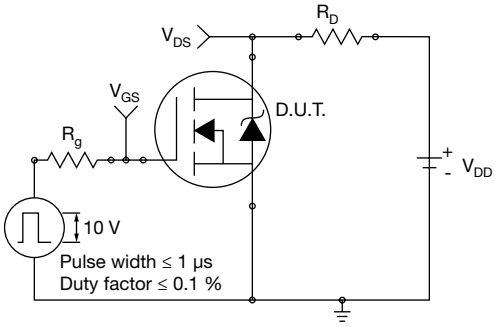


Fig. 10a - Switching Time Test Circuit

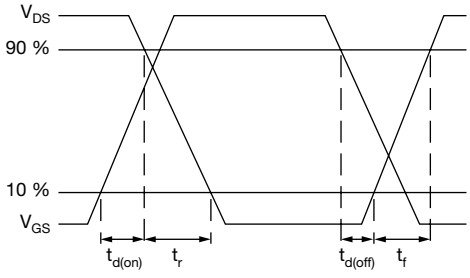


Fig. 10b - Switching Time Waveforms

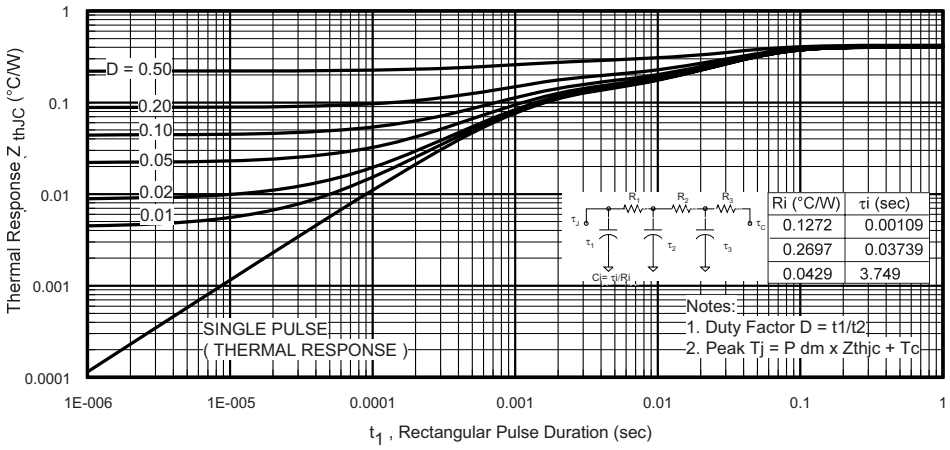


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

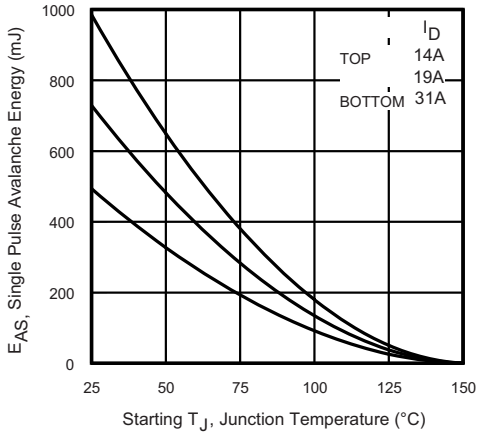


Fig. 12a - Maximum Avalanche Energy vs. Drain Current

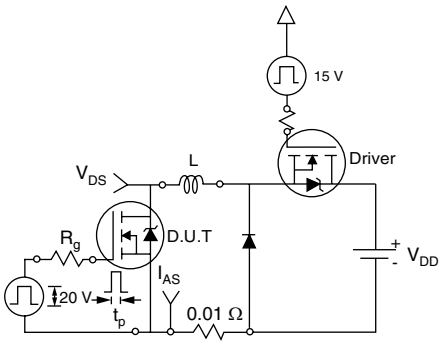


Fig. 12b - Unclamped Inductive Test Circuit

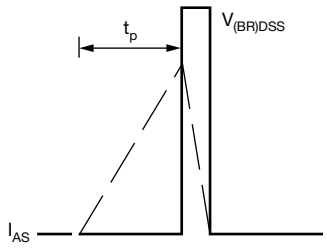


Fig. 12c - Unclamped Inductive Waveforms

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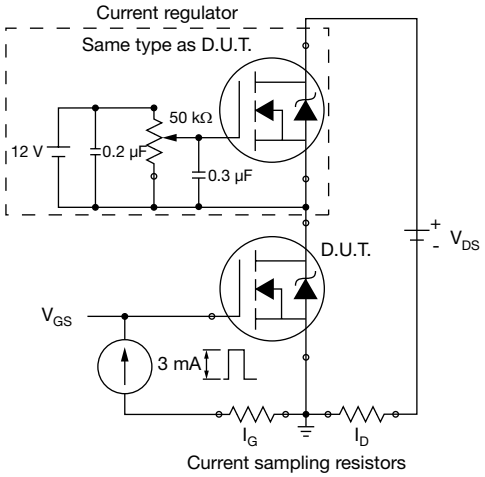


Fig. 13a - Gate Charge Test Circuit

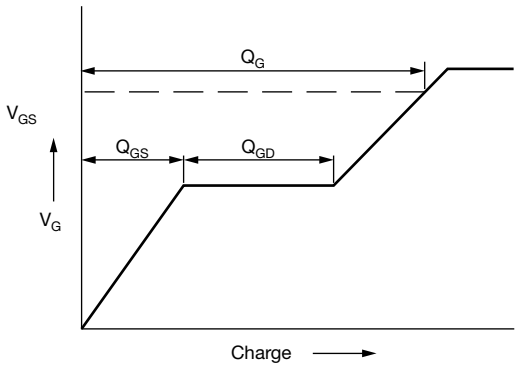


Fig. 13b - Basic Gate Charge Waveform

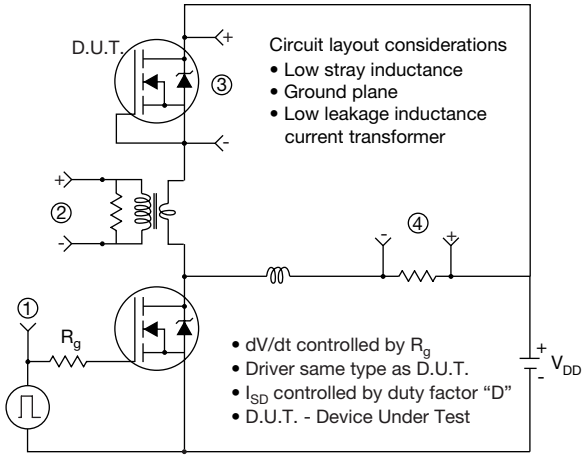
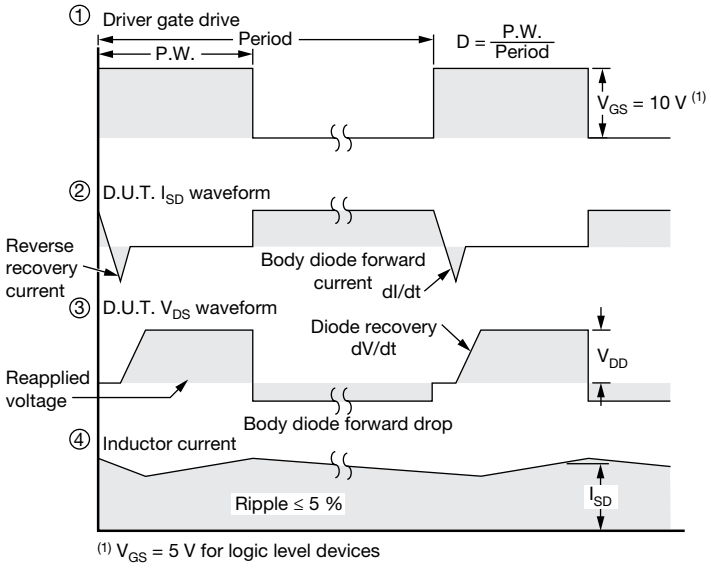


Fig. 14 - Peak Diode Recovery dV/dt Test Circuit



(1) V_{GS} = 5 V for logic level devices

Fig. 15 - For N-Channel Power MOSFETs

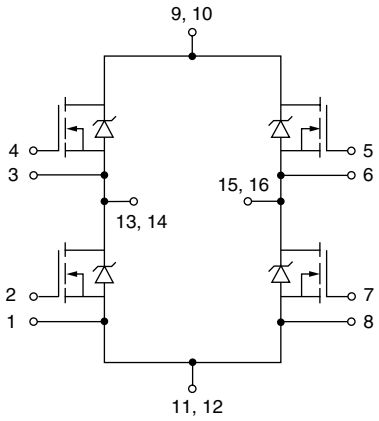


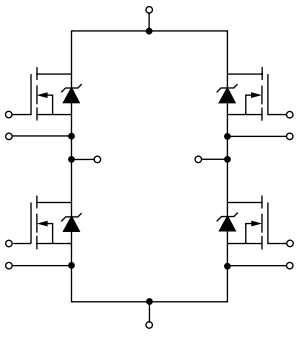
Fig. 16 - Electrical diagram

ORDERING INFORMATION TABLE

Device code

19	MT	050	X	F	A	PbF
1	2	3	4	5	6	7

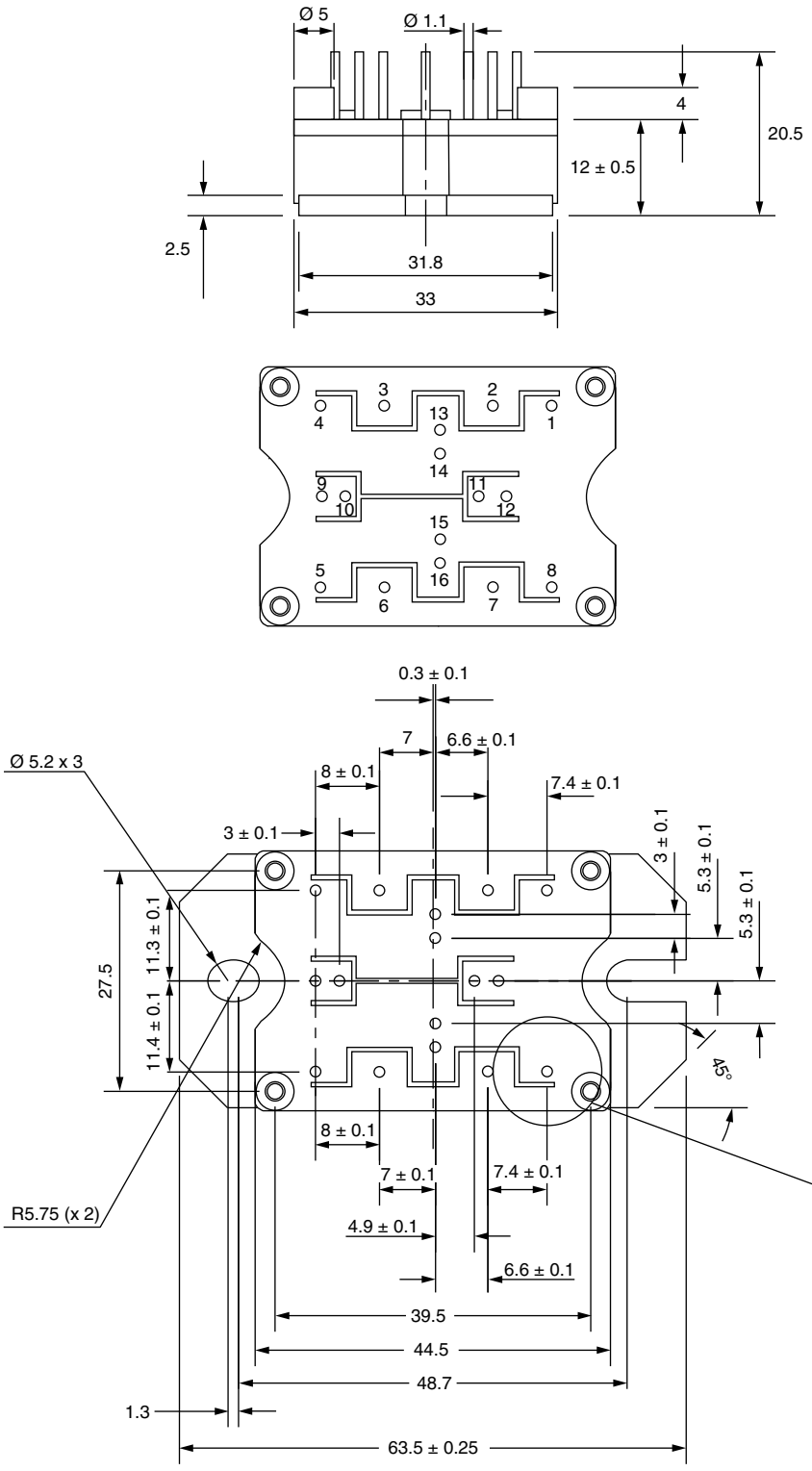
- 1 - Current rating
- 2 - Essential part number
- 3 - Voltage code (050 = 500 V)
- 4 - Speed/type (X = Power MOSFET)
- 5 - Circuit configuration
  (F = Full bridge - see Circuit Configuration table)
- 6 - A = Al_2O_3 DBC substrate
- 7 - PbF = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Full bridge	F	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95245

MTP MOSFET/IGBT Full-Bridge

DIMENSIONS in millimeters



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ООО «НИОКР СИТЕМС»
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Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
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