CC1150
Low Power Sub-1 GHz RF Transmitter

Applications

- *Ultra low power UHF wireless transmitters*
- *Operating in the 315/433/868/915 MHz ISM/SRD bands*
- *AMR – Automatic Meter Reading*
- *Consumer Electronics*
- *RKE – Remote Keyless Entry*
- *Low power telemetry*
- *Home and building automation*
- *Wireless alarm and security systems*
- *Industrial monitoring and control*
- *Wireless sensor networks*

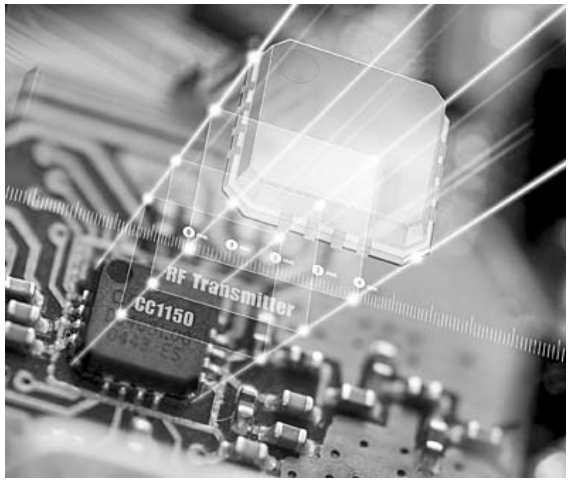
Product Description

The ***CC1150*** is a low cost true single chip UHF transmitter designed for very low power wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 315, 433, 868 and 915 MHz, but can easily be programmed for operation at other frequencies in the 300-348 MHz, 400-464 MHz and 800-928 MHz bands.

The RF transmitter is integrated with a highly configurable baseband modulator. The modulator supports various modulation formats and has a configurable data rate up to 500 kBaud. The ***CC1150*** provides extensive hardware support for packet handling, data buffering and burst transmissions.

The main operating parameters and the 64-byte transmit FIFO of ***CC1150*** can be controlled via an SPI interface. In a typical system, the ***CC1150*** will be used together with a micro-controller and a few additional passive components.

CC1150 is part of Chipcon's SmartRF®04 technology platform based on 0.18 µm CMOS technology.



Key Features

- Small size (QLP 4x4 mm package, 16 pins)
- True single chip UHF RF transmitter
- Frequency bands: 300-348 MHz, 400-464 MHz and 800-928 MHz
- Programmable data rate up to 500 kBaud
- Low current consumption
- Programmable output power up to +10 dBm for all supported frequencies
- Programmable baseband modulator
- Ideal for multi-channel operation
- Very few external components: Completely on-chip frequency synthesizer, no external filters needed
- Configurable packet handling hardware
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer
- Optional Forward Error Correction with interleaving
- 64-byte TX data FIFO

Features (continued from front page)

- Suited for systems compliant with EN 300 220 and FCC CFR Part 15
- Many powerful digital features allow a high-performance RF system to be made using an inexpensive microcontroller
- Efficient SPI interface: All registers can be programmed with one “burst” transfer
- Integrated analog temperature sensor
- Lead-free “green” package
- Flexible support for packet oriented systems: On chip support for sync word insertion, flexible packet length and automatic CRC handling
- OOK and flexible ASK shaping supported
- 2-FSK, GFSK and MSK supported
- Optional automatic whitening of data
- Support for asynchronous transparent transmit mode for backwards compatibility with existing radio communication protocols

Abbreviations

Abbreviations used in this data sheet are described below.

ADC	Analog to Digital Converter
AFC	Automatic Frequency Compensation
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
ASK	Amplitude Shift Keying
BER	Bit Error Rate
CCA	Clear Channel Assessment
CFR	Code of Federal Regulations
CRC	Cyclic Redundancy Check
CW	Contionus Wave (Unmodulated Carrier)
DC	Direct Current
EIRP	Equivalent Isotropic Radiated Power
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FEC	Forward Error Correction
FIFO	First-In-First-Out
FSK	Frequency Shift Keying
GFSK	Gaussian shaped Frequency Shift Keying
ISM	Industrial, Scientific, Medical
LC	Inductor-Capacitor
LO	Local Oscillator
LSB	Least Significant Byte
LQI	Link Quality Indicator
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
N/A	Not Applicable
NRZ	Non Return to Zero (Coding)
OOK	On-Off-Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
POR	Power-On Reset
QLP	Quad Leadless Package
QPSK	Quadrature Phase Shift Keying
RC	Resistor-Capacitor
RCOSC	RC Oscillator
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive, Receive Mode
SAW	Surface Aqustic Wave
SMD	Surface Mount Device
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SRD	Short Range Devices
TBD	To Be Defined
TX	Transmit, Transmit Mode
UHF	Ultra High frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XTAL	Crystal

Table Of Contents

APPLICATIONS **1**
PRODUCT DESCRIPTION **1**
KEY FEATURES **1**
FEATURES (CONTINUED FROM FRONT PAGE) **2**
ABBREVIATIONS 2
TABLE OF CONTENTS **3**
1 ABSOLUTE MAXIMUM RATINGS 5
2 OPERATING CONDITIONS 5
3 GENERAL CHARACTERISTICS 5
4 ELECTRICAL SPECIFICATIONS 6
4.1 CURRENT CONSUMPTION 6
4.2 RF TRANSMIT SECTION 7
4.3 CRYSTAL OSCILLATOR 8
4.4 FREQUENCY SYNTHESIZER CHARACTERISTICS 8
4.5 ANALOG TEMPERATURE SENSOR 9
4.6 DC CHARACTERISTICS 9
4.7 POWER ON RESET 9
5 PIN CONFIGURATION 10
6 CIRCUIT DESCRIPTION 11
7 APPLICATION CIRCUIT 11
7.1 BIAS RESISTOR 11
7.2 BALUN AND RF MATCHING 11
7.3 CRYSTAL 12
7.4 REFERENCE SIGNAL 12
7.5 ADDITIONAL FILTERING 12
7.6 POWER SUPPLY DECOUPLING 12
7.7 ANTENNA CONSIDERATIONS 13
7.8 PCB LAYOUT RECOMMENDATIONS 15
8 CONFIGURATION OVERVIEW 16
9 CONFIGURATION SOFTWARE 17
10 4-WIRE SERIAL CONFIGURATION AND DATA INTERFACE 18
10.1 CHIP STATUS BYTE 19
10.2 REGISTER ACCESS 20
10.3 SPI READ 20
10.4 COMMAND STROBES 20
10.5 FIFO ACCESS 21
10.6 PATABLE ACCESS 22
11 MICROCONTROLLER INTERFACE AND PIN CONFIGURATION 22
11.1 CONFIGURATION INTERFACE 22
11.2 GENERAL CONTROL AND STATUS PINS 22
11.3 OPTIONAL RADIO CONTROL FEATURE 23
12 DATA RATE PROGRAMMING 23
13 PACKET HANDLING HARDWARE SUPPORT 24
13.1 DATA WHITENING 24
13.2 PACKET FORMAT 25
13.3 PACKET HANDLING IN TRANSMIT MODE 26
13.4 PACKET HANDLING IN FIRMWARE 26
14 MODULATION FORMATS 27
14.1 FREQUENCY SHIFT KEYING 27
14.2 MINIMUM SHIFT KEYING 27
14.3 AMPLITUDE MODULATION 28
15 FORWARD ERROR CORRECTION WITH INTERLEAVING 28
15.1 FORWARD ERROR CORRECTION (FEC) 28
15.2 INTERLEAVING 28

16 RADIO CONTROL 30
16.1 POWER ON START-UP SEQUENCE 31
16.2 CRYSTAL CONTROL 31
16.3 VOLTAGE REGULATOR CONTROL 32
16.4 ACTIVE MODE 32
16.5 TIMING 32
17 DATA FIFO 33
18 FREQUENCY PROGRAMMING 34
19 VCO 34
19.1 VCO AND PLL SELF-CALIBRATION 34
20 VOLTAGE REGULATORS 35
21 OUTPUT POWER PROGRAMMING 35
21.1 SHAPING AND PA RAMPING 36
22 GENERAL PURPOSE / TEST OUTPUT CONTROL PINS 37
23 ASYNCHRONOUS AND SYNCHRONOUS SERIAL OPERATION 39
23.1 ASYNCHRONOUS SERIAL OPERATION 39
23.2 SYNCHRONOUS SERIAL OPERATION 39
24 SYSTEM CONSIDERATIONS AND GUIDELINES 39
24.1 SRD REGULATIONS 39
24.2 FREQUENCY HOPPING AND MULTI-CHANNEL SYSTEMS 40
24.3 WIDEBAND MODULATION NOT USING SPREAD SPECTRUM 40
24.4 DATA BURST TRANSMISSIONS 41
24.5 CONTINUOUS TRANSMISSIONS 41
24.6 LOW COST SYSTEMS 41
24.7 BATTERY OPERATED SYSTEMS 41
24.8 INCREASING OUTPUT POWER 41
25 CONFIGURATION REGISTERS 42
25.1 CONFIGURATION REGISTER DETAILS 45
25.2 STATUS REGISTER DETAILS 55
26 PACKAGE DESCRIPTION (QLP 16) 57
26.1 RECOMMENDED PCB LAYOUT FOR PACKAGE (QLP 16) 57
26.2 SOLDERING INFORMATION 57
27 REFERENCES 58
28 GENERAL INFORMATION 59
28.1 DOCUMENT HISTORY 59

1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.



Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.6	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3 max 3.6	V	
Voltage on the pins RF_P, RF_N and DCOUPL	–0.3	2.0	V	
Voltage ramp-up		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020C
ESD		<500	V	According to JEDEC STD 22, method A114, Human Body Model

Table 1: Absolute Maximum Ratings

2 Operating Conditions

The operating conditions for ***CC1150*** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	-40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	300		348	MHz	
	400		464	MHz	
	800		928	MHz	
Data rate	1.2		500	kBaud	2-FSK
	1.2		250	kBaud	GFSK, OOK and ASK
	26		500	kBaud	(Shaped) MSK (also known as differential offset QPSK)
					Optional Manchester encoding (the data rate in kbps will be half the baud rate)

Table 3: General Characteristics

4 Electrical Specifications

4.1 Current Consumption

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1150EM reference design ([1] and [2]).

Parameter	Min	Typ	Max	Unit	Condition
Current consumption		200		nA	Voltage regulator to digital part off, register values lost (SLEEP state)
		222		μA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
		1.1		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		7.7		mA	Only the frequency synthesizer running (FSTXON state). This current consumptions also representative for the other intermediate states when going from IDLE until reaching TX, and frequency calibration states
Current consumption, 315 MHz		25.6 14.1		mA	Transmit mode, +10 dBm output power (0xC4) Transmit mode, 0 dBm output power (0x60) See more in section 21 and DN012 [3]
Current consumption, 433 MHz		26.1 14.6		mA	Transmit mode, +10 dBm output power (0xC2) Transmit mode, 0 dBm output power (0x60) See more in section 21 and DN012 [3]
Current consumption, 868 MHz		29.3 15.5		mA	Transmit mode, +10 dBm output power (0xC3) Transmit mode, 0 dBm output power (0x60) See more in section 21 and DN012 [3]
Current consumption, 915 MHz		29.3 15.2		mA	Transmit mode, +10 dBm output power (0xC0) Transmit mode, 0 dBm output power (0x50) See more in section 21 and DN012 [3]

Table 4: Electrical Specifications

4.2 RF Transmit Section

Tc = 25°C, VDD = 3.0 V, if nothing else stated. All measurement results are obtained using the CC1150EM reference design ([1] and [2]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance 315 MHz 433 MHz 868/915 MHz		 122 + j31 116 + j41 86.5 + j43		 Ω Ω Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC1150EM reference design ([1] and [2]) available from the TI website.
Output power, highest setting		+10		dBm	Output power is programmable, and full range is available across all frequency bands. Output power may be restricted by regulatory limits. See also Application Note AN039 [4] and Design Note DN006 [5]. Delivered to a 50 Ω single-ended load via CC1150 EM reference design ([1] and [2]) RF matching network. Maximum output power can be increased 1-2 dB by using wire-wound inductors instead of multilayer inductors in the balun and filter circuit for the 868/915 MHz band, see more in DN017 [6].
Output power, lowest setting		–30		dBm	Output power is programmable, and full range is available across all frequency bands. Delivered to a 50 Ω single-ended load via CC1150 EM reference design ([1] and [2]) RF matching network
Spurious emissions and harmonics, 433/868 MHz			–36 –54 –30	dBm dBm dBm	25 MHz - 1 GHz 47-74, 87.5 - 118, 174 - 230, 470 - 862 MHz Otherwise above 1 GHz Note that close-in spurs vary with centre frequency and limits the frequencies and output power level which the CC1150 can operate at without violating regulatory restrictions, see more in AN039 [4]. See also section 7.5 for information regarding additional filtering.
Spurious emissions, 315/915 MHz			–49.2 –41.2	dBm EIRP dBm EIRP	<200 μV/m at 3 m below 960 MHz. <500 μV/m at 3 m above 960 MHz
Harmonics 315 MHz			–20 –41.2	dBc dBm	2nd, 3rd and 4th harmonic when the output power is maximum 6 mV/m at 3 m (-19.6 dBm EIRP) 5th harmonic
Harmonics 915 MHz			–20 –41.2	dBc dBm	2nd harmonic with +10 dBm output power 3rd, 4th and 5th harmonic
TX latency		8		Bits	Serial operation. Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports.

Table 5: RF Transmit Parameters

4.3 Crystal Oscillator

Tc = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC1150EM reference design ([1] and [2]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) aging and c) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		µs	Measured on the CC1150EM reference design ([1] and [2]). This parameter is to a large degree crystal dependent.

Table 6: Crystal Oscillator Parameters

4.4 Frequency Synthesizer Characteristics

Tc = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC1150EM reference design ([1] and [2]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26 MHz-27 MHz crystals. The resolution (in Hz) is equal for all frequency bands.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise		–82		dBc/Hz	@ 50 kHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–86		dBc/Hz	@ 100 kHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–90		dBc/Hz	@ 200 kHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–98		dBc/Hz	@ 500 kHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–106		dBc/Hz	@ 1 MHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–113		dBc/Hz	@ 2 MHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–119		dBc/Hz	@ 5 MHz offset from carrier, carrier at 868 MHz
RF carrier phase noise		–127		dBc/Hz	@ 10 MHz offset from carrier, carrier at 868 MHz
PLL turn-on / hop time	85.1	88.4	88.4	µs	Time from leaving the IDLE state until arriving in the FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL calibration time		18739		XOSC cycles	Calibration can be initiated manually or automatically before entering or after leaving TX.
	694	721	721	µs	Min/typ/max time is for 27/26/26 MHz crystal frequency.

Table 7: Frequency Synthesizer Parameters

4.5 Analog Temperature Sensor

Tc = 25°C, VDD = 3.0 V if nothing else is stated. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.651		V	
Output voltage at 0°C		0.747		V	
Output voltage at +40°C		0.847		V	
Output voltage at +80°C		0.945		V	
Temperature coefficient		2.45		mV/°C	Fitted from –20°C to +80°C
Absolute error in calculated temperature	–2 *		2 *	°C	From –20°C to +80°C when using 2.45 mV / °C, after 1-point calibration at room temperature * Indicated minimum and maximum error with 1-point calibration is based on simulated values for typical process parameters
Current consumption increase when enabled		0.3		mA	

Table 8: Analog Temperature Sensor Parameters

4.6 DC Characteristics

Tc = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	–1	μA	Input equals 0 V
Logic "1" input current	N/A	1	μA	Input equals VDD

Table 9: DC Characteristics

4.7 Power on Reset

For proper Power-On-Reset functionality, the power supply must comply with the requirements in Table 10 below. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See section 16.1 on page 31 for a description of the recommended start up sequence after turning power on.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0 V until reaching 1.8 V
Power off time	1			ms	Minimum time between power-on and power-off

Table 10: Power-on Reset Requirements

5 Pin Configuration

The *CC1150* pin-out is shown in Figure 1 and Table 11.

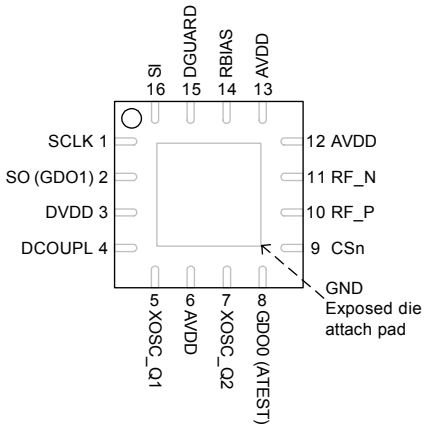


Figure 1: Pinout Top View

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

Pin #	Pin name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input.
2	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when CSn is high.
3	DVDD	Power (Digital)	1.8 V - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator.
4	DCOUPL	Power (Digital)	1.6 V - 2.0 V digital power supply output for decoupling. NOTE: This pin is intended for use with the *CC1150* only. It can not be used to provide supply voltage to other devices.
5	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input.
6	AVDD	Power (Analog)	1.8 V - 3.6 V analog power supply connection.
7	XOSC_Q2	Analog I/O	Crystal oscillator pin 2.
8	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial input TX data Also used as analog test I/O for prototype/production testing.
9	CSn	Digital Input	Serial configuration interface, chip select.
10	RF_P	RF I/O	Positive RF output signal from PA.
11	RF_N	RF I/O	Negative RF output signal from PA.
12	AVDD	Power (Analog)	1.8 V - 3.6 V analog power supply connection.
13	AVDD	Power (Analog)	1.8 V - 3.6 V analog power supply connection.
14	RBIAS	Analog I/O	External bias resistor for reference current .
15	DGUARD	Power (Digital)	Power supply connection for digital noise isolation.
16	SI	Digital Input	Serial configuration interface, data input.

Table 11: Pinout Overview

6 Circuit Description

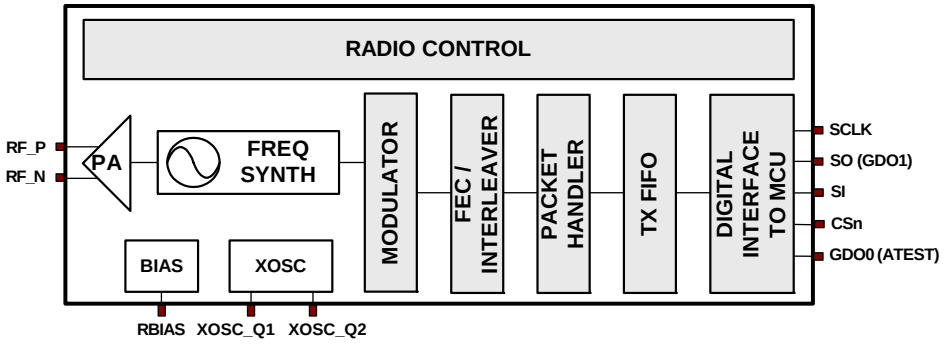


Figure 2: *CC1150* Simplified Block Diagram

A simplified block diagram of ***CC1150*** is shown in Figure 2.

The ***CC1150*** transmitter is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

7 Application Circuit

Only a few external components are required for using the ***CC1150***. The recommended application circuits are shown in Figure 4 and Figure 5. The external components are described in Table 13, and typical values are given in Table 14.

7.1 Bias resistor

The bias resistor R141 is used to set an accurate bias current.

7.2 Balun and RF matching

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C111, C101, L101 and L111 for the 315/433 MHz design. L101, L111, C101, L102, C111, C102 and L112 for the 868/915 MHz reference design) form a balun that converts the differential RF signal on ***CC1150*** to a single-ended RF signal. C104 is needed for DC blocking. Together with an appropriate LC filter network, the balun components also transform the impedance to match a 50 Ω antenna (or cable). C105 provides DC blocking and is only needed if there is a DC path in the antenna. For the 868/915 MHz reference design, this component may also be used for additional filtering, see section 7.5 below.

Suggested values for 315 MHz, 433 MHz and 868/915 MHz are listed in Table 14.

The balun and LC filter component values and their placement are important to achieve optimal performance. It is highly recommended to follow the CC1150EM reference design ([1] and [2]). Gerber files and schematics for the reference designs are available for download from the TI website.

7.3 Crystal

A crystal in the frequency range 26-27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C51 and C71) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{51}} + \frac{1}{C_{71}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator circuit is shown in Figure 3. Typical component values for different values of C_L are given in Table 12.

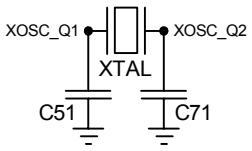


Figure 3: Crystal Oscillator Circuit

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see section 4.3 on page 8).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

Component	C_L= 10 pF	C_L=13 pF	C_L=16 pF
C51	15 pF	22 pF	27 pF
C71	15 pF	22 pF	27 pF

Table 12: Crystal Oscillator Component Values

7.4 Reference signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. The XOSC_Q2 line must be left un-connected. C51 and C71 can be omitted when using a reference signal.

7.5 Additional filtering

In the 868/915 MHz reference design, C106 and L105 together with C105 build an optional filter to reduce emission at 699 MHz. This filter may be necessary for applications seeking compliance with ETSI EN 300-220, for more information, see DN017 [6]. If this filtering is not necessary, C105 will work as a DC block (only necessary if there is a DC path in the antenna). C106 and L105 should in that case be left unmounted.

Additional external components (e.g. an RF SAW filter) may be used in order to improve the performance in specific applications. The use of wire-wound inductors in the application circuit will also improve the RF performance and give higher output power. For more information, see DN017 [6].

7.6 Power supply decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. The CC1150EM reference design should be followed closely ([1] and [2]).

7.7 Antenna Considerations

The reference designs ([1] and [2]) contains a SMA connector and is match for a 50 Ω load. The SMA connector makes it easy to connect evaluation modules and prototypes to different test equipment for example a spectrum analyzer. The SMA connector can also be replaced by an antenna suitable for the desired application. Please refer to the antenna selection guide AN058 [7] for further details regarding antenna solutions provided by TI.

Component	Description
C41	Decoupling capacitor for on-chip voltage regulator to digital part
C51/C71	Crystal loading capacitors
C101/C111	RF balun/matching capacitors
C102	RF LC filter/matching filter capacitor (315 and 433 MHz). RF balun/matching capacitor (868/915 MHz).
C103	RF LC filter/matching capacitors
C104	RF balun DC blocking capacitor
C105	RF LC filter DC blocking capacitor and part of optional RF LC filter (868/915 MHz)
C106	Part of optional RF LC filter and DC Block (868/915 MHz)
L101/L111	RF balun/matching inductors (inexpensive multi-layer type)
L102	RF LC filter/matching filter inductor (315 and 433 MHz). RF balun/matching inductor (868/915 MHz) (inexpensive multi-layer type)
L103	RF LC filter/matching inductor (inexpensive multi-layer type)
L104	RF LC filter/matching inductor (inexpensive multi-layer type)
L105	Part of optional RF LC filter (868/915 MHz)(inexpensive multi-layer type)
R141	Resistor for internal bias current reference
XTAL	26-27 MHz crystal

Table 13: Overview of External Components (excluding supply decoupling capacitors)

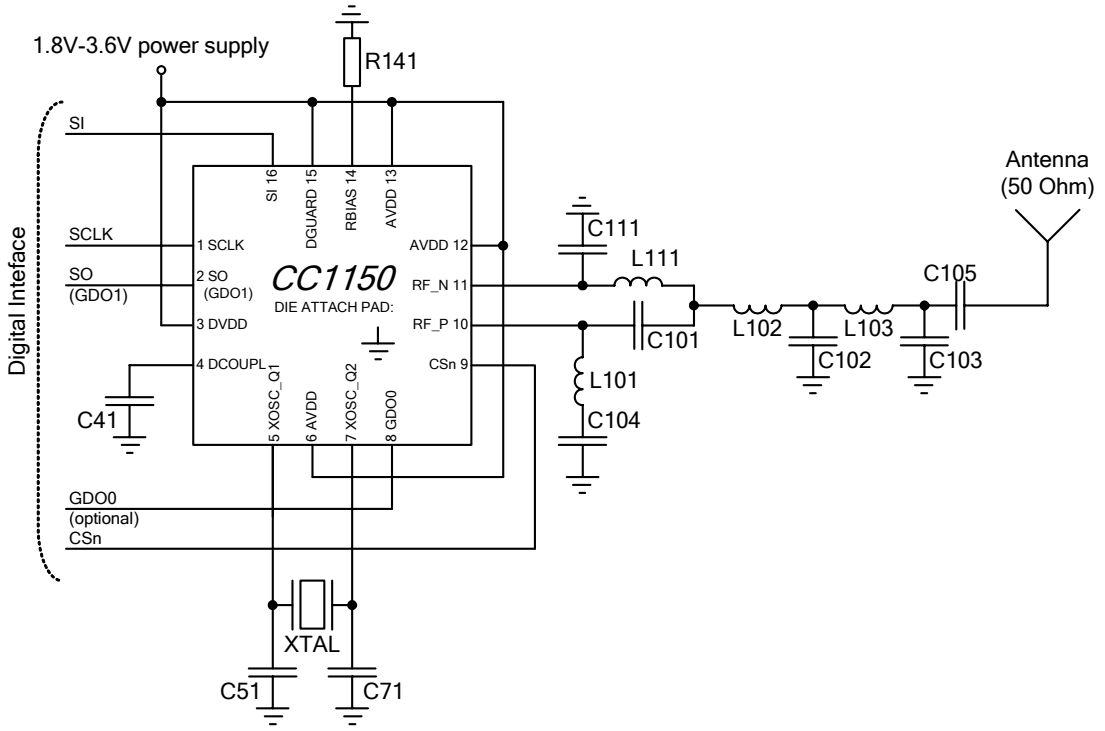


Figure 4: Typical Application and Evaluation Circuit 315/433 MHz (excluding supply decoupling capacitors)

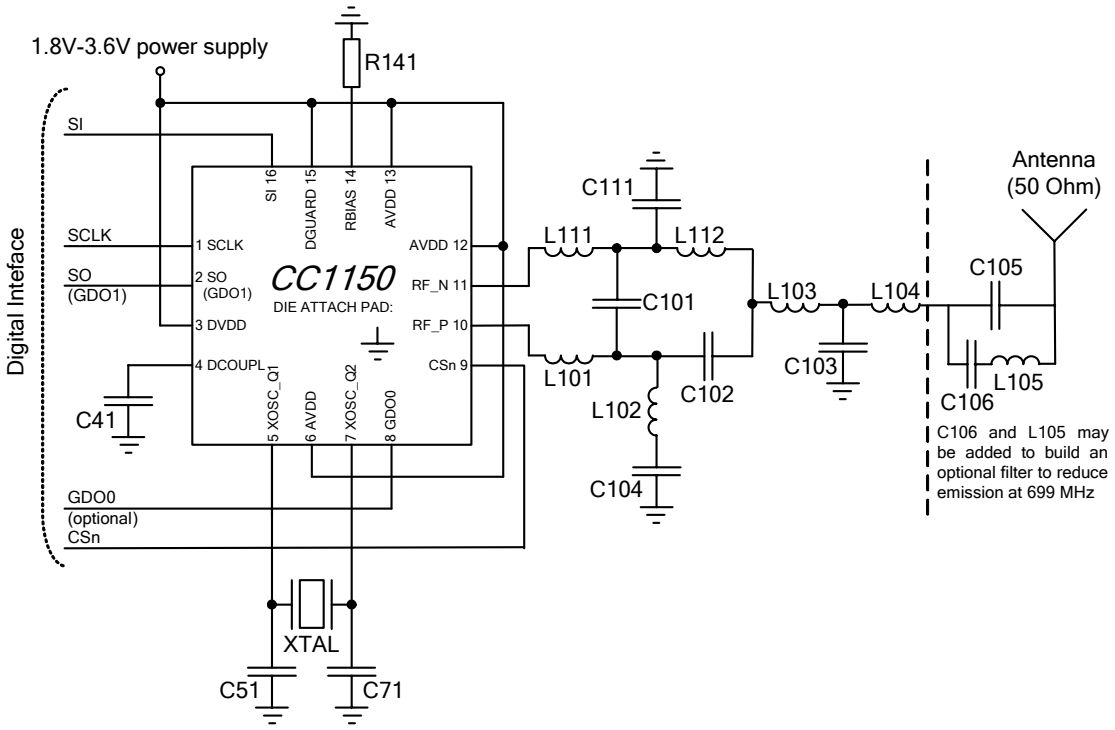


Figure 5: Typical Application and Evaluation Circuit 868/915 MHz (excluding supply decoupling capacitors)

Component	Value at 31 5MHz	Value at 433 MHz	Value at 868/915 MHz
C41	100 nF ± 10%, 0402 X5R		
C51	27 pF ± 5%, 0402 NP0		
C71	27 pF ± 5%, 0402 NP0		
C101	6.8 pF ± 0.5 pF, 0402 NP0	3.9 pF ± 0.25 pF, 0402 NP0	1.0 pF ± 0.25 pF, 0402 NP0
C102	12 pF ± 5%, 0402 NP0	8.2 pF ± 0.5 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0
C103	6.8 pF ± 0.5 pF, 0402 NP0	5.6pF±0.5pF, 0402 NP0	3.3 pF ± 0.25 pF, 0402 NP0
C104	220 pF ± 5%, 0402 NP0	220 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0
C105	220 pF ± 5%, 0402 NP0	220 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0 (12 pF ± 5%, 0402 NP0 if optionally 699 MHz filter is desired)
C106			(47 pF ± 5%, 0402 NP0 if optionally 699 MHz filter is desired)
C111	6.8 pF ± 0.5 pF, 0402 NP0	3.9 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25pF, 0402 NP0
L101	33nH±5%, 0402 monolithic	27 nH ± 5%, 0402 monolithic	12 nH ± 5%, 0402 monolithic
L102	18nH±5%, 0402 monolithic	22 nH ± 5%, 0402 monolithic	18 nH ± 5%, 0402 monolithic
L103	33 nH ± 5%, 0402 monolithic	27 nH ± 5%, 0402 monolithic	12 nH ± 5%, 0402 monolithic
L104			(12 nH ± 5%, 0402 monolithic if optionally 699 MHz filter is desired)
L105			3.3 nH ± 5%, 0402 monolithic
L111	33 nH ± 5%, 0402 monolithic	27 nH ± 5%, 0402 monolithic	12 nH ± 5%, 0402 monolithic
L112			18 nH ± 5%, 0402 monolithic
R141	56 kΩ±1%, 0402		
XTAL	26.0 MHz surface mount crystal		

Table 14: Bill of Materials for the Application Circuit (Murata LQG15HS and GRM1555C series inductors and capacitors, resistor from the Koa RK73 series, and AT-41CD2 crystal from NDK)

7.8 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground.

In the CC1150EM reference designs ([1] and [2]), 5 vias are placed inside the exposed die attached pad. These vias should be “tented” (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using “tented” vias reduces the solder paste coverage below 100%. See Figure 6 for top solder resist and top paste masks.

All the decoupling capacitors should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the ***CC1150*** supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane by separate vias. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary. Routing in the ground plane underneath and between the chip, the balun/RF matching circuit and the decoupling capacitor’s ground vias should also be

avoided. This improves the grounding and ensures the shortest possible return path for stray currents.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components smaller than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

It is strongly advised that the CC1150EM reference design ([1] and [2]) layout is followed very closely in order to get the best performance. Gerber files and schematics for the reference designs are available for download from the TI website.

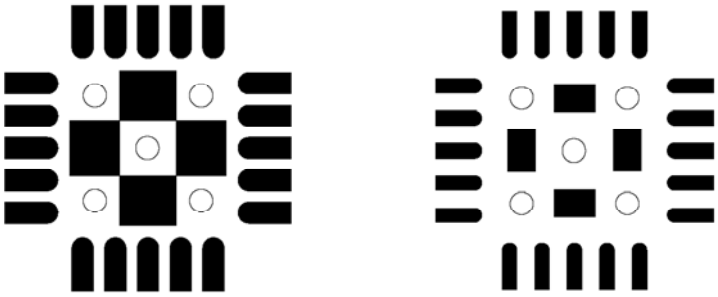


Figure 6: Left: Top Solder Resist Mask (Negative). Right: Top Paste Mask. Circles are Vias

8 Configuration Overview

CC1150 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power-up mode
- Crystal oscillator power-up / power – down
- Transmit mode
- RF channel selection
- Data rate
- Modulation format
- RF output power
- Data buffering with 64-byte transmit FIFO
- Packet radio hardware support
- Forward Error Correction with interleaving
- Data Whitening

Details of each configuration register can be found in section 25, starting on page 42.

Figure 7 shows a simplified state diagram that explains the main *CC1150* states, together with typical usage and current consumption. For detailed information on controlling the *CC1150* state machine, and a complete state diagram, see section 16, starting on page 30.

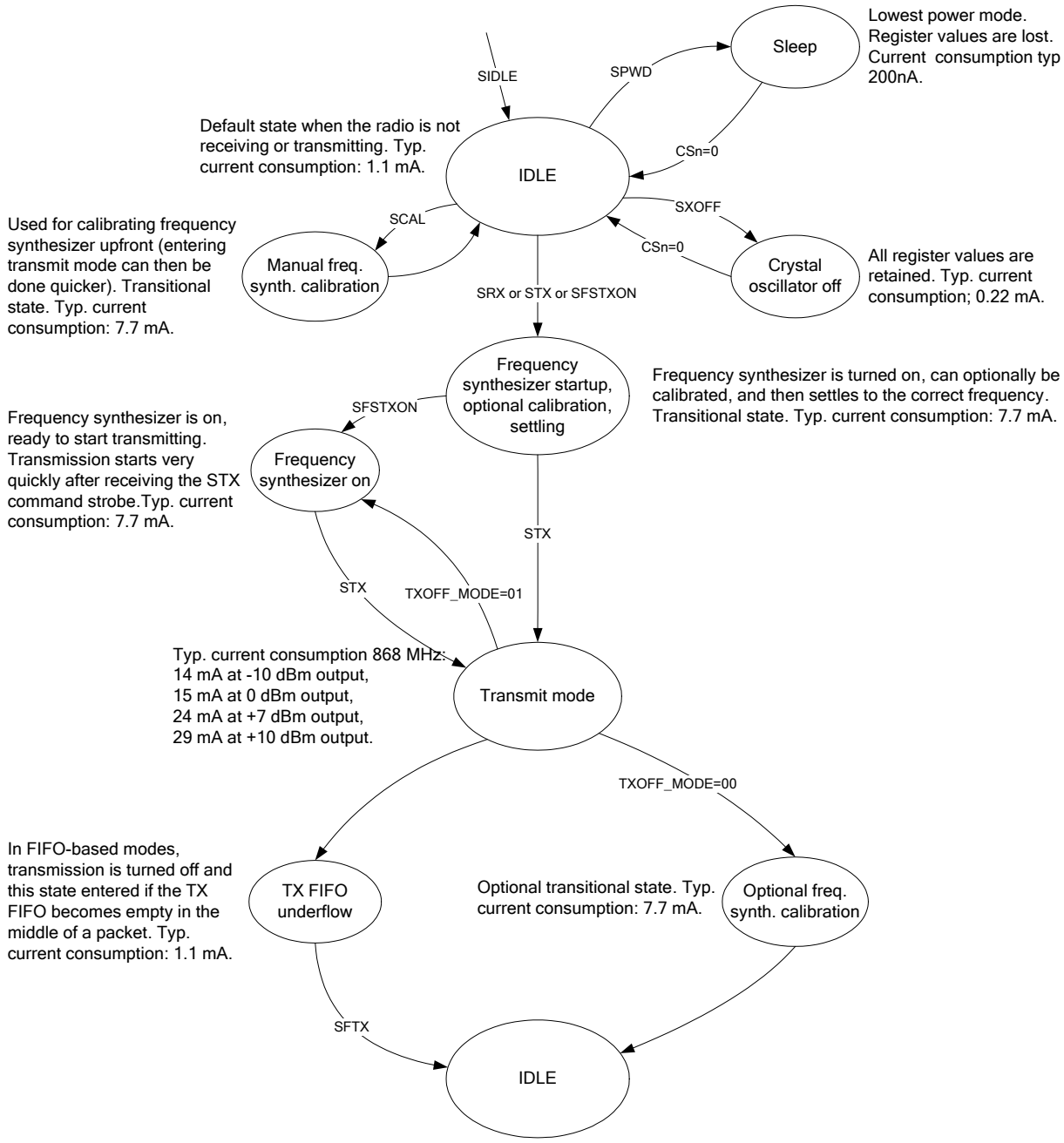


Figure 7: Simplified State Diagram with Typical Usage and Current Consumption

9 Configuration Software

CC1150 can be configured using the SmartRF® Studio [11] software, available for download from www.ti.com/smartrfstudio. The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF Studio user interface for ***CC1150*** is shown in Figure 8.

After chip reset, all the registers have default values as shown in the tables in section 25. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

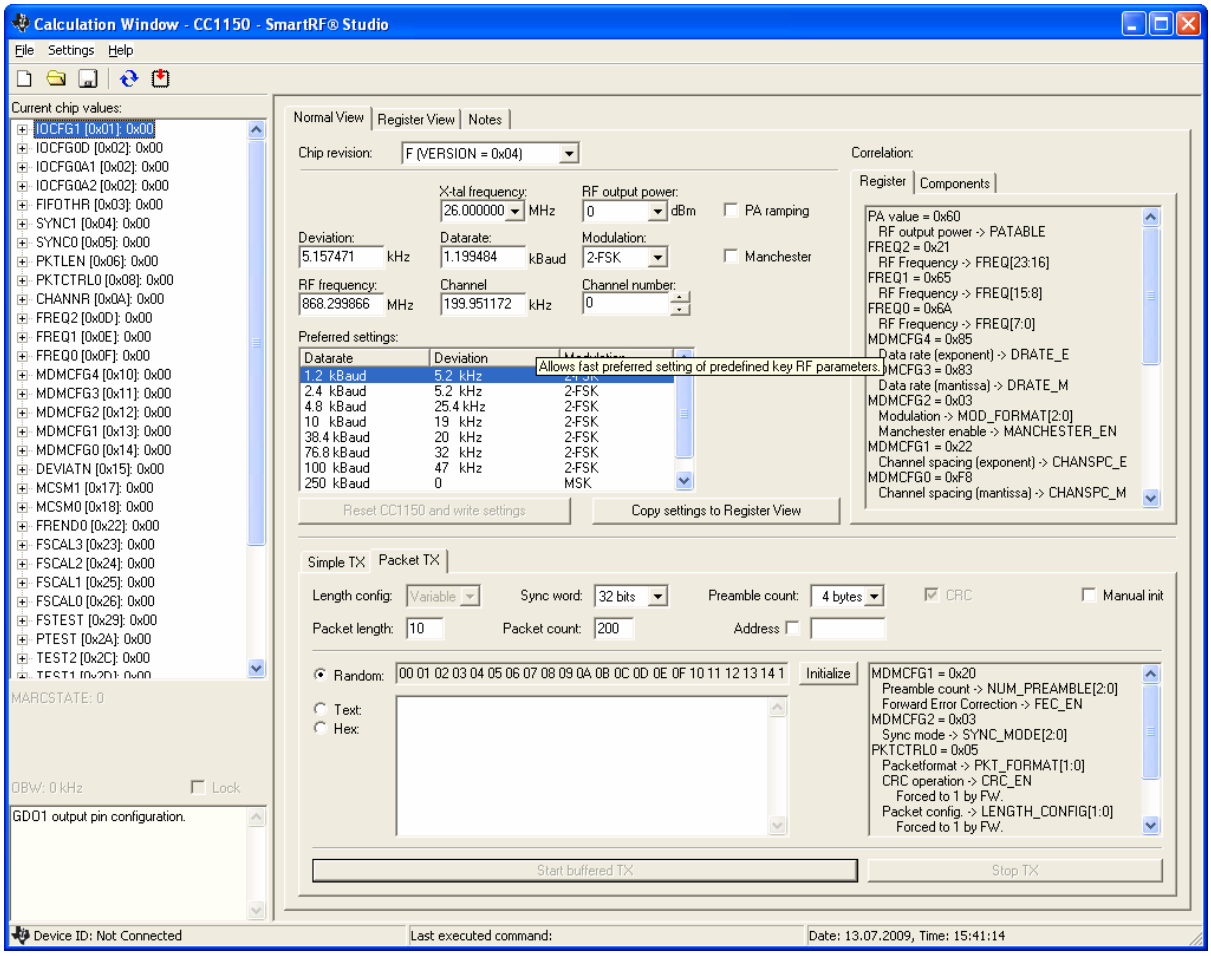


Figure 8: SmartRF Studio User Interface

10 4-wire Serial Configuration and Data Interface

CC1150 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where ***CC1150*** is the slave. This interface is also used to read and write buffered data. All address and data transfer on the SPI interface is done most significant bit first.

All transactions on the SPI interface start with a header byte containing a read/write bit, a burst access bit and a 6-bit address.

During address and data transfer, the CSn pin (Chip Select, active low) must be kept low. If CSn goes high during the access, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 9 with reference to Table 15.

When CSn is pulled low, the MCU must wait until the ***CC1150*** SO pin goes low before starting to transfer the header byte. This indicates that the voltage regulator has stabilized and the crystal is running. Unless the chip is in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

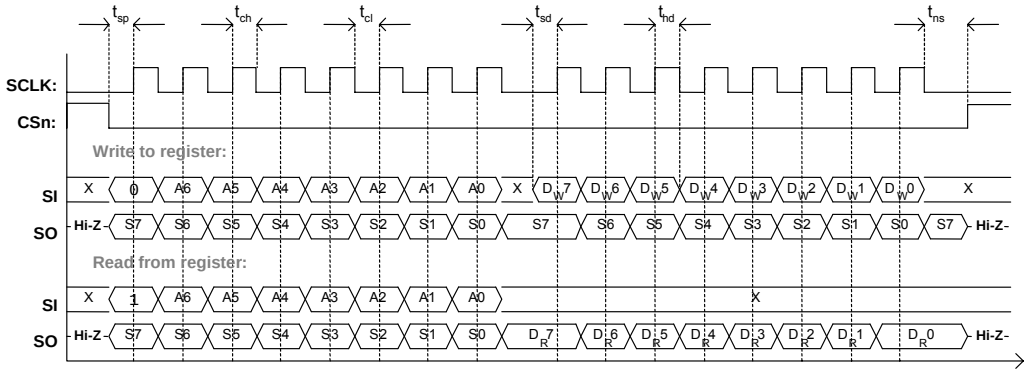


Figure 9: Configuration Registers Write and Read Operations

Parameter	Description		Min	Max	Units
f_{SCLK}	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).		-	10	MHz
	SCLK frequency, single access No delay between address and data byte			9	
	SCLK frequency, burst access No delay between address and data byte, or between data bytes			6.5	
$t_{sp,pd}$	CSn low to positive edge on SCLK, in power-down mode		150	-	µs
t_{sp}	CSn low to positive edge on SCLK, in active mode		20	-	ns
t_{ch}	Clock high		50	-	ns
t_{cl}	Clock low		50	-	ns
t_{rise}	Clock rise time		-	5	ns
t_{fall}	Clock fall time		-	5	ns
t_{sd}	Setup data (negative SCLK edge) to positive edge on SCLK (t_{sd} applies between address and data bytes, and between data bytes)	Single access	55	-	ns
		Burst access	76	-	ns
t_{hd}	Hold data after positive edge on SCLK		20	-	ns
t_{ns}	Negative edge on SCLK to CSn high		20	-	ns

Table 15: SPI Interface Timing Requirements

Note that the minimum $t_{sp,pd}$ figure in Table 15 can be used in cases where the user does not read the CHIP_RDYn signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150 µs in Table 15 is the crystal oscillator start-up time measured using crystal AT-41CD2 from NDK.

10.1 Chip Status Byte

When the header byte, data byte or command strobe is sent on the SPI interface, the chip status byte is sent by the ***CC1150*** on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP_RDYn signal; this signal must go low before the first positive edge of SCLK. The CHIP_RDYn signal indicates that the crystal is running and the regulated digital supply voltage is stable.

Bit 6, 5 and 4 comprises the STATE value. This value reflects the state of the chip. The XOSC and power to the digital core is on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state. The TX state will be active when the chip is transmitting.

The last four bits (3:0) in the status byte contains FIFO_BYTES_AVAILABLE. This field

contains the number of bytes free for writing into the TX FIFO. When FIFO_BYTES_AVAILABLE=15, 15 or more bytes are free. Table 16 gives a status byte summary.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>CHIP_RDYn</td><td>Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.</td></tr>
<tr><td>6:4</td><td>STATE[2:0]</td><td>Indicates the current main state machine mode
<table>
<tr><th>Value</th><th>State</th><th>Description</th></tr>
<tr><td>000</td><td>Idle</td><td>IDLE state
(Also reported for some transitional states instead of SETTLING or CALIBRATE, due to a small error)</td></tr>
<tr><td>001</td><td>Not used</td><td>Not used</td></tr>
<tr><td>010</td><td>TX</td><td>Transmit mode</td></tr>
<tr><td>011</td><td>FSTXON</td><td>Fast TX ready</td></tr>
<tr><td>100</td><td>CALIBRATE</td><td>Frequency synthesizer calibration is running</td></tr>
<tr><td>101</td><td>SETTLING</td><td>PLL is settling</td></tr>
<tr><td>110</td><td>Not used</td><td>Not used</td></tr>
<tr><td>111</td><td>TXFIFO_UNDERFLOW</td><td>TX FIFO has underflowed. Acknowledge with SFTX</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>FIFO_BYTES_AVAILABLE[3:0]</td><td>The number of free bytes in the TX FIFO.</td></tr>
</table>

Table 16: Status Byte Summary

10.2 Register Access

The configuration registers on the ***CC1150*** are located on SPI addresses from 0x00 to 0x2E. Table 26 on page 43 lists all configuration registers. The detailed description of each register is found in Section 25.1, starting on page 45.

All configuration registers can be both written and read. The read/write bit controls if the register should be written or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit in the address header. The address sets the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30-0x3D, the burst bit is used to select between status registers (burst bit is 1) and command strobes (burst bit is 0). See more in section 10.3 below. Because of this, burst access is not available for status registers, so they must be read one at a time. The status registers can only be read.

10.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (e.g. MARCSTATE or TXBYTES), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from TXBYTES being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the ***CC1150*** Errata Notes [8] for more details.

10.4 Command Strobes

Command Strobes may be viewed as single byte instructions to ***CC1150***. By addressing a Command Strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable transmit mode, flush the TX FIFO etc. The nine

command strobes are listed in Table 25 on page 42.

Note that an SIDLE strobe will clear all pending command strobes until IDLE state is reached. This means that if for example an SIDLE strobe is issued while the radio is in TX state, any other command strobes issued before the radio reaches IDLE state will be ignored.

The command strobe registers are accessed in the same way as for a register write operation, but no data is transferred. That is, only the R/W bit (set to 0), burst access (set to 0) and the six address bits (in the range 0x30 through 0x3D) are written.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an SRES command strobe is being issued, on will have to wait for the SO pin to go low before the next command strobe can be issued as shown in Figure 10.The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes that are executed when CSn goes high.

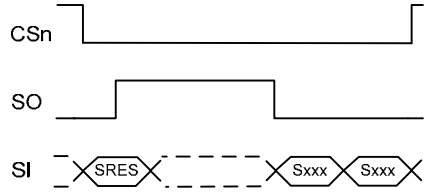


Figure 10: SRES Command Strobe

10.5 FIFO Access

The 64-byte TX FIFO is accessed through the 0x3F addresses. When the read/write bit is zero, the TX FIFO is accessed. The TX FIFO is write-only.

The burst bit is used to determine if FIFO access is single byte or a burst access. The single byte access method expects address with burst bit set to zero and one data byte. After the data byte a new address is expected; hence, CSn can remain low. The burst access method expects one address byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the FIFO:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO

When writing to the TX FIFO, the status byte (see Section 10.1) is output for each new data byte on SO, as shown in Figure 10. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free *before* writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted to the SI pin, the status byte received concurrently on the SO pin will indicate that one byte is free in the TX FIFO.

The TX FIFO may be flushed by issuing a SFTX command strobe. The SFTX command strobe can only be issues in the IDLE or TX_UNDERFLOW states. The FIFO is cleared when going to the SLEEP state.

Figure 11 gives a brief overview of different register access types possible.

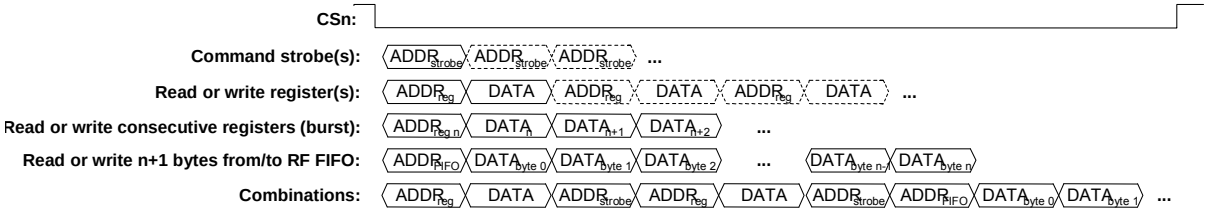


Figure 11: Register Access Types

10.6 PATABLE Access

The 0x3E address is used to access the PATABLE, which is used for selecting PA power control settings. The SPI expects up to eight data bytes after receiving the address. By programming the PATABLE, controlled PA power ramp-up and ramp-down can be achieved, as well as ASK modulation shaping for reduced bandwidth. Note that the ASK modulation shaping is limited to output powers below -1 dBm. See SmartRF Studio [11] for recommended shaping sequence. See also section 21 on page 35 for details on output power programming.

The PATABLE is an 8-byte table that defines the PA control settings to use for each of the eight PA power values (selected by the 3-bit value FREND0.PA_POWER). The table is written and read from the lowest setting (0) to the highest (7), one byte at a time. An index counter is used to control the access to the table. This counter is incremented each time a byte is read or written to the table, and set to the lowest index when CSn is high. When the highest value is reached the counter restarts at zero.

The access to the PATABLE is either single byte or burst access depending on the burst bit. When using burst access the index counter will count up; when reaching 7 the counter will restart at 0. The read/write bit controls whether the access is a write access (R/W=0) or a read access (R/W=1).

If one byte is written to the PATABLE and this value is to be read out then CSn must be set high before the read access in order to set the index counter back to zero.

Note that the content of the PATABLE is lost when entering the SLEEP state. For more information, see DN501 [8].

11 Microcontroller Interface and Pin Configuration

In a typical system, ***CC1150*** will interface to a microcontroller. This microcontroller must be able to:

- Program ***CC1150*** into different modes,
- Write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn).

11.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 10 on page 18.

11.2 General Control and Status Pins

The ***CC1150*** has one dedicated configurable pin (GDO0) and one shared pin (GDO1/SO) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See section 22 page 37 for more details of the signals that can be programmed. The shared pin is the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

The GDO0 pin can also be used for an on-chip analog temperature sensor. By measuring the voltage on the GDO0 pin with an external ADC, the temperature can be calculated. Specifications for the temperature sensor are found in section 4.5 on page 9. With default PTEST register setting (0x7F), the temperature sensor output is only available when the frequency synthesizer is enabled (e.g. the MANCAL, FSTXON and TX states). It is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state. Before leaving the IDLE state, the PTEST register should be restored to its default value (0x7F).

11.3 Optional Radio Control Feature

The *CC1150* has an optional way of controlling the radio by reusing SI, SCLK, and CSn from the SPI interface. This feature allows for a simple three-pin control of the major states of the radio: SLEEP, IDLE, and TX.

This optional functionality is enabled with the MCSM0.PIN_CTRL_EN configuration bit.

State changes are commanded as follows:

- If CSn is high, the SI and SCLK are set to the desired state according to Table 17.
- If CSn goes low, the state of SI and SCLK is latched and a command strobe is generated internally according to the pin configuration.

It is only possible to change state with the latter functionality. That means that for instance TX will not be restarted if SI and SCLK are set to TX and CSn toggles. When CSn is low the SI and SCLK has normal SPI functionality.

All pin control command strobes are executed immediately except the SPWD strobe. The SPWD strobe is delayed until CSn goes high.

CSn	SCLK	SI	Function
1	X	X	Chip unaffected by SCLK/SI
↓	0	0	Generates SPWD strobe
↓	0	1	Generates STX strobe
↓	1	0	Generates SIDLE strobe
↓	1	1	Defined on the transceiver version (*CC1101*)
0	SPI mode	SPI mode	SPI mode (wakes up into IDLE if in SLEEP/XOFF)

Table 17: Optional Pin Control Coding

12 Data Rate Programming

The data rate used when transmitting is programmed by the MDMCFG3.DRATE_M and the MDMCFG4.DRATE_E configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE_M) \cdot 2^{DRATE_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE_E = \left\lfloor \log_2 \left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}} \right) \right\rfloor$$

$$DRATE_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE_E}} - 256$$

If DRATE_M is rounded to the nearest integer and becomes 256, increment DRATE_E and use DRATE_M=0.

The data rate can be set from 0.8 kBaud to 500 kBaud with the minimum data rate step size changes according to Table 18 below.

Min Data rate [kBaud]	Typical data rate [kBaud]	Max Data rate [kBaud]	Data rate step size [kBaud]
0.8	1.2 / 2.4	3.17	0.0062
3.17	4.8	6.35	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.4	0.0496
25.4	38.4	50.8	0.0992
50.8	76.8	101.6	0.1984
101.6	153.6	203.1	0.3967
203.1	250	406.3	0.7935
406.3	500	500	1.5869

Table 18: Data Rate Step Size

13 Packet Handling Hardware Support

The ***CC1150*** has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler can be configured to add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes.
- A two byte Synchronization Word. Can be duplicated to give a 4-byte sync word (recommended). It is not possible to only insert preamble or only insert a sync word.
- Optionally whitening the data with a PN9 sequence.
- Optionally Interleave and Forward Error Code the data.
- Optionally compute and add a 2 byte CRC checksum over the data field.

In a system where ***CC1150*** is used as the transmitter and ***CC1101*** as the receiver the recommended setting is 4-byte preamble and 4-byte sync word except for 500 kBaud data rate where the recommended preamble length is 8 bytes.

Note that register fields that control the packet handling features should only be altered when ***CC1150*** is in the IDLE state.

13.1 Data whitening

From a radio perspective, the ideal over the air data are random and DC free. This results in the smoothest power distribution over the occupied bandwidth. This also gives the regulation loops in the receiver uniform operation conditions (no data dependencies).

Real world data often contain long sequences of zeros and ones. Performance can then be improved by whitening the data before transmitting, and de-whitening in the receiver. With ***CC1150***, in combination with a ***CC1101*** at the receiver end, this can be done automatically by setting `PKTCTRL0.WHITE_DATA=1`. All data, except the preamble and the sync word, are then XOR-ed with a 9-bit pseudo-random (PN9) sequence before being transmitted as shown in Figure 12. The PN9 sequence is initialized to all 1's. At the receiver end, the data are XOR-ed with the same pseudo-random sequence. This way, the whitening is reversed, and the original data appear in the receiver.

Setting `PKTCTRL0.WHITE_DATA=1` is recommended for all uses, except when over-the-air compatibility with other systems is needed.

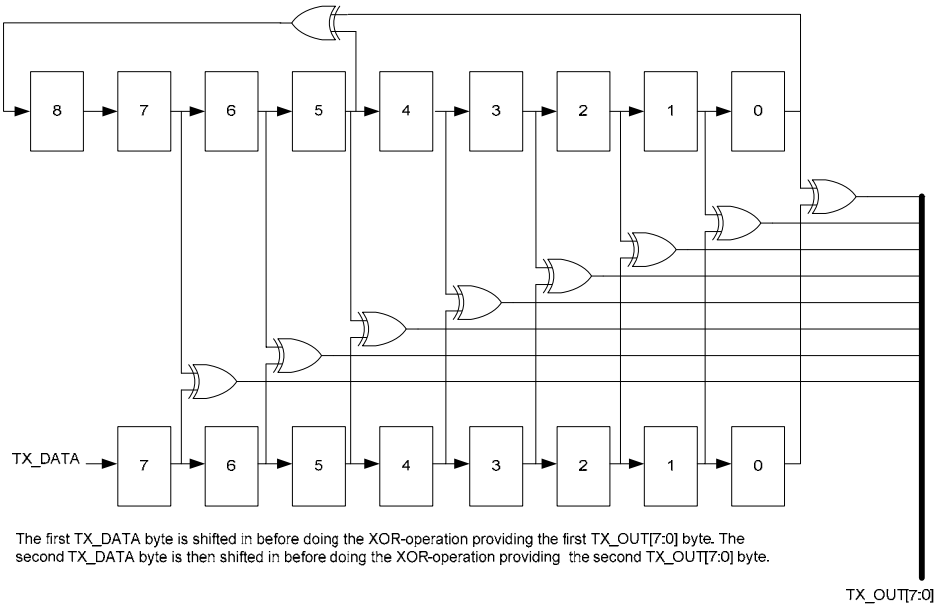


Figure 12: Data Whitening in TX Mode

13.2 Packet Format

The format of the data packet can be configured and consists of the following items:

- Preamble
- Synchronization word
- Optional length byte
- Optional Address byte
- Payload
- Optional 2 byte CRC

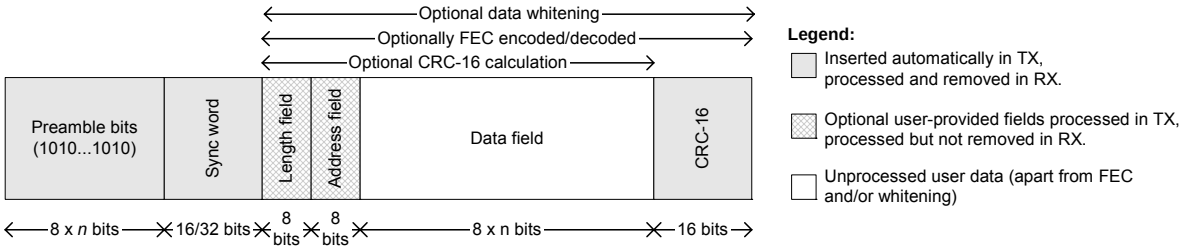


Figure 13: Packet Format

The preamble pattern is an alternating sequence of ones and zeros (01010101…). The number of preamble bytes is programmed with the MDMCFG1.NUM_PREAMBLE value. When enabling TX, the modulator will start transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator will send the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator will continue to send preamble bytes until the first byte is written to the TX FIFO. The modulator will then send the sync word and then the data bytes.

The synchronization word is a two-byte value set in the SYNC1 and SYNC0 registers. The sync word provides byte synchronization of the incoming packet. A one-byte synch word can be emulated by setting the SYNC1 value to the preamble pattern. It is also possible to emulate a 32 bit sync word by using MDMCFG2.SYNC_MODE set to 3 or 7. The sync word will then be repeated twice.

CC1150 supports both fixed packet length protocols and variable packet length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting PKTCTRL0.LENGTH_CONFIG=0. The desired packet length is set by the PKTLEN register. In variable packet length mode PKTCTRL0.LENGTH_CONFIG=1, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional automatic CRC.

With PKTCTRL0.LENGTH_CONFIG=2, the packet length is set to infinite and transmission will continue until turned off manually. The infinite mode can be turned off while a packet is being transmitted. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by ***CC1150***. One should make sure that TX mode is not turned off during the transmission of the first half of any byte. Refer to the ***CC1150*** Errata Notes [8] for more details.

Note that the minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

13.2.1 Arbitrary Length Field Configuration

The packet automation control register, PKTCTRL0, can be reprogrammed during TX. This opens the possibility to transmit packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite mode (PKTCTRL0.LENGTH_CONFIG=2) must be active. The PKTLEN register is set to mod(length, 256). When less than 256 bytes remains of the packet, the MCU disables infinite packet length and activates fixed length packets. When the internal byte counter reaches the PKTLEN value, the transmission ends (the radio enters the state determined by TXOFF_MODE). Automatic CRC appending can be used (by setting PKTCTRL0.CRC_EN=1).

When for example a 600-byte packet is to be transmitted, the MCU should do the following (see also Figure 14):

- Set PKTCTRL0.LENGTH_CONFIG=2.
- Pre-program the PKTLEN register to mod(600,256)=88.
- Transmit at least 345 bytes, for example by filling the 64-byte TX FIFO six times (384 bytes transmitted).
- Set PKTCTRL0.LENGTH_CONFIG=0.
- The transmission ends when the packet counter reaches 88. A total of 600 bytes are transmitted.

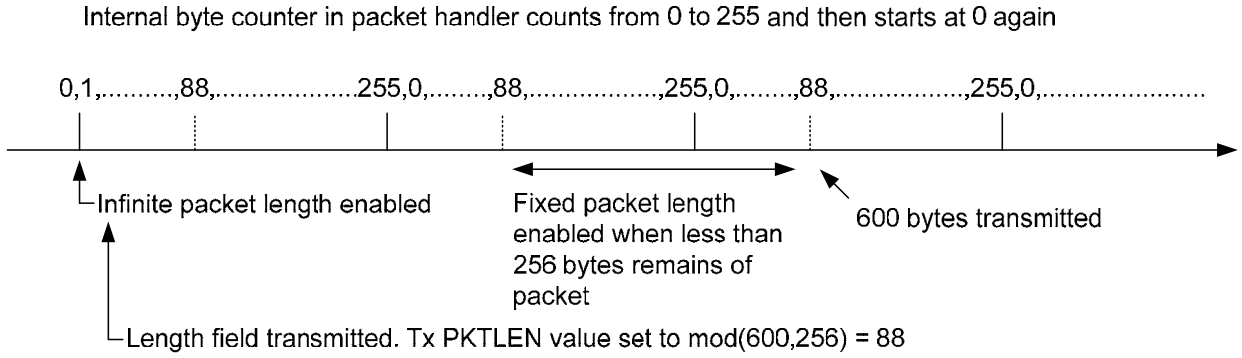


Figure 14: Arbitrary Length Field Configuration

13.3 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If fixed packet length is enabled, then the first byte written to the TX FIFO is interpreted as the destination address, if this feature is enabled in the device that receives the packet.

The modulator will first send the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator will send the two-byte (optionally 4-byte) sync word and then the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO and the result is sent as two extra bytes at the end of the payload data. If the TX FIFO runs empty before the complete packet has been transmitted, the radio will enter TXFIFO_UNDERFLOW state. The only way to exit this state is by issuing an SFTX strobe. Writing to the TX FIFO after it has underflowed will not restart TX mode.

If whitening is enabled, the length byte, payload data and the two CRC bytes will be whitened. This is done before the optional FEC/Interleaver stage. Whitening is enabled by setting PKTCTRL0.WHITE_DATA=1.

If FEC/Interleaving is enabled, the length byte, payload data and the two CRC bytes will be scrambled by the interleaver, and FEC encoded before being modulated. FEC is enabled by setting MDMCFG1.FEC_EN=1.

13.4 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been transmitted. Additionally, for packets longer than 64 bytes, the TX FIFO needs to be refilled while in TX. This means that the MCU needs to know the number of bytes that can be written to the TX FIFO. There are two possible solutions to get the necessary status information:

a) Interrupt Driven Solution

The GDO pins can be used in TX to give an interrupt when a sync word has been transmitted or when a complete packet has been transmitted by setting IOCFGx.GDOx_CFG=0x06. In addition, there are two configurations for the IOCFGx.GDOx_CFG register that can be used as an interrupt source to provide information on how many bytes that is in the TX FIFO. The IOCFGx.GDOx_CFG=0x02 and the

IOCFGx.GDOx_CFG=0x03 configurations are associated with the TX FIFO. See Table 24 for more information.

b) SPI Polling

The PKTSTATUS register can be polled at a given rate to get information about the current GDO2 and GDO0 values respectively. The TXBYTES register can be polled at a given rate to get information about the number of bytes in the TX FIFO. Alternatively, the number of bytes in the TX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

It is recommended to employ an interrupt driven solution due to that when using SPI polling, there is a small, but finite, probability that a single read from registers PKTSTATUS and TXBYTES is being corrupt. The same is the case when reading the chip status byte. This is explained in the ***CC1150*** Errata Notes [8] Refer to the TI website for SW examples [12]

14 Modulation Formats

CC1150 supports amplitude, frequency and phase shift modulation formats. The desired modulation format is set in the MDMCFG2.MOD_FORMAT register.

Optionally, the data stream can be Manchester coded by the modulator. This option is enabled by setting MDMCFG2.MANCHESTER_EN=1. Manchester encoding cuts the effective data rate in half, and thus Manchester is not supported for 500 kBaud. Further note that Manchester encoding is not supported at the same time as using the FEC/Interleaver option or when using MSK modulation.

14.1 Frequency Shift Keying

CC1150 has the possibility to use Gaussian shaped 2_FSK (GFSK). The 2-FSK signal is then shaped by a Gaussian filter with BT=1, producing a GFSK modulated signal. This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth.

In “true” 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift “softer”, the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

The frequency deviation is programmed with the DEVIATION_M and DEVIATION_E values in the DEVIATN register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION_M) \cdot 2^{DEVIATION_E}$$

The symbol encoding is shown in Table 19.

Format	Symbol	Coding
2-FSK/GFSK	‘0’	– Deviation
	‘1’	+ Deviation

Table 19: Symbol Encoding for 2-FSK/GFSK Modulation

14.2 Minimum Shift Keying

When using MSK[1], the complete transmission (preamble, sync word and payload) will be MSK modulated.

Phase shifts are performed with a constant transition time. The fraction of a symbol period used to change the phase can be modified with the DEVIATN.DEVIATION_M setting. This is equivalent to changing the shaping of the symbol.

Note that when using MSK, Manchester encoding must be disabled by setting MDMCFG2.MANCHESTER_EN=0. Further note that the MSK modulation format implemented in ***CC1150*** inverts the data compared to e.g. signal generators.

[1] Identical to offset QPSK with half-sine shaping (data coding may differ)

14.3 Amplitude Modulation

CC1150 supports two different forms of amplitude modulation: On-Off Keying (OOK) and Amplitude Shift Keying (ASK).

OOK modulation simply turns on or off the PA to modulate 1 and 0 respectively.

The ASK variant supported by the ***CC1150*** allows programming of the modulation depth (the difference between 1 and 0), and shaping of the pulse amplitude. Pulse shaping will produce a more bandwidth constrained output spectrum.

Note that the OOK/ASK pulse shaping feature on the ***CC1150*** does only support output power up to about -1 dBm.

The `DEVIATN` register has no effect when using ASK/OOK.

15 Forward Error Correction with Interleaving

15.1 Forward Error Correction (FEC)

CC1150 has built in support for Forward Error Correction (FEC) that can be used with ***CC1101*** at the receiver end. To enable this option, set `MDMCFG1.FEC_EN` to 1. FEC is only supported in fixed packet length mode, i.e. when `PKTCTRL0.LENGTH_CONFIG=0`. FEC is employed on the data field and CRC word in order to reduce the gross bit error rate when operating near the sensitivity limit. Redundancy is added to the transmitted data in such a way that the receiver can restore the original data in the presence of some bit errors.

The use of FEC allows correct reception at a lower Signal-to-Noise RATIO (SNR), thus extending communication range. Alternatively, for a given SNR, using FEC decreases the bit error rate (BER). As the packet error rate (PER) is related to BER by

$$PER = 1 - (1 - BER)^{packet_length}$$

A lower BER can be used to allow longer packets, or a higher percentage of packets of a given length, to be transmitted successfully.

Finally, in realistic ISM radio environments, transient and time-varying phenomena will produce occasional errors even in otherwise good reception conditions. FEC will mask such errors and, combined with interleaving of the coded data, even correct relatively long periods of faulty reception (burst errors).

The FEC scheme adopted for ***CC1150*** is convolutional coding, in which *n* bits are generated based on *k* input bits and the *m* most recent input bits, forming a code stream able to withstand a certain number of bit errors between each coding state (the *m*-bit window).

The convolutional coder is a rate 1/2 code with a constraint length of m=4. The coder codes one input bit and produces two output bits; hence, the effective data rate is halved. This means that in order to transmit at the same effective data rate when using FEC, it is necessary to use twice as high over-the-air data rate.

15.2 Interleaving

Data received through real radio channels will often experience burst errors due to interference and time-varying signal strengths. In order to increase the robustness to errors spanning multiple bits, interleaving is used when FEC is enabled. After de-interleaving, a continuous span of errors in the received stream will become single errors spread apart.

CC1150 employs matrix interleaving, which is illustrated in Figure 15. The on-chip interleaving buffer is a 4 x 4 matrix. In the transmitter, the data bits are written into the rows of the matrix, whereas the bit sequence to be transmitted is read from the columns of the matrix and fed to the rate ½ convolutional coder. Conversely, in a ***CC1101*** receiver, the received symbols are written into the rows of the matrix, whereas the data passed onto the convolutional decoder is read from the columns of the matrix.

When FEC and interleaving is used, at least one extra byte is required for trellis termination. In addition, the amount of data transmitted over the air must be a multiple of

the size of the interleaver buffer (two bytes). The packet control hardware therefore automatically inserts one or two extra bytes at the end of the packet, so that the total length of the data to be interleaved is an even number. Note that these extra bytes are invisible to the user, as they are removed before the received packet enters the RX FIFO in a *CC1101*.

When FEC and interleaving is used, the minimum data payload is 2 bytes in fixed and variable packet length mode.

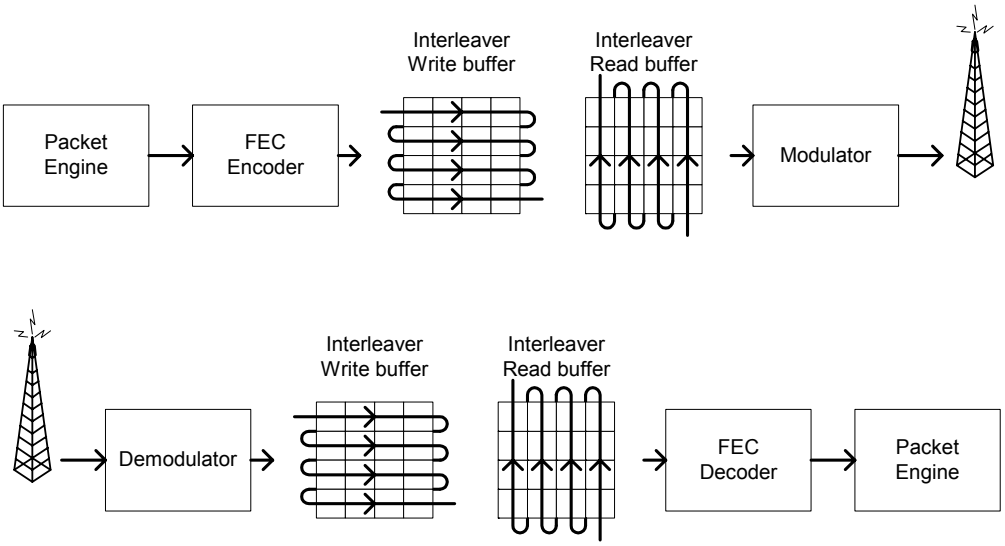


Figure 15: General Principle of Matrix Interleaving

16 Radio Control

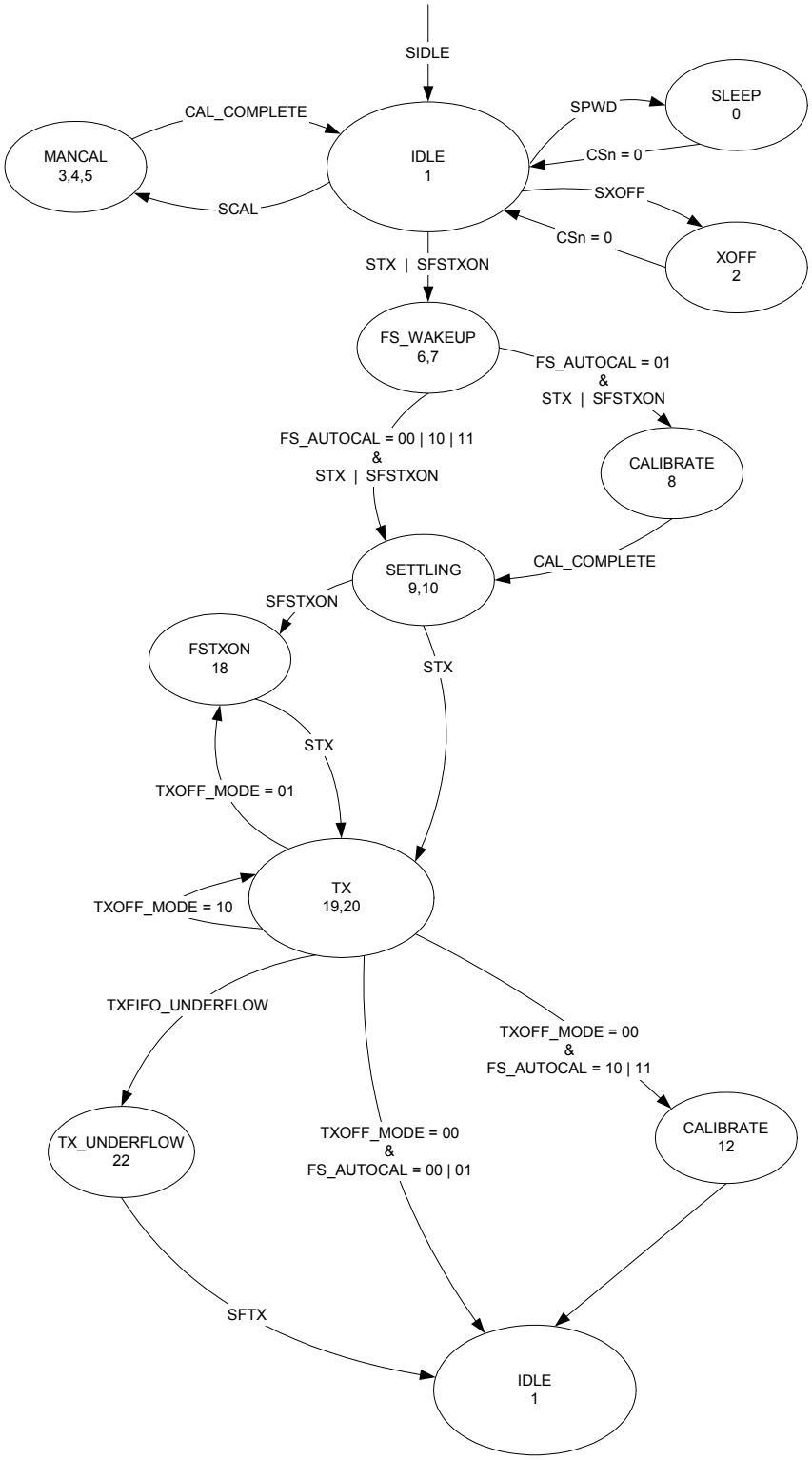


Figure 16: Radio Control State Diagram

CC1150 has a built-in state machine that is used to switch between different operations states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 7 on page 17. The complete radio control state diagram is shown in Figure 16. The numbers refer to the state number readable in the MARCSTATE status register. This functionality is primarily for test purposes.

16.1 Power on Start-up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, i.e. Automatic power-on reset or manual reset. After the automatic power-on reset or manual reset it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK_XOSC/192, but to optimize performance in TX, an alternative GDO setting should be selected from the settings found in Table 24 on page 38.

16.1.1 Automatic POR

A power-on reset circuit is included in the ***CC1150***. The minimum requirements stated in Section 4.7 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when CHIP_RDYn goes low. CHIP_RDYn is observed on the SO pin after CSn is pulled low. See Section 10.1 for more details on CHIP_RDYn.

When the ***CC1150*** reset is completed the chip will be in the IDLE state and the crystal oscillator running. If the chip has had sufficient time for the crystal oscillator and voltage regulator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed the SO pin will first go high, indicating that the crystal oscillator and voltage regulator is not stabilized, before going low as shown in Figure 17.

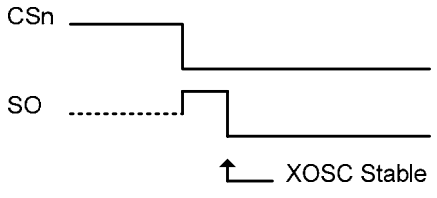


Figure 17: Power-on Reset

16.1.2 Manual Reset

The other global reset possibility on ***CC1150*** is the SRES command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The power-up sequence is as follows (see Figure 18):

- Set SCLK = 1 and SI = 0.
- Strobe CSn low / high. Make sure to hold CSn high for at least 40 µs relative to pulling CSn low.
- Pull CSn low and wait for SO to go low (CHIP_RDYn).
- Issue the SRES strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

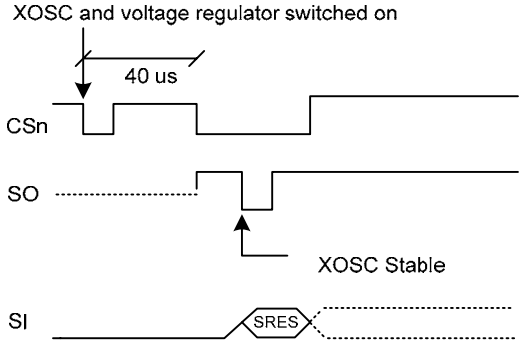


Figure 18: Power-up with SRES

Note that the above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the ***CC1150*** after this, it is only necessary to issue an SRES command strobe.

It is recommended to always send a SRES command strobe on the SPI interface after power-on even though power-on reset is used.

16.2 Crystal Control

The crystal oscillator is automatically turned on when CSn goes low. It will be turned off if the SXOFF or SPWD command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when

CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used; as described in Section 10.1 on page 19.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in section 4.3 on page 8.

16.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state, which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a SPWD command strobe has been sent on the SPI interface. The chip is then in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

On the ***CC1150***, all register values (with the exception of the MCSM0.PO_TIMEOUT field) are lost in the SLEEP state. After the chip gets back to the IDLE state, the registers will have default (reset) contents and must be reprogrammed over the SPI interface.

16.4 Active Mode

The active transmit mode is activated by the MCU by using the STX command strobe.

The frequency synthesizer must be calibrated regularly. ***CC1150*** has one manual calibration option (using the SCAL strobe), and three automatic calibration options, controlled by the MCSM0.FS_AUTOCAL setting:

- Calibrate when going from IDLE to TX (or FSTXON)
- Calibrate when going from TX to IDLE
- Calibrate every fourth time when going from TX to IDLE

The calibration takes a constant number of XOSC cycles; see Table 20 for timing details. When TX is active, the chip will remain in the TX state until the current packet has been successfully transmitted. Then the state will change as indicated by the MCSM1.TXOFF_MODE setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with STX.
- TX: Start sending preambles

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state. Note that if the radio goes from TX to IDLE by issuing an SIDLE strobe, the automatic calibration-when-going-from-TX-to-IDLE will not be performed.

16.5 Timing

The radio controller controls most timing in ***CC1150***, such as synthesizer calibration and PLL lock. Table 20 shows timing in crystal clock cycles for key state transitions. Timing from IDLE to TX is constant, dependent on the auto calibration setting. The calibration time is constant 18739 clock periods. Power on time and XOSC start-up times are variable, but within the limits stated in Table 6. Note that in a frequency hopping spread spectrum or a multi-channel protocol the calibration time can be reduced from 721 µs to approximately 150 µs. This is explained in section 24.2.

Description	XOSC periods	26 MHz crystal
Idle to TX/FSTXON, no calibration	2298	88.4 µs
Idle to TX/FSTXON, with calibration	~21037	809 µs
TX to IDLE, no calibration	2	0.1 µs
TX to IDLE, including calibration	~18739	721 µs
Manual calibration	~18739	721 µs

Table 20: State Transition Timing

17 Data FIFO

The ***CC1150*** contains a 64 byte FIFO for data to be transmitted. The SPI interface is used for writing to the TX FIFO. Section 10.5 contains details on the SPI FIFO access. The FIFO controller will detect underflow in the TX FIFO.

When writing to the TX FIFO, it is the responsibility of the MCU to avoid TX FIFO overflow. This will not be detected by the ***CC1150***. A TX FIFO overflow will result in an error in the TX FIFO content.

FIFO_THR	Bytes in TX FIFO
0 (0000)	61
1 (0001)	57
2 (0010)	53
3 (0011)	49
4 (0100)	45
5 (0101)	41
6 (0110)	37
7 (0111)	33
8 (1000)	29
9 (1001)	25
10 (1010)	21
11 (1011)	17
12 (1100)	13
13 (1101)	9
14 (1110)	5
15 (1111)	1

Table 21: FIFO_THR Settings and the corresponding FIFO Thresholds

The chip status byte that is available on the SO pin while transferring the SPI address contains the fill grade of the TX FIFO. Section 10.1 on page 19 contains more details on this.

The number of bytes in the TX FIFO can also be read from the TXBYTES.NUM_TXBYTES status register.

The 4-bit FIFOTHR.FIFO_THR setting is used to program the FIFO threshold point. Table 21 lists the 16 FIFO_THR settings and the corresponding thresholds for the TX FIFO.

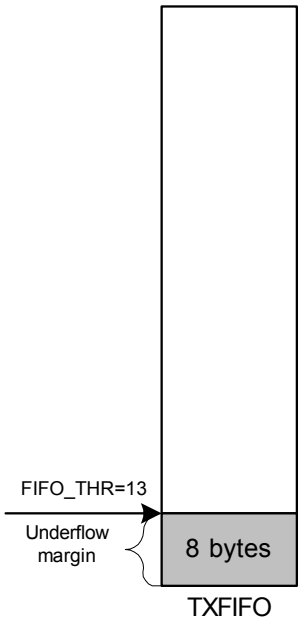


Figure 19: Example of FIFO at Threshold

A flag will assert when the number of bytes in the FIFO is equal to or higher than the programmed threshold. The flag is used to generate the FIFO status signals that can be viewed on the GDO pins (see section 22 on page 37).

Figure 19 shows the number of bytes in the TX FIFO when the threshold flag toggles, in the case of FIFO_THR=13. Figure 20 shows the flag as the FIFO is filled above the threshold, and then drained below.

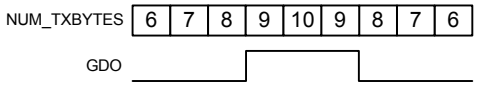


Figure 20: FIFO_THR=13 vs. Number of Bytes in FIFO

18 Frequency Programming

The frequency programming in ***CC1150*** is designed to minimize the programming needed in a channel-oriented system.

To set up a system with channel numbers, the desired channel spacing is programmed with the MDMCFG0.CHANSPC_M and MDMCFG1.CHANSPC_E registers. The channel spacing registers are mantissa and exponent respectively.

The base or start frequency is set by the 24 bit frequency word located in the FREQ2, FREQ1 and FREQ0 registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, CHANNR.CHAN, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot \left(FREQ + CHAN \cdot \left((256 + CHANSPC_M) \cdot 2^{CHANSPC_E-2} \right) \right)$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get e.g. 1 MHz channel spacing on solution is to use 333 kHz channel spacing and select each third channel in CHANNR.CHAN.

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency programming should only be updated when the radio is in the IDLE state.

19 VCO

The VCO is completely integrated on-chip.

19.1 VCO and PLL Self-Calibration

The VCO characteristics will vary with temperature and supply voltage changes, as well as the desired operating frequency. In order to ensure reliable operation, ***CC1150*** includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 20 on page 33.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off. This is configured with the MCSM0.FS_AUTOCAL register setting.

In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

The calibration values are not maintained in sleep mode. Therefore, the ***CC1150*** must be recalibrated after reprogramming the configuration registers when the chip has been in the SLEEP state.

To check that the PLL is in lock the user can program register IOCFGx.GDOx_CFG to 0x0A and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1 or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F. See more information in the ***CC1150*** Errata Notes [8].

For more robust operation the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

20 Voltage Regulators

CC1150 contains several on-chip linear voltage regulators, which generate the supply voltage needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 1 and Table 11 are not exceeded.

Setting the CSn pin low turns on the voltage regulator to the digital core and start the crystal oscillator. The SO pin on the SPI interface must go low before the first positive edge on the SCLK (setup time is s given in Table 15).

If the chip is programmed to enter power-down mode (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator for the digital core requires one external decoupling capacitor. The voltage regulator output should only be used for driving the *CC1150*.

21 Output Power Programming

The RF output power level from the device has two levels of programmability, as illustrated in Figure 21. Firstly, the special PATABLE register can hold up to eight user selected output power settings. Secondly, the 3-bit FREND0.PA_POWER value selects the PATABLE entry to use. This two-level functionality provides flexible PA power ramp up and ramp down at the start and end of transmission, as well as ASK modulation shaping. In each case, all the PA power settings in the PATABLE from index 0 up to the FREND0.PA_POWER value are used.

The power ramping at the start and at the end of a packet can be turned off by setting FREND0.PA_POWER to zero and then programming the desired output power to index 0 in the PATABLE.

If OOK modulation is used, the logic 0 and logic 1 power levels shall be programmed to index 0 and 1 respectively.

Table 22 contains recommended PATABLE settings for various output levels and frequency bands. DN012 [3] gives complete tables for the different frequency bands. Using PA settings from 0x61 to 0x6F is not recommended. Table 23 contains output power and current consumption for default PATABLE setting (0xC6).

PATABLE must be programmed in burst mode if you want to write to other entries than PATABLE[0]. See section 10.6 on page 22 for PATABLE programming details.

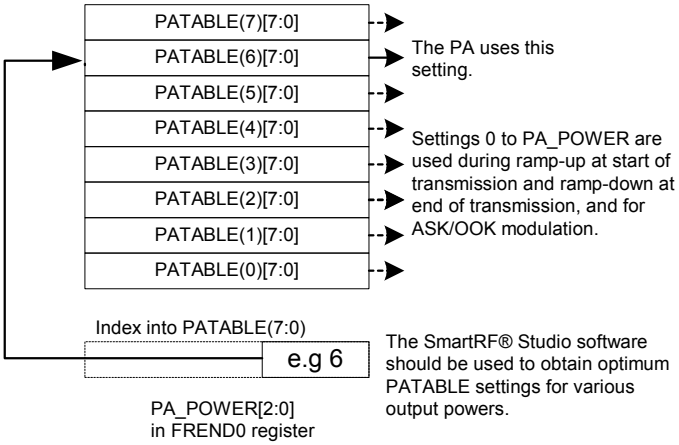


Figure 21: PA_POWER and PATABLE

	315 MHz		433 MHz		868 MHz		915 MHz	
Output power [dBm]	Setting	Current consumption, typ. [mA]	Setting	Current consumption, typ. [mA]	Setting	Current consumption, typ. [mA]	Setting	Current consumption, typ. [mA]
-30	0x12	9.9	0x03	10.8	0x03	11.2	0x03	11.1
-20	0x0E	10.4	0x0E	11.4	0x0C	11.7	0x0F	11.7
-10	0x26	12.5	0x26	13.3	0x26	13.7	0x34	13.6
-5	0x57	12.2	0x57	12.9	0x57	13.3	0x56	13.3
0	0x60	14.1	0x60	14.6	0x60	15.5	0x50	15.2
3	0x8B	15.8	0x8A	16.5	0x8A	17.4	0x89	17.4
7	0xCC	21.4	0xC8	23.0	0xCC	24.4	0xC8	24.6
10	0xC4	25.6	0xC2	26.1	0xC3	29.3	0xC0	29.3

Table 22: Optimum PATABLE Settings for Various Output Power Levels and Frequency Bands

	315 MHz		433 MHz		868 MHz		915 MHz	
Default power setting	Output power [dBm]	Current consumption, typ. [mA]	Output power [dBm]	Current consumption, typ. [mA]	Output power [dBm]	Current consumption, typ. [mA]	Output power [dBm]	Current consumption, typ. [mA]
0xC6	9.3	24.4	8.1	23.9	8.9	27.3	7.7	25.5

Table 23: Output Power and Current Consumption for Default PATABLE Setting

21.1 Shaping and PA Ramping

With ASK modulation, up to eight power settings are used for shaping. The modulator contains a counter that counts up when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate. The counter saturates at FREND0.PA_POWER and 0 respectively. This counter value is used as an index for a lookup in the power table. Thus, in order to utilize the whole table, FREND0.PA_POWER should be 7 when ASK is active. The shaping of the ASK signal is dependent on the configuration of the PATABLE. Figure 22 shows some examples of ASK shaping. Note that the OOK/ASK pulse shaping feature on the *CC1150* is only supported for output power levels below -1 dBm.

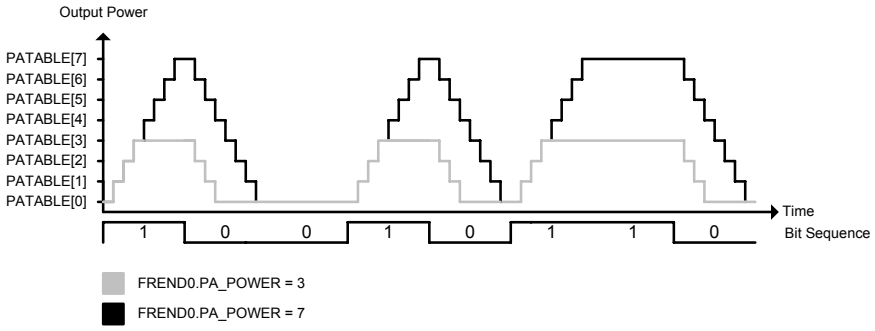


Figure 22: Shaping of ASK Signal

22 General Purpose / Test Output Control Pins

The two digital output pins GDO0 and GDO1 are general control pins. Their functions are programmed by IOCFG0.GDO0_CFG and IOCFG1.GDO1_CFG respectively. Table 24 shows the different signals that can be monitored on the GDO pins. These signals can be used as an interrupt to the MCU.

GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. The default value for GDO1 is 3-stated, which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 125 - 146 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running it can change the clock frequency by writing to IOCFG0.GDO0_CFG.

An on-chip analog temperature sensor is enabled by writing the value 128 (0x80h) to the IOCFG0.GDO0_CFG register. The voltage on the GDO0 pin is then proportional to temperature. See section 4.5 on page 9 for temperature sensor specifications.

GDOx_CFG[5:0]	Description	
0 (0x00)	Reserved – defined on the transceiver version (*CC1101*).	
1 (0x01)	Reserved – defined on the transceiver version (*CC1101*).	
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled at or above the TX FIFO threshold. De-asserts when the TX FIFO is below the same threshold.	
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below the TX FIFO threshold.	
4 (0x04)	Reserved – defined on the transceiver version (*CC1101*).	
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.	
6 (0x06)	Asserts when sync word has been sent, and de-asserts at the end of the packet. In TX the pin will also de-assert if the TX FIFO underflows.	
7 (0x07)	Reserved – defined on the transceiver version (*CC1101*).	
8 (0x08)	Reserved – defined on the transceiver version (*CC1101*).	
9 (0x09)	Reserved – defined on the transceiver version (*CC1101*).	
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.	
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. In TX mode, data is sampled by *CC1150* on the rising edge of the serial clock when GDOx_INV=0.	
12 (0x0C)	Reserved – defined on the transceiver version (*CC1101*).	
13 (0x0D)	Reserved – defined on the transceiver version (*CC1101*).	
14 (0x0E)	Reserved – defined on the transceiver version (*CC1101*).	
15 (0x0F)	Reserved – defined on the transceiver version (*CC1101*).	
16 (0x10)	Reserved – used for test.	
17 (0x11)	Reserved – used for test.	
18 (0x12)	Reserved – used for test.	
19 (0x13)	Reserved – used for test.	
20 (0x14)	Reserved – used for test.	
21 (0x15)	Reserved – used for test.	
22 (0x16)	Reserved – defined on the transceiver version (*CC1101*).	
23 (0x17)	Reserved – defined on the transceiver version (*CC1101*).	
24 (0x18)	Reserved – used for test.	
25 (0x19)	Reserved – used for test.	
26 (0x1A)	Reserved – used for test.	
27 (0x1B)	PA_PD. PA is enabled when 1, in power-down when 0.	
28 (0x1C)	Reserved – defined on the transceiver version (*CC1101*).	
29 (0x1D)	Reserved – defined on the transceiver version (*CC1101*).	
30 (0x1E)	Reserved – used for test.	
31 (0x1F)	Reserved – used for test.	
32 (0x20)	Reserved – used for test.	
33 (0x21)	Reserved – used for test.	
34 (0x22)	Reserved – used for test.	
35 (0x23)	Reserved – used for test.	
36 (0x24)	Reserved – defined on the transceiver version (*CC1101*).	
37 (0x25)	Reserved – defined on the transceiver version (*CC1101*).	
38 (0x26)	Reserved – used for test.	
39 (0x27)	Reserved – defined on the transceiver version (*CC1101*).	
40 (0x28)	Reserved – used for test.	
41 (0x29)	CHIP_RDYn.	
42 (0x2A)	Reserved – used for test.	
43 (0x2B)	XOSC_STABLE.	
44 (0x2C)	Reserved – used for test.	
45 (0x2D)	GDO0_Z_EN_N. When this output is 0, GDO0 is configured as input (for serial TX data).	
46 (0x2E)	High impedance (3-state).	
47 (0x2F)	HW to 0 (HW1 achieved by setting GDOx_INV=1).	
48 (0x30)	CLK_XOSC/1	Note: There are 2 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other GDO pin must be configured to values less than 0x30. The GDO0 default value is CLK_XOSC/192. To optimize RF performance, these signals should not be used while the radio is in TX mode.
49 (0x31)	CLK_XOSC/1.5	
50 (0x32)	CLK_XOSC/2	
51 (0x33)	CLK_XOSC/3	
52 (0x34)	CLK_XOSC/4	
53 (0x35)	CLK_XOSC/6	
54 (0x36)	CLK_XOSC/8	
55 (0x37)	CLK_XOSC/12	
56 (0x38)	CLK_XOSC/16	
57 (0x39)	CLK_XOSC/24	
58 (0x3A)	CLK_XOSC/32	
59 (0x3B)	CLK_XOSC/48	
60 (0x3C)	CLK_XOSC/64	
61 (0x3D)	CLK_XOSC/96	
62 (0x3E)	CLK_XOSC/128	
63 (0x3F)	CLK_XOSC/192	

Table 24: GDO signal selection(x = 0 or 1)

23 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the *CC1150* to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller and simplify software development.

23.1 Asynchronous Serial Operation

For backward compatibility with systems already using the asynchronous data transfer from other Chipcon products, asynchronous transfer is also included in *CC1150*.

When asynchronous transfer is enabled, several of the support mechanisms for the MCU that are included in *CC1150* will be disabled, such as packet handling hardware, buffering in the FIFO and so on. The asynchronous transfer mode does not allow the use of the data whitener, interleaver and FEC, and it is not possible to use Manchester encoding. MSK is not supported for asynchronous transfer.

Setting PKTCTRL0.PKT_FORMAT to 3 enables asynchronous transparent (serial) mode. In TX, the GDO0 pin is used for data input (TX data).

The MCU must control start and stop of transmit with the STX and SIDLE strobes.

The *CC1150* modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

23.2 Synchronous Serial Operation

Setting PKTCTRL0.PKT_FORMAT to 1 enables synchronous serial operation mode. In this operational mode the data must be NRZ encoded (MDMCFG2.MANCHESTER_EN=0). In synchronous serial operation mode, data is transferred on a two wire serial interface. The *CC1150* provides a clock that is used to set up new data on the data input line. Data input (TX data) is the GDO0 pin. This pin will automatically be configured as an input when TX is active. The TX latency is 8 bits.

Preamble and sync word insertion may or may not be active, dependent on the sync mode set by the MDMCFG3.SYNC_MODE.

If preamble and sync word is disabled, all other packet handler features and FEC should also be disabled. The MCU must then handle preamble and sync word insertion in software.

If preamble and sync word insertion is left on, all packet handling features and FEC can be used. When using the packet handling features synchronous serial mode, the *CC1150* will insert the preamble and sync word and the MCU will only provide the data payload. This is equivalent to the recommended FIFO operation mode.

24 System considerations and Guidelines

24.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. Short Range Devices (SRDs) for license free operation below 1 GHz are usually operated in the 315 MHz, 433 MHz, 868 MHz or 915 MHz frequency bands. The *CC1150* is specifically designed for such use with its 300-348 MHz, 400-464 MHz and 800-928 MHz operating ranges. The most important regulations when using the *CC1150* in the 315 MHz, 433 MHz, 868 MHz or 915 MHz frequency bands are EN 300 220 (Europe) and FCC CFR47 part 15 (USA). A summary of the most important aspects of these regulations can be found in AN001 [10].

Please note that compliance with regulations is dependent on complete system performance. It is the end product manufactor's

responsibility to ensure that the system complies with regulations.

24.2 Frequency Hopping and Multi-Channel Systems

The 315 MHz, 433 MHz, 868 MHz or 915 MHz bands are shared by many systems both in industrial, office and home environments. It is therefore recommended to use frequency hopping spread spectrum (FHSS) or a multi-channel protocol because the frequency diversity makes the system more robust with respect to interference from other systems operating in the same frequency band. FHSS also combats multipath fading.

CC1150 is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface. Using the packet handling support and data buffering is also beneficial in such systems as these features will significantly offload the host controller.

Charge pump current, VCO current and VCO capacitance array calibration data is required for each frequency when implementing frequency hopping for ***CC1150***. There are 3 ways of obtaining the calibration data from the chip:

1) Frequency hopping with calibration for each hop. The PLL calibration time is approximately 720 µs. The blanking interval between each frequency hop is then approximately 810 µs.

2) Fast frequency hopping without calibration for each hop can be done by calibrating each frequency at startup and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values in MCU memory. The VCO capacitance calibration FSCAL1 register value must be found for each RF frequency to be used. The VCO current calibration value and the charge pump current calibration value available in FSCAL2 and FSCAL3 respectively are not dependent on the RF frequency, so the same value can therefore be used for all RF frequencies for these two registers. Between each frequency hop, the calibration process can then be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values that corresponds to the next RF frequency. The PLL turn on time is approximately 90 µs. The blanking interval between each frequency hop is then approximately 90 µs.

3) Run calibration on a single frequency at startup. Next write 0 to FSCAL3[5:4] to disable the charge pump calibration. After writing to FSCAL3[5:4], strobe STX with MCSM0.FS_AUTOCAL=1 for each new frequency hop. That is, VCO current and VCO capacitance calibration is done, but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from approximately 720 µs to approximately 150 µs. The blanking interval between each frequency hop is then approximately 240 µs.

There is a trade off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. This solution also requires that the supply voltage and temperature do not vary much in order to have a robust solution. Solution 3) gives approximately 570 µs smaller blanking interval than solution 1).

The recommended settings for TEST0.VCO_SEL_CAL_EN change with frequency. This means that one should always use SmartRF Studio [11] to get the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is being used. It must be noted that the content of the ***CC1150*** is not retained in SLEEP state, and thus it is necessary to write to the TEST0 register, along with other registers, when returning from the SLEEP state and initiating calibrations.

24.3 Wideband Modulation not using Spread Spectrum

Digital modulation systems under FFC part 15.247 include FSK and GFSK modulation. A maximum peak output power of 1W (+30 dBm) is allowed if the 6 dB bandwidth of the modulated signal exceeds 500 kHz. In addition, the peak power spectral density conducted to the antenna shall not be greater than +8 dBm in any 3 kHz band.

Operating at high data rates and frequency deviation the ***CC1150*** is suited for systems targeting compliance with digital modulation system as defined by FFC part 15.247. An external power amplifier is needed to increase the output above +10 dBm. Please refer to DN006 [5] for further details concerning wideband modulation and ***CC1150***.

24.4 Data Burst Transmissions

The high maximum data rate of *CC1150* opens up for burst transmissions. A low average data rate link (e.g. 10 kBaud), can be realized using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (e.g. 500 kBaud) will reduce the time in active mode, and hence also reduce the average current consumption significantly. Reducing the time in active mode will reduce the likelihood of collisions with other systems in the same frequency range.

24.5 Continuous Transmissions

In data streaming applications the *CC1150* opens up for continuous transmissions at 500 kBaud effective data rate. As the modulation is done with a closed loop PLL, there is no limitation in the length of a transmission (open loop modulation used in some transceivers often prevents this kind of continuous data streaming and reduces the effective data rate).

24.6 Low Cost Systems

As the *CC1150* provides 500 kBaud multi-channel performance without any external filters, a very low cost system can be made. A HC-49 type SMD crystal is used in the CC1150EM reference design ([1] and [1]). Note that the crystal package strongly influences the price. In a size constrained PCB design a smaller, but more expensive, crystal may be used.

24.7 Battery Operated Systems

In low power applications, the SLEEP state should be used when the *CC1150* is not active.

24.8 Increasing Output Power

In some applications it may be necessary to extend the link range. Adding an external power amplifier is the most effective way of doing this. The power amplifier should be inserted between the antenna and the balun as shown in Figure 23.

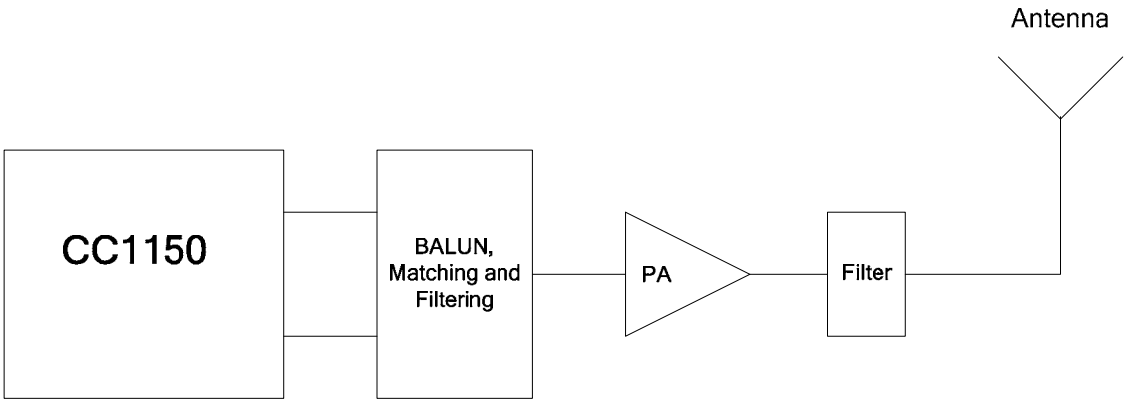


Figure 23 Block Diagram of *CC1150* Usage with External Power Amplifier

25 Configuration Registers

The configuration of ***CC1150*** is done by programming 8-bit registers. The configuration data based on selected system parameters are most easily found by using the SmartRF Studio [11] software. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 9 Command Strobe Registers, listed in Table 25 Accessing these registers will initiate the change of an internal state or mode. There are 29 normal 8-bit Configuration Registers, listed in Table 26. Many of these registers are for test purposes only, and need not be written for normal operation of ***CC1150***.

There are also 6 Status registers, which are listed in Table 27. These registers, which are read-only, contain information about the status of ***CC1150***.

The TX FIFO is accessed through one 8-bit register. Only write operations are allowed to the TX FIFO.

During the address transfer and while writing to a register or the TX FIFO, a status byte is returned. This status byte is described in Table 16 on page.20.

Table 28 summarizes the SPI address space. Registers that are only defined on the ***CC1101*** transceiver are also listed. ***CC1101*** and ***CC1150*** are register compatible, but registers and fields only implemented in the transceiver always contain 0 in ***CC1150***.

The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL=1).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off (enables quick start). SCAL can be strobed in IDLE state without setting manual calibration mode (MCSM0.FS_AUTOCAL=0)
0x35	STX	Enable TX. Perform calibration first if MCSM0.FS_AUTOCAL=1.
0x36	SIDLE	Exit TX and turn off frequency synthesizer.
0x39	SPWD	Enter power down mode when CSn goes high.
0x3B	SFTX	Flush the TX FIFO buffer.
0x3D	SNOP	No operation. May be used to pad strobe commands to two bytes for simpler software.

Table 25: Command Strobes

Address	Register	Description	Details on page number
0x01	IOCFG1	GDO1 output pin configuration	45
0x02	IOCFG0	GDO0 output pin configuration	45
0x03	FIFOTHR	FIFO threshold	45
0x04	SYNC1	Sync word, high byte	46
0x05	SYNC0	Sync word, low byte	46
0x06	PKTLEN	Packet length	46
0x08	PKTCTRL0	Packet automation control	46
0x09	ADDR	Device address	47
0x0A	CHANNR	Channel number	47
0x0D	FREQ2	Frequency control word, high byte	47
0x0E	FREQ1	Frequency control word, middle byte	47
0x0F	FREQ0	Frequency control word, low byte	47
0x10	MDMCFG4	Modulator configuration	47
0x11	MDMCFG3	Modulator configuration	48
0x12	MDMCFG2	Modulator configuration	49
0x13	MDMCFG1	Modulator configuration	50
0x14	MDMCFG0	Modulator configuration	50
0x15	DEVIATN	Modulator deviation setting	51
0x17	MCSM1	Main Radio Control State Machine configuration	51
0x18	MCSM0	Main Radio Control State Machine configuration	52
0x22	FREND0	Front end TX configuration	52
0x23	FSCAL3	Frequency synthesizer calibration	53
0x24	FSCAL2	Frequency synthesizer calibration	53
0x25	FSCAL1	Frequency synthesizer calibration	53
0x26	FSCAL0	Frequency synthesizer calibration	53
0x29	FSTEST	Frequency synthesizer calibration control	54
0x2A	PTEST	Production test	54
0x2C	TEST2	Various test settings	54
0x2D	TEST1	Various test settings	54
0x2E	TEST0	Various test settings	54

Table 26: Configuration Registers Overview

Address	Register	Description	Details on page number
0x30 (0xF0)	PARTNUM	Part number for *CC1150*	55
0x31 (0xF1)	VERSION	Current version number	55
0x35 (0xF5)	MARCSTATE	Control state machine state	55
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	56
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module	56
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	56

Table 27: Status Registers Overview

	Write		Read		
	Single byte	Burst	Single byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	WOREVT1				
0x1F	WOREVT0				
0x20	WORCTRL				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	RCCTRL1				
0x28	RCCTRL0				
0x29	FSTEST				
0x2A	PTEST				
0x2B	AGCTEST				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	LQI	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	WORTIME1	
0x37	SAFC		SAFC	WORTIME0	
0x38	SWOR		SWOR	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	SWORRST		SWORRST		
0x3D	SNOP		SNOP		
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 28: SPI Address Space (greyed text: not implemented on *CC1150* thus only valid for the transceiver version (*CC1101*))

25.1 Configuration Register Details

0x01: IOCFG1 – GDO1 output pin configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0).
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is tri-state (See Table 24 on page 38).

0x02: IOCFG0 – GDO0 output pin configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0).
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (See Table 24 on page 38). It is recommended to disable the clock output during initialization in order to optimize RF performance.

0x03: FIFOTHR – FIFO threshold

Bit	Field Name	Reset	R/W	Description
7:4	Reserved	0	R/W	Write 0 for compatibility with possible future extensions.
3:0	FIFO_THR[3:0]	7 (0x07)	R/W	Set the threshold for the TX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.

Setting	Bytes in TX FIFO
0 (0000)	61
1 (0001)	57
2 (0010)	53
3 (0011)	49
4 (0100)	45
5 (0101)	41
6 (0110)	37
7 (0111)	33
8 (1000)	29
9 (1001)	25
10 (1010)	21
11 (1011)	17
12 (1100)	13
13 (1101)	9
14 (1110)	5
15 (1111)	1

0x04: SYNC1 – Sync word, high byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word.

0x05: SYNC0 – Sync word, low byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word.

0x06: PKTLEN – Packet length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed length packets are enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed.

0x08: PKTCTRL0 – Packet automation control

Bit	Field Name	Reset	R/W	Description
7			R0	Not Used.
6	WHITE_DATA	1	R/W	Turn data whitening on / off 0: Whitening off 1: Whitening on
5:4	PKT_FORMAT[1:0]	0	R/W	Format of TX data Setting: Packet format 0 (00): Normal mode, use TX FIFO 1 (01): Serial Synchronous mode, data in on GDO0 2 (10): Random TX mode; sends random data using PN9 generator. Used for test/debug. 3 (11): Asynchronous transparent mode. Data in on GDO0
3		0	R/W	Not used.
2	CRC_EN	1	R/W	1: CRC calculation enabled 0: CRC disabled
1:0	LENGTH_ CONFIG[1:0]	1	R/W	Configure the packet length Setting: Packet length configuration 0 (00): Fixed length packets, length configured in PKTLEN register 1 (01): Variable length packets, packet length configured by the first byte after sync word 2 (10): Infinite packet length packets 3 (11): Reserved

0x09: ADDR – Device address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDRESS [7:0]	0	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR – Channel number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0D: FREQ2 – Frequency control word, high byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0	R	FREQ[23:22] is always 0 (the FREQ2 register is less than 36 with 26 MHz or higher crystal frequency).
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:0] is the base frequency for the frequency synthesiser in increments of $F_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 – Frequency control word, middle byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. FREQ2 register.

0x0F: FREQ0 – Frequency control word, low byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. FREQ2 register.

0x10: MDMCFG4 – Modulator configuration

Bit	Field Name	Reset	R/W	Description
7:4	Reserved	8 (0x08)	R0	Defined on the transceiver version (*CC1101*).
3:0	DRATE_E[3:0]	12 (0x0C)	R/W	The exponent of the user specified symbol rate.

0x11: MDMCFG3 – Modulator configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE_M) \cdot 2^{DRATE_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 – Modulator configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved</td><td>0</td><td>R0</td><td>Defined on the transceiver version (CC1101).</td></tr>
<tr><td>6:4</td><td>MOD_FORMAT[2:0]</td><td>0</td><td>R/W</td><td>The modulation format of the radio signal
<table><tr><td>Setting</td><td>Modulation format</td></tr><tr><td>0 (000)</td><td>2-FSK</td></tr><tr><td>1 (001)</td><td>GFSK</td></tr><tr><td>2 (010)</td><td>-</td></tr><tr><td>3 (011)</td><td>ASK/OOK</td></tr><tr><td>4 (100)</td><td>-</td></tr><tr><td>5 (101)</td><td>-</td></tr><tr><td>6 (110)</td><td>-</td></tr><tr><td>7 (111)</td><td>MSK</td></tr></table>The OOK/ASK pulse shaping feature is only supported for output powers up to -1 dBm.
MSK is only supported for data rates above 26 kBaud.</td></tr>
<tr><td>3</td><td>MANCHESTER_EN</td><td>0</td><td>R/W</td><td>Enables Manchester encoding/decoding.
0 = Disable
1 = Enable</td></tr>
<tr><td>2:0</td><td>SYNC_MODE[2:0]</td><td>2</td><td>R/W</td><td>Combined sync-word qualifier mode.
The values 0 (000) and 4 (100) disables preamble and sync word transmission. The values 1 (001), 2 (001), 5 (101) and 6 (110) enables 16-bit sync word transmission. The values 3 (011) and 7 (111) enables repeated sync word transmission. The table below lists the meaning of each mode (for compatibility with the CC1101 transceiver):
<table><tr><td>Setting</td><td>Sync-word qualifier mode</td></tr><tr><td>0 (000)</td><td>No preamble/sync word</td></tr><tr><td>1 (001)</td><td>15/16 sync word bits detected</td></tr><tr><td>2 (010)</td><td>16/16 sync word bits detected</td></tr><tr><td>3 (011)</td><td>30/32 sync word bits detected</td></tr><tr><td>4 (100)</td><td>No preamble/sync, carrier-sense above threshold</td></tr><tr><td>5 (101)</td><td>15/16 + carrier-sense above threshold</td></tr><tr><td>6 (110)</td><td>16/16 + carrier-sense above threshold</td></tr><tr><td>7 (111)</td><td>30/32 + carrier-sense above threshold</td></tr></table></td></tr>
</table>

0x13: MDMCFG1 – Modulator configuration

Bit	Field Name	Reset	R/W	Description
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload 0 = Disable 1 = Enable (Only supported for fixed packet length mode, i.e. `PKTCTRL0.LENGTH_CONFIG=0`)
6:4	NUM_PREAMBLE[2:0]	2	R/W	Sets the minimum number of preamble bytes to be transmitted
3:2			R0	Not Used.
1:0	CHANSPC_E[1:0]	2	R/W	2 bit exponent of channel spacing.

Setting	Number of preamble bytes
0 (000)	2
1 (001)	3
2 (010)	4
3 (011)	6
4 (100)	8
5 (101)	12
6 (110)	16
7 (111)	24

0x14: MDMCFG0 – Modulator configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing (initial 1 assumed). The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC_M) \cdot 2^{CHANSPC_E} \cdot CHAN$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN – Modulator deviation setting

Bit	Field Name	Reset	R/W	Description
7			R0	Not Used.
6:4	DEVIATION_E[2:0]	4	R/W	Deviation exponent.
3			R0	Not Used.
2:0	DEVIATION_M[2:0]	7	R/W	When MSK modulation is enabled: Specifies the fraction of symbol period (1/8-8/8) during which a phase change occurs ('0': +90deg, '1':-90deg). Refer to the SmartRF Studio [11] software for correct DEVIATN setting when using MSK. When 2-FSK/GFSK modulation is enabled: Deviation mantissa, interpreted as a 4-bit value with MSB implicit 1. The resulting frequency deviation is given by: $f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION_M) \cdot 2^{DEVIATION_E}$ The default values give ±47.607 kHz deviation, assuming 26.0 MHz crystal frequency. When ASK/OOK modulation is enabled: This setting has no effect.

0x17: MCSM1 – Main Radio Control State Machine configuration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not Used.
5:2	Reserved	12 (0x0C)	R0	Defined on the transceiver version (*CC1101*).
1:0	TXOFF_MODE[1:0]	0	R/W	Select what should happen when a packet has been sent (TX)

Setting	Next state after finishing packet transmission
0 (00)	IDLE
1 (01)	FSTXON
2 (10)	Stay in TX (start sending preamble)
3 (11)	Do not use, not implemented on *CC1150*

0x18: MCSM0 – Main Radio Control State Machine configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td>Not Used.</td></tr>
<tr><td>5:4</td><td>FS_AUTOCAL[1:0]</td><td>0)</td><td>R/W</td><td>Automatically calibrate when going to TX, or back to IDLE
<table><tr><td>Setting</td><td>When to perform automatic calibration</td></tr><tr><td>0 (00)</td><td>Never (manually calibrate using SCAL strobe)</td></tr><tr><td>1 (01)</td><td>When going from IDLE to TX (or FSTXON)</td></tr><tr><td>2 (10)</td><td>When going from TX back to IDLE</td></tr><tr><td>3 (11)</td><td>Every 4th time when going from TX to IDLE</td></tr></table></td></tr>
<tr><td>3:2</td><td>PO_TIMEOUT</td><td>1</td><td>R/W</td><td>Programs the number of times the six-bit ripple counter must expire after XOSC has stabilized before CHP_RDY_N goes low.
The XOSC is off during power-down and if the regulated digital supply voltage has sufficient time to stabilize while waiting for the crystal to be stable, PO_TIMEOUT can be set to 0. For robust operation it is recommended to use PO_TIMEOUT=2.
<table><tr><td>Setting</td><td>Expire count</td><td>Timeout after XOSC start</td></tr><tr><td>0 (00)</td><td>1</td><td>Approx. 2.3 µs – 2.7 µs</td></tr><tr><td>1 (01)</td><td>16</td><td>Approx. 37 µs – 43 µs</td></tr><tr><td>2 (10)</td><td>64</td><td>Approx. 146 µs – 171 µs</td></tr><tr><td>3 (11)</td><td>256</td><td>Approx. 585 µs – 683 µs</td></tr></table>Exact timeout depends on crystal frequency.
In order to reduce start up time from the SLEEP state, this field is preserved in powerdown (SLEEP state).</td></tr>
<tr><td>1:0</td><td>Reserved</td><td></td><td>R0</td><td>Defined on the transceiver version (CC1101)</td></tr>
</table>

0x22: FREND0 – Front end TX configuration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not Used.
5:4	LODIV_BUF_ CURRENT_TX[1:0]	1	R/W	Adjusts current TX LO buffer (input to PA). The value to use in register field is given by the SmartRF Studio [11] software.
3			R0	Not Used.
2:0	PA_POWER[2:0]	0	R/W	Selects PA power setting. This value is an index to the PATABLE, which can be programmed with up to 8 different PA settings. In ASK mode, this selects the PATABLE index to use when transmitting a '1'. PATABLE index zero is used in ASK when transmitting a '0'. The PATABLE settings from index '0' to the PA_POWER value are used for ASK TX shaping, and for power ramp-up/ramp-down at the start/end of transmission in all TX modulation formats.

0x23: FSCAL3 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (0x02)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF® Studio software.
5:4	CHP_CURR_CAL_EN[1:0]	2 (0x02)	R/W	Disable charge pump calibration stage when 0.
3:0	FSCAL3[3:0]	9 (0x09)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: I_OUT = I0·2FSCAL3[3:0]/4 Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x24: FSCAL2 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not Used.
5	VCO_CORE_H_EN	0	R/W	Choose high (1)/ low (0) VCO.
5:0	FSCAL2[5:0]	10 (0x0A)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not Used.
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency synthesizer calibration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	Not Used.
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in register field is given by the SmartRF Studio [11] software.

0x29: FSTEST – Frequency synthesizer calibration control

Bit	Field Name	Reset	R/W	Description
7:0	FSTEST[7:0]	87 (0x57)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production test

Bit	Field Name	Reset	R/W	Description
7:0	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2C: TEST2 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]		R/W	The value to use in this register is given by the SmartRF Studio [11] software.

0x2D: TEST1 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x21)	R/W	The value to use in this register is given by the SmartRF Studio [11] software.

0x2E: TEST0 – Various test settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2(0x02)	R/W	The value to use in this register is given by the SmartRF Studio [11] software.
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1. The value to use in this register is given by the SmartRF Studio [11] software.
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF Studio [11] software.

25.2 Status register details

0x30 (0xF0): PARTNUM – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	2 (0x02)	R	Chip part number.

0x31 (0xF1): VERSION – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	4 (0x04)	R	Chip version number.

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine state

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	MARC_STATE[4:0]		R	Main Radio Control FSM State

Value	State name	State (Figure 16, page 30)
0 (0x00)	SLEEP	SLEEP
1 (0x01)	IDLE	IDLE
2 (0x02)	XOFF	XOFF
3 (0x03)	VCOON_MC	MANCAL
4 (0x04)	REGON_MC	MANCAL
5 (0x05)	MANCAL	MANCAL
6 (0x06)	VCOON	FS_WAKEUP
7 (0x07)	REGON	FS_WAKEUP
8 (0x08)	STARTCAL	CALIBRATE
9 (0x09)	BWBOOST	SETTLING
10 (0x0A)	FS_LOCK	SETTLING
11 (0x0B)	N/A	N/A
12 (0x0C)	ENDCAL	CALIBRATE
13 (0x0D)	N/A	N/A
14 (0x0E)	N/A	N/A
15 (0x0F)	N/A	N/A
16 (0x10)	N/A	N/A
17 (0x11)	N/A	N/A
18 (0x12)	FSTXON	FSTXON
19 (0x13)	TX	TX
20 (0x14)	TX_END	TX
21 (0x15)	N/A	N/A
22 (0x16)	TX_UNDERFLOW	TX_UNDERFLOW

Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.

0x38 (0xF8): PKTSTATUS – Current GDOx status

Bit	Field Name	Reset	R/W	Description
7:2	Reserved		R0	Defined on the transceiver version (*CC1101*).
1			R0	Not Used.
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective what IOCFG0.GDO0_INV is programmed to. It is not recommended to check for PLL lock by reading PKTSTATUS[0] with GDO0_CFG = 0x0A.

0x39 (0xF9): VCO_VC_DAC – Current setting from PLL calibration module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]		R	Status registers for test only.

0x3A (0xFA): TXBYTES – Underflow and number of bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO.

26 Package Description (QLP 16)

26.1 Recommended PCB layout for package (QLP 16)

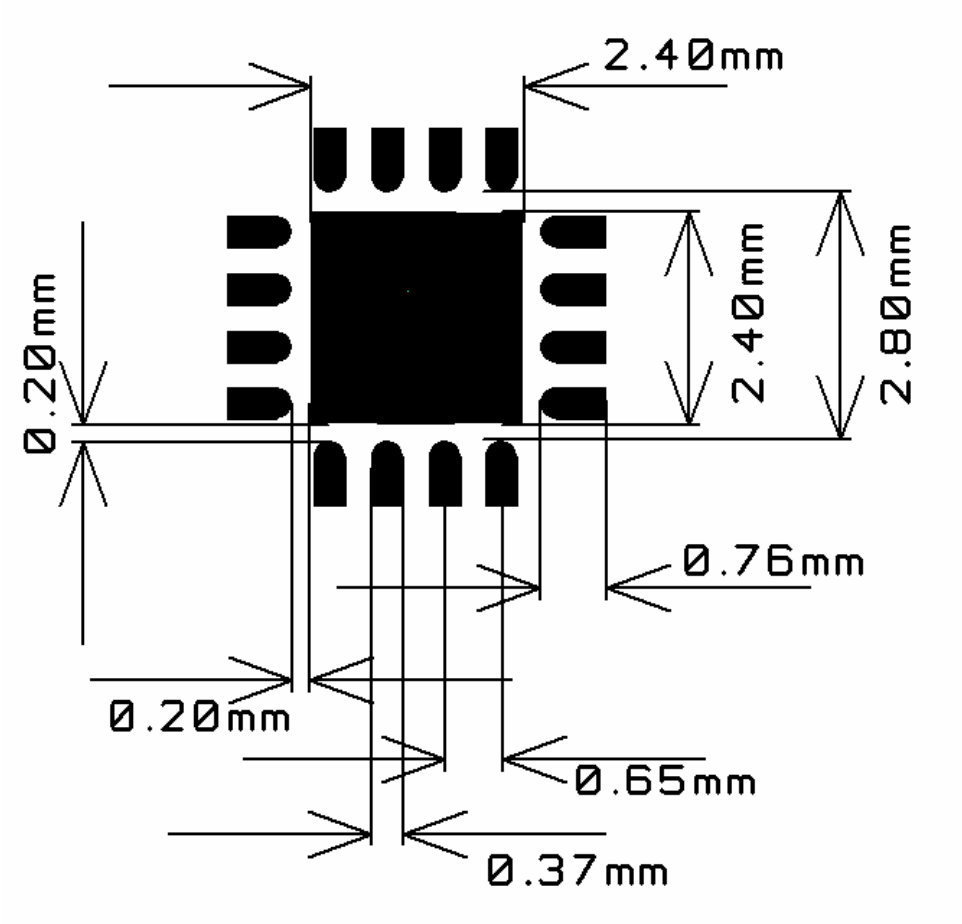


Figure 24: Recommended PCB layout for QLP 16 package

Note: The figure is an illustration only and not to scale. There are five 10 mil diameter via holes distributed symmetrically in the ground pad under the package. See also the CC1150EM reference design ([1] and [2]).

26.2 Soldering information

The recommendations for lead-free reflow in IPC/JEDEC J-STD-020 should be followed.

27 References

[1] CC1150EM 315 - 433 MHz Reference Design www.ti.com/lit/zip/swrr041
[2] CC1150EM 868 - 915 MHz Reference Design www.ti.com/lit/zip/swrr042
[3] DN012 Programming Output Power on CC1100 and CC1150 www.ti.com/lit/swra150
[4] AN039 Using the CC1100/CC1150 in the European 433 and 868 MHz ISM Bands www.ti.com/lit/swra054
[5] DN006 CC11xx Settings for FCC 15.247 Solutions www.ti.com/lit/swra123
[6] DN017 CC11xx 868/915 MHz Matching www.ti.com/lit/swra168
[7] AN058 Antenna Selection Guide www.ti.com/lit/swra161
[8] CC1150 Errata Notes www.ti.com/lit/swrz018
[9] DN501 PATABLE Access www.ti.com/lit/swra110
[10] AN001 SRD Regulations for Licence Free Transceiver Operation www.ti.com/lit/swra090
[11] SmartRF Studio http://www.ti.com/smartrfstudio
[12] CC1100/CC1150DK& CC2500/CC2550DK Development Kit Examples and Libraries User Manual www.ti.com/lit/swru109

28 General Information

28.1 Document History

Revision	Date	Description/Changes
SWRS037A	2009-07-20	• Changed title of the datasheet • Updated from preliminary datasheet to active • Removed “Chipcon Products from Texas Instruments” Logo • Generally updated text, edited and formatted text • Added Voltage ramp-up and ESD info in Table 1 • Moved the General Characteristics before the Electrical Specifications • Updated data rate and modulation info in Table 3 • Added links to reference designs • Updated numbers in Table 4 and added link to DN012 • Added links to AN039 and DN006 • Added information regarding load impedance, TX harmonics and spurious emission information and TX latency in Table 5 • Added information regarding crystal load capacitance and changed start-up time in Table 6 • Added phase noise information in Table 7 • Updated information regarding the analog temperature sensor in Table 8 • Updated the application circuit figures and corresponding information and tables in section 7 • Moved and added figures and information regarding the crystal to section 7.3 and regarding using an external reference signal instead of a crystal in section 7.4, removed information regarding SmartRF Studio and crystal choice • Added information regarding the 699 MHz filter and wire wound inductors in section 7.5 and added link to DN017 • Added information regarding the 699 MHz filter and wire wound inductors in section 7.5 and added link to DN017 • Added section 7.7 and link to AN058 • Added section regarding PCB layout recommendations (section 7.8) and Figure 6 • Updated Figure 7 • Updated SmartRF Studio appearance figure and added information on where to find default configuration register values • Added more information in section 10 • Moved Figure 9 and added Figure 11 and Table 15 and Table 16. • Added section 10.3 SPI Read and link to the CC1150 Errata Notes • Added information in section 10.4 and Figure 10 • Added link to DN501 and output power limit when using ASK • Added section 11.3 and Table 17 • Added Table 18 • Added more information in section 13 (recommended number of preamble and sync word bytes, not turn of TX during first part of a byte, how to leave TXFIFO UNDERFLOW etc) • Added section 13.4

Revision	Date	Description/Changes
		• Added more information in section 14 • Added Figure 12 • Added Table 19 • Added more information in section 15 and updated Figure 15 • Updated section 16.1 and added Figure 17 • Added information regarding the PLL lock signal in section 19 • Updated section 21, Table 22 and Table 23 and added Figure 22 • Updated Table 24 • Added more information in section 23 • Added section 24 and link to AN001 • Updated section 25 and register descriptions • Changed IOCFG0 – GDO0 output pin configuration description • Changed MDMCFG2 – Modulator configuration description • Updated the FSCAL registers and TEST registers • Replaced old Chipcon packet information with the TI packet information and updated this to fit TI formatting. • Added reference to SmartRF Studio website • Link to swru109 • Added the Reference Chapter
1.1	2005-06-27	Added matching information. Added information about using a reference signal instead of a crystal.
1.0	2005-04-20	First preliminary data sheet release

Table 29: Document History

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CC1150-RTR1	ACTIVE	VQFN	RST	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1150	Samples
CC1150-RTY1	ACTIVE	VQFN	RST	16	490	TBD	Call TI	Call TI	-40 to 85	CC1150	Samples
CC1150RST	ACTIVE	VQFN	RST	16	490	TBD	Call TI	Call TI	-40 to 85	CC1150	Samples
CC1150RSTG3	ACTIVE	VQFN	RST	16	490	TBD	Call TI	Call TI	-40 to 85	CC1150	Samples
CC1150RSTR	ACTIVE	VQFN	RST	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1150	Samples
CC1150RSTRG3	ACTIVE	VQFN	RST	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1150	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

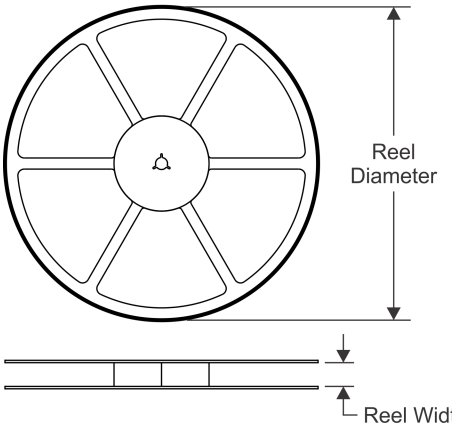
(4) Only one of markings shown within the brackets will appear on the physical device.

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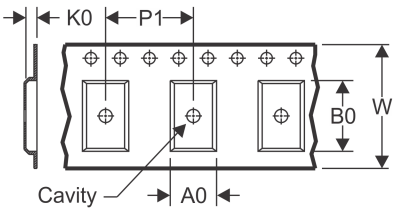
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

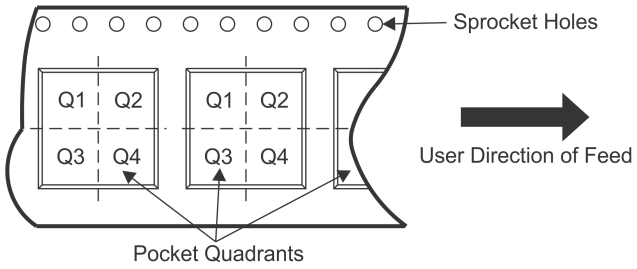


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

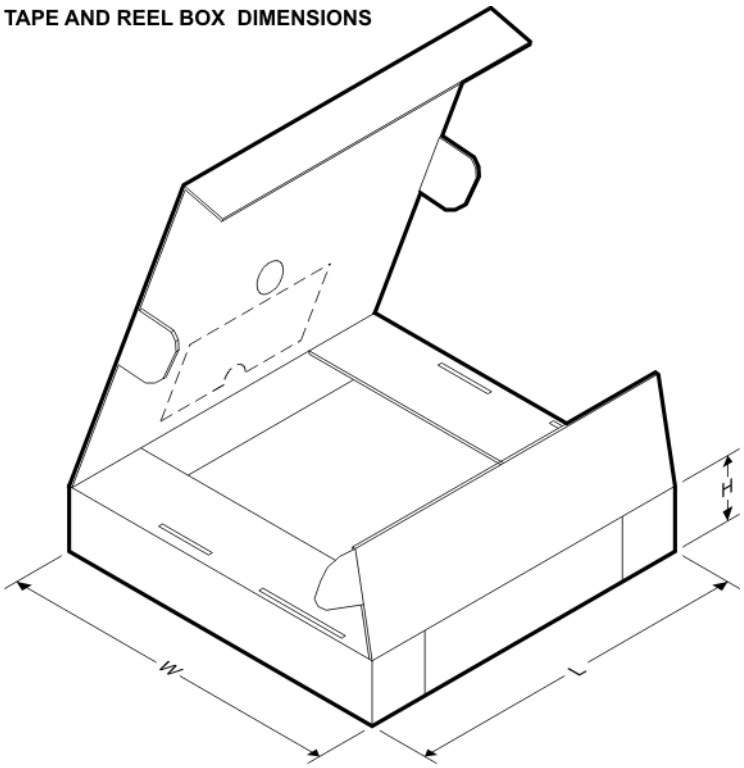
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1150RSTR	VQFN	RST	16	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

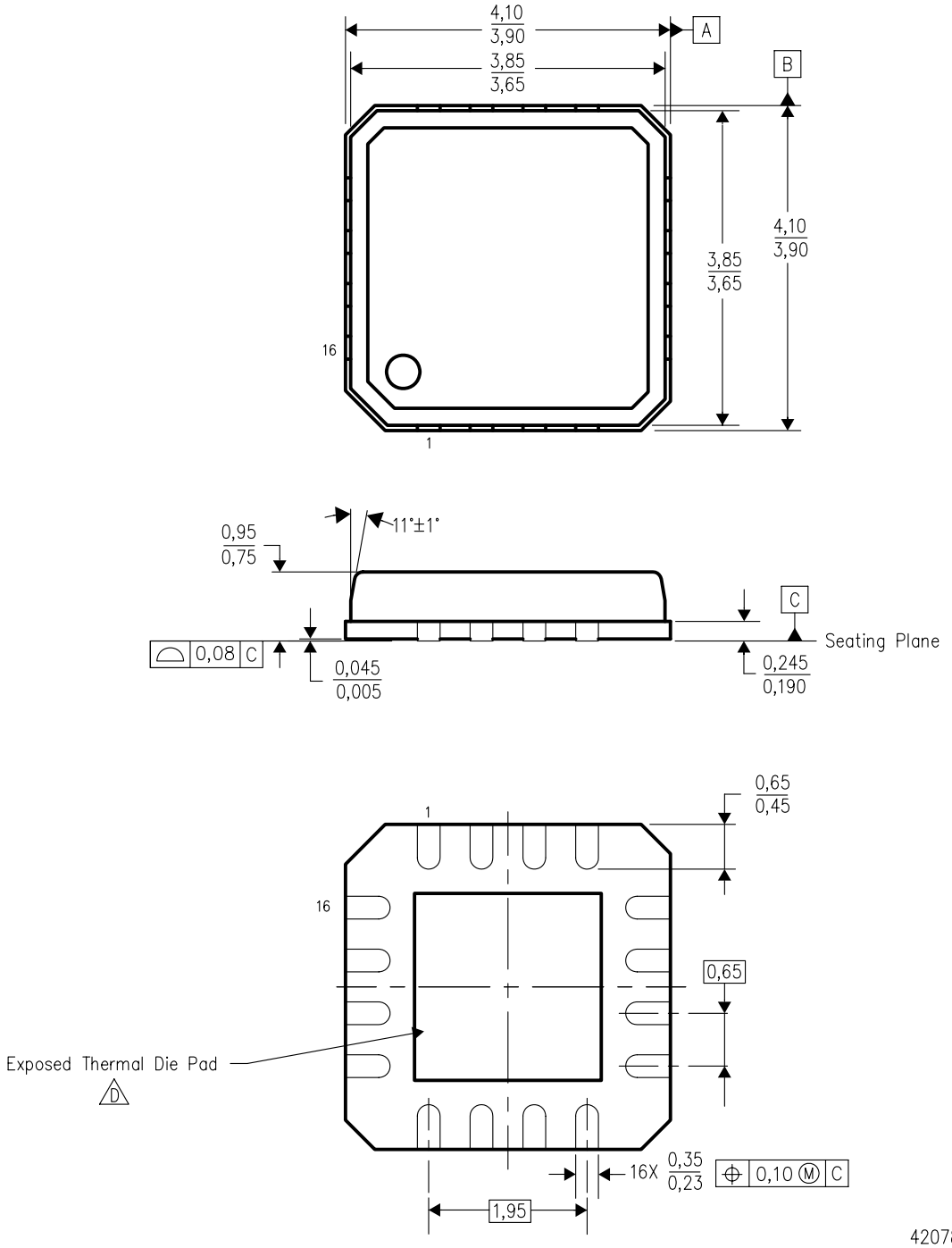
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1150RSTR	VQFN	RST	16	2500	338.1	338.1	20.6

RST (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

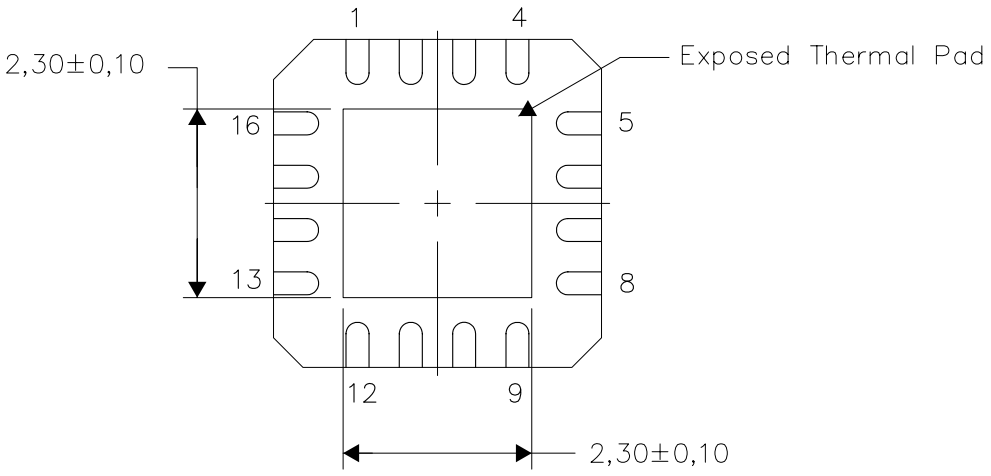
RST (S–PVQFN–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

NOTES:
All linear dimensions are in millimeters

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