

AFEDRI8201

SBWS017F − SEPTEMBER 2003 − REVISED AUGUST 2005

IF ADC Front End for AM/FM and HD Radios

FEATURES

- **Interfaces To Texas Instruments DRIx50 HD Radio Baseband Processors**
- **12-Bit, 80MSPS ADC Reduces Noise and Improves Sensitivity**
- **Typical SNR of 102dB in 3kHz Bandwidth**
- **Programmable Input Range For Optimum Tuner Dynamic Range**
- **Integrated Digital Downconverter (DDC)**
  - **Quadrature Mixer, NCO, CIC Decimation Filter, And FIR Filters**
- **Mixer: 32-Bit Frequency and Phase**
- **Decimation Ratio: 32 to 4096**
- **User-Programmable FIR Filters with 16-Bit Coefficients**
- **12-Bit Auxiliary DAC**
- **Code Composer Module for Easy Software Generation**
- **SPI™ Control Interface**

APPLICATIONS

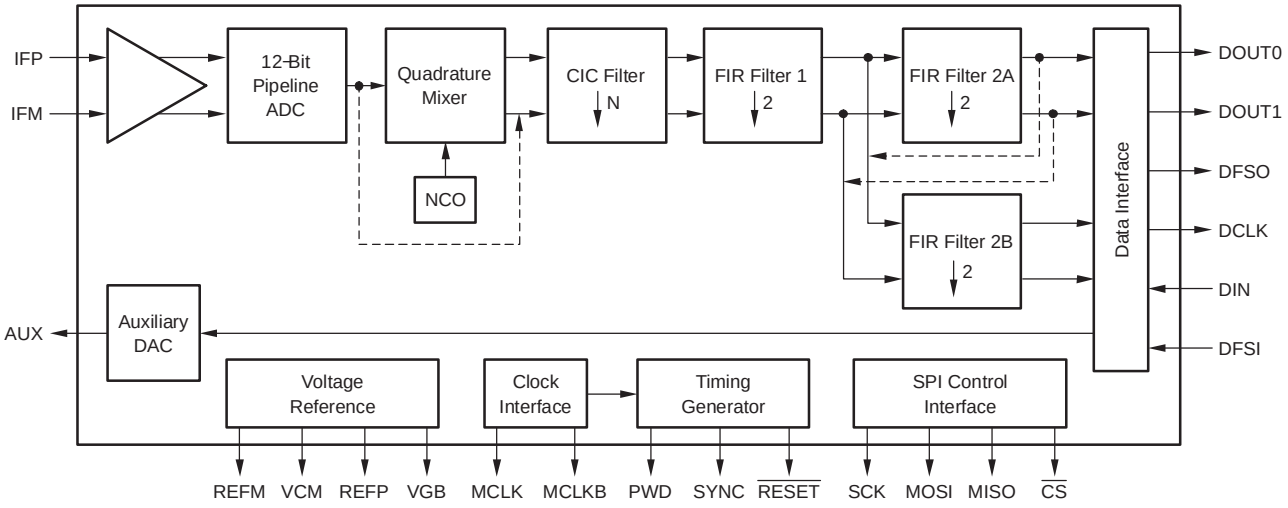
- **AM/FM and HD Radio Receivers**
- **IF Receive Channels**
- **Software Radios**
- **Narrowband Receivers**

DESCRIPTION

The AFEDRI8201 implements the receive channel analog functions required for intermediate-frequency (IF) sampled AM/FM and HD digital radio receivers. It is designed to be used with TI's DRIx50 digital baseband processor. The AFEDRI8201 is programmed by the DRIx50 for use in AM/FM and HD radio. The AFEDRI8201 oversamples the radio tuner IF output at speeds of up to 80MHz to reduce noise and improve dynamic range. The radio tuner output IF is typically 10.7MHz for AM or FM as well as 450kHz or 455kHz for AM, as desired. The AFEDRI8201 then mixes, filters, and decimates the signal to provide baseband I and Q output signals to the digital baseband processor. The AFEDRI8201 also includes a general-purpose 12-bit control digital-to-analog converter (DAC) to provide a gain control signal or other analog feedback to the tuner.

The DRIx50 digital baseband device writes control register data as well as decimation filter coefficients to the AFEDRI8201 through the industry-standard SPI control interface. The baseband output signals are transported to the DRIx50 through a general-purpose, high-speed serial interface (TI's Buffered Serial Ports, McBSP).

This unit uses 3.3V analog and 1.8V digital power supplies. Typical power dissipation is 490mW. The digital I/O lines can be powered by a 3.3V supply.



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ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFEDRI8201	TQFP-48	PFB	−40°C to +85°C	DRI8201	AFEDRI8201PFBT	Tape and Reel, 250
					AFEDRI8201PFBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		AFEDRI8201	UNIT
Supply Voltage Range	AVDD	−0.5 to 4.0	V
	DVDD	−0.5 to 2.3	V
	IOVDD	−0.5 to 3.6	V
Voltage between AGND and DGND		−0.3 to 0.5	V
Voltage between AVDD and DVDD		−3.3 to 3.3	V
Digital inputs(2)		−0.3 to DVDD + 0.3	V
Digital data output		−0.3 to DVDD + 0.3	V
Operating free-air temperature range, T_A		−40 to +85	°C
Storage temperature range		−55 to +125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Measured with respect to DGND.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supplies and References	Operating free-air temperature range, T_A	−40		+85	°C
	Analog supply voltage range, AVDD	3.15	3.3	3.45	V
	Digital supply voltage range, DVDD	1.71	1.8	1.89	V
	Output driver supply voltage range, IOVDD	3.15	3.3	3.45	V
	Input common-mode voltage		V_{CM}		V
	Differential input voltage		2		V_{PP}
Clock Inputs: MCLK and MCLKB	Sample rate, f_S	5		80	MHz
	Differential input mode voltage input swing	0.4		3.3	V
	Single-ended mode high-level input voltage, V_{IHC}	2			V
	Single-ended mode low-level input voltage, V_{ILC}			0.8	V
	Clock pulse width high, $t_{W(H)}$	5.625	6.25		ns
	Clock pulse width low, $t_{W(L)}$	5.625	6.25		ns

AUXILIARY DAC CHARACTERISTICS

All specifications at +25°C, AVDD = +3.3V, and DVDD = +1.8V, unless otherwise noted.

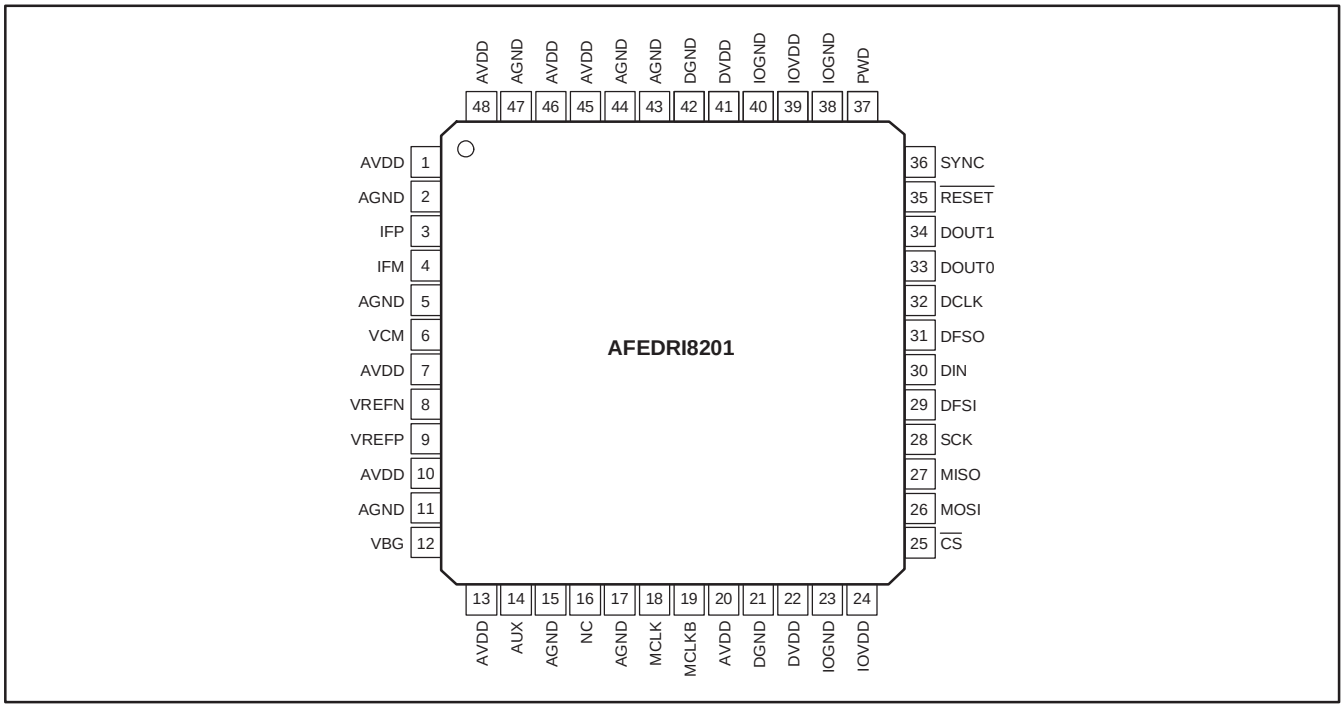
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		bits
Output voltage range		Input code 0x000		0.0		V
		Input code 0xFFF		2.75		V
Output impedance				1		kΩ
Settling time		to 0.1% FSR			10	µs
DC performance	Offset			±1		% of FSR
	Gain error			±5		% of FSR
	Differential nonlinearity, DNL	Ensured monotonic		±0.5		LSB
	Integral nonlinearity, INL	After correcting for gain and offset errors		±2		LSB
	Power-supply rejection ratio, PSRR	Input code 0x400, AVDD = 3.15VDC to 3.45VDC		60		dB

RECEIVE CHANNEL CHARACTERISTICS

All specifications at +25°C, f_S = 80MSPS, AVDD = +3.3V, DVDD = +1.8V, IOVDD = +3.3V, Gain = 1, Decimation Ratio = 80, Internal Digital Filter Bandwidth = 284kHz, and Input Signal = 10.7MHz, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy					
Input impedance			6.25		kΩ
Differential nonlinearity, DNL		−0.0244	±0.0122	+0.0244	%FSR
Integral nonlinearity, INL		−0.0244	±0.012	+0.0244	%FSR
Offset error			3		mV
Gain error			1		%FS
Full-scale input level (peak differential)	Gain = 1		1.0		V
	Gain = 1.14		0.875		V
	Gain = 1.33		0.75		V
	Gain = 1.6		0.625		V
	Gain = 2.0		0.5		V
	Gain = 2.67		0.375		V
	Gain = 4.0		0.25		V
Gain change settling time	Number of samples to achieve rated accuracy		2		Samples
Power-supply rejection ratio, PSRR	AVDD = 3.15VDC to 3.45VDC		70		dB
References					
Negative reference, VREFN		1.1	1.25	1.4	V
Positive reference, VREFP		2.1	2.25	2.4	V
Common-mode voltage, VCM			1.8		V
AC Performance					
Spurious-free dynamic range, SFDR	Input 455kHz, −1dBFS		76		dBc
	Input 10.7MHz, −1dBFS	76	86		dBc
Signal-to-noise ratio, SNR	Input 455kHz, −1dBFS		75		dB
	Input 10.7MHz, −1dBFS	70	74		dB
	In 3kHz bandwidth, −1dBFS, 10.7MHz, 20kHz from fundamental		102		dB
Aperture delay			2		ns
Aperture uncertainty			0.2		ps
Power Supply					
Analog supply voltage, AVDD		3.15	3.3	3.45	V
Digital supply voltage, DVDD		1.71	1.8	1.89	V
Output driver supply voltage, IOVDD		3.15	3.3	3.45	V
Power dissipation	Normal operation		490	570	mW
	Power-down		20		mW
Digital I/O supply current			7		mA
Digital supply current			72		mA
Analog supply current			103		mA

PIN ASSIGNMENTS



PIN DESCRIPTIONS

NAME	PIN	TYPE	FUNCTION
IFP	3	Input	Positive IF input
IFM	4	Input	Negative IF input
VCM	6	Output	Common-mode voltage output
VREFN	8	Output	Negative reference voltage output
VREFP	9	Output	Positive reference Voltage output
VBG	12	Output	Bandgap voltage output
AUX	14	Output	Auxiliary DAC output
MCLK	18	Input	Master clock input
MCLKB	19	Input	Complementary master clock input
$\overline{CS}$	25	Input	SPI chip select (active low)
MOSI	26	Input	SPI serial Input
MISO	27	Output	SPI serial output
SCK	28	Input	SPI serial clock
DFSI	29	Input	Data interface input frame sync
DIN	30	Input	Data interface input data
DFSO	31	Output	Data interface output frame sync
DCLK	32	Output	Data interface clock output
DOUT0	33	Output	Data interface filter 0 output data
DOUT1	34	Output	Data interface filter 1 output data
$\overline{RESET}$	35	Input	Global reset (active low). Resets all registers to zero, except for FIR filters.
SYNC	36	Input	External sync
PWD	37	Input	Power-down: PWD = 1; normal operation: PWD = 0
AVDD	1, 7, 10, 13, 20, 45, 46, 48	Supply	Analog supply (3.3V)
AGND	2, 5, 11, 15, 17, 43, 44, 47	Ground	Analog ground
DVDD	22, 41	Supply	Digital supply (1.5V to 1.8V)
DGND	21, 42	Ground	Digital ground
IOVDD	24, 39	Supply	Digital I/O supply (3.3V)
IOGND	23, 38, 40	Ground	Digital I/O ground
NC	16	—	Not connected

DIGITAL INTERFACE SPECIFICATIONS

All specifications at +25°C, AVDD = 3.3V, DVDD = 1.8V, IOVDD = 3.3V, and maximum 20pF load, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-level input current, I_{IH}	V_{IH} = 1.6V to 3.6V	−10		10	µA
Low-level input current, I_{IL}	V_{IL} = 0V to 0.4V	−10		10	µA
High-level output voltage, V_{OH}	I_{OH} = −50µA	0.8 × IOVDD			V
Low-level output voltage, V_{OL}	I_{OL} = 50µA			0.2 × IOVDD	V
High-level input voltage, V_{IH}		0.7 × IOVDD			V
Low-level input voltage, V_{IL}				0.25 × IOVDD	V

DATA INTERFACE TIMING

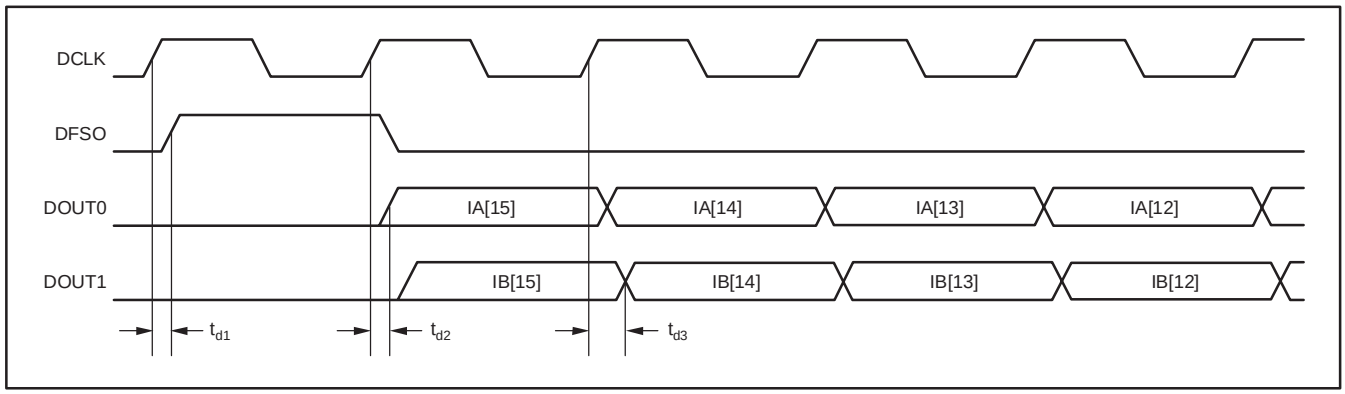


Figure 1. Output Data Interface TIming

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DCLK to DFSO delay, t_{d1}		−0.4		3.2	ns
DCLK to DOUT0 delay, t_{d2}		−0.2		2.5	ns
DCLK to DOUT1 delay, t_{d3}		−0.2		2.5	ns

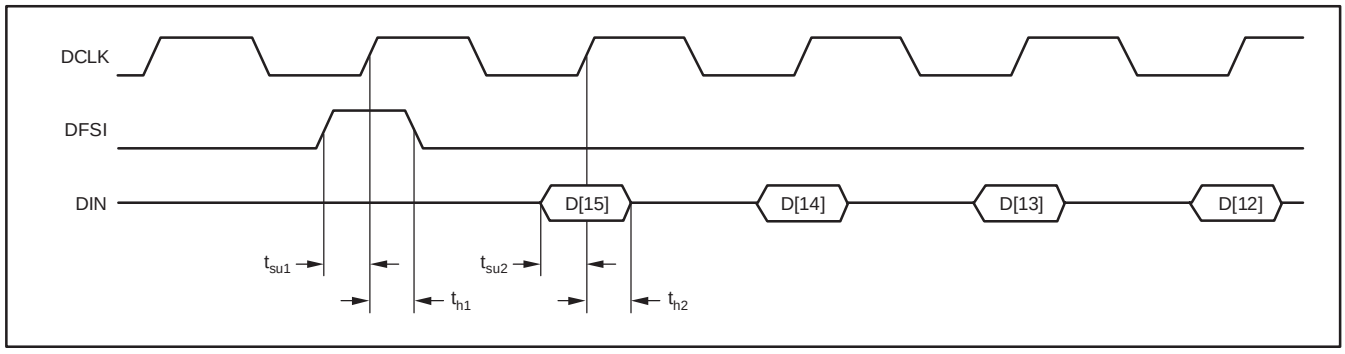


Figure 2. Input Data Interface TIming

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DFSI to DCLK setup time, t_{su1}		1.2			ns
DFSI to DCLK hold time, t_{h1}		0.4			ns
DIN to DCLK setup time, t_{su2}		1.0			ns
DIN to DCLK hold time, t_{h2}		0.4			ns

CONTROL INTERFACE TIMING

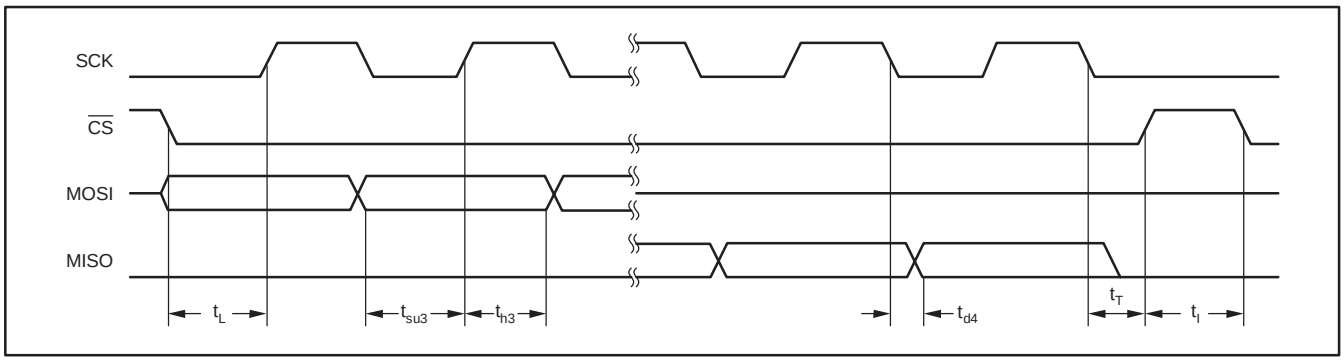


Figure 3. Control Interface Timing

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum SCK frequency				1	MHz
$\overline{CS}$ leading time, t_L	Trailing $\overline{CS}$ to leading SCK	5.0			ns
$\overline{CS}$ trailing time, t_T	Trailing SCK to leading $\overline{CS}$	5.0			ns
$\overline{CS}$ idle time, t_I	Leading $\overline{CS}$ to trailing $\overline{CS}$	5.0			ns
MOSI to SCK setup time, t_{su3}		5.0			ns
MOSI to SCK hold time, t_{h3}		1.0			ns
SCK to MISO delay time, t_{d4}		1.0		8	ns

DETAILED DESCRIPTION

The AFEDRI8201 consists of a general-purpose, 80MSPS, 12-bit analog-to-digital converter (ADC) with programmable input range, digital downconverter (DDC), and user programmable digital filters with 16-bit coefficients. It is designed to sample narrowband (up to 2.5MHz) IF signals and digitally mix, filter, and decimate the signals to baseband. The ADC integrates a programmable gain sample-and-hold amplifier that is variable over gains of 1x to 4x to change the full-scale input voltage range of the device from 1.0V peak to 0.25V peak. When the gain is changed, two sample periods may be needed for the output of the ADC to settle to the correct value.

The DDC consists of a digital quadrature mixer followed by a CIC decimation filter and FIR filters (FIR1 and FIR2). The mixer frequency and initial phase are independently programmed by 32-bit control words. The quadrature mixer generates I and Q signals, each of which are decimated by the CIC filter. The CIC is a 5th-order Comb filter with a decimation factor that is programmable over a range of 8 to 1024. Each of the FIR filters adds an additional decimation factor of 2, for a total range of 32 to 4096.

The I and Q signals generated by the quadrature mixer are then passed on to the first FIR filter (FIR1). This decimate-by-two FIR filter can implement even, odd, halfband, and arbitrary impulse responses. The length of the filter response is dependent on the decimation factor of the CIC filter and the FIR filter response type, up to a maximum of 62 taps. Coefficients for multiple filter responses may be stored in the coefficient memory (up to 64 unique coefficients may be stored); responses can be changed by changing a control register to point the filter to a different section of coefficient memory.

Following FIR1 are two parallel decimate-by-two FIR filters (FIR2A and FIR2B). These filters are similar to FIR1, but have twice the data and coefficient memory and can therefore realize longer filter responses. The responses of the FIR2A and FIR2B can be different from each other (with some limitations). In addition, FIR2A and FIR2B can be optionally interleaved to form a single extra-long FIR filter that can realize up to 251 taps.

Control register information, as well as decimation filter coefficients, are written to the AFEDRI8201 through the industry-standard SPI control interface. The baseband output signals are transported through a high-speed serial interface that is compatible with the TI C5x/C6x DSP buffered serial ports (McBSP).

The AFEDRI8201 also contains a 12-bit auxiliary digital-to-analog converter (DAC) which can be used for a number of purposes, including tuner automatic gain control or frequency control. Input data for the DAC may be sent either from the DSP through the serial data port or from a microcontroller through the SPI control interface.

CONTROL INTERFACE

The AFEDRI8201 uses an SPI slave interface to read and write control data. Control data consists of eleven 16-bit control registers, as shown in Table 1, and three memory banks (see Table 2). The control registers are used to program all chip parameters. The memory banks store 16-bit FIR filter coefficient data.

To read and write to control registers and memory banks, data is transferred by a 16-bit instruction followed by 16 bits of data. Memory bank read and write operations also support block transfer. Memory bank block transfer consists of a 16-bit instruction followed by multiple 16-bit data words.

Table 1. Control Registers

REGISTER ADDRESS	DESCRIPTION
0	Data interface parameters DIV, MODE
1	NCO frequency (bits 0−15)
2	NCO frequency (bits 16−31)
3	NCO Initial Phase (bits 0−15)
4	NCO Initial Phase (bits 16−31)
5	CIC Filter Decimation Rate: DEC_RATE
6	CIC Filter Parameters: SCALE, SHIFT
7	First FIR Filter Parameters: BASE_ADDR, NCOEFF, MODE
8	Second FIR A Filter Parameters: BASE_ADDR, NCOEFF, MODE
9	Second FIR B Filter Parameters: BASE_ADDR, NCOEFF, MODE
10	Setup for the Second FIR
11	Auxiliary DAC: DAC_DATA
12	ADC Parameters: GAIN, PWD

Table 2. Memory Banks

MEMORY BANK ADDRESS	DESCRIPTION	SIZE	DATA MEMORY
00	FIR Filter 1 Coefficients	64 Coefficients	62 Samples
01	FIR Filter 2A Coefficients	128 Coefficients	126 Samples
10	FIR Filter 2B Coefficients	128 Coefficients	126 Samples

The SPI interface consists of four signals: a serial clock (SCK), an active-low chip select ($\overline{CS}$), a serial data input (MOSI—Master Out, Slave In), and a serial data output (MISO—Master In, Slave Out). Data is transferred in groups of 32 bits. The first 16 bits are the instruction, which indicate:

(1) if data is to be written or to be read;

(2) if the data target is a control register or a memory bank; and

(3) the address of the data target.

The second 16 bits are the data transfer, which is input on MOSI for a write cycle or output on MISO for a read cycle.

A single data word write cycle is shown in Figure 4. The cycle is initiated by the high-to-low transition of the $\overline{CS}$ line. 32 SCK pulses clock the instruction and the data into the MOSI line. Instructions and data are clocked in MSB first. The first 16 bits are the instruction; the second 16 bits are the data word. There are two possible single data word write cycle instructions: register write and memory write. The formats for these instructions are shown in Figure 5 and Figure 6.

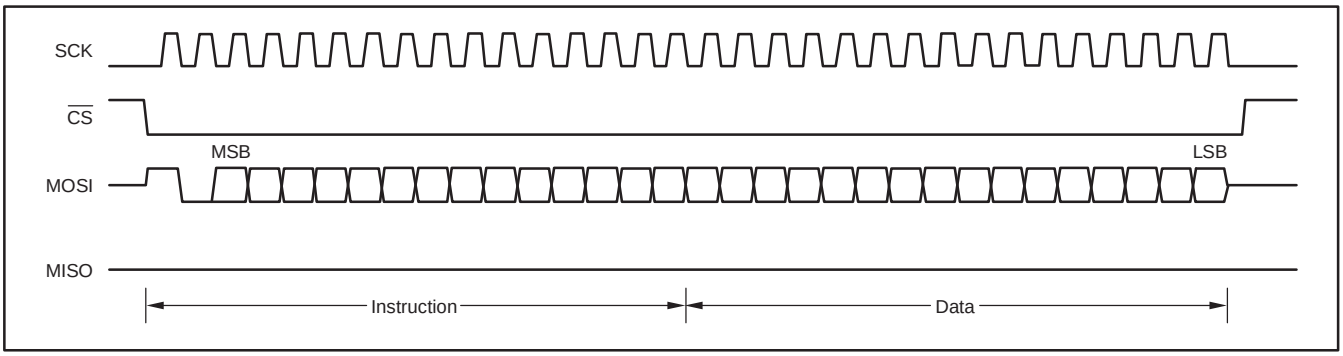


Figure 4. Single Data Word Control Interface Write Cycle for Registers or Memory

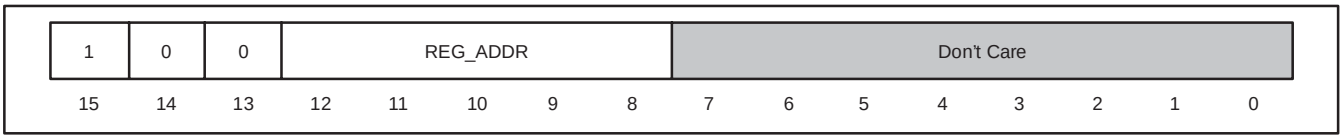


Figure 5. Register Write Instruction Format

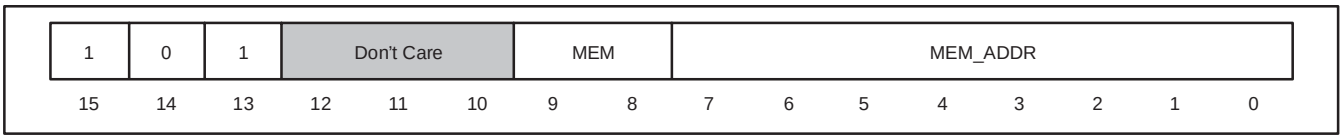


Figure 6. Memory Write Instruction Format

In case $\overline{RESET}$ is applied, either wait at least three SCK clocks before applying $\overline{CS}$, or execute a dummy read operation (either from a register or memory) in order to initialize the SPI interface correctly. The only information required for a register write is the 5-bit register address (REG_ADDR). For a memory write, the 2-bit memory select (MEM) and the 8-bit memory address (MEM_ADDR) are required (see Table 2).

Following the 16-bit instruction, the 16-bit data word is clocked in, again MSB first. At the end of the write cycle this data word is written to the appropriate register or memory location in the AFE.

The read cycle is illustrated in Figure 7. It is similar to the write cycle, except that instead of the data word being clocked into MOSI during the second half of the cycle, the data word is clocked out of MISO. The two data read instructions are similar to the corresponding data write instructions and are shown in Figure 8 and Figure 9.

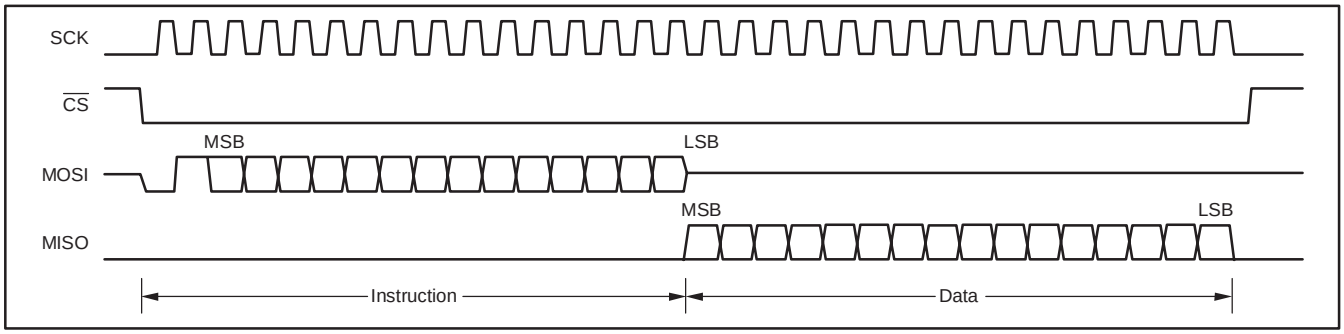


Figure 7. Single Data Word Control Interface Read Cycle for Registers or Memory

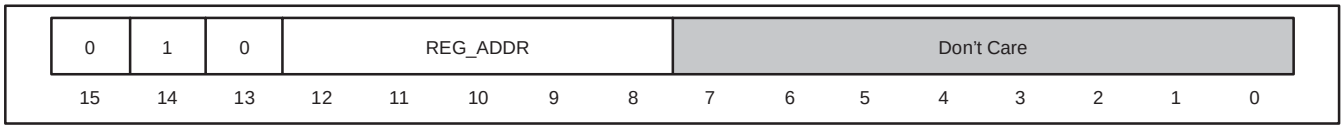


Figure 8. Register Read Instruction Format

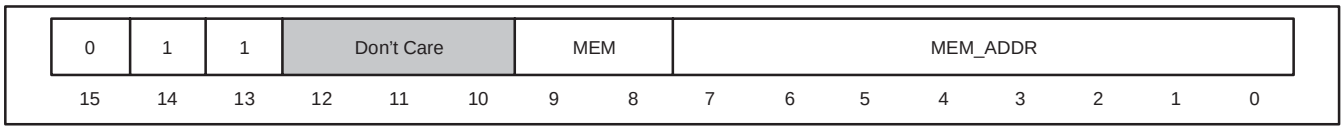


Figure 9. Memory Read Instruction Format

Block transfers are supported for memory reading and writing. Multiple data words are transmitted following the memory read or write instruction for a block transfer. The data words are sequentially read from or written to RAM sequentially starting at the address contained in the instruction. The sequential RAM access terminates when the $\overline{CS}$ line goes high. Figure 10 shows a memory block read cycle. In the illustration, three successive memory locations are read starting at address N. The memory block write cycle is similar, except of course data is clocked into MOSI.

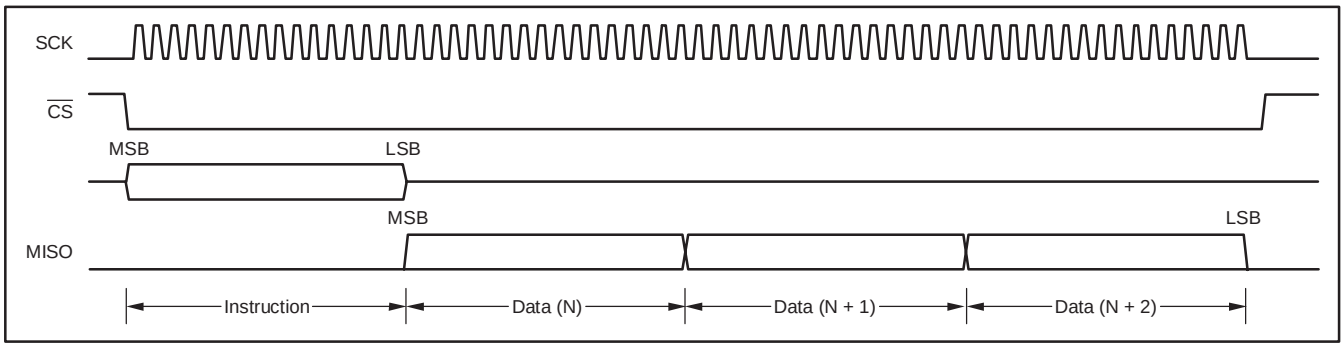


Figure 10. Block Memory Read Cycle Control Interface

In all cases, the control interface is reset when $\overline{CS}$ goes high. If the final SCK is not received before $\overline{CS}$ goes high, then the cycle will end prematurely. For a read cycle, transfer of data will terminate; for a write cycle, no data will be written to register or memory.

DATA INTERFACE

The data interface consists of six signals:

1. serial data clock DCLKO;
2. output frame sync DFSO;
3. output data line DOUT0;
4. output data line DOUT1;
5. input frame sync DFSI; and
6. input data line DIN.

The decimation filter outputs from the DDC (either IA and QA, or IA, QA, IB, and QB) are multiplexed onto the data outputs. The control DAC data is shifted into the data input. Control Register 0 programs the functionality of the data interface, as seen in Figure 11.

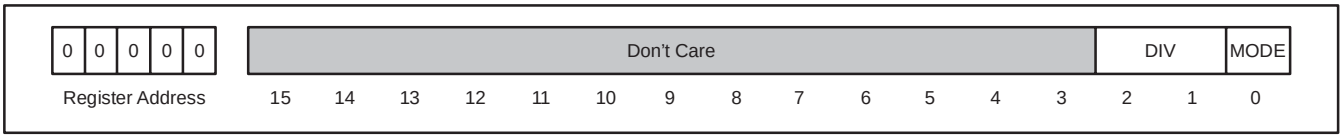


Figure 11. Data Interface Control Register

Two parameters, DIV and MODE, control the data interface and are programmed by register 0. The first parameter is DIV. The serial data clock, DCLKO, is derived from MCLK in a manner controlled by DIV such that the frequency of DCLKO is:

$$f_{DCLKO} = \frac{f_{MCLK}}{2^{DIV}} \quad (1)$$

where DIV ranges from 0 to 3.

As an example, if MCLK is 80MHz, DCLK0 can be either 80MHz, 40MHz, 20MHz, or 10MHz. DCLK0, of course, must be fast enough to clock out the I and Q data words generated by the on-chip DDC and filters.

The second parameter is MODE. When MODE is 0, all four DDC outputs are time multiplexed onto DOUT0, as shown in Figure 12. When MODE is 1, IA and QA outputs are multiplexed onto DOUT0 while IB and QB outputs are multiplexed onto DOUT1, see Figure 13. If only one set of I/Q outputs is used, MODE 1 is recommended so that data is output through DOUT0.

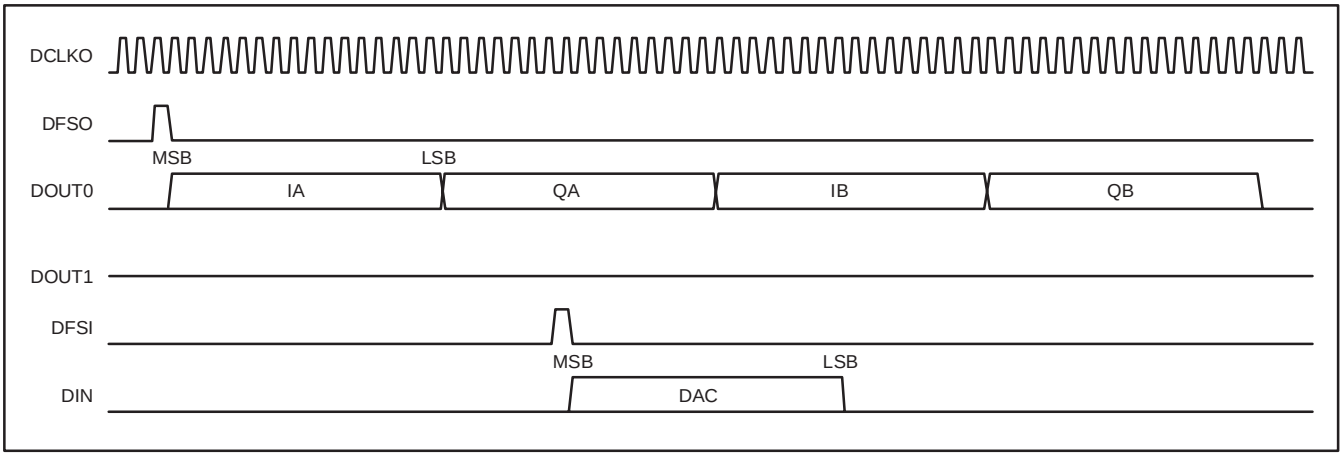


Figure 12. Data Interface Timing for MODE = 0

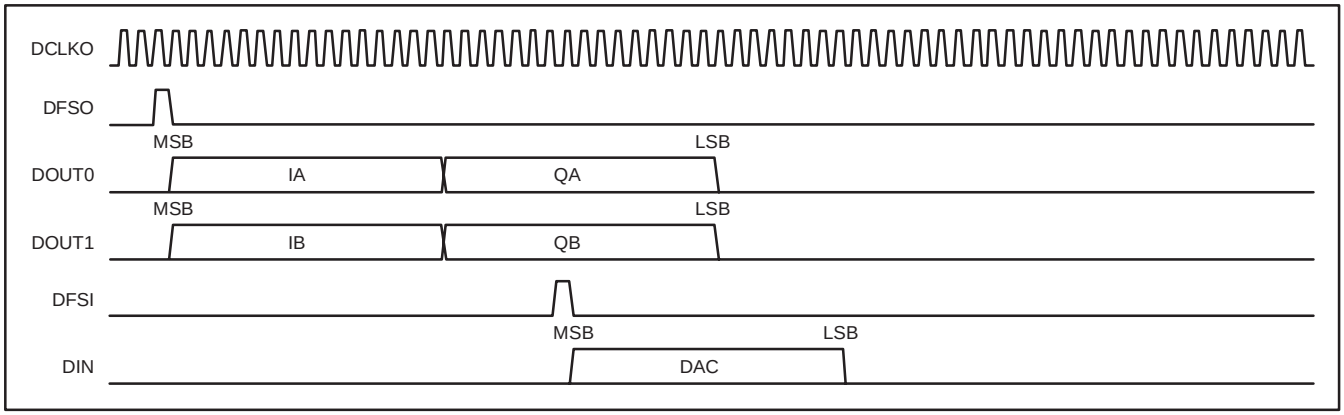


Figure 13. Data Interface Timing for MODE = 1

When the data interface receives new outputs from the decimation filters, an output cycle is started by asserting DFSO for one DCLKO period. On successive leading edges of DCLKO, the filter output data is shifted out MSB first on DOUT0 (and DOUT1 for MODE = 1), as shown in the timing diagrams. The spacing of the DFSO pulses depends on two settings: the overall decimation ratio R of the DDC and the factor DIV. The number of bits which need to be transmitted in one frame, NBITS, is 64 for MODE = 0 and 32 for MODE = 1. In order to have enough DCLKO cycles between DFSO pulses, the following relationship must be true:

$$\frac{R}{2^{DIV}} \geq NBITS \tag{2}$$

or

$$DIV \leq \log_2\left(\frac{R}{NBITS}\right) \tag{3}$$

For example, assume the overall decimation ratio, R, for the DDC is 80. For MODE = 0, the largest allowable value for DIV is 0. In other words, if MCLK is 80MHz, for R = 80, DCLKO must be 80MHz so that all of the 64 data bits may be clocked out before the next I and Q data words must be clocked out.

For MODE = 1, since only 32 bits need to be clocked out during one cycle, DCLKO can be reduced to 40MHz (which means that DIV may be increased to 1, cutting the frequency of DCLKO in half).

DFSI and DIN are used to send control DAC data to the AFEDRI8201. DCLKO supplied by the AFEDRI8201 is used as the serial clock. An input cycle is initiated by holding DFSI high through one rising edge of DCLKO. On the successive 16 leading edges of DCLKO the input data word is read in serially, MSB first. The lower 12 bits of the data word are sent to the DAC as the unsigned DAC input.

Note that the input data does not need to bear any timing relationship to the output data, except that both data streams are synchronous with DCLKO.

QUADRATURE MIXER/NCO

The NCO frequency and initial phase are set by the 32-bit unsigned variables FREQ and PHASE. Each of these variables is set via a pair of control registers; see Figure 14. The I and Q outputs of the mixer are given by:

$$I = ADC \times \sin(2\pi ft + \phi) \tag{4}$$

and

$$Q = ADC \times \cos(2\pi ft + \phi) \tag{5}$$

where ADC is the output of the IF analog-to-digital converter, f is the NCO frequency given by:

$$f = f_{MCLK}\frac{FREQ}{2^{32}} \tag{6}$$

and ϕ is the NCO phase offset (in radians) given by:

$$\phi = 2\pi\frac{PHASE}{2^{32}} \tag{7}$$

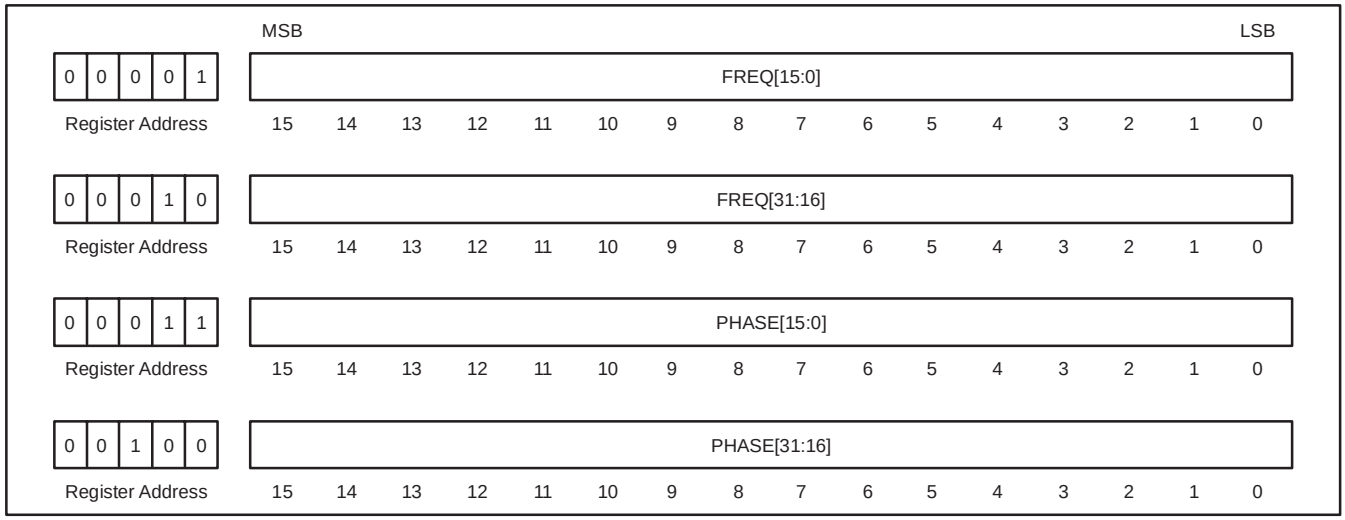


Figure 14. Mixer Control Registers

The SYNC pin can be used to externally control the phase of the mixer. While the SYNC pin is high, the phase accumulator is held to a constant value PHASE, essentially holding t to zero in the I and Q equations. When the SYNC pin is brought low, the phase accumulator is incremented by the value FREQ once per MCLK cycle.

Note that the mixer can be bypassed by setting FREQ and PHASE to 0 and using only the Q (real) output.

CIC FILTER

The first stage of decimation filtering is provided by a 5th-order CIC filter. The operation of the CIC filter is controlled by the unsigned variable DEC_RATE, SCALE, and SHIFT which are mapped into control registers as illustrated in Figure 15. The valid range for DEC_RATE is from 8 to 1024.

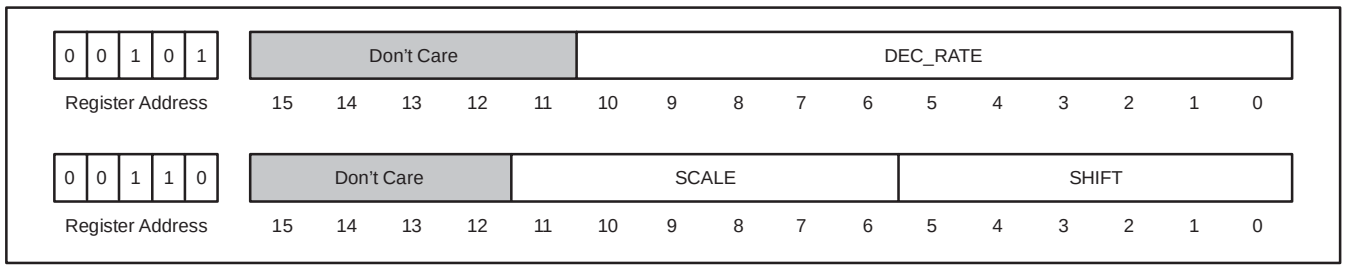


Figure 15. CIC Filter Control Registers

The inherent dc gain of the CIC filter is DEC_RATE^5. The control variables SHIFT and SCALE are used to reduce this very high gain before the signal is output to the next stage of decimation filter. The combined effect of DEC_RATE, SHIFT, and SCALE produces an overall dc gain for the CIC filter of:

$$Gain = DEC_RATE^5 \left(\frac{Scale/32}{2^{shift}} \right) \quad (8)$$

In general, SHIFT and SCALE should be chosen to make GAIN as close to 1 as possible. For example, if DEC_RATE is 20, setting SHIFT to 22 and scale to 41 will result in a GAIN of 0.9775.

FIRST FIR FILTER

The block following the CIC filter is a decimate-by-two FIR filter with programmable coefficients. MODE sets the type of filter response—ODD (MODE = 00: symmetric impulse response, odd number of taps), EVEN (MODE = 01: symmetric impulse response, even number of taps), HALFBAND (MODE = 10), and ARBITRARY (MODE = 11: non-symmetric impulse response).

The 16-bit wide filter coefficients are stored in memory bank 0. Up to 64 coefficients can be stored in this memory. Depending on the types of filters desired and the number of taps, coefficients for multiple filter responses may be stored in the memory bank. The filter response may be changed simply by updating the control register with new values for MODE, NCOEFF, and BASE_ADDR, as shown in Figure 16.

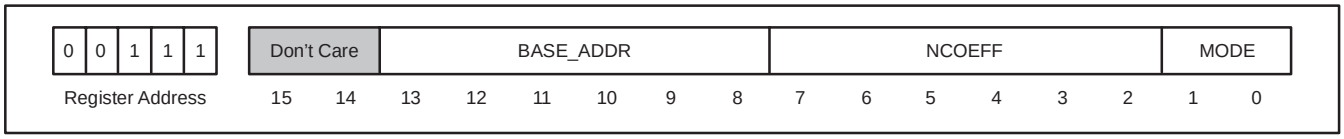


Figure 16. First FIR Filter Control Register

NCOEFF defines the number of unique filter coefficients which make up the filter response. BASE_ADDR defines the memory location where the first filter coefficient is stored. The actual filter length is a function of MODE and NCOEFF:

Filter length = 2(NCOEFF − 1) + 1 for ODD

Filter length = 2NCOEFF for EVEN

Filter length = 4(NCOEFF − 1) + 1 for HALFBAND

Filter length = NCOEFF for ARBITRARY

The maximum filter length which can be realized is limited by two factors. First, the number of clock cycles between successive filter outputs limits the number of coefficients which can be processed to:

$$NCOEFF \leq 2 \times DEC_RATE - 4 \quad (9)$$

where DEC_RATE is the decimation ration of the CIC filter. Second, the size of the data memory (which stores incoming data samples) limits filter length to 62 taps.

A filter response is defined by a set of NCOEFF 16-bit filter coefficients stored in memory bank 0 (MEM = 0) starting at address BASE_ADDR. MODE determines how the coefficients are applied to the samples stored in data memory.

Figure 17 is an example illustrating how the filter coefficients are applied to stored input samples in the various filter modes with NCOEFF = 6. Because NCOEFF = 6 in this example, six computation cycles are required to calculate the filter output regardless of the filter mode. The leftmost grouping in Figure 17 represents the six filter coefficients stored at ascending memory address in the coefficient memory starting at BASE_ADDR. At each computation cycle, the coefficient being applied to the input data is highlighted.

The leftmost grouping in Figure 17 represents the six filter coefficients stored at ascending memory address in the coefficient memory starting at BASE_ADDR. At each computation cycle, the coefficient being applied to the input data is highlighted.

The four groupings on the right in Figure 17 represent the four filter modes: EVEN, ODD, HALFBAND, and ARBITRARY. In each column, the locations in data memory that are operated on at each computation cycle is shown. The leftmost data sample in each group is the newest sample, the rightmost sample is the oldest. The chart illustrates the order in which computation on data occurs. To use the chart, select the filter mode of interest, then move down the chart through the six computation cycles to understand the sequence of calculations.

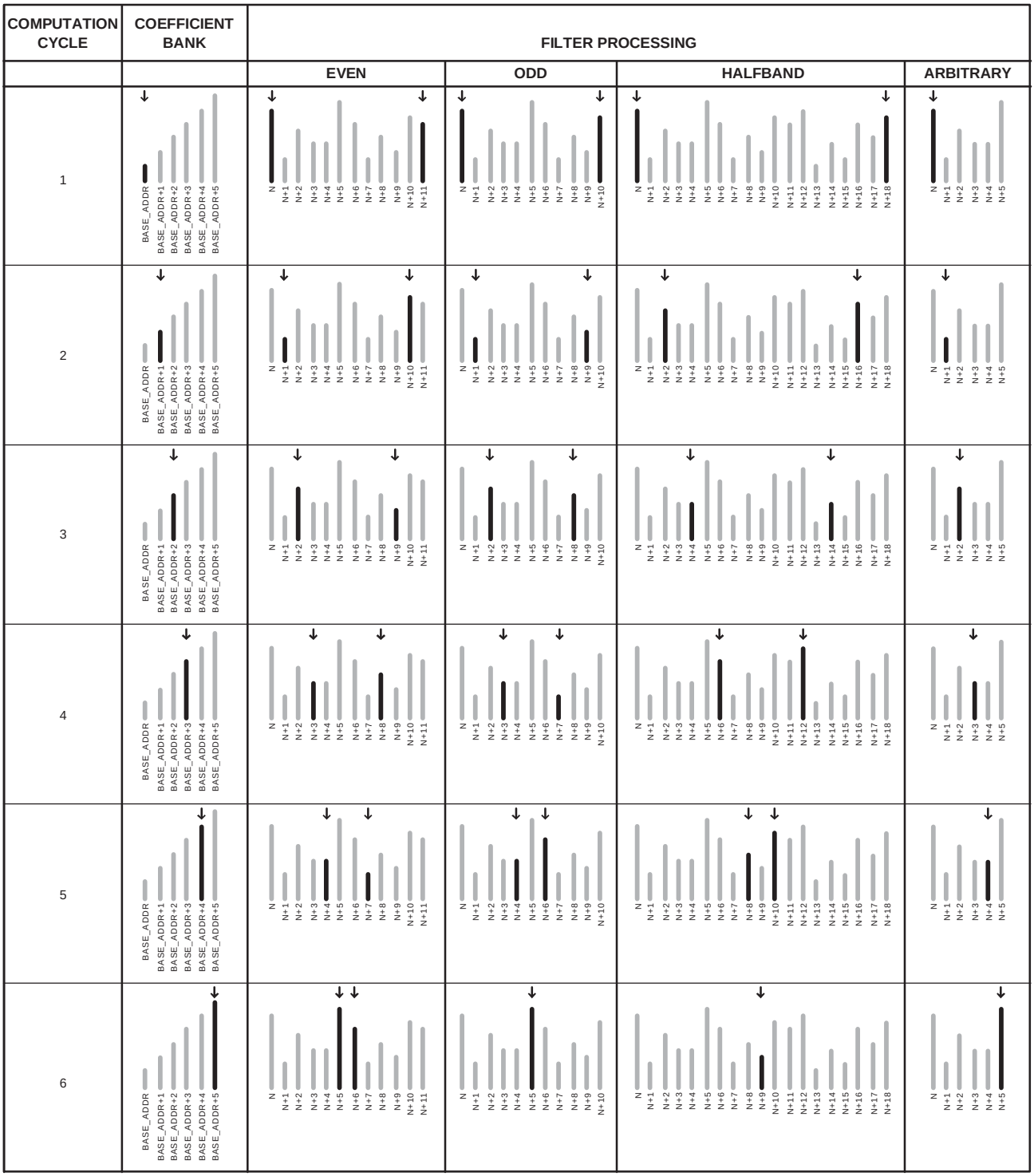


Figure 17. Application of Filter Coefficients in Different Filter Modes

For example, using the ODD mode in the first cycle of MCLK, the filter coefficient at BASE_ADDR is applied to two values in data memory, the most recent at address N and the oldest at address N+10. In the next cycle of MCLK the coefficient at BASE_ADDR+1 is applied to the data values at N+1 and N+9, and so on until the last coefficient at BASE_ADDR+5 is reached. Because this is an odd filter, the final coefficient is applied only to the data value at address N+5. The full cycle is shown in Table 3.

Table 3. ODD Mode Calculation Example with Six Filter Coefficients

CYCLE	FILTER COEFFICIENT ADDRESS	APPLIED TO DATA ADDRESS
1	BASE_ADDR	N and N+10
2	BASE_ADDR+1	N+1 and N+9
3	BASE_ADDR+2	N+2 and N+8
4	BASE_ADDR+3	N+3 and N+7
5	BASE_ADDR+4	N+4 and N+6
6	BASE_ADDR+5	N+5

Figure 17 clearly illustrates that the overall filter length is different in different filter modes even if NCOEFF is unchanged. For NCOEFF = 6, filter length ranges from 6 taps for ARBITRARY mode to 19 taps for HALFBAND mode.

The dc gain of the FIR filter depends on the coefficient values and the filter mode.

For ODD mode and for HALFBAND mode, the dc gain is given by:

$$\text{GAIN} = \left(h_{\text{NCOEFF}} + \sum_{n=1}^{\text{NCOEFF}-1} 2h_n \right) / \left(2^{15} - 1\right) \tag{10}$$

where h_n is the *nth* of NCOEFF filter coefficients stored in memory.

For EVEN mode the dc gain is:

$$\text{GAIN} = \left(\sum_{n=1}^{\text{NCOEFF}} 2h_n \right) / \left(2^{15} - 1\right) \tag{11}$$

while for ARBITRARY mode the gain is:

$$\text{GAIN} = \left(\sum_{n=1}^{\text{NCOEFF}} h_n \right) / \left(2^{15} - 1\right) \tag{12}$$

SECOND FIR FILTER

The second FIR filter, shown in Figure 18, is similar to the first FIR filter with four notable exceptions.

1. The depth of the coefficient and data memories are doubled to 128. This allows for filters up to 126 taps to be realized without running out of data memory. It also allows longer sets of filter coefficients to be stored in coefficient memory. Note that BASE_ADDR and NCOEFF are each one bit wider in the control register.
2. Because of the additional decimation by two from the first FIR filter, twice as many MCLK cycles are available to process coefficients, increasing the maximum allowable value of NCOEFF to:

$$NCOEFF \leq 4 \times DEC_RATE - 4 \quad (13)$$

3. In the first FIR filter, the total of all the filter tap weights must add up to $2^{15} - 1$ in order to achieve unity gain through the filter. With longer filters (and thus smaller coefficients), frequency response errors may be introduced because of coefficient truncation. A shift parameter has been added to the second FIR filter to alleviate this problem. The total of all filter tap weights must add up to $2^{15+SHIFT} - 1$ to achieve unity gain through FIR2A or FIR2B. Note that shift values for FIR2A and FIR2B can be set separately.
4. A second coefficient memory and computational unit is added to allow the simultaneous implementation of two filters with differing responses acting on the same input data stream. Coefficients for filter A are stored in memory bank 1 (MEM = 1) and coefficients for filter B are stored in memory bank 2 (MEM = 2).

Note that while the coefficient values for filter A and filter B can be different, the two filters share the same values for MODE, NCOEFF, and BASE_ADDR.

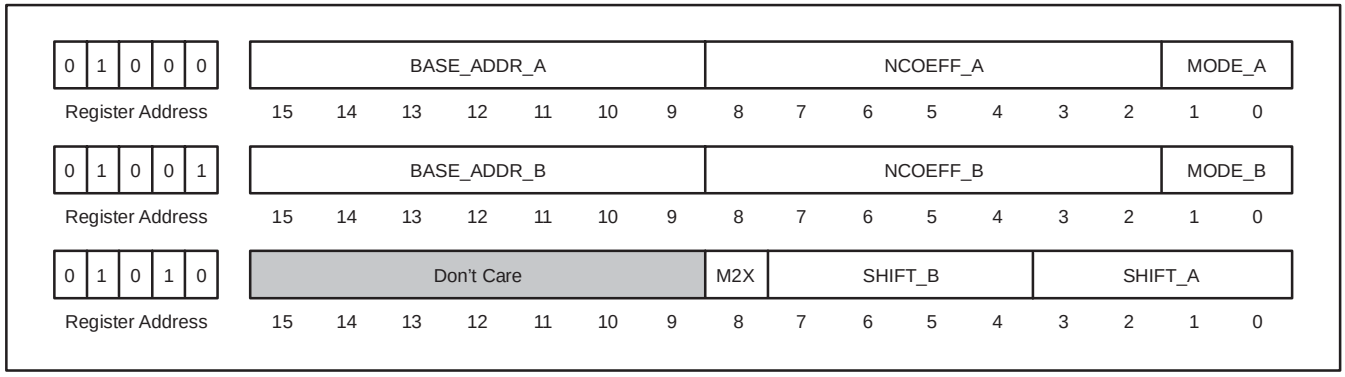


Figure 18. Second FIR Filter Control Register

EXTENDED-LENGTH FILTER MODE

If FIR2A or FIR2B cannot provide enough filter taps to achieve the desired frequency response, setting control bit M2X to '1' will put the two filters into an interleaved mode, which will double the length of filter which can be realized. The limitations are:

1. only odd symmetrical filters may be realized;
2. the filter length M must be such that (M + 1)/4 is an integer; and
3. only one filter can be realized (in M2X mode the A and B outputs are identical: IB = IA and QB = QA).

In addition to setting the M2X bit to '1', FIR2A must be set to EVEN mode and FIR2B must be set to ODD mode. NCOEFF_A and NCOEFF_B are both set to (M+1)/4. SHIFT_A and SHIFT_B should be identical. There are no restrictions on BASE_ADDR_A or BASE_ADDR_B.

The M-tap filter will have (M+1)/2 unique coefficients. The first, third, fifth, etc. coefficients are loaded into the FIR2A coefficient memory; the second, fourth, sixth, etc. are loaded into the FIR2B memory. The center coefficient of the filter will end up as the last coefficient loaded into FIR2B.

AUXILIARY DAC

In normal operation the auxiliary DAC values are sent over the data interface through input pin DIN and framed by DFSI. The auxiliary DAC control register, shown in Figure 19, allows the DAC value to be set through the control interface as an alternative. A new DAC value through either interface will cause the DAC output to change, regardless of which interface set the previous DAC value. Please note, however, that unpredictable results will occur if both interfaces write to the DAC at the same time.

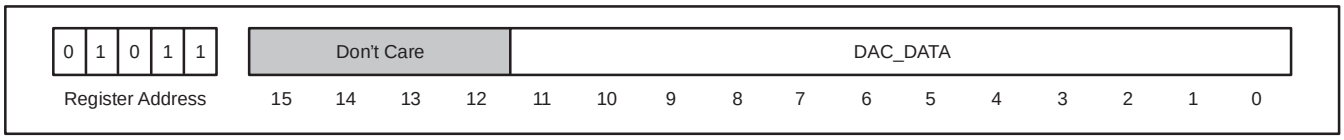


Figure 19. Auxiliary DAC Control Register

PGA AND POWER-DOWN

The gain of PGA and the power-down mode can be set in register 12. The gain setting of the PGA is shown in Table 4.

Table 4. PGA Gain Setting

PGA GAIN RANGE	3-BIT CODE (B4, B3, AND B2)
1.00	000
1.14	100
1.33	010
1.60	110
2.00	001
2.67	101
4.00	011

Bit 0

PWD = 0 for normal operation.

PWD = 1 for power-down.

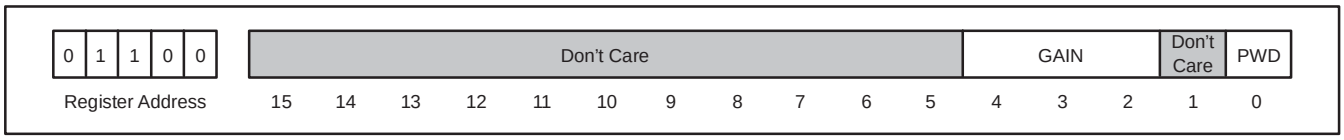


Figure 20. PGA and PWD Register

AFEDRI8201 Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/25/05	F	6	Control Interface Timing	Changed *Maximum SCK Frequency* from 10MHz to 1MHz.
		8	Control Interface	Changed “16 bit” to “16-bit” (added hyphen) in last sentence of 2nd paragraph.
				Changed “16 bits is” to “16 bits are” in last paragraph.
		9		Changed 1st sentence of 4th paragraph to include additional info on initializing the SPI interface correctly.
		13	Quadrature Mixer/NCO	Changed “mixer” to “the mixer” in 1st sentence of 1st paragraph.
		16	Control Interface	Changed “mode” to “modes” in 1st sentence of 2nd paragraph.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
AFEDRI8201PFBR	NRND	TQFP	PFB	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Call Local Sales Office
AFEDRI8201PFBRG4	NRND	TQFP	PFB	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Call Local Sales Office
AFEDRI8201PFBT	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Call Local Sales Office
AFEDRI8201PFBTG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Call Local Sales Office

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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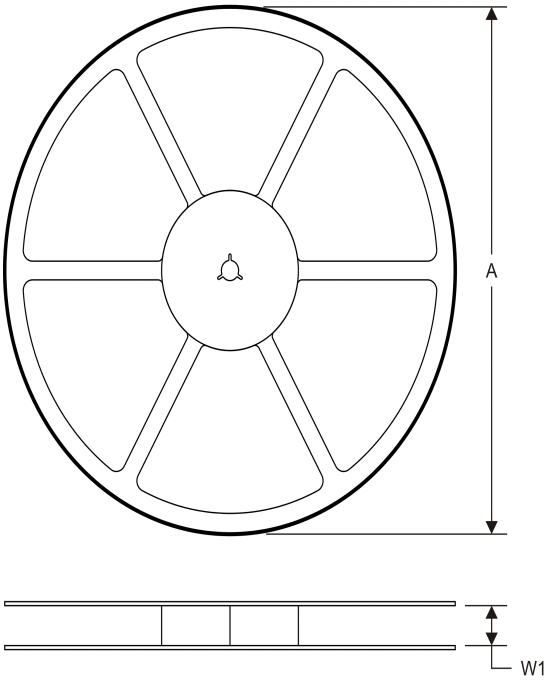
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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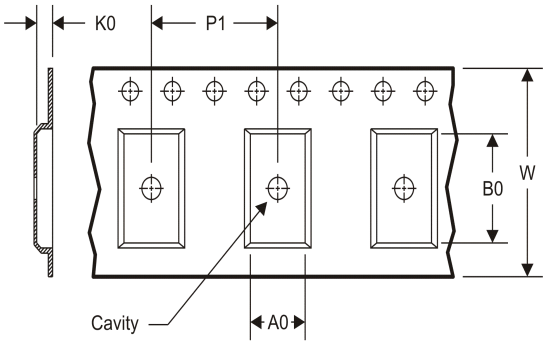
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



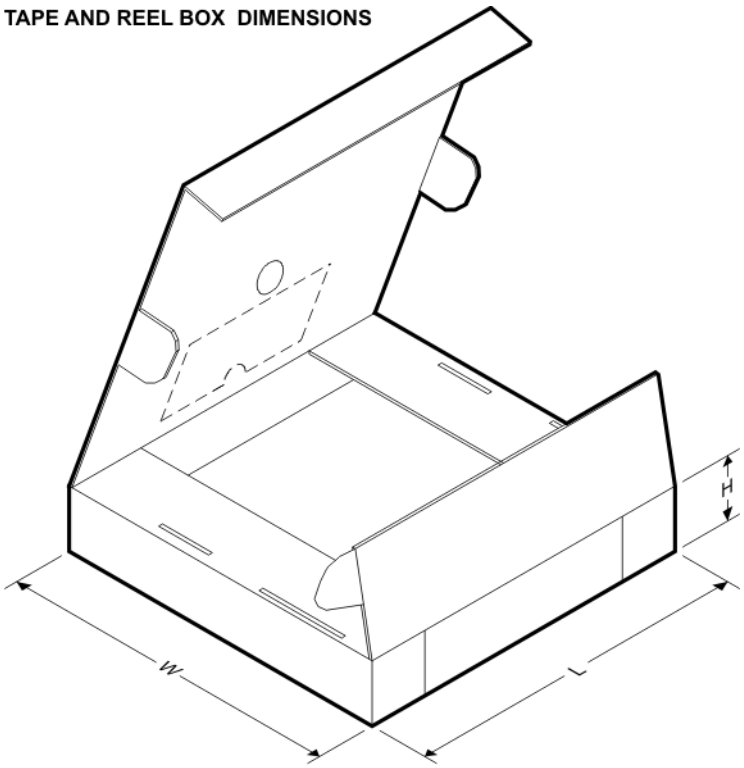
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFEDRI8201PFBR	TQFP	PFB	48	2000	330.0	16.8	9.6	9.6	1.5	12.0	16.0	Q2
AFEDRI8201PFBT	TQFP	PFB	48	250	177.8	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

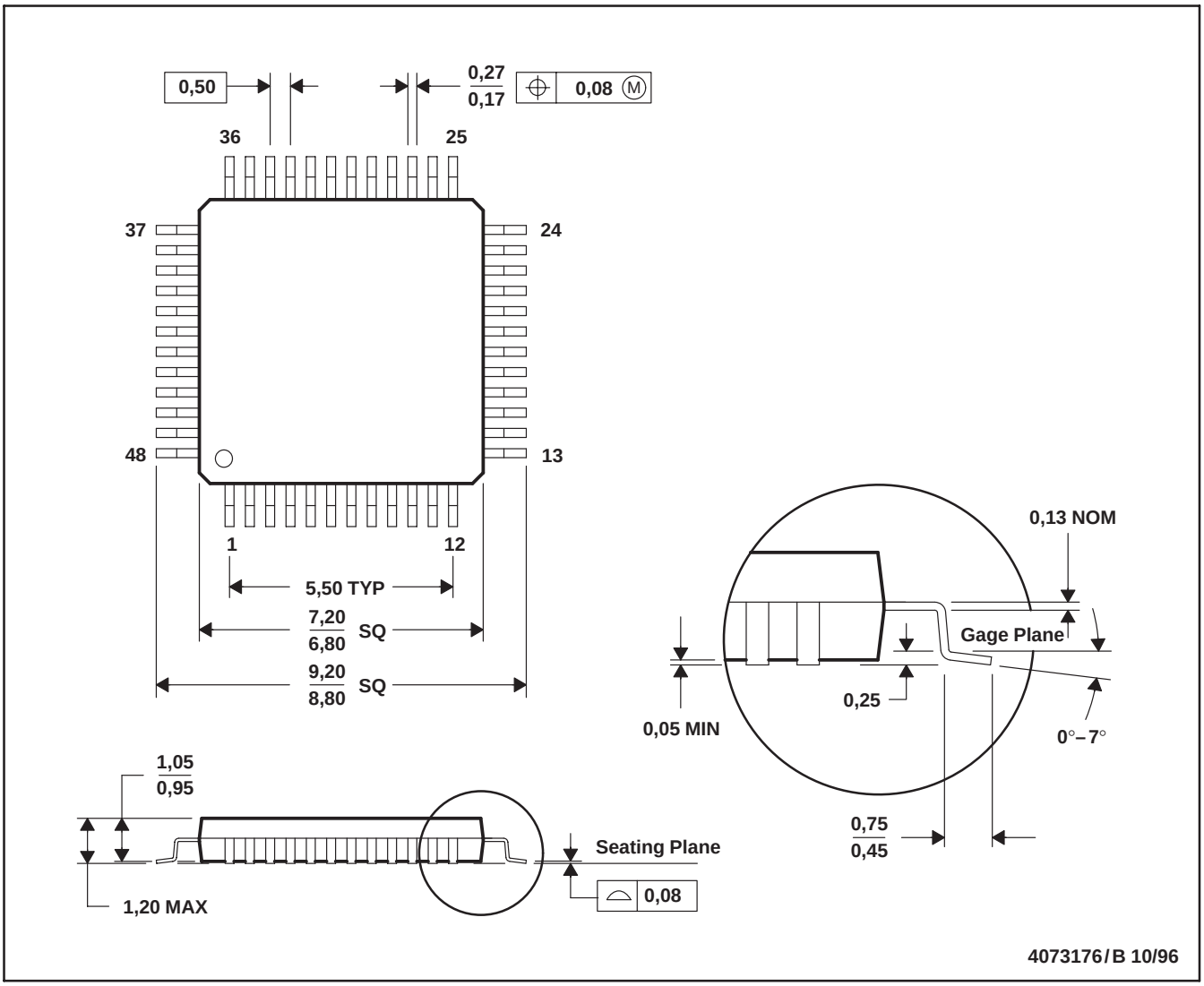


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFEDRI8201PFBR	TQFP	PFB	48	2000	367.0	367.0	38.0
AFEDRI8201PFBT	TQFP	PFB	48	250	210.0	185.0	35.0

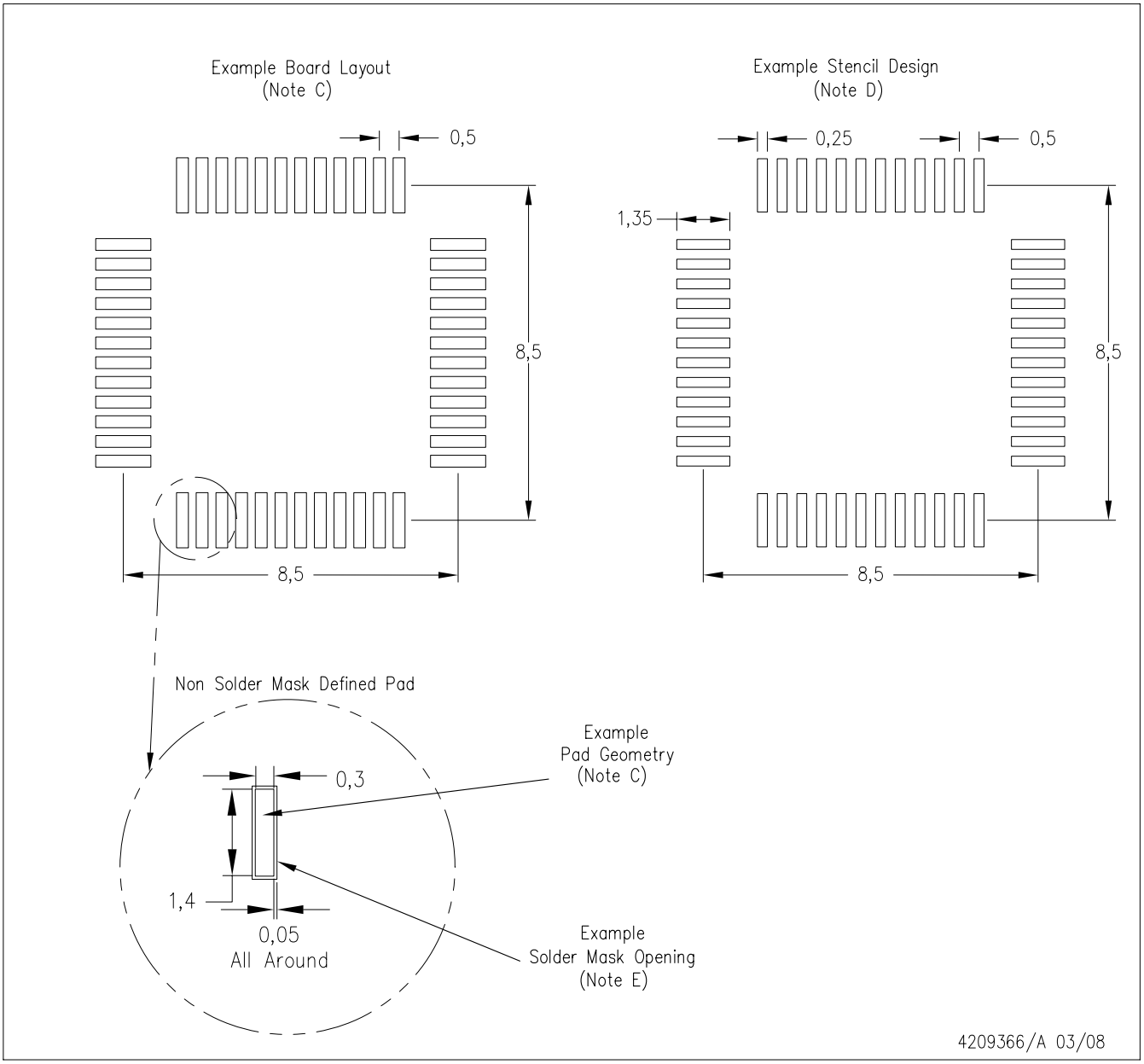
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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