DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT6323A

Programmable ripple counter with oscillator; 3-state

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

September 1993

Philips
Semiconductors

PHILIPS

Programmable ripple counter with oscillator; 3-state

74HC/HCT6323A

FEATURES

- 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 50 MHz (V_{CC} = 5 V ± 10%)
- 3-state output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3 to 6 V
- Oscillator stop function ($\overline{MR}$)
- Output capability: bus driver → (15 LSTTL)
- I_{CC} category: MSI.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation.

GENERAL DESCRIPTION

The HC/HCT6323A are high-speed Si-gate CMOS devices.

They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT6323A are oscillators designed for quartz crystal combined with a programmable 3-state counter, a 3-state output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-by-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator and sets the output buffer in the 3-state condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive. In the HCT version, the $\overline{MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay X1 to OUT (S1 = S2 = LOW)	C_L = 15 pF; V_{CC} = 5 V	17	17	ns
f_{max}	maximum clock frequency		90	90	MHz
C_I	input capacitance except X1 and X2		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	+1; notes 1 and 2	54	54	pF
		+2; notes 1 and 2	42	42	pF
		+4; notes 1 and 2	36	36	pF
		+8; notes 1 and 2	33	33	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$

   where:

   f_i = input frequency in MHz; f_o = output frequency in MHz.

   V_{CC} = supply voltage in V; C_L = output load capacitance in pF.

   $I_{pull\text{-}up}$ = pull-up currents in μA.

2. For HC and HCT an external clock is applied to X1 with:

   $t_r = t_f \leq 6$ ns, V_i is GND to V_{CC}, $\overline{MR}$ = HIGH

   $I_{pull\text{-}up}$ is the summation of $-I_I$ (μA) of S1 and S2 inputs at the LOW state.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT6323AD	8	SO	plastic	SOT96

PINNING

SYMBOL	PIN	DESCRIPTION
OUT	1	counter output
S1 - S2	3, 2	mode select inputs for divide by 1, 2, 4 or 8
GND	4	ground (0 V)
$\overline{MR}$	5	master reset (active LOW)
X2	6	oscillator pin
X1	7	clock input/oscillator pin
V_{CC}	8	positive supply

FUNCTION TABLE

INPUTS		OUTPUTS
S1	S2	OUT
0	0	f_i
0	1	$f_i/2$
1	0	$f_i/4$
1	1	$f_i/8$

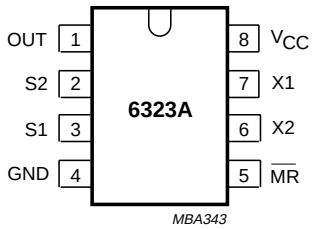


Fig.1 Pin configuration.

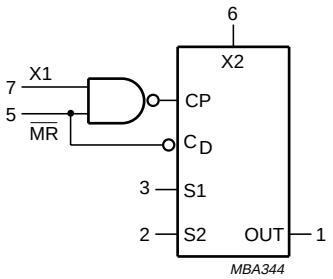


Fig.2 IEC logic symbol.

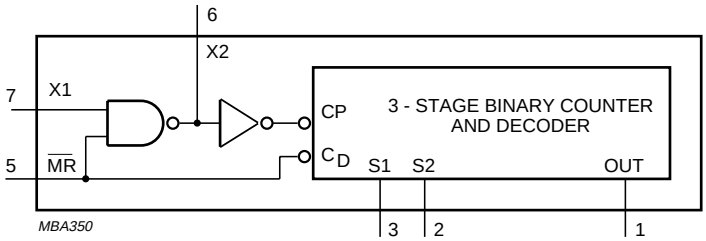
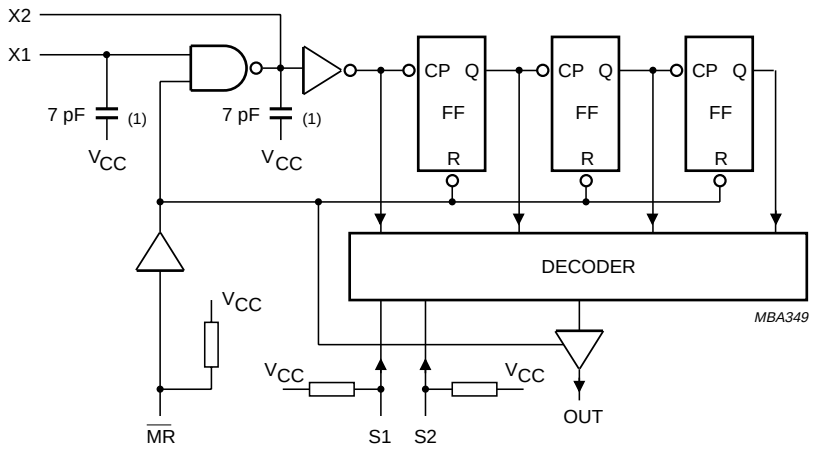


Fig.3 Functional diagram.



Internal capacitors typical 7 pF each. Including stray capacitors on pin X1 and X2, total capacitance will be typical 12 pF per pin.

Fig.4 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: non-standard; bus driver (except for X2)

I_{CC} category: MSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TEST CONDITION		
		25			–40 to 85		–40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	HIGH level input voltage $\overline{MR}$, X1 input	1.5 3.15 4.2	1.2 2.4 3.2	– – –	1.5 3.15 4.2	– – –	1.50 3.15 4.20	– – –	V V V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage $\overline{MR}$, X1 input	– – –	0.8 2.1 2.8	0.5 1.35 1.80	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V V V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage X2 output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = –2.6 mA I_O = –3.3 mA
		3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = –2.6 mA I_O = –3.3 mA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	X1 = GND and $\overline{MR}$ = V_{CC}	–I_O = 20 μA I_O = –20 μA I_O = –20 μA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = –20 μA I_O = –20 μA I_O = –20 μA
V_{OH}	HIGH level output voltage OUT	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = –20 μA I_O = –20 μA I_O = –20 μA
V_{OH}	HIGH level output voltage OUT	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = –6 mA I_O = –7.8 mA
V_{OL}	LOW level output voltage X2 output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 2.6 mA I_O = 3.3 mA
		– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage OUT	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TEST CONDITION		
		25			–40 to 85		–40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OL}	LOW level output voltage OUT	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = 6 mA I_O = 7.8 mA
$\pm I_{LI}$	input leakage current X1	–	–	0.1	–	1	–	1	μA	6.0	$\overline{MR}$ = V_{CC} S1 = V_{CC} S2 = V_{CC}	
$-I_I$	input pull-up current S1, S2 and $\overline{MR}$	5	30	100	–	–	–	–	μA	6.0	GND	see Fig.11 and Fig.12
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 1	– – –	61 22 19	185 37 31	– – –	230 46 39	– – –	275 55 47	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = GND S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 2	– – –	74 27 23	235 47 40	– – –	290 58 49	– – –	350 70 60	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = GND S2 = V_{CC}
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 4	– – –	91 33 28	285 57 48	– – –	355 71 60	– – –	425 85 72	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = V_{CC} S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 8	– – –	105 38 32	335 67 57	– – –	415 83 71	– – –	500 100 85	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = V_{CC} S2 = V_{CC}
t_{PLZ}/t_{PHZ}	3-state output disable time $\overline{MR}$ to OUT	– – –	75 15 13	150 30 26	– – –	185 37 31	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.8	
t_{PZL}	3-state output enable time $\overline{MR}$ to OUT	– – –	36 13 11	150 30 26	– – –	185 37 31	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.8	
t_{PZH}	3-state output enable time $\overline{MR}$ to OUT	– – –	61 22 19	200 40 34	– – –	250 50 43	– – –	300 60 51	ns ns ns	2.0 4.5 6.0	Fig.8	note 1
t_{THL}/t_{TLH}	output transition time	– – –	14 5 4	60 12 10	– – –	75 15 13	– – –	90 19 15	ns ns ns	2.0 4.5 6.0	Fig.7	
t_W	clock pulse width X1, HIGH or LOW	50 10 9	17 6.0 5	– – –	60 12 10	– – –	75 15 13	– – –	ns ns ns	2.0 4.5 6.0	Fig.7	
t_W	master reset pulse width $\overline{MR}$; LOW	80 16 14	22 8 7	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.9	
t_{rem}	removal time $\overline{MR}$ to X1	100 20 17	19 7 6.0	– – –	125 25 21	– – –	150 30 26	– – –	ns ns ns	2.0 4.5 6.0	Fig.9	
f_{max}	maximum clock pulse frequency	10 50 59	17 85 100	– – –	8 40 47	– – –	6.6 33 39	– – –	MHz MHz MHz	2.0 4.5 6.0	Fig.7	

Note to the 74HC AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (except for X2).

I_{CC} category: MSI.

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	HIGH level input voltage $\overline{MR}$, S1 and S2 inputs	2.0	–	–	2.0	–	2.0	–	V	4.5 to 5.5		
V_{IL}	LOW level input voltage $\overline{MR}$, S1 and S2 inputs	–	–	0.8	–	0.8	–	0.8	V	4.5 to 5.5		
V_{IH}	HIGH level input voltage X1 input	3.15 3.85	– –	– –	3.15 3.85	– –	3.15 3.85	– –	V V	4.5 5.5		
V_{IL}	LOW level input voltage X1 input	– –	– –	1.35 1.65	– –	1.35 1.65	– –	1.35 1.65	V V	4.5 5.5		
V_{OH}	HIGH level output voltage X2 output	3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = −2.6 mA
		3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −2.6 mA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = −20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −20 mA
V_{OH}	HIGH level output voltage OUT	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage OUT	3.98	–	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −6 mA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OL}	LOW level output voltage X2 output	–	–	0.26	–	0.33	–	0.4	V	4.5	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 2.6 mA
		–	0	0.1	–	0.1	–	0.1	V	4.5	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 20 μA
V_{OL}	LOW level output voltage OUT	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage OUT	–	–	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6 mA
$\pm I_{LI}$	input leakage current	–	–	0.1	–	1.0	–	1.0	μA	5.5	$\overline{MR}$ = V_{CC}; S1 = V_{CC}; S2 = V_{CC}	
$-I_I$	input pull-up current S1, S2 and $\overline{MR}$	5	25	100	–	–	–	–	μA	5.5	GND	see Fig.11 and Fig.12
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	μA	5.5	V_{CC} or GND	I_o = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1	–	100	360	–	450	–	490	μA	5.5	V_{CC} or GND	other inputs at V_{CC} or GND; I_o = 0; (note 1)

Note to the HCT DC Characteristics

1. The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$, S1, S2	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-1	–	24	40	–	50	–	60	ns	4.5	Fig.7	S1 = GND S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-2	–	29	50	–	62	–	75	ns	4.5	Fig.7	S1 = GND S2 = V_{CC}
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-4	–	35	60	–	75	–	90	ns	4.5	Fig.7	S1 = V_{CC} S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-8	–	40	70	–	87	–	105	ns	4.5	Fig.7	S1 = V_{CC} S2 = V_{CC}
t_{PLZ}/t_{PHZ}	3-state output disable time $\overline{MR}$ to OUT	–	21	35	–	43	–	52	ns	4.5	Fig.8	
t_{PZ}	3-state output enable time $\overline{MR}$ to OUT	–	16	30	–	37	–	45	ns	4.5	Fig.8	
t_{PZH}	3-state output enable time $\overline{MR}$ to OUT	–	22	38	–	47	–	57	ns	4.5	Fig.8	see note 1
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	19	ns	4.5	Fig.7	
t_W	clock pulse width X1, HIGH or LOW	10	6	–	12	–	15	–	ns	4.5	Fig.7	
t_W	master reset pulse width $\overline{MR}$; LOW	16	8	–	20	–	24	–	ns	4.5	Fig.9	
t_{rem}	removal time $\overline{MR}$ to X1	24	12	–	30	–	36	–	ns	4.5	Fig.9	
f_{max}	maximum clock pulse frequency	50	85	–	40	–	33	–	MHz	4.5	Fig.7	

Note to the 74HCT AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

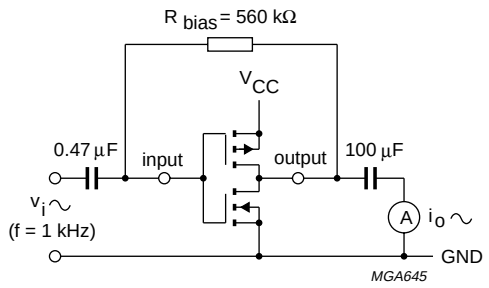


Fig.5 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also Fig.6); $\overline{MR}$ = HIGH.

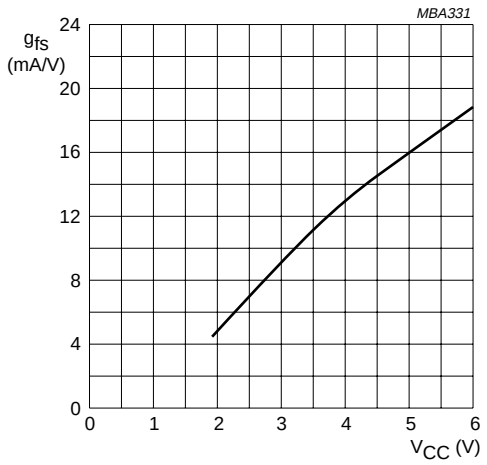
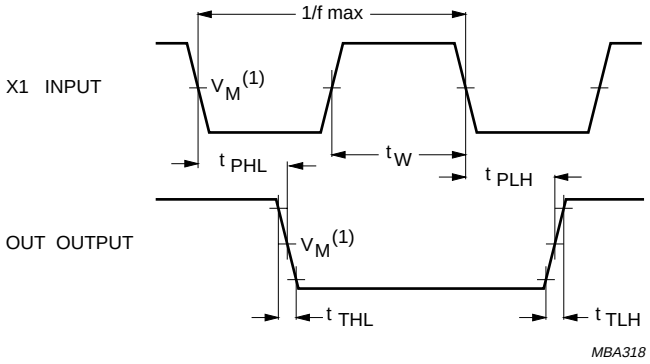
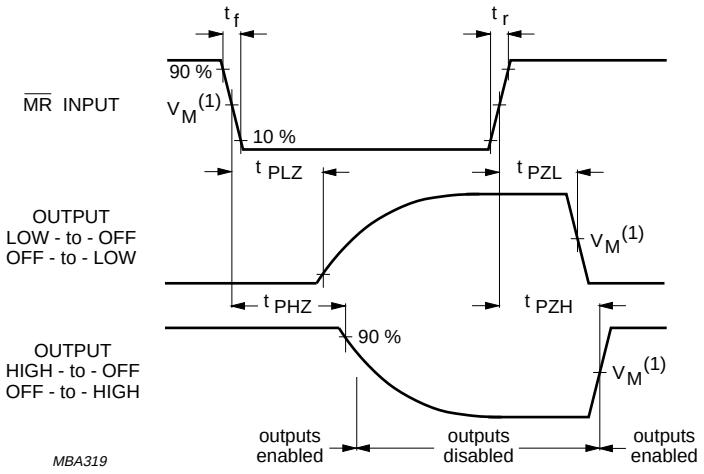


Fig.6 Typical forward transconductance g_{fs} as a function of the supply voltage V_{cc} at T_{amb} = 25 °C.



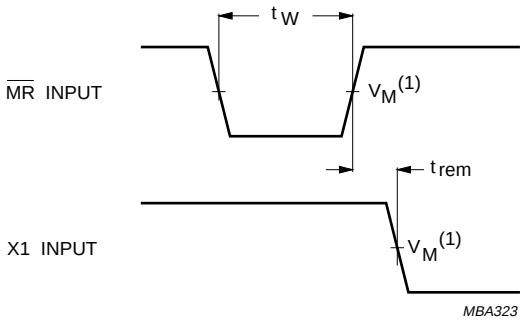
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the clock (X1) to output (OUT) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

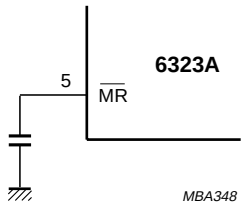
Fig.8 Waveforms showing the input $\overline{MR}$ to output OUT, 3-state enable and disable times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the $\overline{MR}$ minimum pulse width and $\overline{MR}$ to X1 removal time.

APPLICATION INFORMATION



The input pull-up current is used to create a power-on delay time at $\overline{MR}$.

Fig.10 Power-on reset.

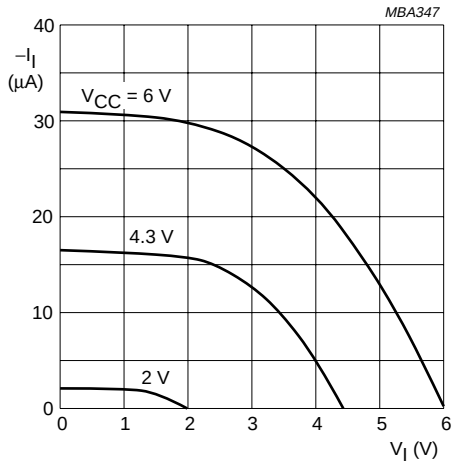


Fig.11 Typical input pull-up current as a function of the input voltage (V_I).

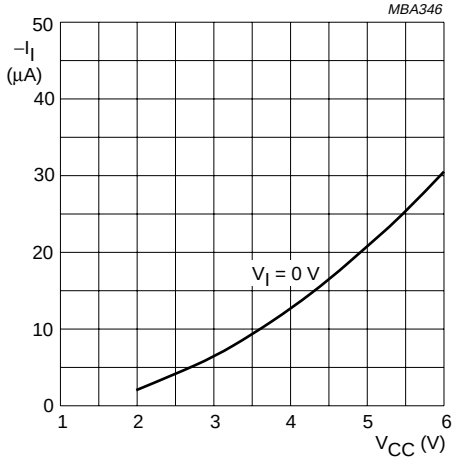


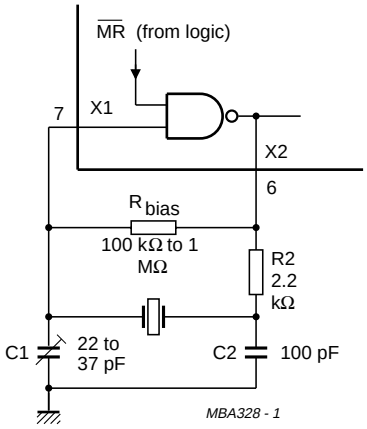
Fig.12 Typical input pull-up current as a function of the supply voltage (V_{CC}).

Table 1 Typical application values

f (MHz)	R2 (kΩ)	C1 (pF)	C2 (pF)
1	4.7	47 to 68	
10	2.2	47 to 68	
25	1	33	33

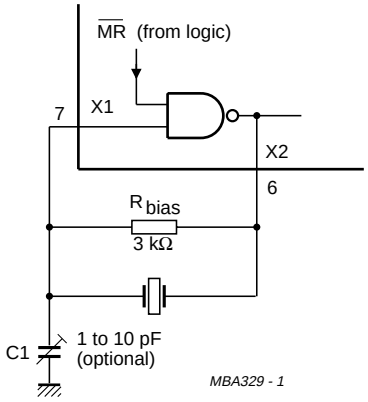
Table 2 Typical Application Values

f (MHz)	R_{bias} (kΩ)	C1 (pF)
50	3.0	4.7



Above 5 MHz replace R2 by a capacitor of half the value of C2.
C_L at which a crystal is specified (or adjusted) equals for this application C1 . C2/C1 + C2.

Fig.13 Typical setup for a crystal oscillator operating in the fundamental mode (1 MHz to 25 MHz).



Applicable for third overtone crystals (lower damping resistance at the third harmonic frequency) at typical 50 MHz. For lower frequencies extra load capacitors must be supplied, or increase bias resistor.

Fig.14 Typical set-up for a crystal oscillator operating in the third overtone mode without the use of an inductor.

Typical Crystal Oscillator

In Fig.13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external components. There are two on-chip capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to run the oscillator in the third overtone without external capacitors applied. If a certain frequency is chosen, the IC parameters, as forward transconductance, and the crystal parameters such as the motional resistances R1 (fundamental), R3 (third overtone) and R5 (fifth overtone), are of paramount importance. Also the values of the external components as R_s (series resistance) and the crystal load capacitances play an important role. Especially in overtone mode oscillations, R_b (bias resistance) and the load capacitance values are very important.

Considerations for Fundamental Oscillator:

In the fundamental oscillator mode, the R_b has only the function of biasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. 100 kΩ up to 10 MΩ. The load capacitors C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load capacitance. C1 can be used to trim the oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in the crystal. R_s also suppresses overtone oscillations and introduces a phase shift over a broad frequency range. This is of less concern provided R_s is not too high a value.

Note

A combination of a small load capacitor value and a small series resistance, may cause a third overtone oscillation.

Considerations for Third-overtone Oscillator:

In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for third overtone can be too small for oscillation. A simple solution to suppress the fundamental oscillation, is to spoil the crystal fundamental activity. By dramatically reducing the value of the bias resistor of the inverting stage, and applying small load capacitors, it is possible to have an insufficient phase in the total loop for fundamental oscillation. However the phase for third overtone is good. It can be explained by the $R_b \times C_l$ time constant. During oscillation the crystal with the load capacitors cause a phase shift of 180°. Because R_b is parallel with the crystal (no R_s), R_b spoils the phase for fundamental. $R_b \times C_l$ must be of a value, that it is not spoiling the phase for third overtone too much. Because third overtone is a 3 times higher frequency than the fundamental, the $R_b \times C_l$ cannot 'maintain' the higher third overtone frequency, which results in a less spoiled overtone phase.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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