DATA SHEET

BF908WR
N-channel dual-gate MOS-FET

Preliminary specification

1995 Apr 25

N-channel dual-gate MOS-FET BF908WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

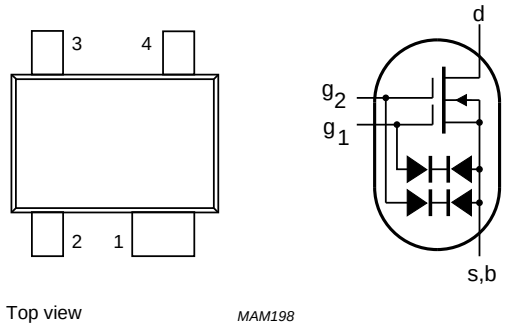
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT343R package. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MD.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		2.4	3.1	4	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

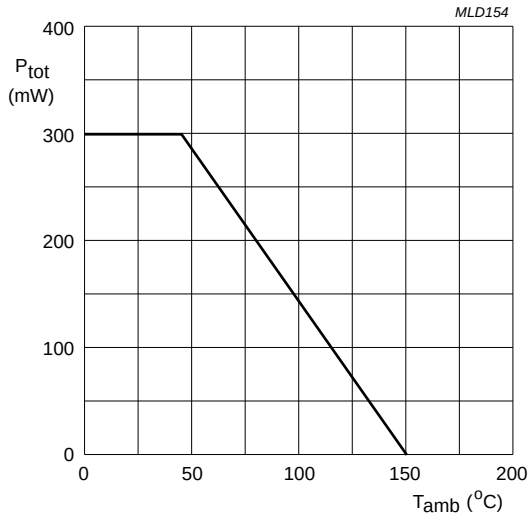


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 87 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

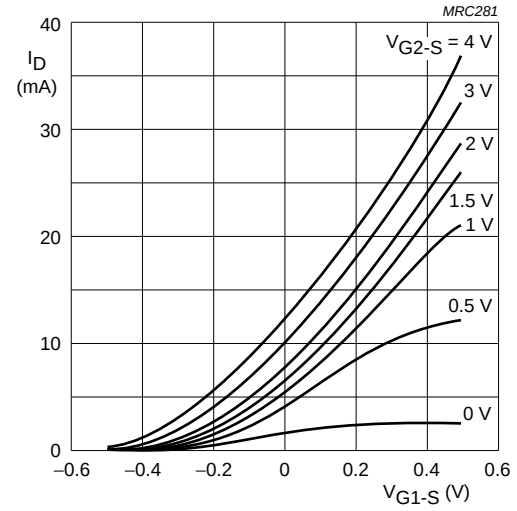
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	8	–	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	8	–	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	–	–2	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	–	–1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0	3	15	27	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	–	50	nA

DYNAMIC CHARACTERISTICS

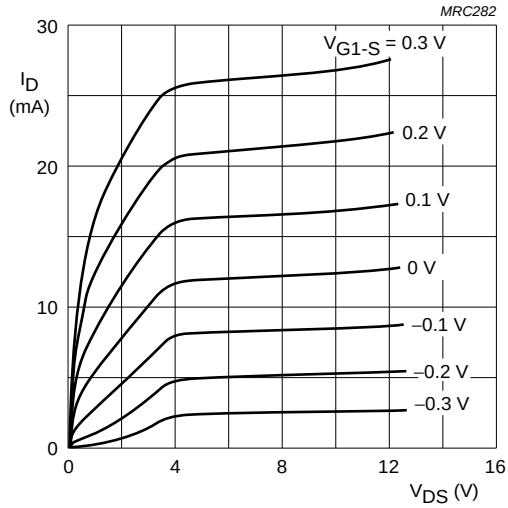
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	drain-source capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	0.6	1.2	dB
		f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	1.5	2.5	dB



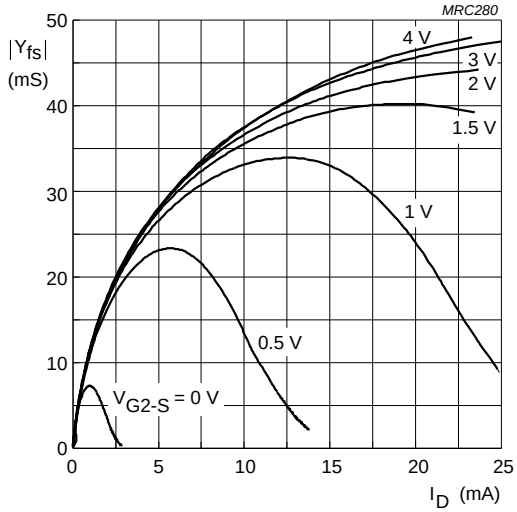
V_{DS} = 8 V.
T_j = 25 °C.

Fig.3 Transfer characteristics; typical values.



V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



V_{DS} = 8 V.
T_j = 25 °C.

Fig.5 Forward transfer admittance as a function of drain current; typical values.

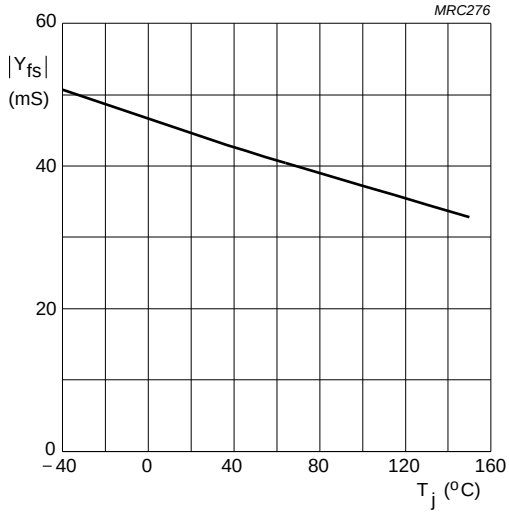
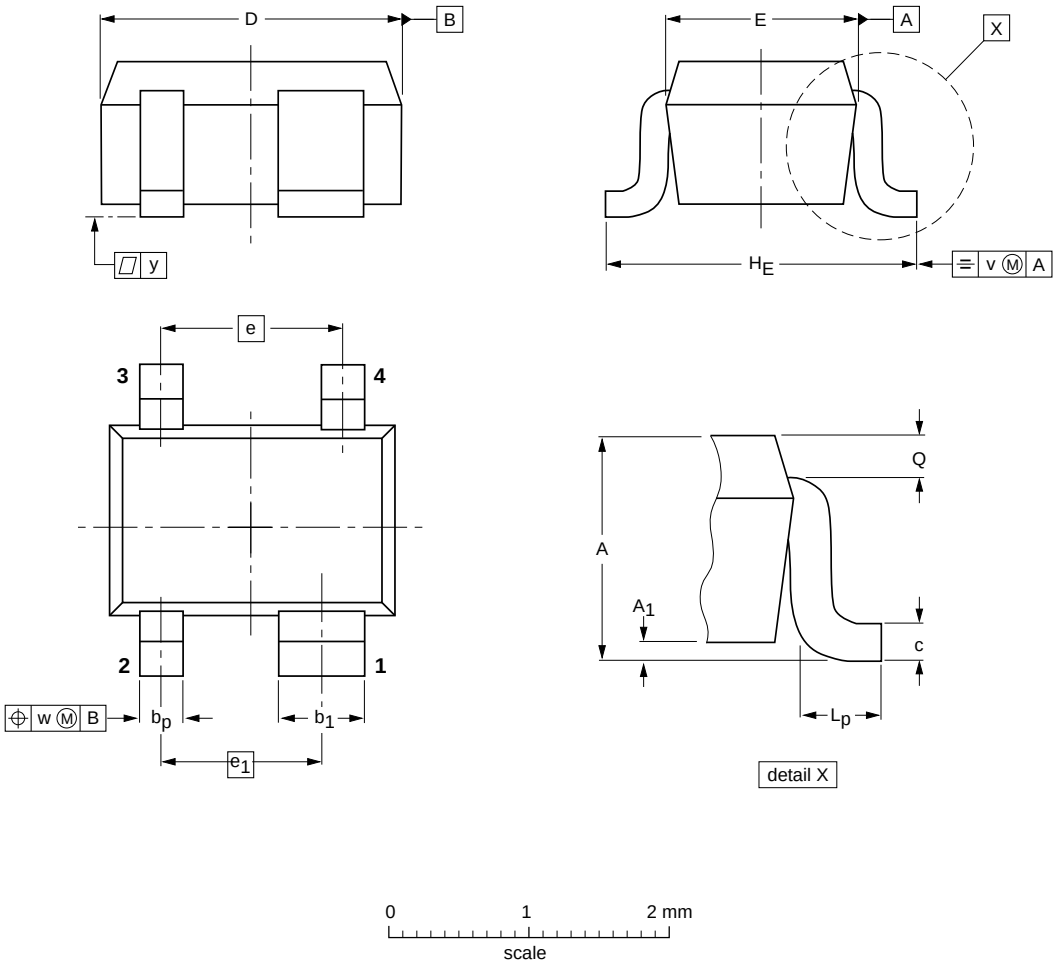


Fig.6 Forward transfer admittance as a function of junction temperature; typical values.

PACKAGE OUTLINE

Plastic surface-mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						~~97-05-21~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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