DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4538
Dual retriggerable precision monostable multivibrator

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

Dual retriggerable precision monostable multivibrator

74HC/HCT4538

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I_{CC} category: MSI
- Power-on reset on-chip

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with “4538” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ($n\overline{A}_0$), an active HIGH trigger/retrigger input (nA_1) , an overriding active LOW direct reset input ($n\overline{R}_D$), an output (nQ) and its complement ($n\overline{Q}$), and two pins (nC_{TC} and nRC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ± 0.2%.

The “4538” may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $0.7 \times R_t \times C_t$. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at $n\overline{R}_D$ terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	27	30	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multivibrator	notes 1 and 2	136	138	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) +$
   $+ 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC}$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   D = duty factor in %

   C_{EXT} = timing capacitance in pF

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

Dual retriggerable precision monostable multivibrator

74HC/HCT4538

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}$, $2C_{TC}$	external capacitor connections
2, 14	$1RC_{TC}$, $2RC_{TC}$	external resistor/capacitor connections
3, 13	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1A_1$, $2A_1$	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{A}_0$, $2\overline{A}_0$	trigger inputs (HIGH-to-LOW, edge-triggered)
6, 10	1Q, 2Q	pulse outputs
7, 9	$1\overline{Q}$, $2\overline{Q}$	complementary pulse outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

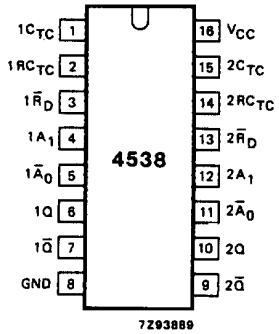


Fig.1 Pin configuration.

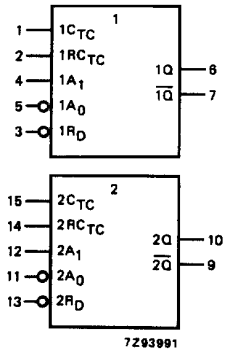


Fig.2 Logic symbol.

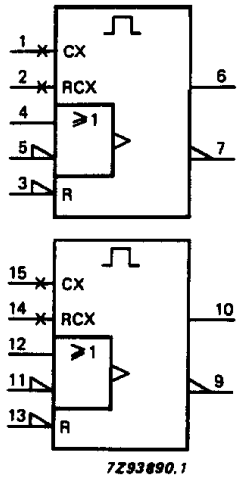


Fig.3 IEC logic symbol.

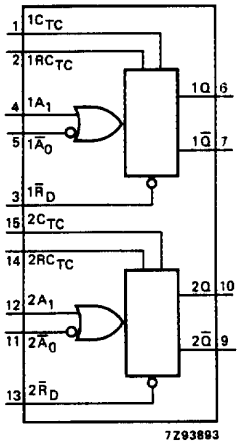
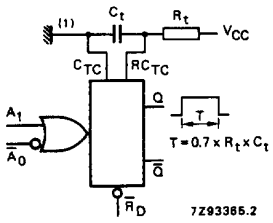


Fig.4 Functional diagram.



(1) Connect C_{TC} (pins 1 and 15) to GND (pin 8).

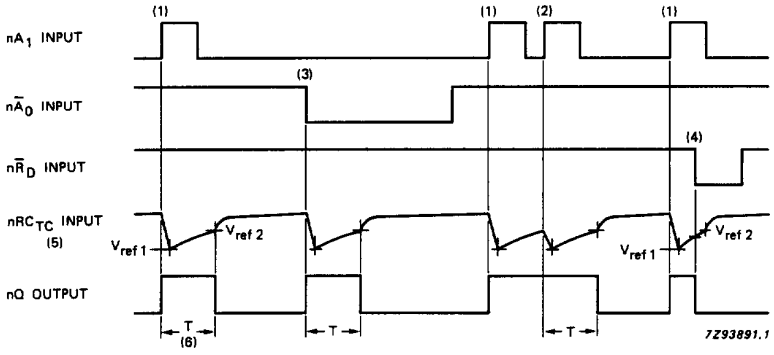
Fig.5 Connection of the external timing components R_t and C_t.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{A}_0$	nA_1	$n\bar{R}_D$	nQ	$n\bar{Q}$
↓	L	H	⎍	⎍
H	↑	H	⎍	⎍
X	X	L	L	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH transition
   ↓ = HIGH-to-LOW transition
   ⎍ = one HIGH level output pulse
   ⎍ = one LOW level output pulse



(1) Positive edge triggering.
(2) Positive edge retriggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) V_{ref1} and V_{ref2} are internal reference voltages.
(6) $T = 0.7 \times R_t \times C_t$ (see also Fig.5).

Fig.6 Timing diagram.

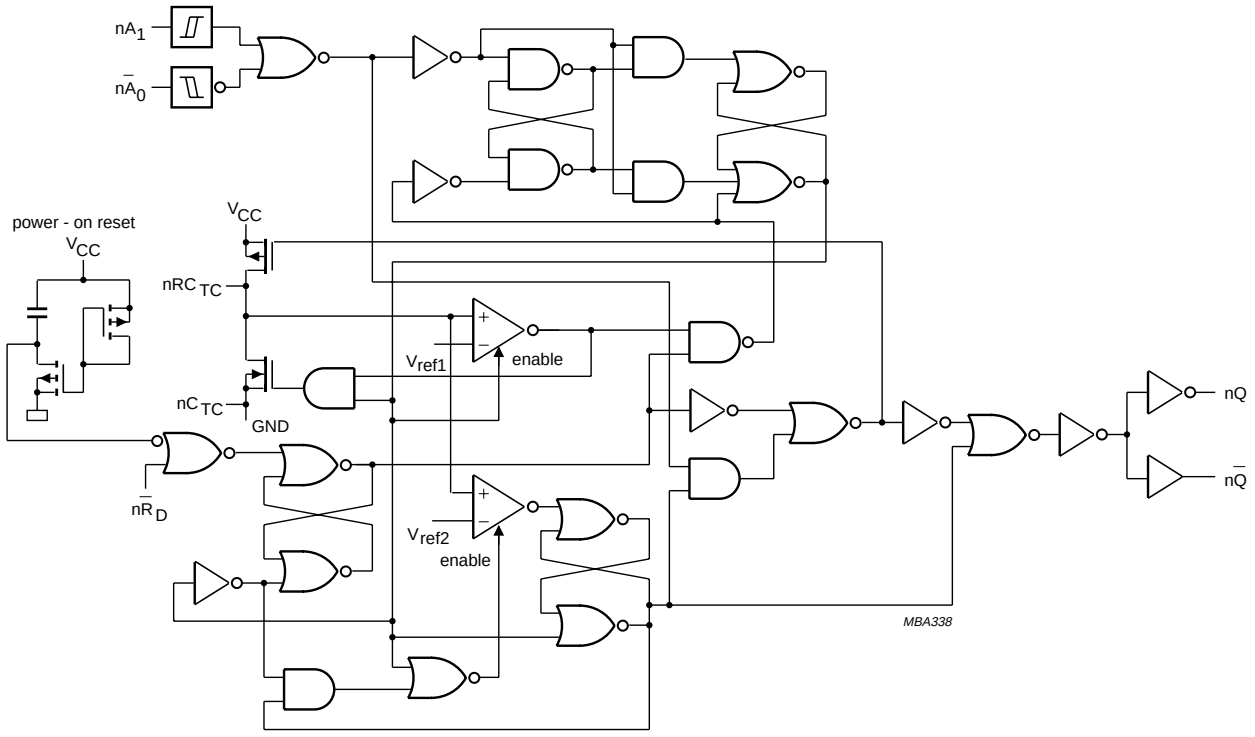


Fig.7 Logic diagram (V_{ref1} and V_{ref2} are internal reference voltages).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay $n\overline{A}_0$, nA_1 to $n\overline{Q}$		83 30 24	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		80 29 23	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		83 30 24	265 53 45		340 68 58		400 80 68	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8
t_W	$n\overline{A}_0$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_W	nA_1 pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_W	$n\overline{R}_D$ pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_W	nQ, $n\overline{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig.8; R_t = 10 kΩ; C_t = 0.1 µF
t_{rem}	removal time $\overline{R}_D$ to $n\overline{A}_0$, nA_1	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.8

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{rt}	retrigger time $n\overline{A}_0$, nA_1	– – –	455+X 80+X 55+X		– – –		– – –		ns	2.0 4.5 6.0	Fig.8 X = C_{EXT} / (4.5 × V_{CC})
R_{EXT}	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0	
C_{EXT}	external timing capacitor	no limits							pF	5.0	

NON-STANDARD DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I (V)	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ	max.	min.	max.	min.	max.				
$\pm I_I$	input leakage current nRC_{EXT}			0.5		5.0		10.0	µA	6.0	2.0 or GND	V_{CC} or GND; note 1

Note

1. This measurement can only be carried out after a trigger pulse is applied.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{A}_0$, nA_1	0.50
$n\overline{R}_D$	0.65

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ		35	60		75		90	ns	4.5	Fig.8
t_{PHL}	propagation delay $n\overline{A}_0$, nA_1 to $n\overline{Q}$		35	60		75		90	ns	4.5	Fig.8
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		35	60		75		90	ns	4.5	Fig.8
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		35	60		75		90	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		21	ns	4.5	Fig.8
t_W	$n\overline{A}_0$ pulse width LOW	20	11		25		30		ns	4.5	Fig.8
t_W	nA_1 pulse width HIGH	16	5		20		24		ns	4.5	Fig.8
t_W	$n\overline{R}_D$ pulse width LOW	20	11		25		30		ns	4.5	Fig.8
t_W	nQ, $n\overline{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig.8; R_t = 10 kΩ; C_t = 0.1 µF
t_{rem}	removal time $\overline{R}_D$ to $n\overline{A}_0$, nA1	7	2		9		11		ns	4.5	Fig.8
t_{rt}	retrigger time $n\overline{A}_0$, nA_1	–	80+X		–		–		ns	4.5	Fig.8 X = C_{EXT} / (4.5 × V_{CC})
R_{EXT}	external timing resistor	2		1000					kΩ	5.0	
C_{EXT}	external timing capacitor	no limits							pF	5.0	

NON-STANDARD DC CHARACTERISTICS FOR 74HCT

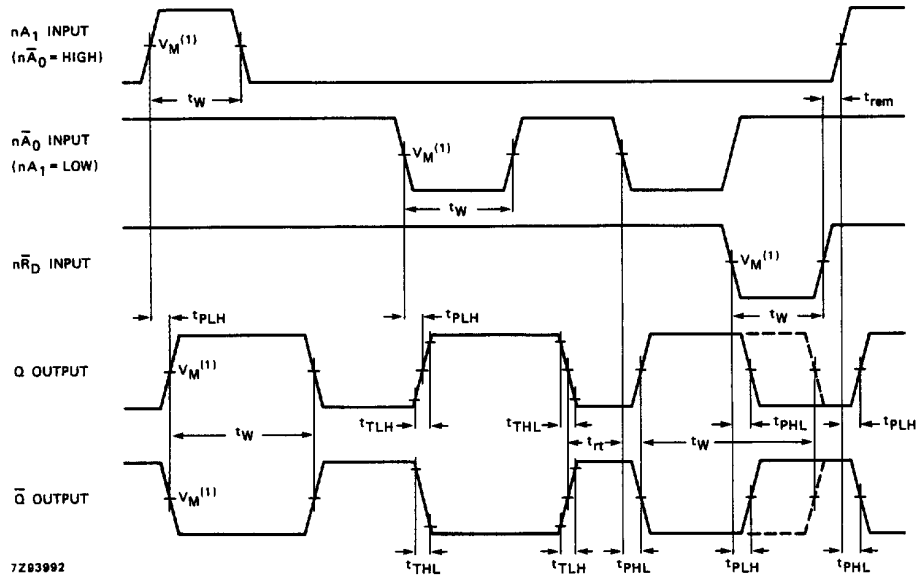
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I (V)	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ	max.	min.	max.	min.	max.				
$\pm I_I$	input leakage current nRC_{EXT}			0.5		5.0		10.0	μA	5.5	2.0 or GND	V_{CC} or GND; note 1

Note

1. This measurement can only be carried out after a trigger pulse is applied.

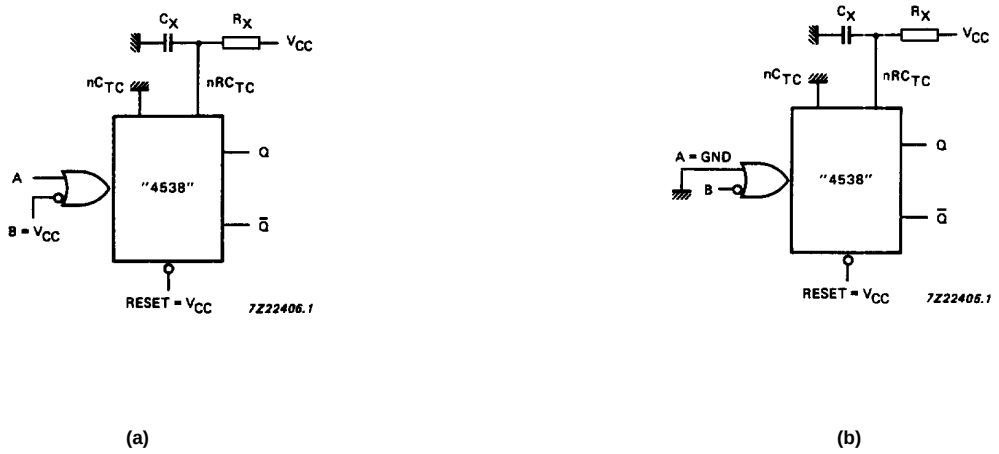
AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

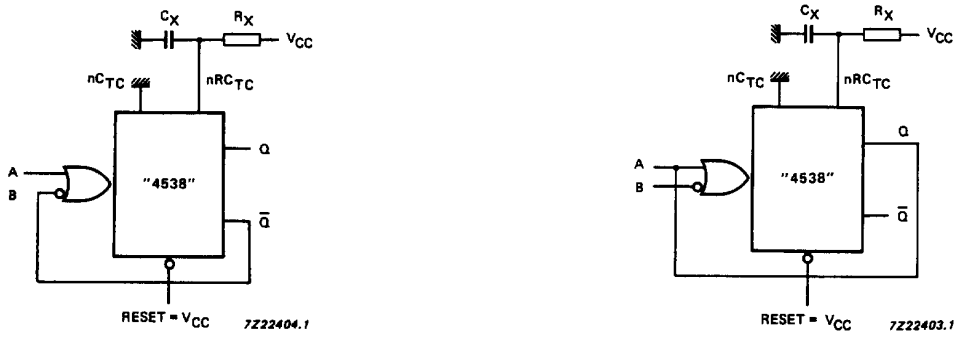
Fig.8 Waveforms showing the input (nA_1, $n\overline{A}_0$, $n\overline{R}_D$) to output (nQ, $n\overline{Q}$) propagation delays, the output transition times, the input and output pulse widths, the removal time from direct reset ($n\overline{R}_D$) to input (nA_1, $n\overline{A}_0$), and the input retrigger time.

APPLICATION INFORMATION



(a) (b)

Fig.9 Retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.



(a) (b)

Fig.10 Non-retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.

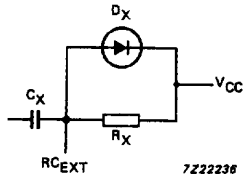


Fig.11 Power-down protection circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig.11.

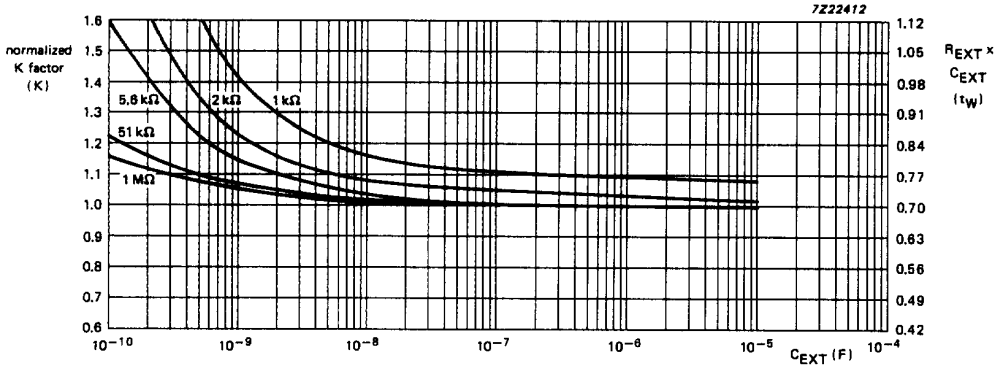


Fig.12 Typical pulse width accuracy versus external capacitance; V_{CC} = 4.5 V; T_{amb} = 25 °C.

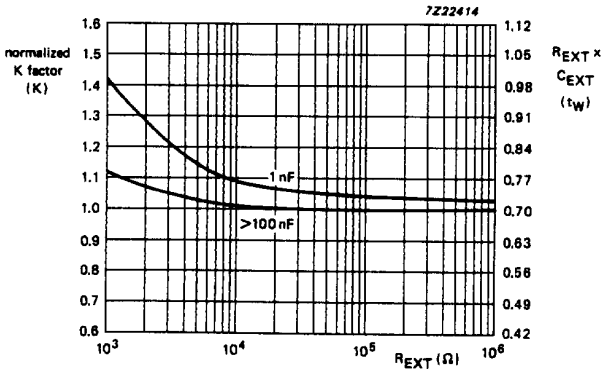


Fig.13 Typical pulse width accuracy versus external resistance; V_{CC} = 4.5 V; T_{amb} = 25 °C.

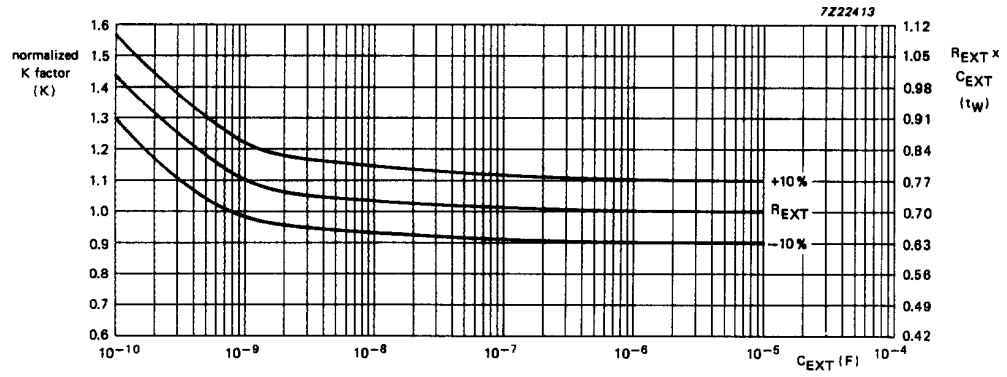


Fig.14 Typical pulse width accuracy versus external capacitance; R_{EXT} = 10 kΩ; V_{CC} = 4.5 V; T_{amb} = 25 °C.

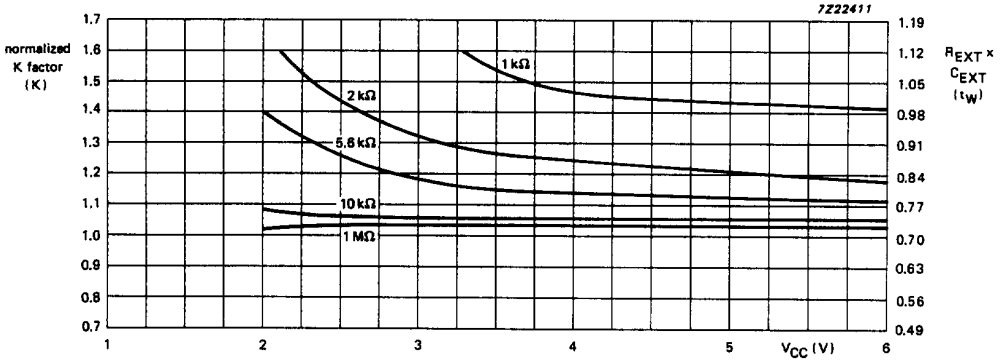


Fig.15 Typical pulse width accuracy versus power supply; C_{EXT} = 1 nF; T_{amb} = 25 °C.

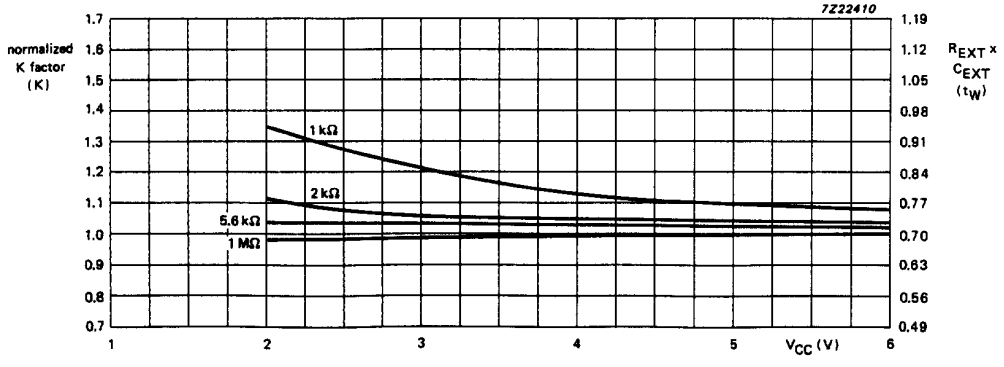


Fig.16 Typical pulse width accuracy versus power supply; C_{EXT} = 100 nF; T_{amb} = 25 °C.

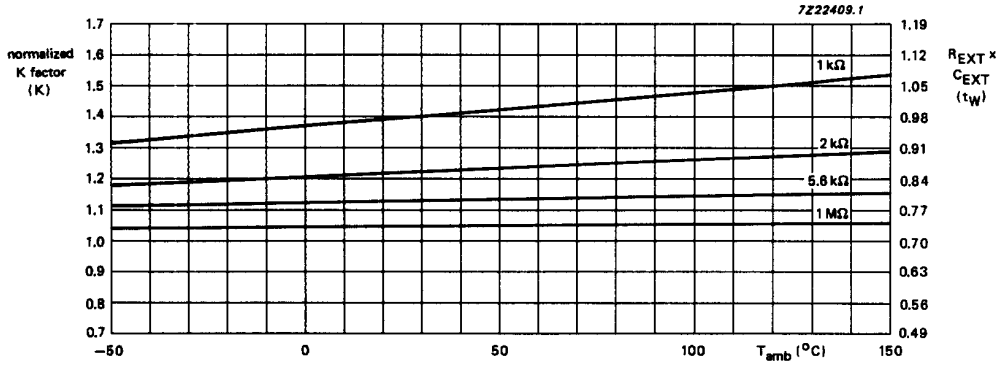


Fig.17 Typical pulse width accuracy versus temperature; C_{EXT} = 1 nF; V_{CC} = 4.5 V.

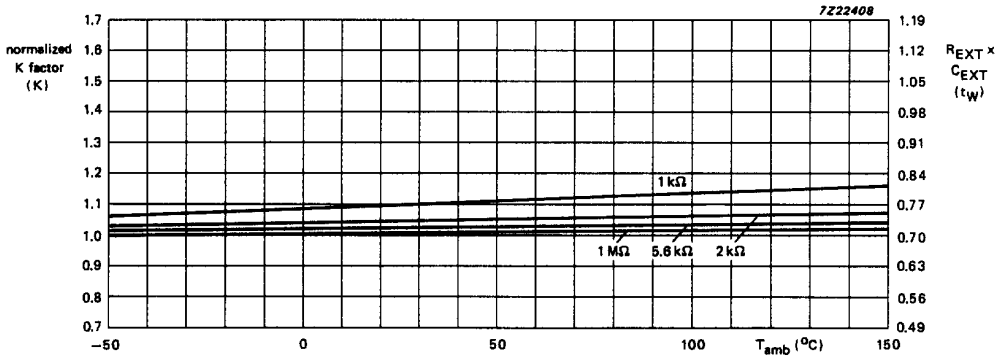


Fig.18 Typical pulse width accuracy versus temperature; C_{EXT} = 1 µF; V_{CC} = 4.5 V.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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