TQFP, BGA
Commercial Temp
Industrial Temp

256K x 18, 128K x 32, 128K x 36 4Mb Sync Burst SRAMs

190 MHz–100 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipelined operation
- Dual Cycle Deselect (DCD) operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipelined mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Common data inputs and data outputs
- Clock control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC standard 100-lead TQFP or 119-Bump BGA package
- Pb-Free 100-lead TQFP package available

Functional Description

Applications

The GS840E18/32/36A is a 4,718,592-bit (4,194,304-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications ranging from DSP main store to networking chip set support. The GS84018/32/36A is available in a JEDEC standard 100-lead TQFP or 119-Bump BGA package.

Controls

Addresses, data I/Os, chip enables ($\overline{E}_1$, E_2, $\overline{E}_3$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin/bump (pin 14 in the TQFP and bump 5R in the BGA). Holding the $\overline{FT}$ mode pin/bump low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipelined mode, activating the rising-edge-triggered Data Output Register.

DCD Pipelined Reads

The GS840E18/32/36A is a DCD (Dual Cycle Deselect) pipelined synchronous SRAM. SCD (Single Cycle Deselect) versions are also available. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock.

Byte Write and Global Write

Byte write operation is performed by using byte write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

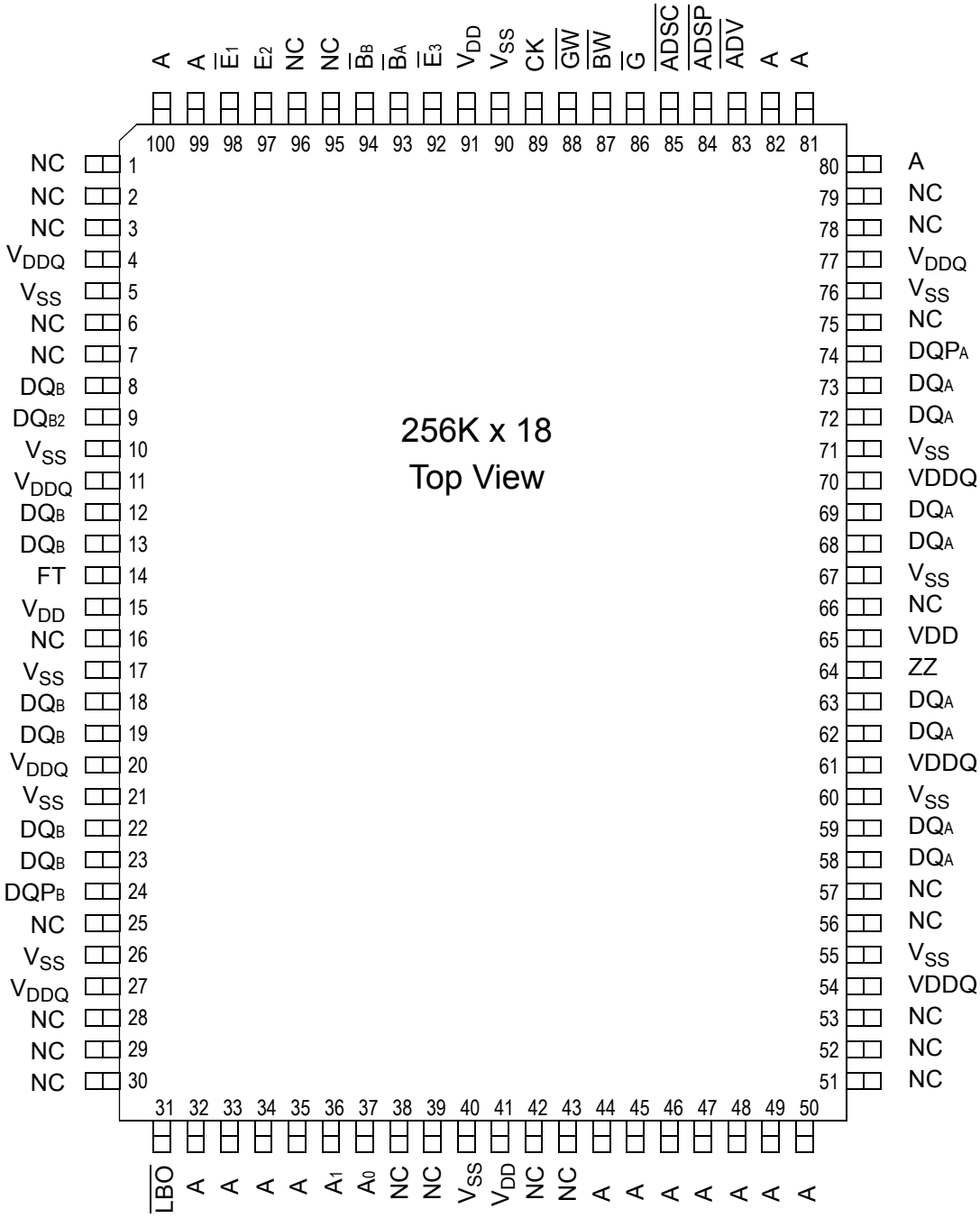
The GS840E18/32/36A operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to de-couple output noise from the internal circuit.

Parameter Synopsis

		–190	–180	–166	–150	–100
Pipeline 3-1-1-1	tCycle	5.3 ns	5.5 ns	6.0 ns	6.6 ns	10 ns
	t_{KQ}	3.0 ns	3.0 ns	3.5 ns	3.8 ns	4.5 ns
	I_{DD}	370 mA	335 mA	310 mA	280 mA	190 mA
Flow Through 2-1-1-1	t_{KQ}	7.5 ns	8 ns	8.5 ns	10 ns	12 ns
	tCycle	8.5 ns	9 ns	10 ns	12 ns	15 ns
	I_{DD}	245 mA	210 mA	190 mA	165 mA	135 mA

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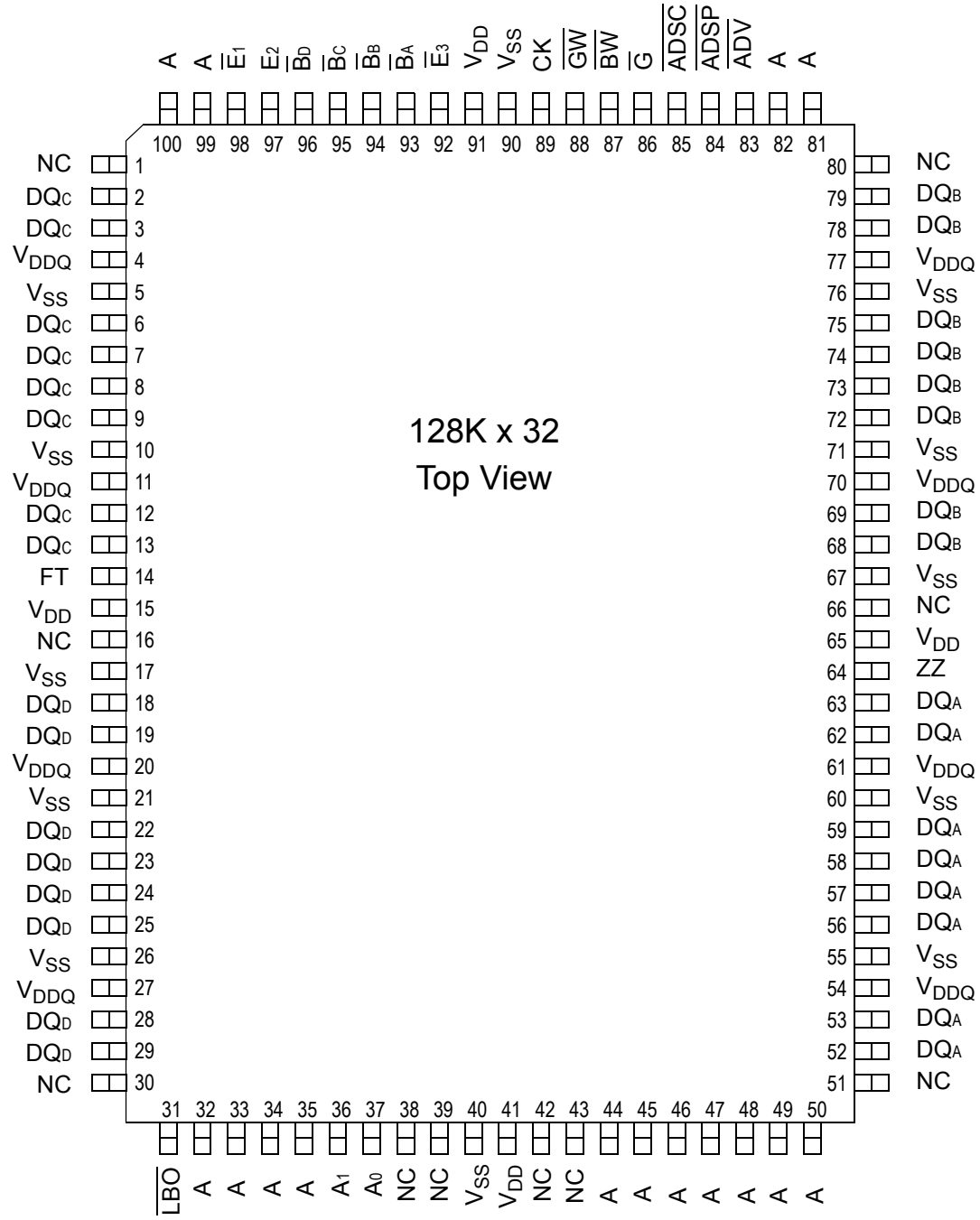
GS840E18A 100-Pin TQFP Pinout (Package T)



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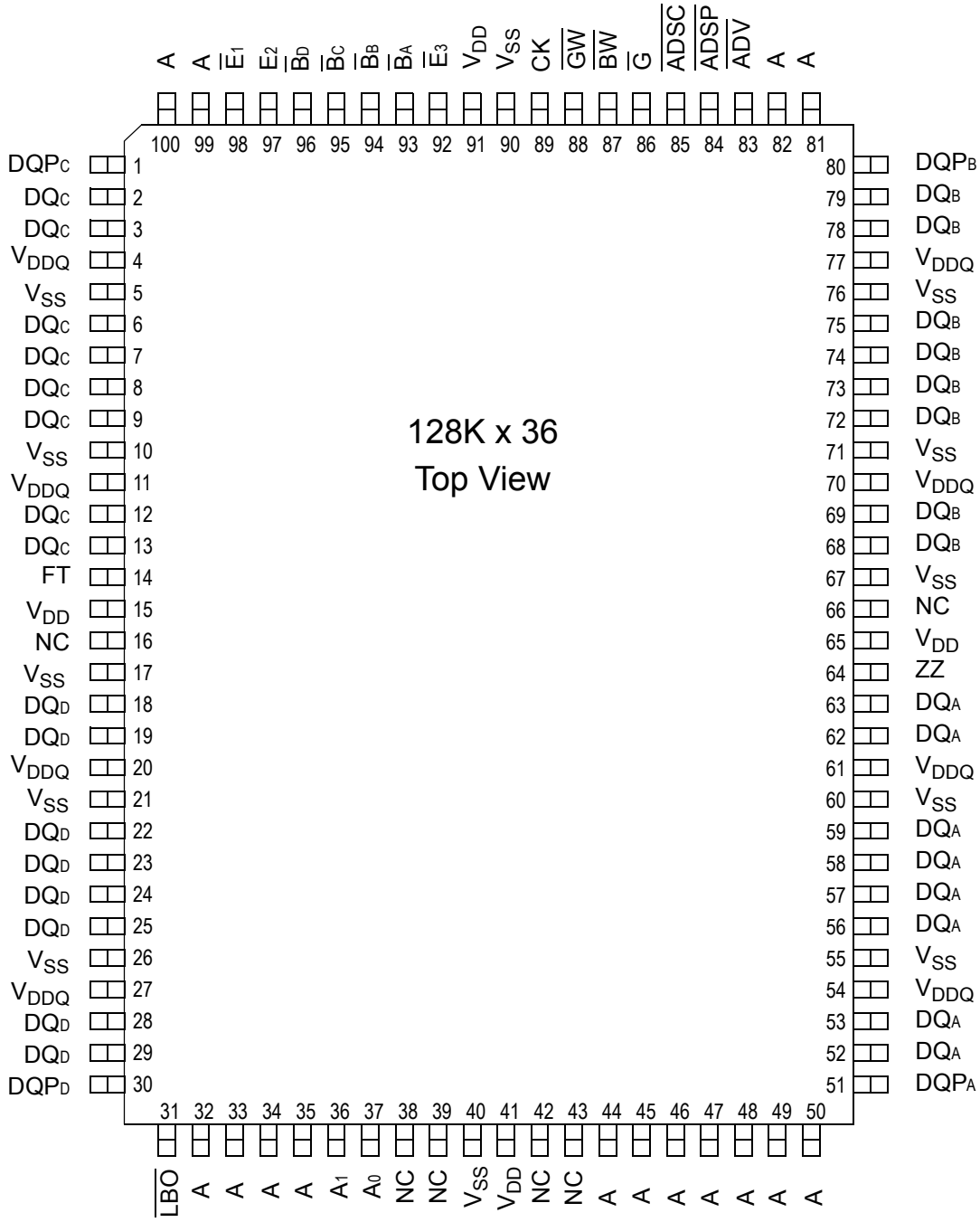
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GS840E32A 100-Pin TQFP Pinout (Package T)



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GS840E36A 100-Pin TQFP Pinout (Package T)



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TQFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/'s; active low
$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	-	No Connect

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GS840E18A Pad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	E	A	$\overline{ADSC}$	A	$\overline{E}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{E}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{B}_B$	$\overline{ADV}$	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{B}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A_1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A_0	V_{SS}	NC	DQ_A
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

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GS840E32A Pad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	E	A	$\overline{ADSC}$	A	$\overline{E}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	NC	V_{SS}	NC	V_{SS}	NC	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{E}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{G}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{B}_C$	$\overline{ADV}$	$\overline{B}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{B}_D$	NC	$\overline{B}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BW}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A_1	V_{SS}	DQ_A	DQ_A
P	DQ_D	NC	V_{SS}	A_0	V_{SS}	NC	DQ_A
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

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GS840E36APad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	E	A	$\overline{ADSC}$	A	$\overline{E}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{E}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{G}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{B}_C$	$\overline{ADV}$	$\overline{B}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{B}_D$	NC	$\overline{B}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BW}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A_1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A_0	V_{SS}	DQP_A	DQ_A
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

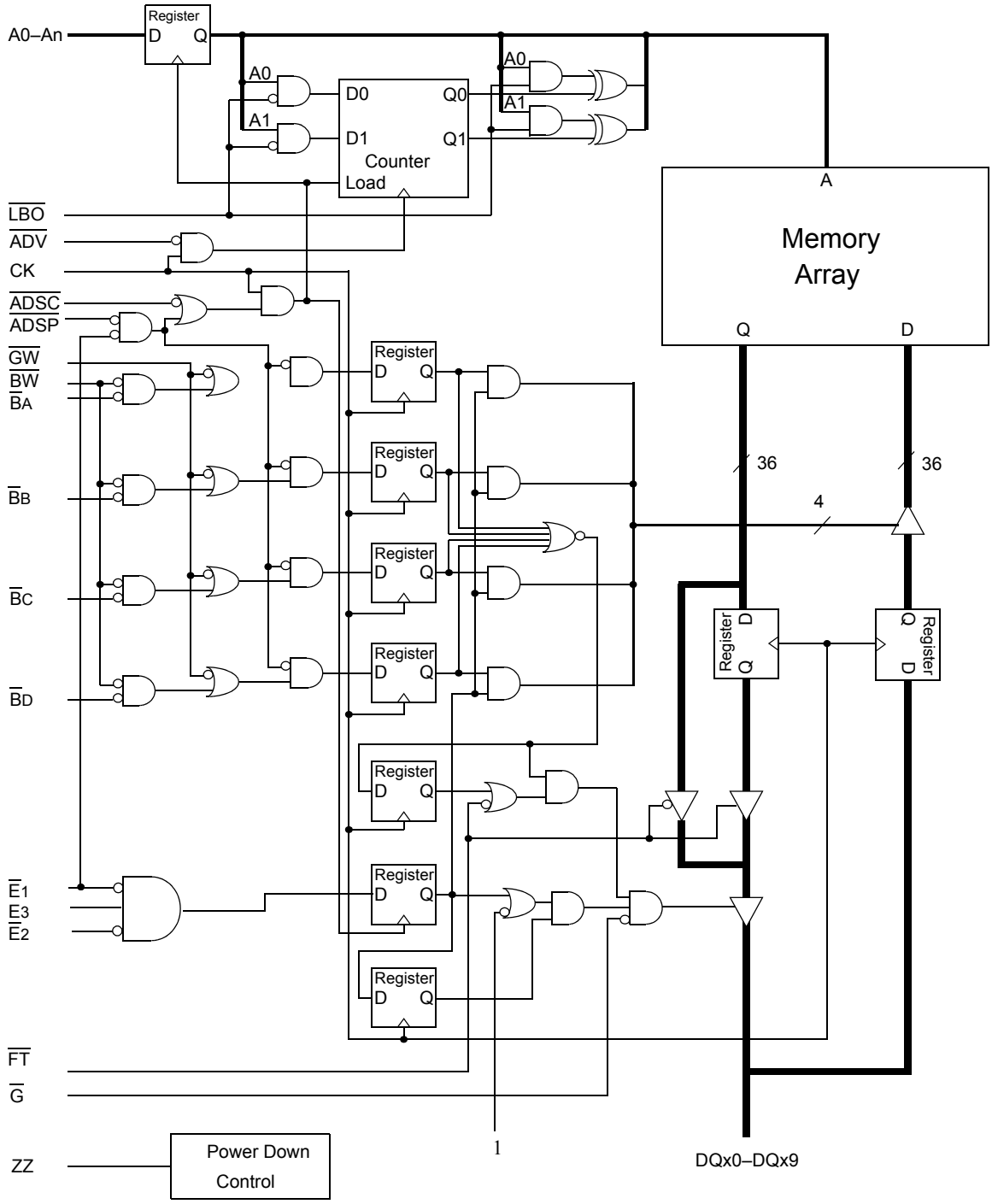
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BGA Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	—	No Connect

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GS840E18/32/36A Block Diagram



Note: Only x36 version shown for simplicity.

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Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There are pull-up devices on $\overline{LBO}$ and $\overline{FT}$ pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte A	H	L	L	H	H	H	2, 3
Write byte B	H	L	H	L	H	H	2, 3
Write byte C	H	L	H	H	L	H	2, 3, 4
Write byte D	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$ and/or $\overline{B_D}$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

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Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E}_1$	E^2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W^3	DQ^4
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

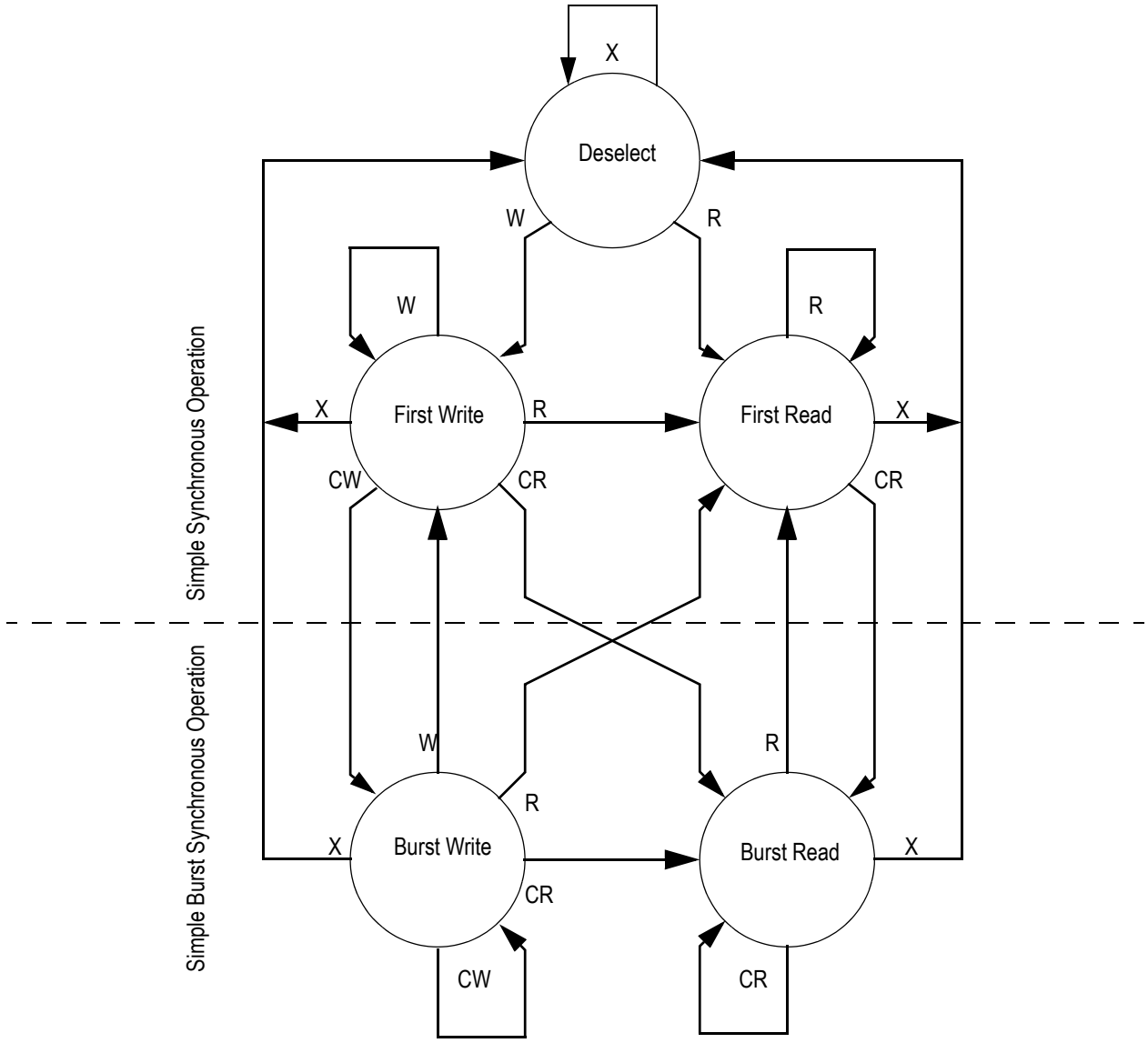
Notes:

1. X = Don't Care, H = High, L = Low.
2. E = T (True) if E_2 = 1 and $\overline{E}_3$ = 0; E = F (False) if E_2 = 0 or $\overline{E}_3$ = 1.
3. W = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying ADSP high and ADSC low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying ADSP high and ADV low while using ADSC to load new addresses allows simple burst operations. See *ITALIC* items above.

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Simplified State Diagram

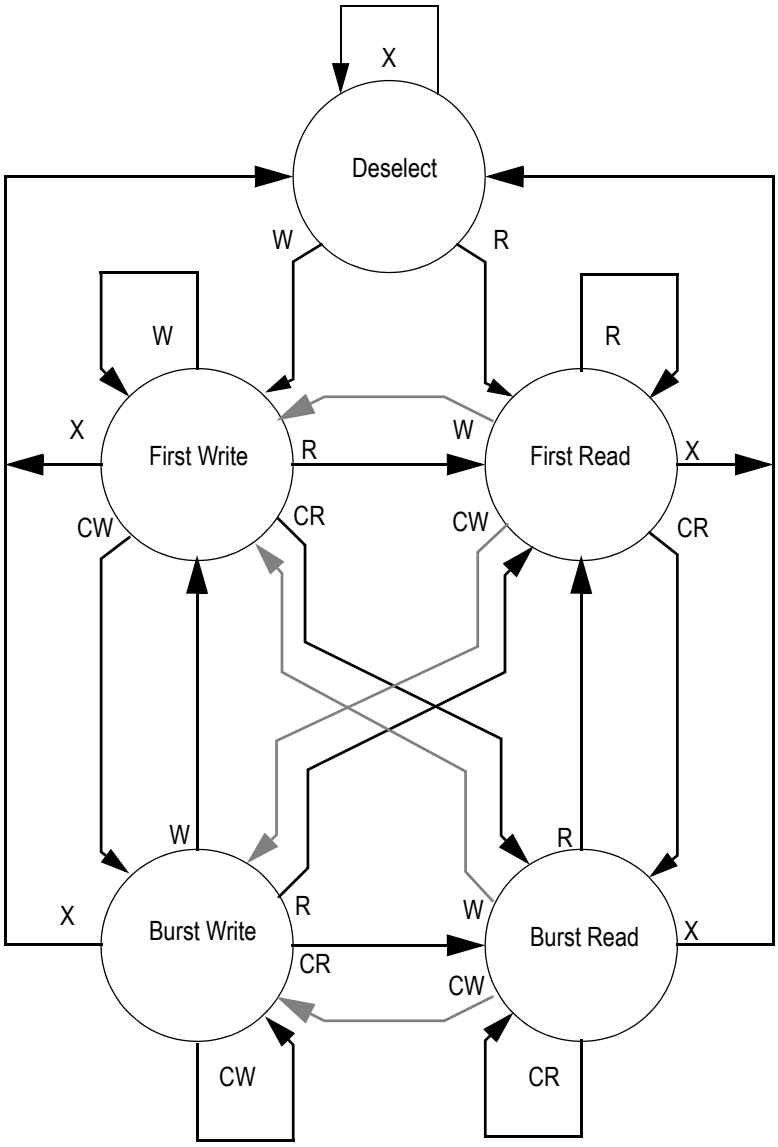


Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied Low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E}_1$, E_2, $\overline{E}_3$) and Write ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$, $\overline{BW}$ and $\overline{GW}$) control inputs and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

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Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

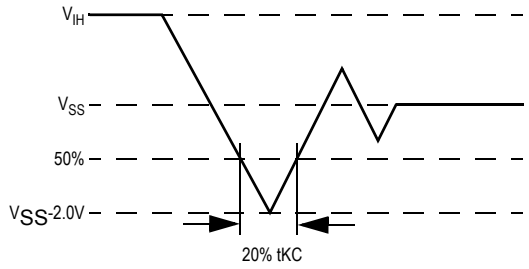
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	3

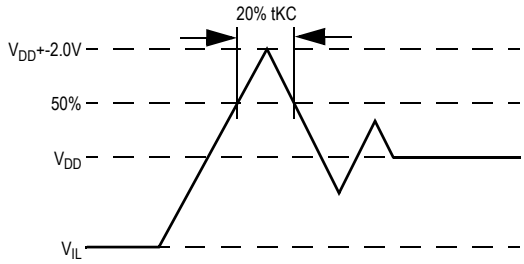
Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ V_{DDQ} ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ V_{DDQ} ≤ 3.135 V (i.e., 3.3 V I/O) and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < V_{DD}+2 V with a pulse width not to exceed 20% tKC.

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Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Control Input Capacitance	C_I	V_{DD} = 3.3 V	3	4	pF
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF

Note:
This parameter is sample tested.

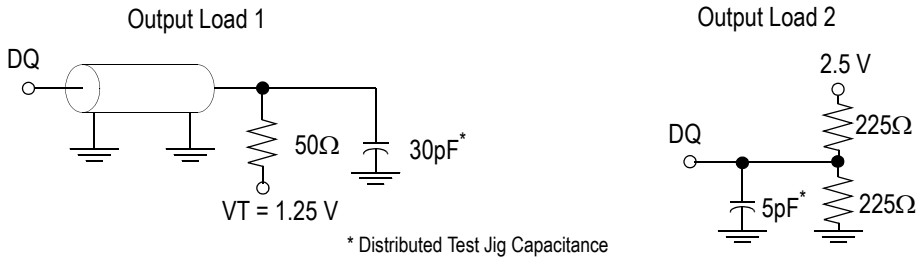
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AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.
4. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0V \leq V_{IN} \leq V_{IL}$	–300 uA –1uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375 V	1.7 V	
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135 V	2.4 V	
Output Low Voltage	V_{OL}	I_{OL} = 4 mA		0.4 V

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Operating Currents

Parameter	Test Conditions	Symbol	-190		-180		-166		-150		-100		Unit
			0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs ≥VIH or ≤ VIL Output open	IDD Pipeline	370	380	335	345	310	320	280	290	190	200	mA
		IDD Flow Through	245	255	210	220	190	200	165	175	135	145	mA
Standby Current	ZZ ≥ VDD – 0.2 V	ISB Pipeline	20	30	20	30	20	30	20	30	20	30	mA
		ISB Flow Through	20	30	20	30	20	30	20	30	20	30	mA
Deselect Current	Device Deselected; All other inputs ≥ VIH or ≤ VIL	IDD Pipeline	60	70	55	65	50	60	50	60	40	50	mA
		IDD Flow Through	45	55	40	50	40	50	35	45	35	45	mA

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AC Electrical Characteristics

	Parameter	Symbol	-190		-180		-166		-150		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	5.3	—	5.5	—	6.0	—	6.7	—	10	—	ns
	Clock to Output Valid	tKQ	—	3.0	—	3.0	—	3.5	—	3.8	—	4.5	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	8.5	—	9.0	—	10.0	—	12.0	—	15.0	—	ns
	Clock to Output Valid	tKQ	—	7.5	—	8.0	—	8.5	—	10.0	—	12.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.3	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	3.0	1.5	3.2	1.5	3.5	1.5	3.8	1.5	5	ns
	$\overline{G}$ to Output Valid	tOE	—	3.0	—	3.2	—	3.5	—	3.8	—	5	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	3.0	—	3.2	—	3.5	—	3.8	—	5	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	2.0	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

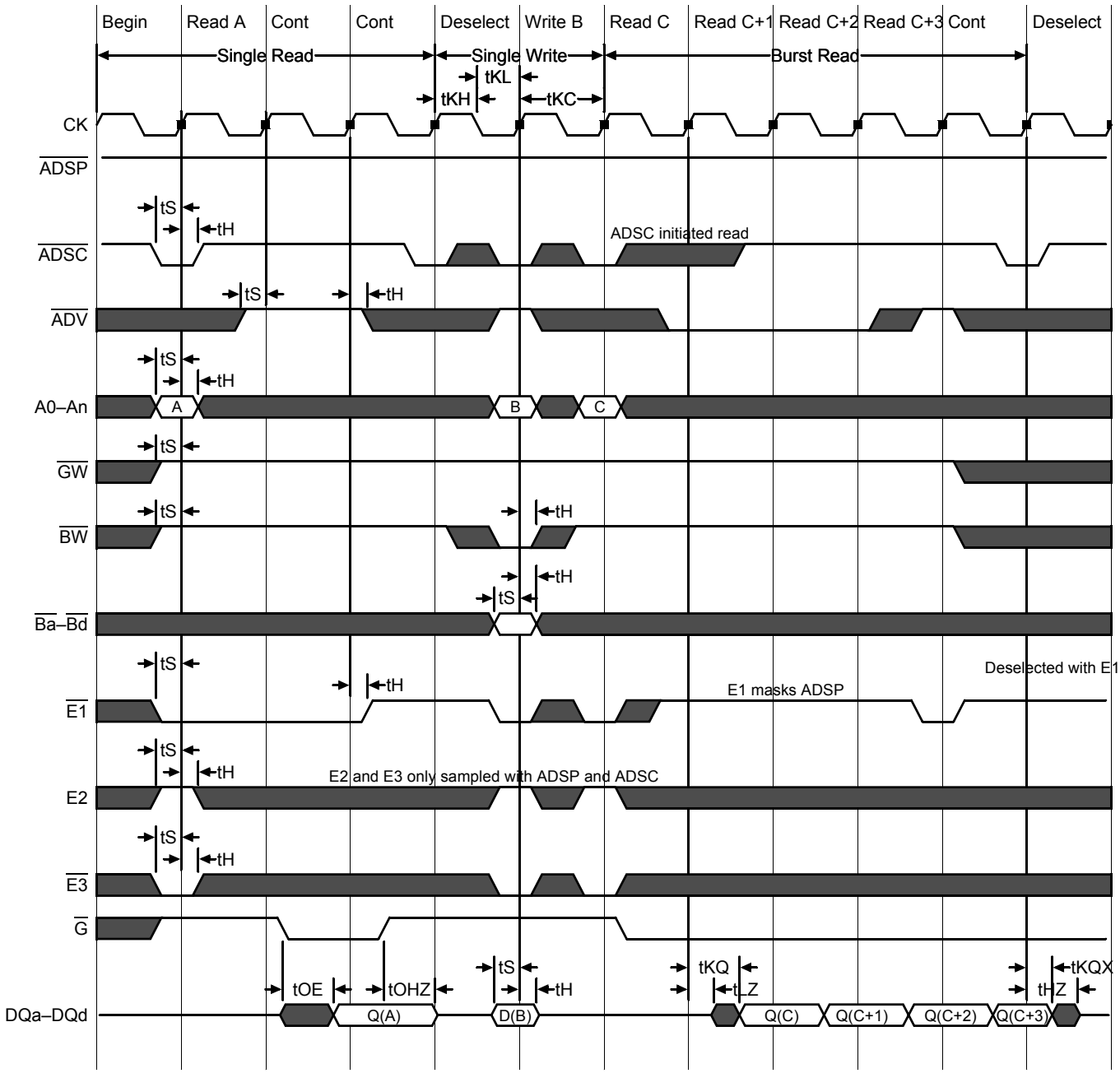
Notes:

1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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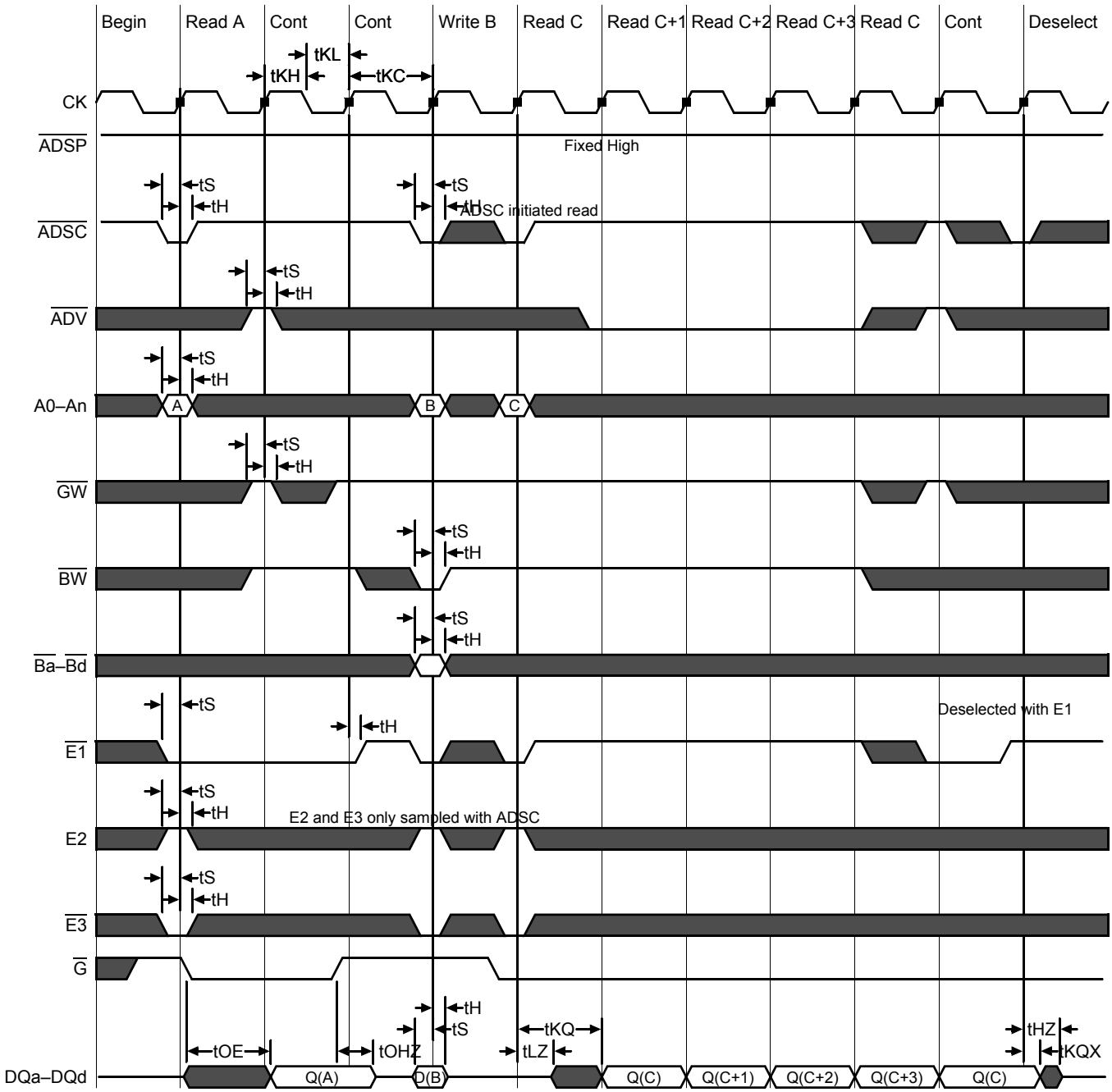
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Pipeline Mode Timing



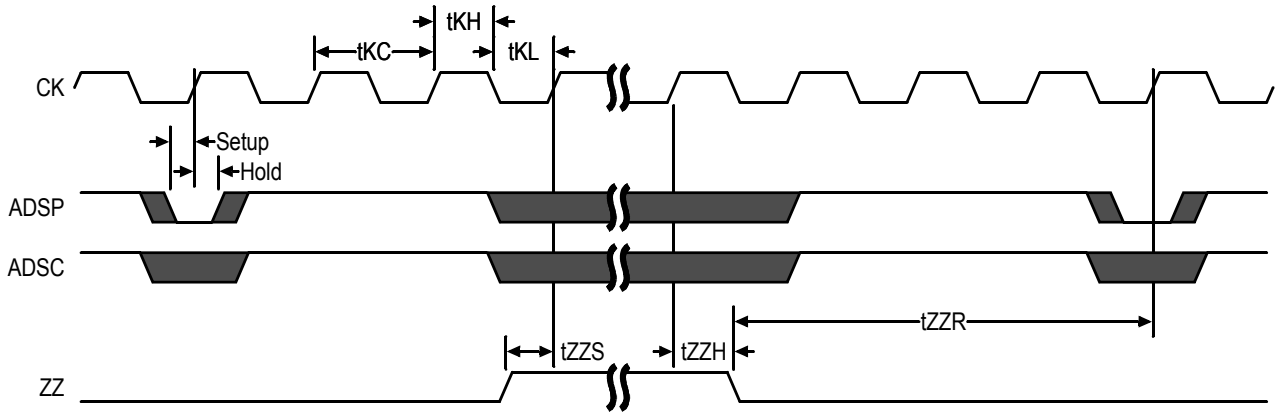
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Flow Through Mode Timing



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Sleep Mode Timing Diagram



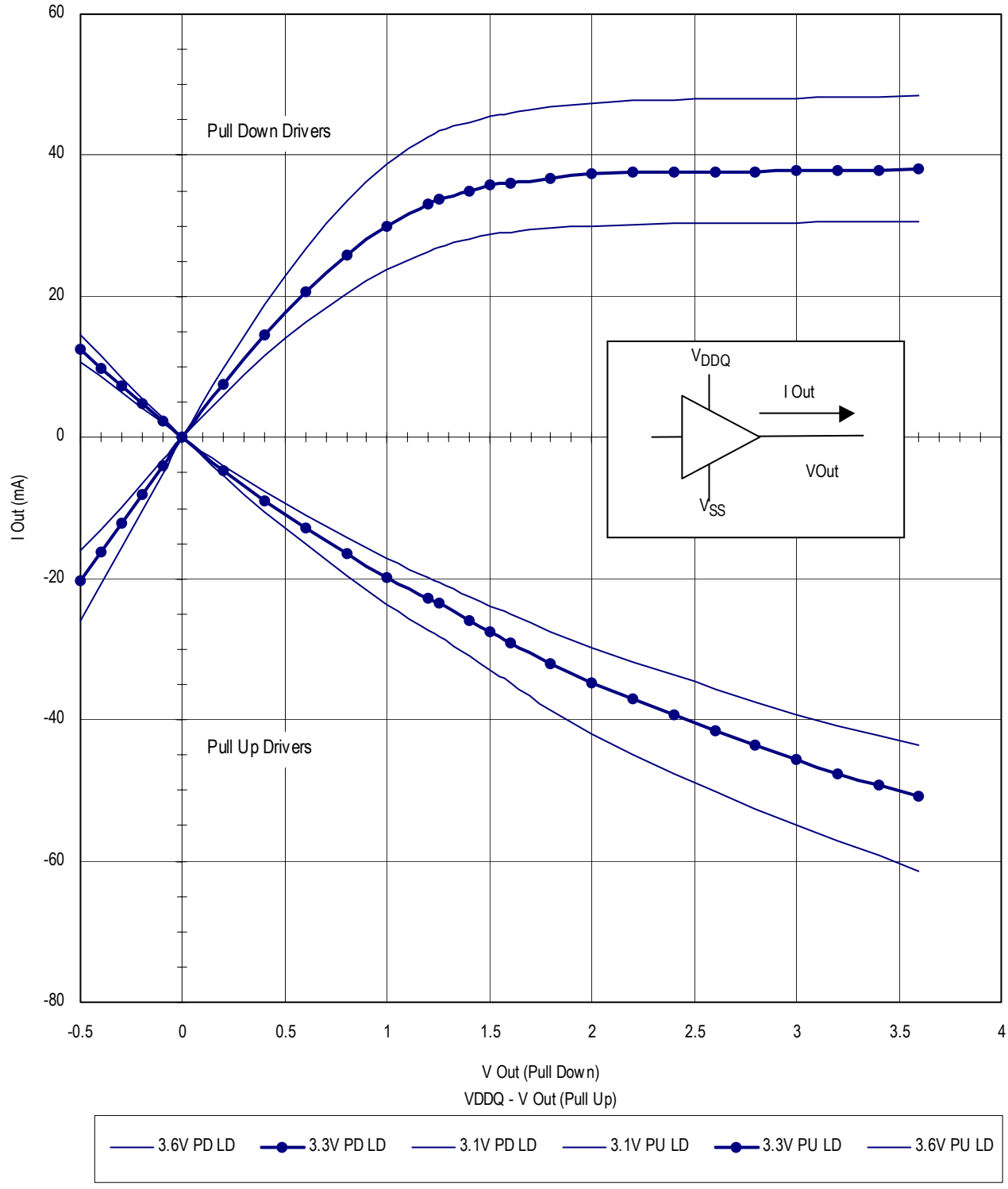
Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

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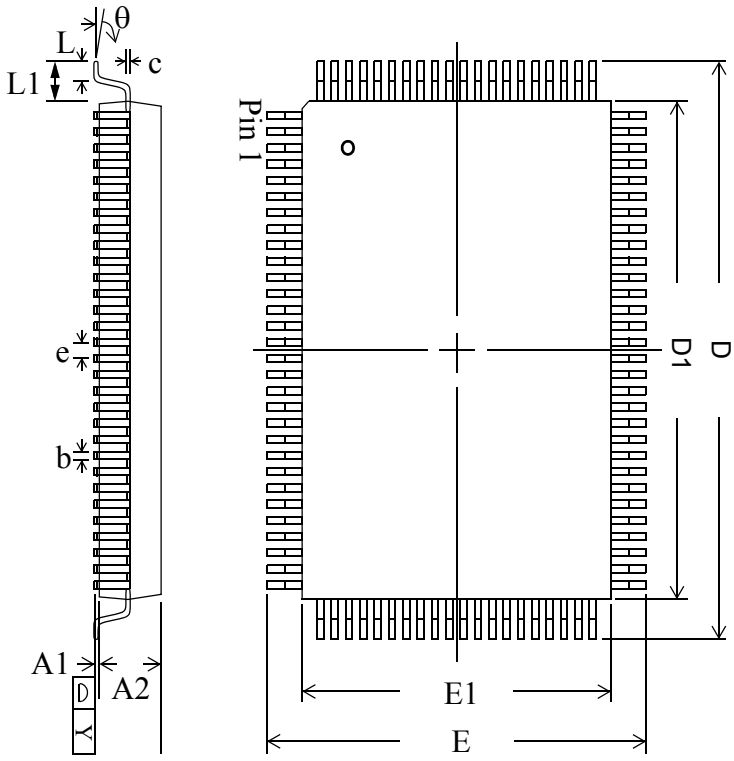
GS840E18/32/36A Output Driver Characteristics



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TQFP Package Drawing (Package T)

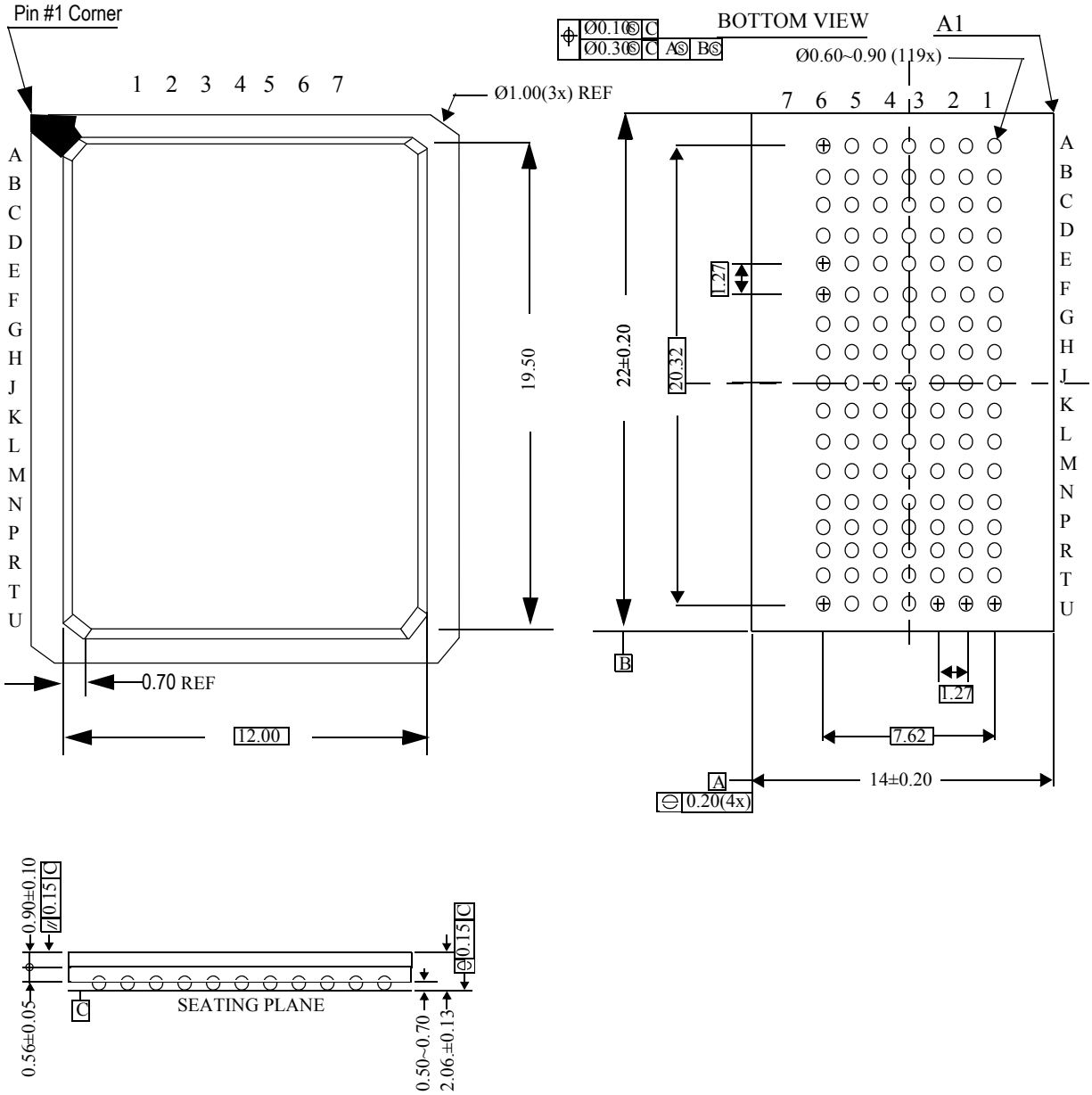
Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

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Package Dimensions—119-Bump FPBGA (Package B, Variation 1)



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Ordering Information for GSI Synchronous Burst RAMS

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
256K x 18	GS840E18AT-190	DCD Pipeline/Flow Through	TQFP	190/7.5	C	
256K x 18	GS840E18AT-180	DCD Pipeline/Flow Through	TQFP	180/8	C	
256K x 18	GS840E18AT-166	DCD Pipeline/Flow Through	TQFP	166/8.5	C	
256K x 18	GS840E18AT-150	DCD Pipeline/Flow Through	TQFP	150/10	C	
256K x 18	GS840E18AT-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
128K x 32	GS840E32AT-190	DCD Pipeline/Flow Through	TQFP	190/7.5	C	
128K x 32	GS840E32AT-180	DCD Pipeline/Flow Through	TQFP	180/8	C	
128K x 32	GS840E32AT-166	DCD Pipeline/Flow Through	TQFP	166/8.5	C	
128K x 32	GS840E32AT-150	DCD Pipeline/Flow Through	TQFP	150/10	C	
128K x 32	GS840E32AT-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
128K x 36	GS840E36AT-190	DCD Pipeline/Flow Through	TQFP	190/7.5	C	
128K x 36	GS840E36AT-180	DCD Pipeline/Flow Through	TQFP	180/8	C	
128K x 36	GS840E36AT-166	DCD Pipeline/Flow Through	TQFP	166/8.5	C	
128K x 36	GS840E36AT-150	DCD Pipeline/Flow Through	TQFP	150/10	C	
128K x 36	GS840E36AT-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
256K x 18	GS840E18AT-190I	DCD Pipeline/Flow Through	TQFP	190/7.5	I	
256K x 18	GS840E18AT-180I	DCD Pipeline/Flow Through	TQFP	180/8	I	
256K x 18	GS840E18AT-166I	DCD Pipeline/Flow Through	TQFP	166/8.5	I	
256K x 18	GS840E18AT-150I	DCD Pipeline/Flow Through	TQFP	150/10	C	
256K x 18	GS840E18AT-100I	DCD Pipeline/Flow Through	TQFP	100/12	C	
128K x 32	GS840E32AT-190I	DCD Pipeline/Flow Through	TQFP	190/7.5	I	
128K x 32	GS840E32AT-180I	DCD Pipeline/Flow Through	TQFP	180/8	I	
128K x 32	GS840E32AT-166I	DCD Pipeline/Flow Through	TQFP	166/8.5	I	
128K x 32	GS840E32AT-150I	DCD Pipeline/Flow Through	TQFP	150/10	C	
128K x 32	GS840E32AT-100I	DCD Pipeline/Flow Through	TQFP	100/12	C	
128K x 36	GS840E36AT-190I	DCD Pipeline/Flow Through	TQFP	190/7.5	I	
128K x 36	GS840E36AT-180I	DCD Pipeline/Flow Through	TQFP	180/8	I	
128K x 36	GS840E36AT-166I	DCD Pipeline/Flow Through	TQFP	166/8.5	I	
128K x 36	GS840E36AT-150I	DCD Pipeline/Flow Through	TQFP	150/10	C	
128K x 36	GS840E36AT-100I	DCD Pipeline/Flow Through	TQFP	100/12	C	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS840E32AT-8T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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Ordering Information for GSI Synchronous Burst RAMS (Continued)

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
256K x 18	GS840E18AGT-190	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	C	
256K x 18	GS840E18AGT-180	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	C	
256K x 18	GS840E18AGT-166	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	C	
256K x 18	GS840E18AGT-150	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
256K x 18	GS840E18AGT-100	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
128K x 32	GS840E32AGT-190	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	C	
128K x 32	GS840E32AGT-180	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	C	
128K x 32	GS840E32AGT-166	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	C	
128K x 32	GS840E32AGT-150	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
128K x 32	GS840E32AGT-100	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
128K x 36	GS840E36AGT-190	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	C	
128K x 36	GS840E36AGT-180	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	C	
128K x 36	GS840E36AGT-166	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	C	
128K x 36	GS840E36AGT-150	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
128K x 36	GS840E36AGT-100	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
256K x 18	GS840E18AGT-190I	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	I	
256K x 18	GS840E18AGT-180I	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	I	
256K x 18	GS840E18AGT-166I	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	I	
256K x 18	GS840E18AGT-150I	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
256K x 18	GS840E18AGT-100I	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
128K x 32	GS840E32AGT-190I	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	I	
128K x 32	GS840E32AGT-180I	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	I	
128K x 32	GS840E32AGT-166I	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	I	
128K x 32	GS840E32AGT-150I	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
128K x 32	GS840E32AGT-100I	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
128K x 36	GS840E36AGT-190I	DCD Pipeline/Flow Through	Pb-free TQFP	190/7.5	I	
128K x 36	GS840E36AGT-180I	DCD Pipeline/Flow Through	Pb-free TQFP	180/8	I	
128K x 36	GS840E36AGT-166I	DCD Pipeline/Flow Through	Pb-free TQFP	166/8.5	I	
128K x 36	GS840E36AGT-150I	DCD Pipeline/Flow Through	Pb-free TQFP	150/10	C	
128K x 36	GS840E36AGT-100I	DCD Pipeline/Flow Through	Pb-free TQFP	100/12	C	
256K x 18	GS840E18AB-190	DCD Pipeline/Flow Through	119 BGA (var. 1)	190/7.5	C	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS840E32AT-8T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
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Ordering Information for GSI Synchronous Burst RAMS (Continued)

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
256K x 18	GS840E18AB-180	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	C	
256K x 18	GS840E18AB-166	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	C	
256K x 18	GS840E18AB-150	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
256K x 18	GS840E18AB-100	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	
128K x 32	GS840E32AB-190	DCD Pipeline/Flow Through	119 BGA (var. 1)	190/7.5	C	
128K x 32	GS840E32AB-180	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	C	
128K x 32	GS840E32AB-166	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	C	
128K x 32	GS840E32AB-150	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
128K x 32	GS840E32AB-100	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	
128K x 36	GS840E36AB-190	DCD Pipeline/Flow Through	119 BGA (var. 1)	190/7.5	C	
128K x 36	GS840E36AB-180	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	C	
128K x 36	GS840E36AB-166	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	C	
128K x 36	GS840E36AB-150	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
128K x 36	GS840E36AB-100	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	
256K x 18	GS840E18AB-190I	DCD Pipeline/Flow Through	119 BGA (var. 1)	190/7.5	I	
256K x 18	GS840E18AB-180I	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	I	
256K x 18	GS840E18AB-166I	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	I	
256K x 18	GS840E18AB-150I	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
256K x 18	GS840E18AB-100I	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	
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128K x 32	GS840E32AB-180I	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	I	
128K x 32	GS840E32AB-166I	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	I	
128K x 32	GS840E32AB-150I	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
128K x 32	GS840E32AB-100I	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	
128K x 36	GS840E36AB-190I	DCD Pipeline/Flow Through	119 BGA (var. 1)	190/7.5	I	
128K x 36	GS840E36AB-180I	DCD Pipeline/Flow Through	119 BGA (var. 1)	180/8	I	
128K x 36	GS840E36AB-166I	DCD Pipeline/Flow Through	119 BGA (var. 1)	166/8.5	I	
128K x 36	GS840E36AB-150I	DCD Pipeline/Flow Through	119 BGA (var. 1)	150/10	C	
128K x 36	GS840E36AB-100I	DCD Pipeline/Flow Through	119 BGA (var. 1)	100/12	C	

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4Mb Burst SRAM Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page /Revisions;Reason
GS840E18/32/36 Rev 1.02c 5/ 1999; GS840E18/32/36 2.00 8/1999D	Format/Typos	• Document/Continued changing to new format.
	Content	• Added Fine Pitch BGA Package.
GS840E18/32/362.00 8/ 1999;GS840E18/32/362.01 9/ 1999E	Format/Typos	• Took “E” out of 840HE...in Core and Interface Voltages. • Pin outs/New small caps format. • Timing Diagrams/New format. • Block Diagrams/New small caps format.
	Content	• Pin outs/x32 & x36 TQFP/Changed pin 72 from DQA3 to DQB3. • Pin Description/Rearranged Address Inputs to match order on TQFP Pinout. • TQFP Package Diagram/Corrected Dimension D Max from 20.1 to 22.1.
GS840E18/32/362.01 9/ 1999E;GS840E18/32/362.02		• Took out Fine Pitch BGA Package. Package change in progress.
GS840E18/32/362.0210-11/ 1999;GS840E18/32/362.032/ 2000G	Format	• New GSI Logo • Took “Pin” out of heading for consistency.
GS840E18/32/362.032/2000G; 840E18_r1_04	Content	• Updated pin description table
840E18_r1_04; 840E18_r1_05	Content	• Updated BGA pin description table to meet JEDEC standard
840E18A_r1_05; 840E18A_r1_06	Content/Format	• Added “non-A” speed bins to Operating Currents table, AC Electrical Characteristics table, and Ordering Information table • Updated format to fit Technical Documentation standards
840E18A_r1_06; 840E18A_r1_07	Content/Format	• Updated table on page 1 • Updated Operating Currents table on page 18 • Updated Electrical Characteristics table on page 19 • Updated format to comply with present Technical Documentation standards • Corrected typos in revision history table on page 31
840E18A_r1_07, 840E18A_r1_08	Content	• Reduced I_{DD} by 20 mA in table on page 1 and Operating Currents table
840E18A_r1_08, 840E18A_r1_09	Content	• Removed 200 MHz references from entire datasheet
840E18A_r1_09, 840E18A_r1_10	Content	• Updated format • Added 190 MHz speed bin

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4Mb Burst SRAM Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page /Revisions;Reason
840E18A_r1_10, 840E18A_r1_11	Content	• Updated entire format • Corrected current numbers to match NBT parts • Removed Preliminary banner
840E18A_r1_11, 840E18A_r1_12	Content	• Added Pb-free TQFP information • Added variation number to 119 BGA information

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