

# FQA13N80\_F109

## N-Channel QFET® MOSFET

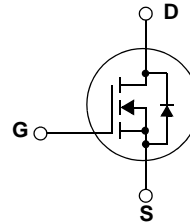
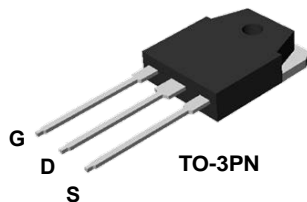
### 800 V, 12.6 A, 750 mΩ

#### Features

- 12.6 A, 800 V,  $R_{DS(on)} = 750 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$   
 $I_D = 6.8 \text{ A}$
- Low Gate Charge (Typ. 68 nC)
- Low Crss (Typ. 30 pF)
- 100% Avalanche Tested

#### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



#### Absolute Maximum Ratings

Symbol	Parameter	FQA13N80_F109	Unit
$V_{DSS}$	Drain-Source Voltage	800	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	12.6	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	8.0	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	50.4	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1100	mJ
$I_{AR}$	Avalanche Current (Note 1)	12.6	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	30	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	300	W
	- Derate above $25^\circ\text{C}$	2.38	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FQA13N80_F109	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQA13N80	FQA13N80_F109	TO-3PN	--	--	30

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

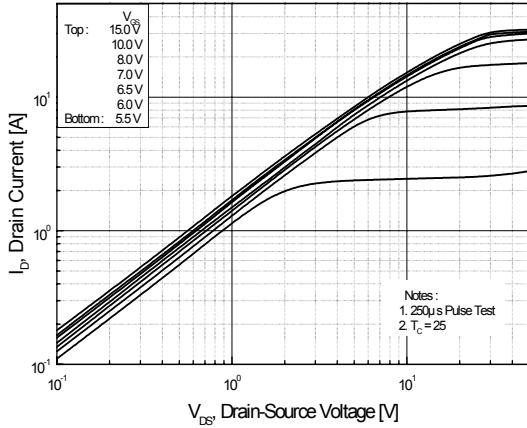
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	800	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.95	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 640 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.3A	--	0.58	0.75	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 6.3A (Note 4)	--	13	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	2700	3500	pF
C <sub>oss</sub>	Output Capacitance		--	275	360	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	30	39	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 12.6A, R <sub>G</sub> = 25 Ω  (Note 4, 5)	--	60	130	ns
t <sub>r</sub>	Turn-On Rise Time		--	150	310	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	155	320	ns
t <sub>f</sub>	Turn-Off Fall Time		--	110	230	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 640 V, I <sub>D</sub> = 12.6A, V <sub>GS</sub> = 10 V  (Note 4, 5)	--	68	88	nC
Q <sub>gs</sub>	Gate-Source Charge		--	15	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	32	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	12.6	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	50.4	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 12.6A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 12.6 A, dI <sub>F</sub> / dt = 100 A/μs  (Note 4)	--	850	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	11.3	--	μC

### NOTES:

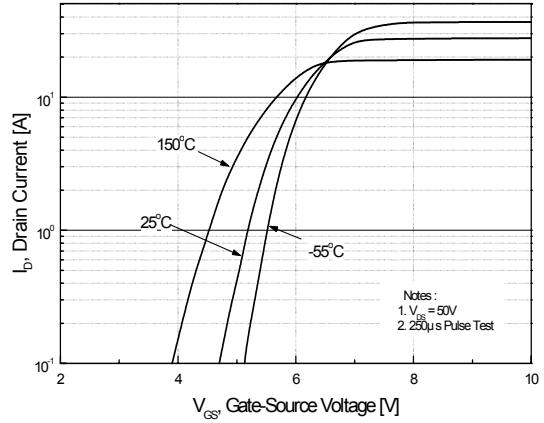
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 13mH, I<sub>AS</sub> = 12.6A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 12.6A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Performance Characteristics

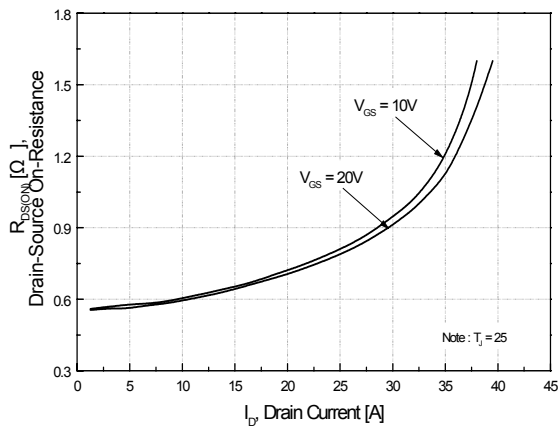
**Figure 1. On-Region Characteristics**



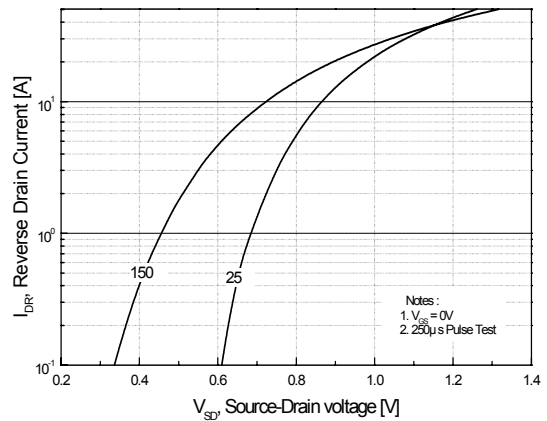
**Figure 2. Transfer Characteristics**



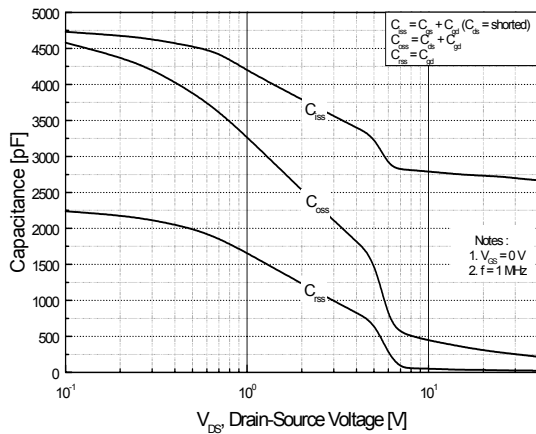
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



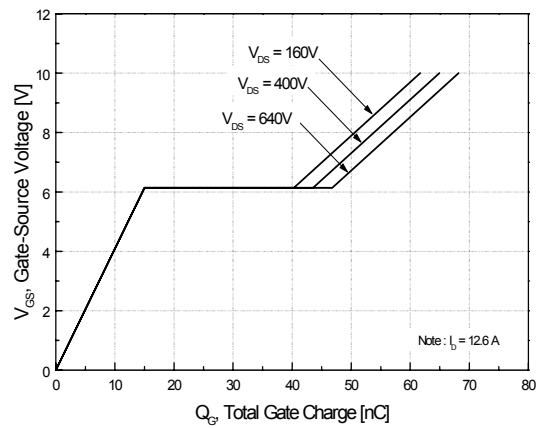
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

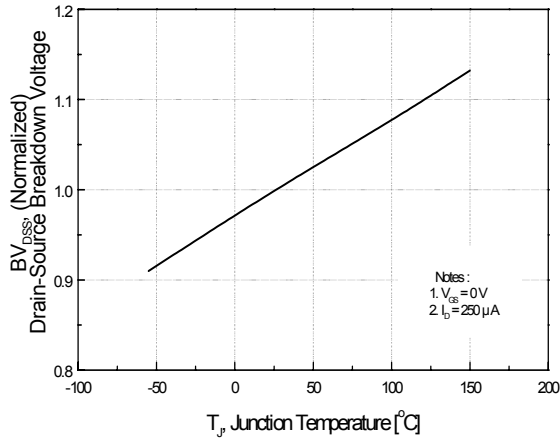


**Figure 6. Gate Charge Characteristics**

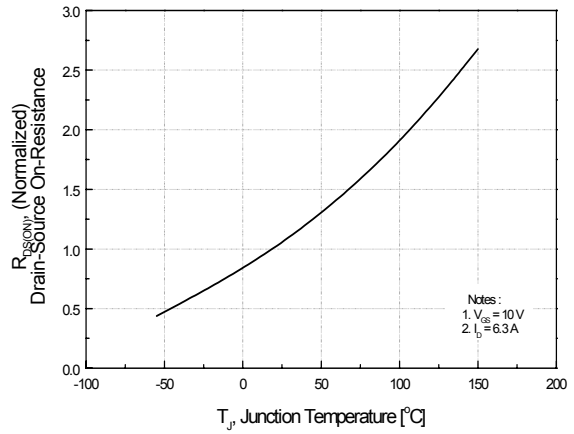


**Typical Performance Characteristics** (Continued)

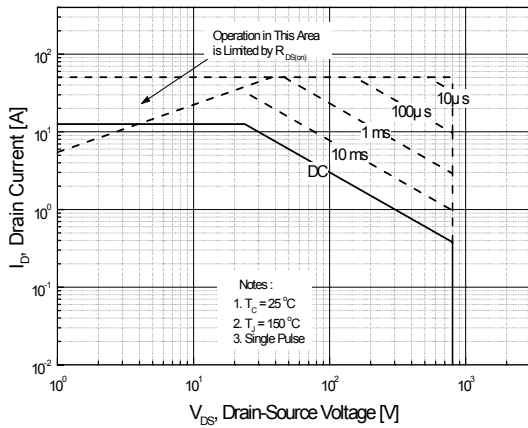
**Figure 7. Breakdown Voltage Variation vs. Temperature**



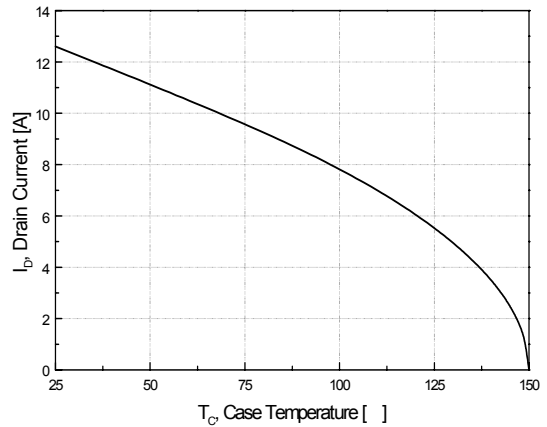
**Figure 8. On-Resistance Variation vs. Temperature**



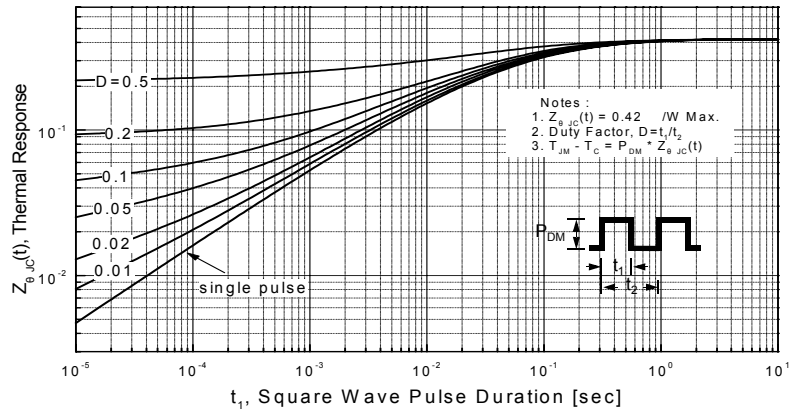
**Figure 9. Maximum Safe Operating Area**



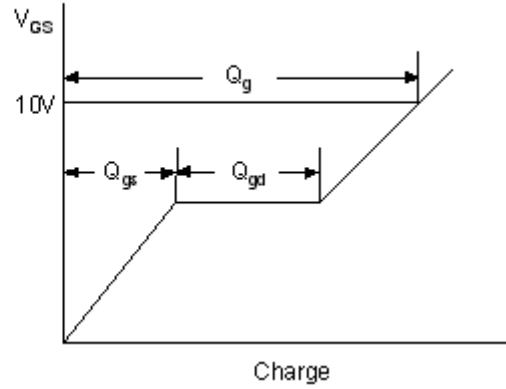
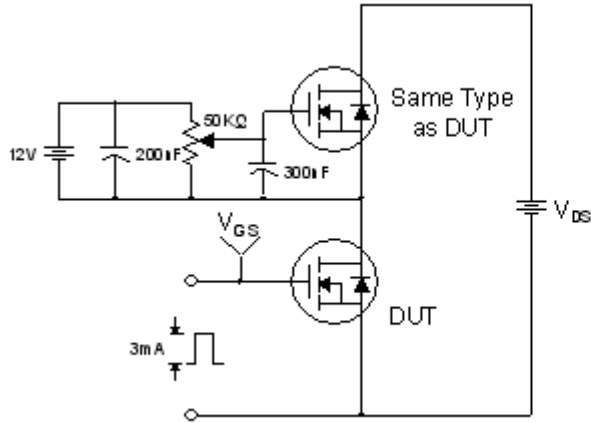
**Figure 10. Maximum Drain Current vs. Case Temperature**



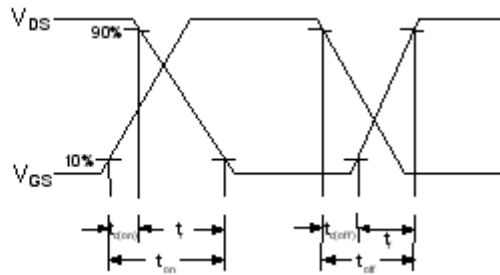
**Figure 11. Transient Thermal Response Curve**



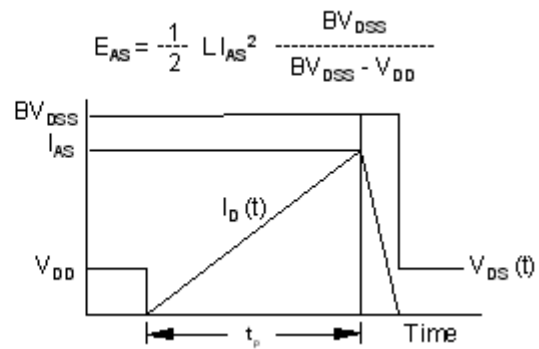
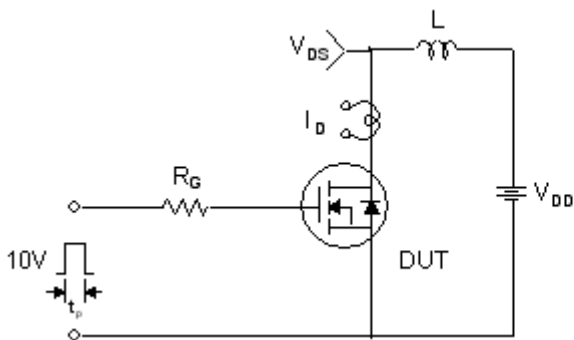
**Gate Charge Test Circuit & Waveform**



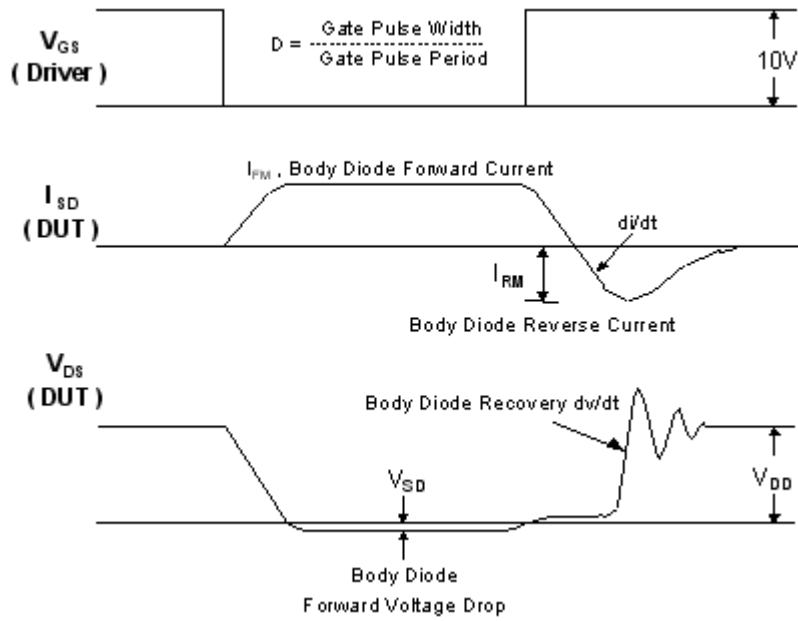
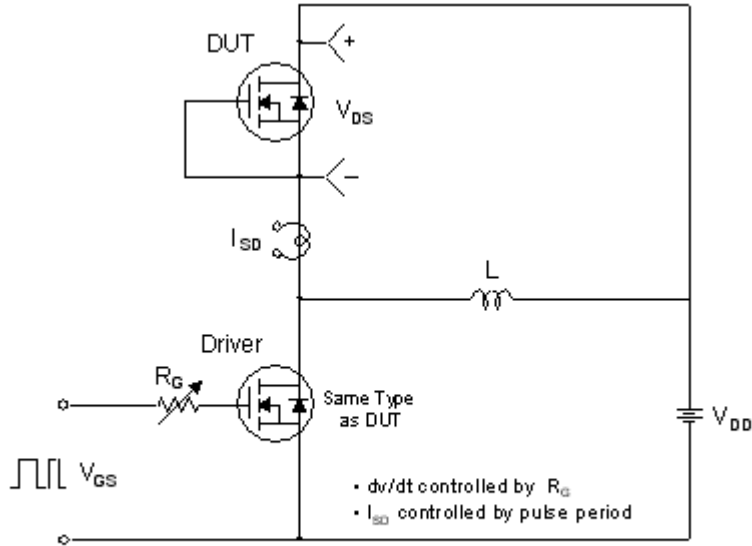
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

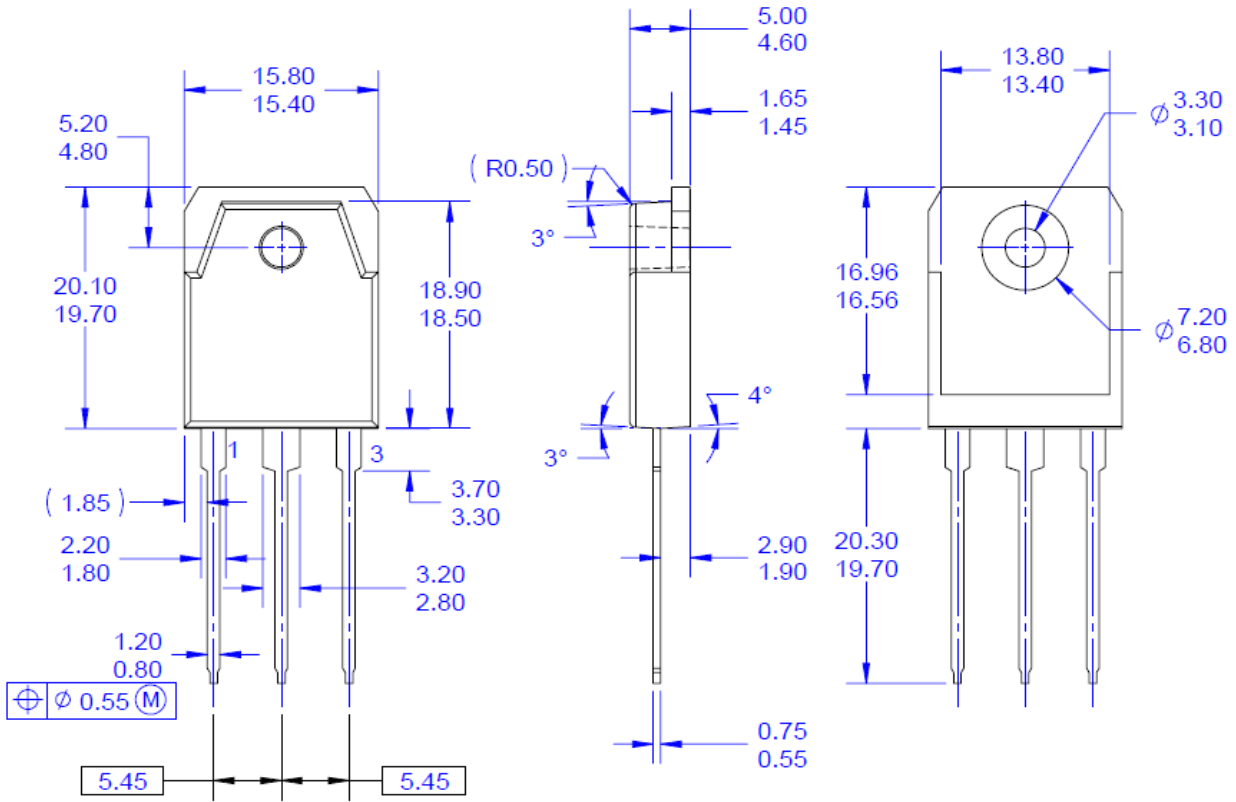


Peak Diode Recovery dv/dt Test Circuit & Waveforms



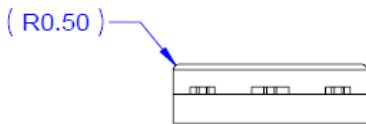
**Mechanical Dimensions**

**TO-3PN**



NOTES: UNLESS OTHERWISE SPECIFIED

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Dimensions in Millimeters



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Rev. 164





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