DDR SDRAM Module 128Mbyte (16Mx64bit), based on16Mx8,4Banks, 4K Ref., DIMM, Part No. HDD16M64D8W

GENERAL DESCRIPTION

The HANBiT HDD16M64D8W is 16M bit x 64 Double Data Rate SDRAM high density memory modules. The HANBiT HDD16M64D8W consists of eight CMOS 16M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD16M64D8W is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

• Part Identification

HDD16M64D8W – 10A : 100MHz (CL=2)

HDD16M64D8W – 13A : 133MHz (CL=2)

HDD16M64D8W – 13B : 133MHz (CL=2.5)

• Power supply : V_{DD}: 2.5V ± 0.2V, V_{DDQ}: 2.5V ± 0.2V
• Double-data-rate architecture; two data transfers per clock cycle
• Bidirectional data strobe(DQS)
• Differential clock inputs(CK and CK)
• DLL aligns DQ and DQS transition with CK transition
• Programmable Read latency 2, 2.5 (clock)
• Programmable Burst length (2, 4, 8)
• Programmable Burst type (sequential & interleave)
• Edge aligned data output, center aligned data input
• Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
• Serial presence detect with EEPROM
• PCB : **Height 1250 mi**l, double sided component

PIN ASSIGNMENT

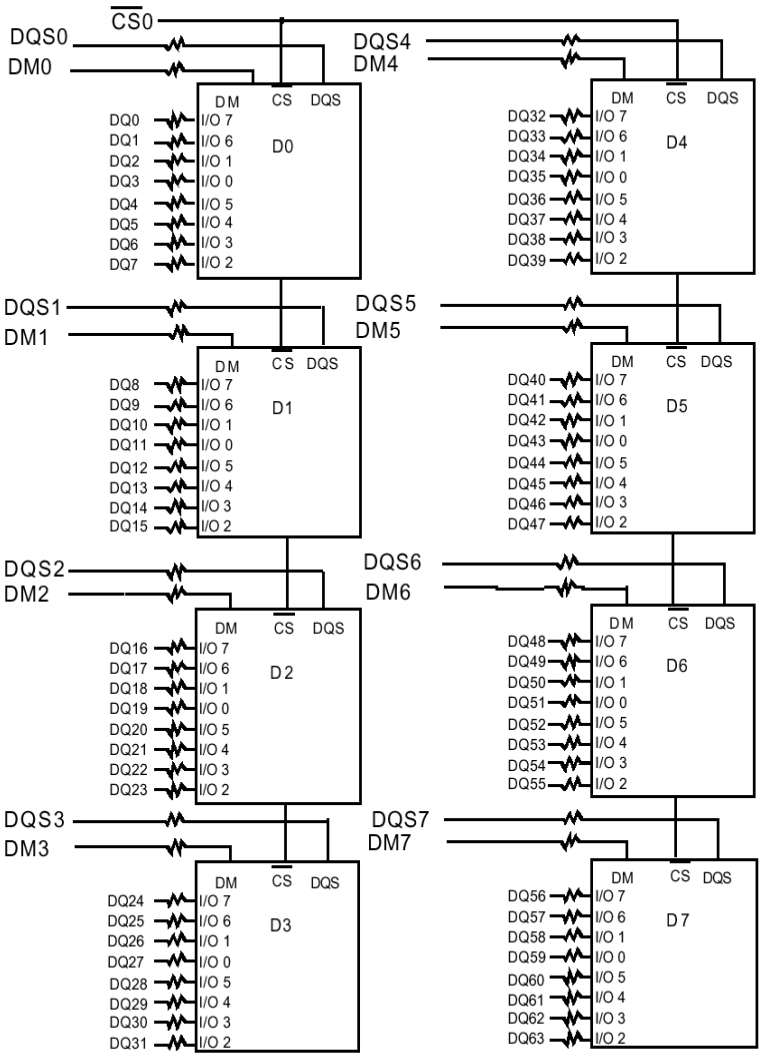
P1						P2					
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	VREF	35	DQ25	69	DQ43	103	NC	138	/CK0	172	VDDQ
2	DQ1	36	DQS3	70	VDD	104	VDDQ	139	VSS	173	NC
3	VSS	37	A4	71	*/CS2	105	DQ12	140	*DM8	174	DQ60
4	DQ1	38	VDD	72	DQ48	106	DQ13	141	A10	175	DQ61
5	DQS0	39	DQ26	73	DQ49	107	DM1	142	*CB6	176	VSS
6	DQ2	40	DQ27	74	VSS	108	VDD	143	VDDQ	177	DM7
7	VDD	41	A2	75	/CK2	109	DQ14	144	*CB7	178	DQ62
8	DQ3	42	VSS	76	CK2	110	DQ15	145	VSS	179	DQ63
9	NC	43	A1	77	VDDQ	111	DM1	146	DQ36	180	VDDQ
10	NC	44	*CB0	78	DQS6	112	VDDQ	147	DQ37	181	SA0
11	VSS	45	*CB1	79	DQ50	113	*BA2	148	VDD	182	SA1
12	DQ8	46	VDD	80	DQ51	114	DQ20	149	DM4	183	SA2
13	DQ9	47	*DQS8	81	VSS	115	*A12	150	DQ38	184	VDDSPD
14	DQS1	48	A0	82	VDDID	116	VSS	151	DQ39		
15	VDDQ	49	*CB2	83	DQ56	117	DQ21	152	VSS		
16	CK1	50	VSS	84	DQ57	118	A11	153	DQ44		
17	/CK1	51	*CB3	85	VDD	119	DM2	154	/RAS		
18	VSS	52	BA1	86	DQS7	120	VDD	155	DQ45		
19	DQ10	53	DQ32	87	DQ58	121	DQ22	156	VDDQ		
20	DQ11	54	VDDQ	88	DQ59	122	A8	157	/CS0		
21	CKE0	55	DQ33	89	VSS	123	DQ23	158	*/CS1		
22	VDDQ	56	DQS4	90	NC	124	VSS	159	DM5		
23	DQ16	57	DQ34	91	SDA	125	A6	160	VSS		
24	DQ17	58	VSS	92	SCL	126	DQ28	161	DQ46		
25	DQS2	59	BA0	93	VSS	127	DQ29	162	DQ47		
26	VSS	60	DQ35	94	DQ4	128	VDDQ	163	*/CS3		
27	A9	61	DQ40	95	DQ5	129	DM3	164	VDDQ		
28	DQ18	62	VDDQ	96	VDDQ	131	A3	165	DQ52		
29	A7	63	/WE	97	DM0	132	VSS	166	DQ53		
30	VDDQ	64	DQ41	98	DQ6	133	DQ31	167	*A13		
31	DQ19	65	/CAS	99	DQ7	134	*CB4	168	VDD		
32	A5	66	VSS	100	VSS	135	*CB5	169	DM6		
33	DQ24	67	DQS5	101	NC	136	VDDQ	170	DQ54		
34	VSS	68	DQ42	102	NC	137	CK0	171	DQ55		

* These pins should be NC in the system which does not support SPD

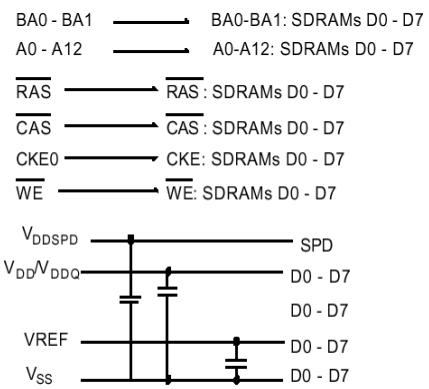
PIN	PIN DESCRIPTION	PIN	PIN DESCRIPTION
A0~A12	Address input	VDD	Power supply(2.5V)
BA0~BA1	Bank Select Address	VDDQ	Power supply for DQs(2.5V)
DQ0~DQ63	Data input/output	VREF	Power supply for reference
CB0~CB7	Check bit(Data input/output)	VDDSPD	Serial EEPROM Power supply(3.3)
DQS0~DQS7	Data Strobe input/output	VSS	Ground
DM0~DM7	Data-in Mask	SA0~SA2	Address in EEPROM
CK0~CK2,/CK0~/CK2	Clock input	SDA	Serial data I/O
CKE0	Clock enable input	SCL	Serial clock
/CS0	Chip Select input	/WE	Write enable
/RAS	Row Address strobe	VDDID	VDD indentification flag

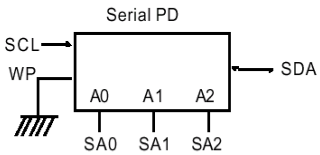
/CAS	Column Address strobe	NC	No connection

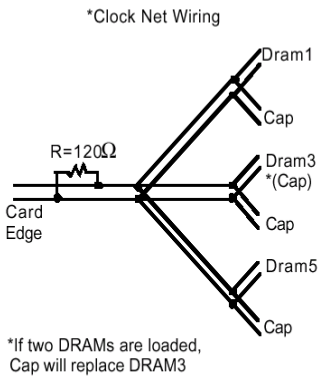
FUNCTIONAL BLOCK DIAGRAM



* Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs
CK1/CK1	3 SDRAMs
CK2/CK2	3 SDRAMs







Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNTE
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8.0	W
Short circuit current	I_{OS}	50	mA

Notes: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	V_{DDQ}/2-50mV	V_{DDQ}/2+50mV	V	1
I/O Termination Voltage(system)	V_{TT}	V_{REF} – 0.04	V_{REF} + 0.04	V	2
Input High Voltage	V_{IH} (DC)	V_{REF} + 0.15	V_{REF} + 0.3	V	4
Input Low Voltage	V_{IL} (DC)	-0.3	V_{REF} - 0.15	V	4
Input Voltage Level, CK and /CK inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Differential Voltage, CK and /CK inputs	V_{ID} (DC)	0.3	V_{DDQ} + 0.6	V	3
Input crossing point voltage, CK and CK inputs	V_{Ix} (DC)	1.15	1.35	V	5
Input leakage current	I_{LI}	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High current (V_{OUT} = 1.95V)	I_{OH}	-16.8		mA	
Output Low current (V_{OUT} = 0.35V)	I_{OL}	16.8		mA	
Output High Current(Half strengh driver)	I_{OH}	-9		mA	
Output High Current(Half strengh driver)	I_{OL}	9		mA	

Notes

1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of £ 3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.
6. These characterictics obey the SSTL-2 class II standards.

DDR SDRAM IDD SPEC TABLE

SYMBOL		B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	UNIT	NOTE
IDD0		840	760	760	mA	
IDD1		1040	960	960	mA	
IDD2P		28	24	24	mA	
IDD2F		200	176	176	mA	
IDD2Q		144	120	120	mA	
IDD3P		280	280	280	mA	
IDD3N		440	440	440	mA	
IDD4R		1280	1136	1136	mA	
IDD4W		1216	1040	1040	mA	
IDD5		1480	1480	1480	mA	
IDD6	Normal	16	16	16	mA	
	Low power	8	8	8	mA	Optional
IDD7A		2640	2400	2400	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

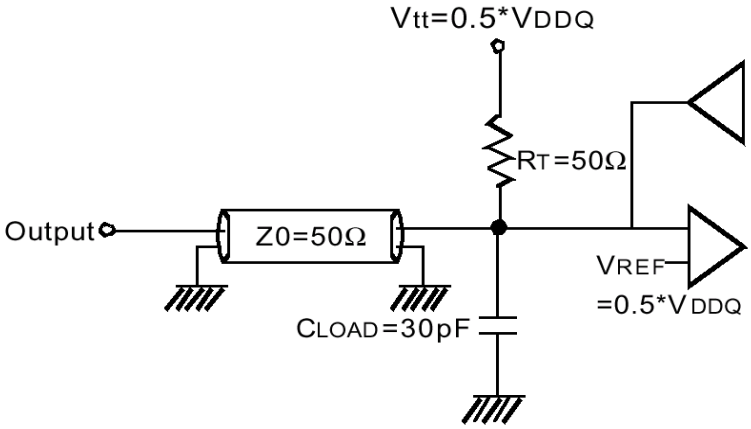
AC OPERATING CONDITIONS

PARAMETER/ CONDITION	STMBOL	MIN	MAX	UNIT	NOTE
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH} (AC)	V_{REF} + 0.31			3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V_{IL} (AC)		V_{REF} - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V_{ID} (AC)	0.7	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V_{IX} (AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	2

Note 1. V_{ID} is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of V_{IX} is expected to equal 0.5* V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a V_{REF} envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

PARAMETER	VALUE	UNIT	NOTE
Input reference voltage for Clock	0.5 * V_{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	0.5	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}-0.31	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{TT}	V	
Output load condition	See Load Circuit	V	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE (V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 25°C, f = 1MHz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance(A0 ~ A12, BA0 ~ BA1,RAS,CAS, WE)	C_{IN1}	49	57	pF
Input Capacitance(CKE0)	C_{IN2}	42	50	pF
Input Capacitance(CS0)	C_{IN3}	42	50	pF
Input Capacitance(CLK0, CLK1,CLK2)	C_{IN4}	22	25	pF
Data & DQS input/output Capacitance(DQ0~DQ63)	C_{OUT1}	6	8	pF
Input Capacitance(DM0~DM8)	C_{IN5}	6	8	pF

AC TIMMING PARAMETERS & SPECIFICATIONS (THESE AC CHARICTERISTICS WERE TESTED ON THE COMPONENT)

PARAMETER		SYMBOL	DDR200 -10A		DDR266A -13A		DDR266B -13B		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
Row cycle time		t_{RC}	70		65		65		ns	1
Refresh row cycle time		t_{RFC}	80		75		75		ns	1,2
Row active time		t_{RAS}	48	120K	45	120K	45	120K	ns	1,2
/RAS to /CAS delay		t_{RCD}	20		20		20		ns	3
Row precharge time		t_{RP}	20		20		20		ns	3
Row active to Row active delay		t_{RRD}	15		15		15		ns	3
Write recovery time		t_{WR}	2		2		2		t_{CK}	3
Last data in to Read command		t_{CDLR}	1		1		1		t_{CK}	2
Col. address to Col. address delay		t_{CCD}	1		1		1		t_{CK}	
Clock cycle time	CL=2.0	t_{CK}	10	12	7.5	12	10	12	ns	
	CL=2.5			12	7.5	12	7.5	12	ns	

Clock high level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK	t_{DQSCK}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK	t_{AC}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge	t_{DQSQ}	-	+0.6	-	+0.5	-	+0.5	ns	
Read Preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Read Postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Data out high impedence time from CK-/CK	t_{HZQ}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	2
CK to valid DQS-in	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time	t_{WPRES}	0		0		0		ns	3
DQS-in hold time	t_{WPREH}	0.25		0.25		0.25		t_{CK}	
DQS-in falling edge to CK rising-setup time	t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS-in falling edge to CK rising hold time	t_{DSH}	0.2		0.2		0.2		t_{CK}	
DQS-in high level width	t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS-in low level width	t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-in cycle time	t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time	t_{IS}	1.1		0.9		0.9		ns	
Address and Control Input hold time	t_{IH}	1.1		0.9		0.9		ns	
Mode register set cycle time	t_{MRD}	16		15		15		ns	
DQ & DM setup time to DQS	t_{DS}	0.6		0.5		0.5		ns	
DQ & DM hold time to DQS	t_{DH}	0.6		0.5		0.5		ns	
DQ & DM input pulse width	t_{DIPW}	2		1.75		1.75		ns	
Power down exit time	t_{PDEX}	10		10		10		ns	
Exit self refresh to write command	t_{XSW}	116		95				ns	
Exit self refresh to bank active command	t_{XSA}	80		75		75		ns	
Exit self refresh to read command	t_{XSR}	200		200		200		Cycle	
Refresh interval time	t_{REF}	15.6		15.6		15.6		us	1
Output DQS valid window	t_{QH}	0.35		0.35		0.35		t_{CK}	
DQS write postamble time	t_{WPST}	0.25		0.25		0.25		t_{CK}	4

Notes :

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter (t_{JIT}(HP)) of the PLL and the half jitter due to crosstalk (t_{JIT}(crosstalk)) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	Δt_{DS}	Δt_{DH}
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310$mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall

Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.
10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is actual to the system clock cycle time.

COMMAND TRUTH TABLE (V=VALID, X=DOν¢T CARE, H=LOGIC HIGH, L=LOGIC LOW)

COMMAND			CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DM	BA 0,1	A10/ AP	A11 A9~A0	NOTE
Register	Extended MRS		H	X	L	L	L	L	X	OP code			1,2
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & Row Addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge eable										H		4
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		5
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					

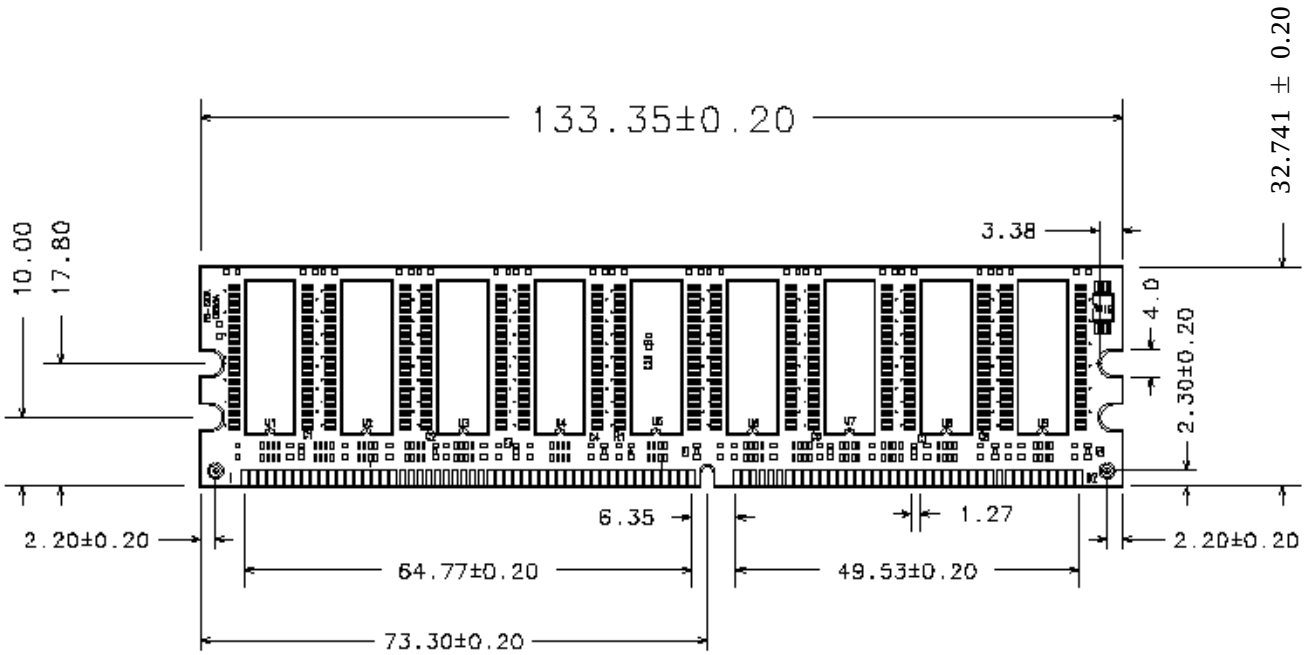
	Exit	L	H	H	X	X	X	X		
				L	V	V	V			
DM		H	X					V	X	8
No operation command		H	X	H	X	X	X	X	X	9
				L	H	H	H			9

Note :
1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state.
A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

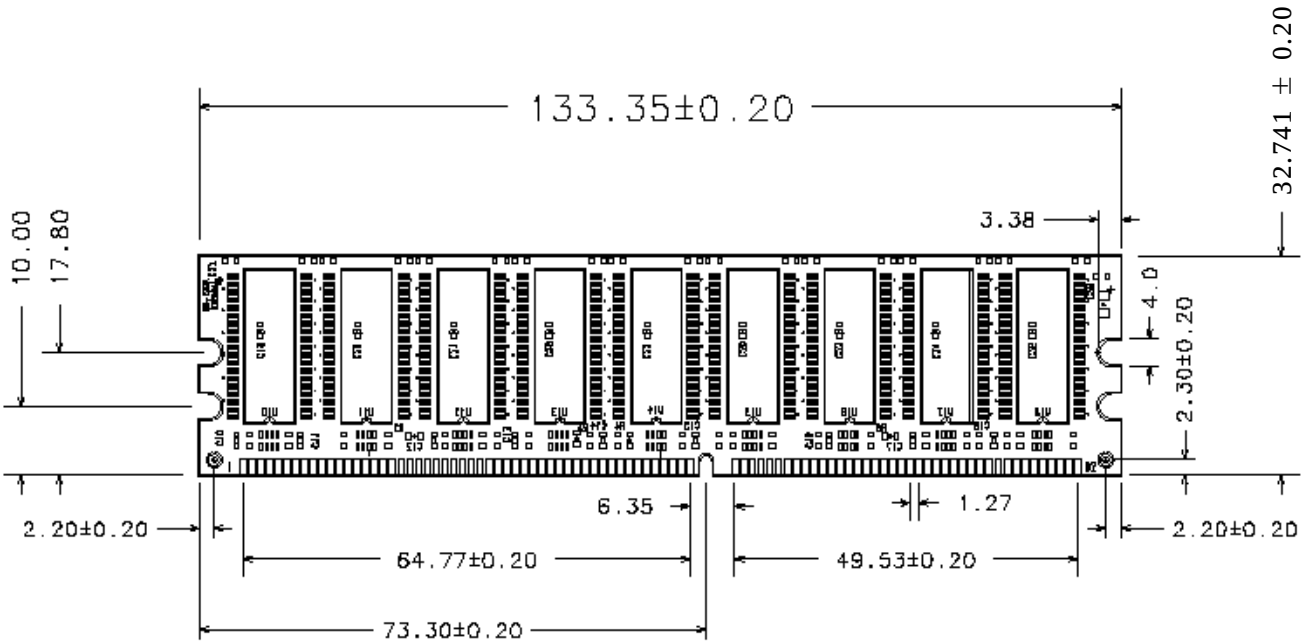
PACKAGE DIMENSIONS

Unit **:** mm

Front –Side



Rear-Side



ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HDD16M64D8W-10A	128MByte	16M x 64	184PIN DIMM	4K	2.5V	DDR	100MHz/CL2
HDD16M64D8W -13A	128MByte	16M x 64	184PIN DIMM	4K	2.5V	DDR	133MHz/CL2
HDD16M64D8W -13B	128MByte	16M x 64	184PIN DIMM	4K	2.5V	DDR	133MHz/CL2.5

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