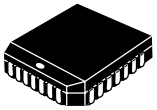
MC10E446, MC100E446

5V ECL 4-Bit Parallel/Serial Converter



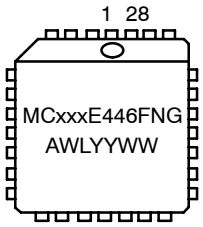
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PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Description

The MC10E/100E446 is an integrated 4-bit parallel to serial data converter. The device is designed to operate for NRZ data rates of up to 1.3 Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8 bit conversion applications. Note that the serial output data clocks off of the negative input clock transition.

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and thus select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the internal load clock will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E446's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 1.3 Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

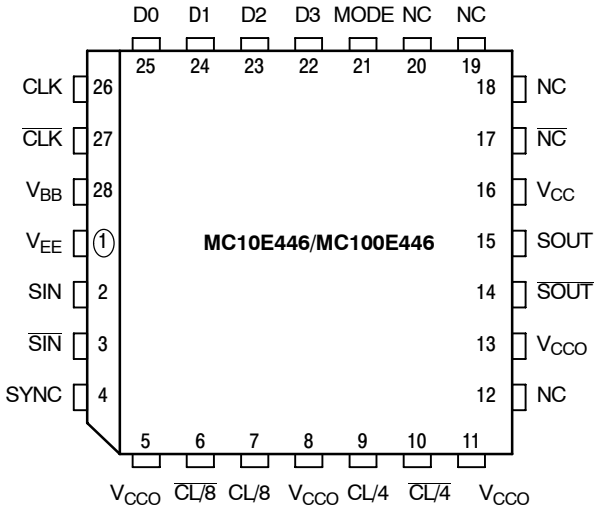
The 100 Series contains temperature compensation.

Features

- On Chip Clock ÷4 and ÷8
- 1.5 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8 Bits
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
- Internal Input 50 kΩ Pulldown Resistors
- ESD Protection: Human Body Model; > 2 kV, Machine Model; > 100 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 525 devices
- Moisture Sensitivity Level: Pb = 1; Pb−Free = 3 For Additional Information, see Application Note AND8003/D
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: PLCC−28 (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
SIN	ECL Differential Serial Data Input
D0 – D3	ECL Parallel Data Inputs
SOUT, SOUT	ECL Differential Serial Data Output
CLK, CLK	ECL Differential Clock Inputs
CL/4, CL/4	ECL Differential ÷4 Clock Output
CL/8, CL/8	ECL Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNC	ECL Conversion Synchronizing Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

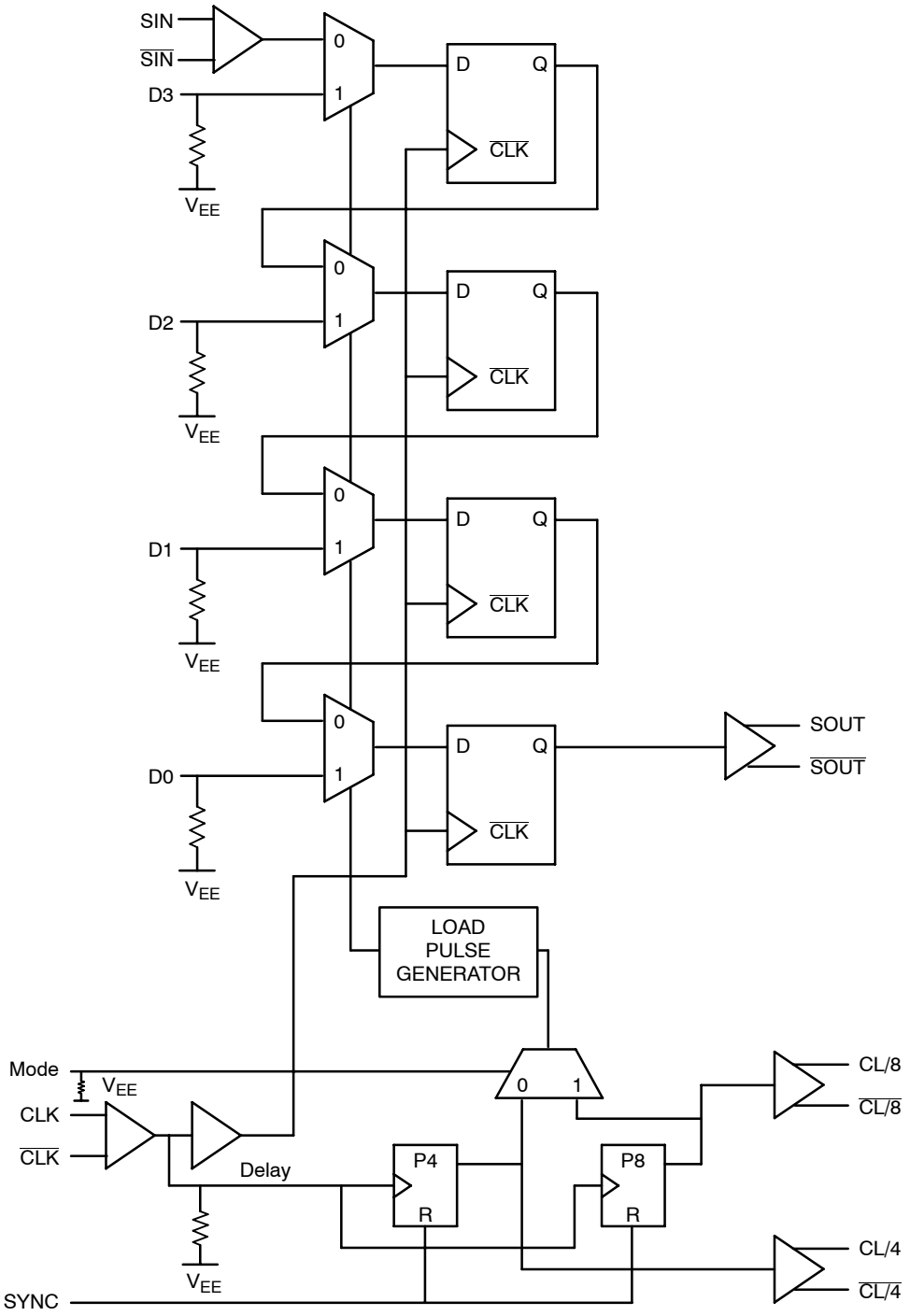


Figure 2. Logic Diagram

Table 2. FUNCTION TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	PLCC−28 PLCC−28	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	PLCC−28	22 to 26	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. 10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		126	151	mA
V_{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
VOH_{SOUT}	Output HIGH Voltage SOUT/$\overline{SOUT}$	3980		4210	4020		4240	4090		4330	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.65		3.75	3.69		3.81	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 5. 10E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 3)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		126	151	mA
V_{OH}	Output HIGH Voltage (Note 4)	−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
VOH_{SOUT}	Output HIGH Voltage SOUT/$\overline{SOUT}$	−1020		−790	−980		−760	−910		−670	mV
V_{OL}	Output LOW Voltage (Note 4)	−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V_{IH}	Input HIGH Voltage	−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V_{IL}	Input LOW Voltage	−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
V_{BB}	Output Voltage Reference	−1.38		−1.27	−1.35		−1.25	−1.31		−1.19	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
4. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 6. 100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 5)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		145	174	mA
V_{OH}	Output HIGH Voltage (Note 6)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
VOH_{SOUT}	Output HIGH Voltage SOUT/$\overline{SOUT}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 6)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.62		3.74	3.62		3.74	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 7. 100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 7)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		145	174	mA
V_{OH}	Output HIGH Voltage (Note 8)	−1025	−950	−880	−1025	−950	−880	−1025	−950	−880	mV
VOH_{SOUT}	Output HIGH Voltage SOUT/$\overline{SOUT}$	−1025		−830	−1025		−830	−1025		−830	mV
V_{OL}	Output LOW Voltage (Note 8)	−1810	−1705	−1620	−1810	−1745	−1620	−1810	−1740	−1620	mV
V_{IH}	Input HIGH Voltage	−1165	−1025	−880	−1165	−1025	−880	−1165	−1025	−880	mV
V_{IL}	Input LOW Voltage	−1810	−1645	−1475	−1810	−1645	−1475	−1810	−1645	−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.27	−1.38		−1.26	−1.38		−1.26	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
8. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 8. AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 9)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
F_{MAX}	Max Conversion Frequency	1.3	1.6		1.3	1.6		1.3	1.6		Gb/s NRZ
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to SOUT (Note 10) CLK to CL/4 CLK to CL/8 SYNC to CL/4, CL/8	 1020 650 800 650	 1200 850 1050 850	 1480 1050 1300 1100	 1020 650 800 650	 1200 850 1050 850	 1480 1050 1300 1100	 1020 650 800 650	 1200 850 1050 850	 1480 1050 1300 1100	ps
t_s	Setup Time (Note 11) SIN, Dn	-200	-450		-200	−450		−200	−450		ps
t_h	Hold Time (Note 11) SIN, Dn	900	650		900	650		900	650		ps
t_{RR}	Reset Recovery Time SYNC	500	300		500	300		500	300		ps
t_{PW}	Min Pulse Width CLK, MR	300			300			300			ps
t_{JITTER}	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150		1000	150		1000	150		1000	mV
t_r t_f	Rise/Fall Times (20% - 80%) SOUT Other	100 200	225 425	350 650	100 200	225 425	350 650	100 200	225 425	350 650	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. 10 Series: V_{EE} can vary −0.46 V / +0.06 V.
   100 Series: V_{EE} can vary −0.46 V / +0.8 V.
10. Propagation delays measured from negative going clock edge.
11. Relative to negative clock edge.

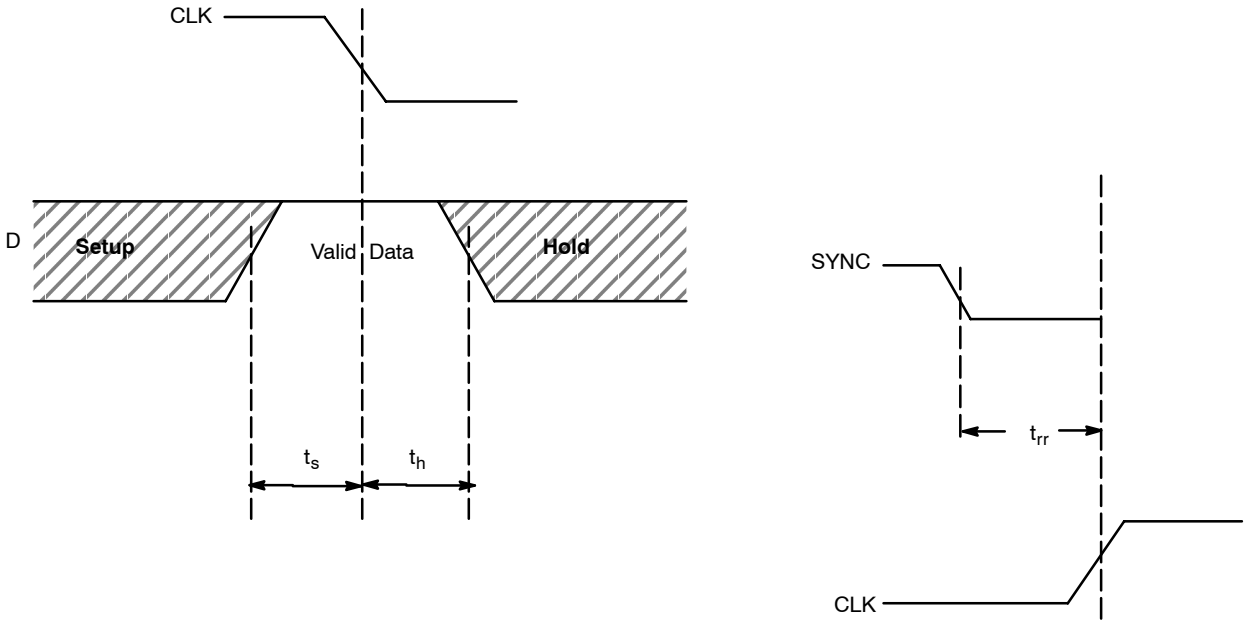
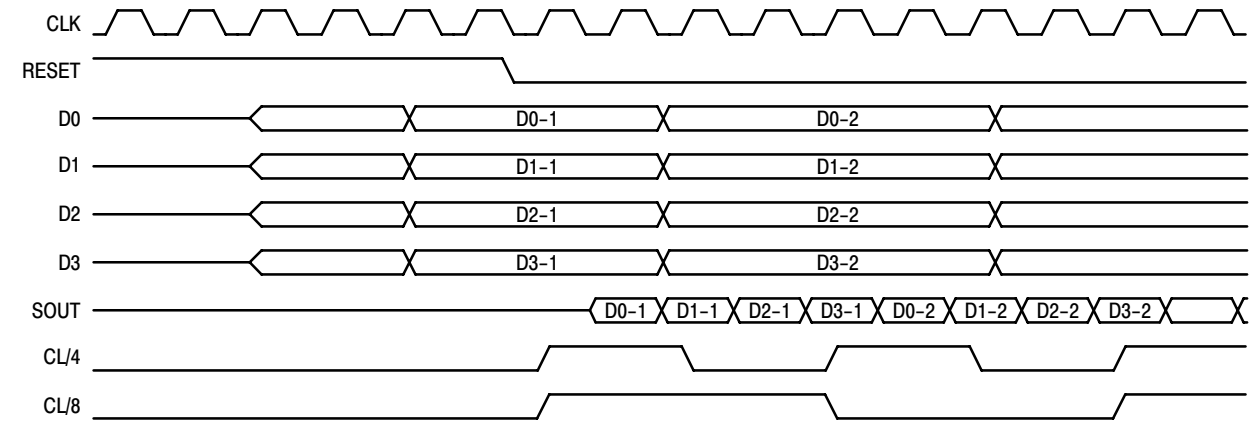
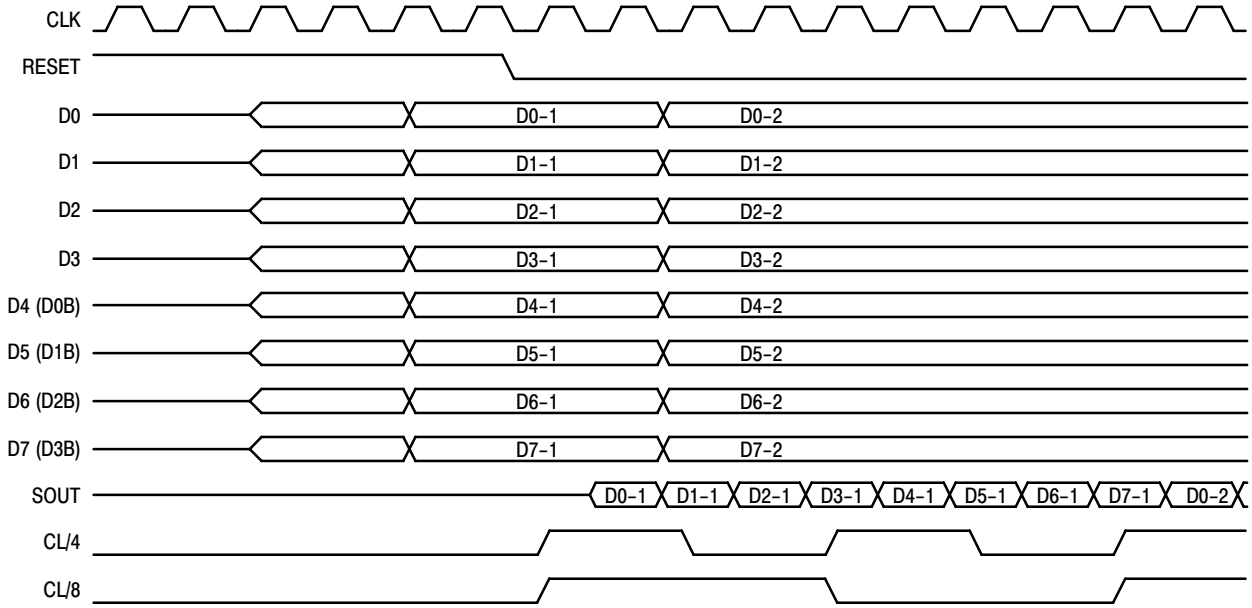


Figure 3.



Timing Diagram A. 4:1 Parallel to Serial Conversion



Timing Diagram B. 8:1 Parallel to Serial Conversion

Figure 4. Timing Diagrams

Applications Information

The MC10E/100E446 is an integrated 4:1 parallel to serial converter. The chip is designed to work with the E445 device to provide both transmission and receiving of a high speed serial data path. The E446 can convert 4 bits of data into a 1.3 Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see timing diagram A).

The E446 features a differential serial input and internal divide by 8 circuitry to facilitate the cascading of two devices to build a 8:1 multiplexer. Figure 1 illustrates the architecture for a 8:1 multiplexer using two E446's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the higher order converter feed the serial inputs of the the lower order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1480 ps and tS for SIN = −200 ps, yields a minimum period of 1280 ps or a clock frequency of 780 MHz.

The clock frequency is somewhat lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E446. By delaying the clock feeding E446A relative to the clock of E446B the frequency of operation can be increased.

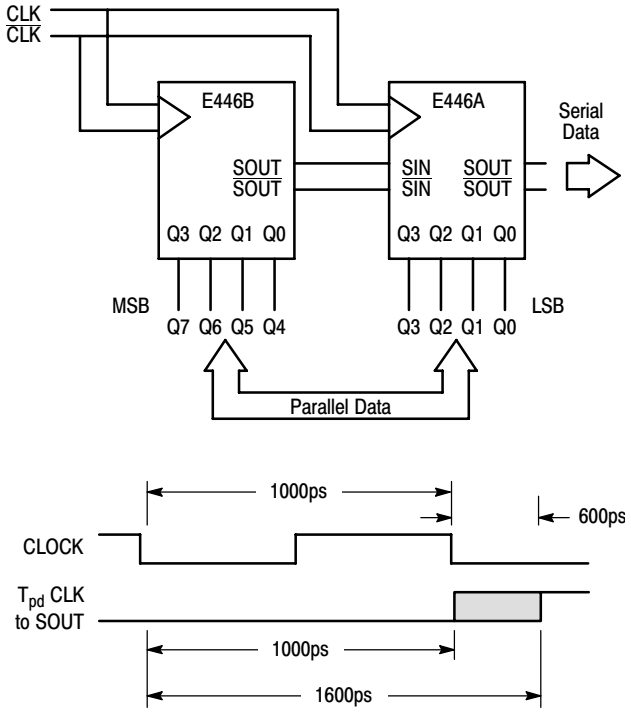


Figure 5. Cascaded 8:1 Converter Architecture

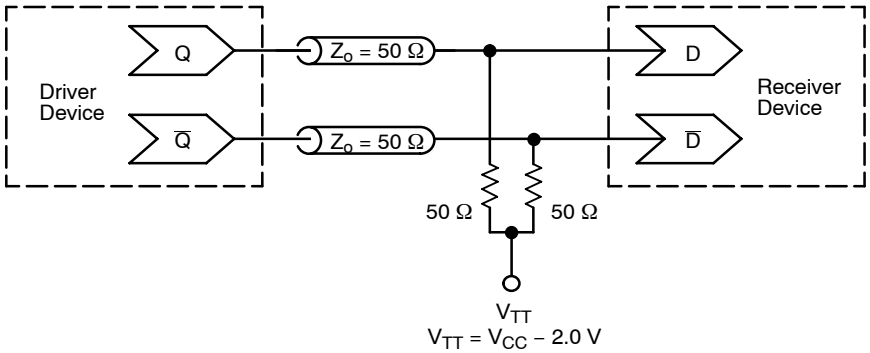


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC10E446FN	PLCC−28	37 Units / Rail
MC10E446FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10E446FNR2	PLCC−28	500 / Tape & Reel
MC10E446FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100E446FN	PLCC−28	37 Units / Rail
MC100E446FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100E446FNR2	PLCC−28	500 / Tape & Reel
MC100E446FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

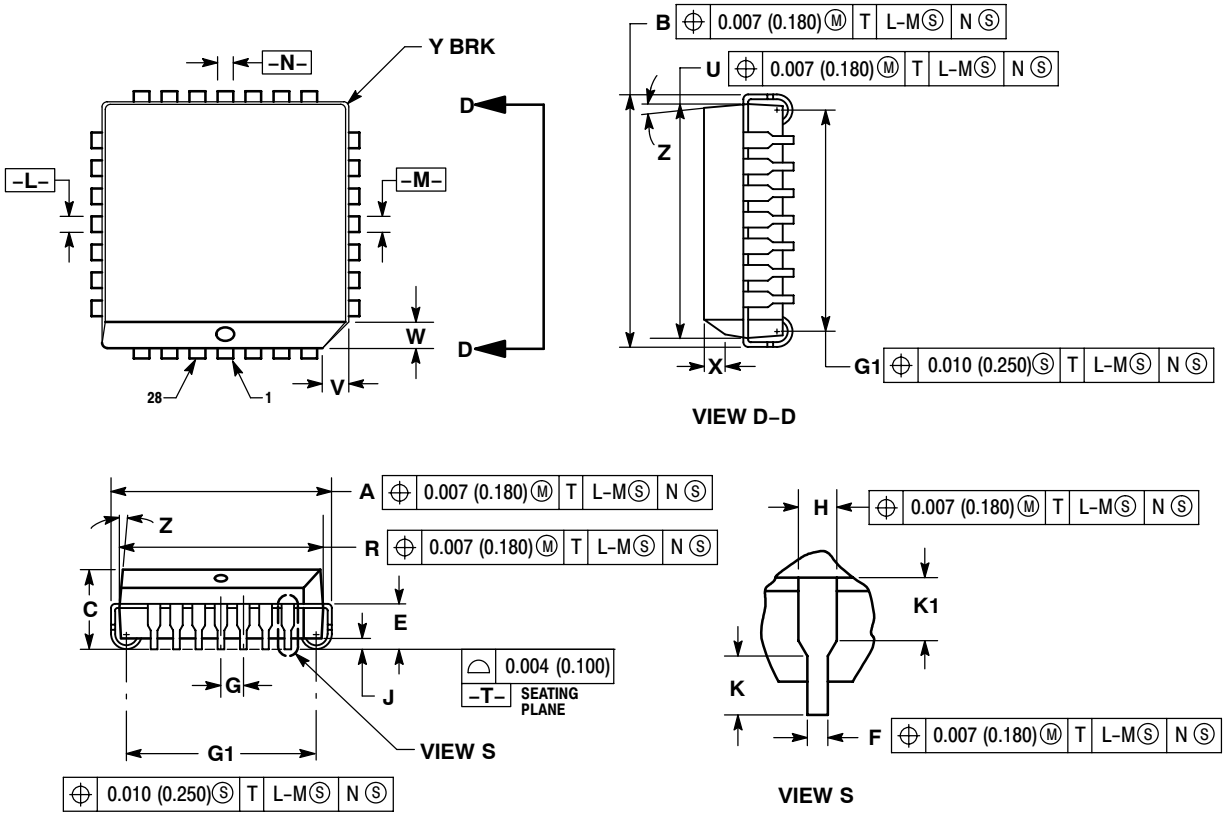
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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