FAIRCHILD SEMICONDUCTOR®

March 2008

FAN5109
Dual Bootstrapped 12V MOSFET Driver

Features

- Drives N-Channel High-Side and Low-Side MOSFETs in a Synchronous Buck Configuration
- Enhanced Upgrade to FAN5009
- Direct Interface to FAN5019, FAN5182, and Other Compatible PWM Controllers
- 12V High-Side and 12V Low-Side Drive
- Internal Adaptive Shoot-Through Protection
- Fast Rise and Fall Times
- Switching Frequency Above 500kHz
- $\overline{OD}$ input for Output Disable – Allows Synchronization with PWM Controller
- SOIC-8 Package

Applications

- Multi-Phase VRM/VRD Regulators for Microprocessor Power
- High-Current, High-Frequency DC/DC Converters
- High-Power Modular Supplies

Related Application Notes

- *Application Note AN-6003 — "Shoot-through" in Synchronous Buck Converters*
- *Application Note AN-6065 — FAN5109 V_{CC} Bypass Considerations to Reduce Voltage Spikes*

Description

The FAN5109 is a dual high-frequency MOSFET driver, specifically designed to drive N-Channel power MOSFETs in a synchronous-rectified buck converter. These drivers, combined with a Fairchild multi-phase pulse-width-modulated (PWM) controller and power MOSFETs, form a complete core voltage regulator solution for advanced microprocessors.

The FAN5109 drives the upper and lower MOSFET gates of a synchronous buck regulator to $12V_{GS}$. The upper gate drive includes an integrated boot diode and requires only an external bootstrap capacitor (C_{BOOT}). The output drivers have the capacity to efficiently switch power MOSFETs at frequencies up to 500KHz. The circuit's adaptive shoot-through protection prevents both MOSFETs from conducting simultaneously.

The FAN5109 is rated for operation from 0°C to +85°C and is available in a low-cost SOIC-8 package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Quantity Per Reel
FAN5109MX	0°C to 85°C	SOIC-8	Tape and Reel	2500

All packages are lead free per JEDEC: J-STD-020B standard.

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Application Diagram

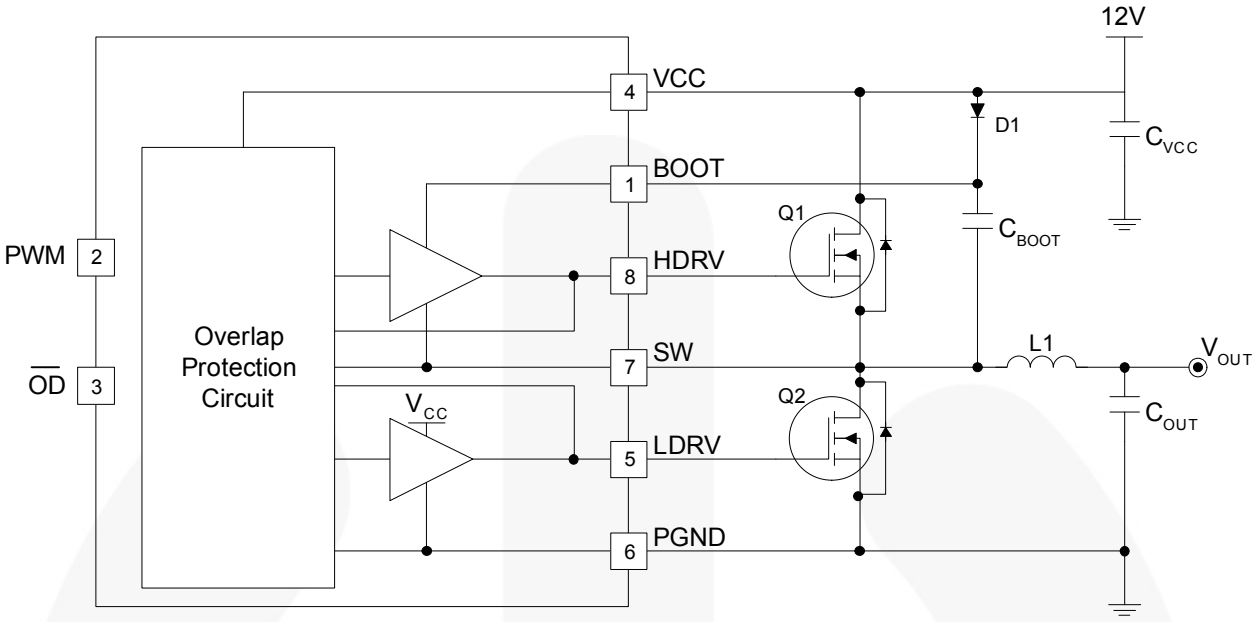


Figure 1. Typical FAN5109 Application

Block Diagram

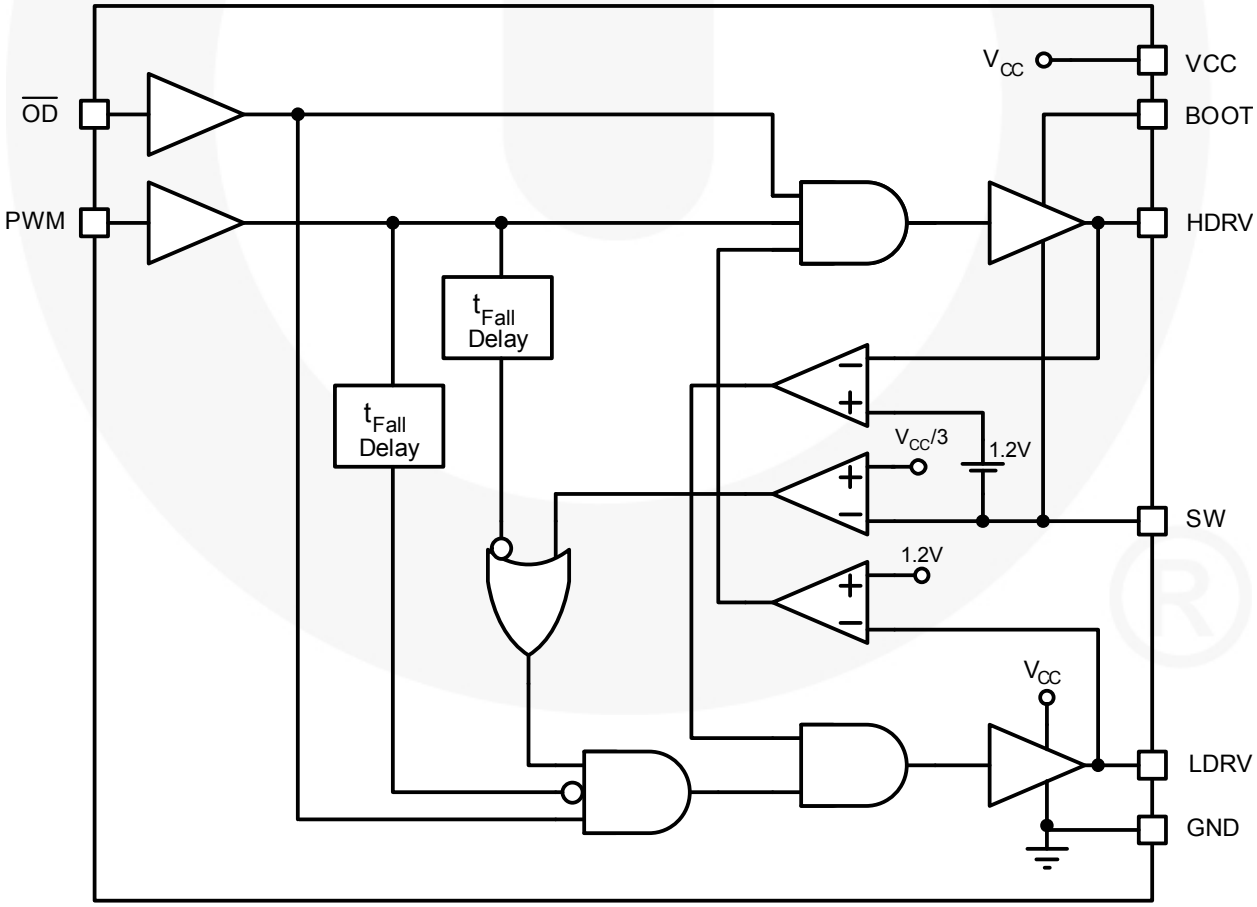


Figure 2. Functional Block Diagram

Pin Configuration

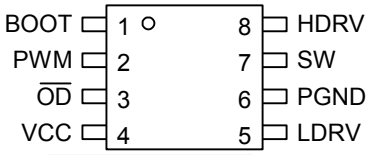


Figure 3. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	BOOT	**Bootstrap Supply Input.** Provides voltage supply to the high-side MOSFET driver. Connect to the bootstrap capacitor (*see the Applications section*).
2	PWM	**PWM Signal Input.** This pin accepts a logic-level PWM signal from the controller.
3	$\overline{OD}$	**Output Disable.** When LOW, this pin disables FET switching (HDRV and LDRV are held LOW).
4	VCC	**Power Input**. +12V chip bias power. Bypass with a 1μF ceramic capacitor.
5	LDRV	**Low-Side Gate Drive Output.** Connect to the gate of low-side power MOSFET(s).
6	PGND	**Power ground.** Connect directly to the source of the low-side MOSFET(s).
7	SW	**Switch Node Input**. Connect as shown in Figure 1. SW provides return for the high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
8	HDRV	**High-Side Gate Drive Output**. Connect to the gate of high-side power MOSFET(s).

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Absolute maximum ratings apply individually, not in combination. Unless otherwise specified, voltages are referenced to PGND.

Parameter		Min.	Max.	Unit
VCC to GND	Continuous	-0.3	15.0	V
VCC to GND	Transient (t=4ns, f=500kHz)	-0.3	19.0	
PWM and $\overline{OD}$ to GND		-0.3	5.5	V
SW to GND	Continuous	-1	15	V
	Transient (t=100ns, f=500kHz)	-5[1]	25	
BOOT to SW	Continuous	-0.3	15.0	V
	Transient (t<20ns, f=500kHz)	-2.0	17.0	
BOOT to GND	Continuous	-0.3	30.0	V
	Transient (t=100ns, f=500kHz)		38	
HDRV to GND		V_{SW} -1	V_{BOOT}+0.3	V
LDRV to GND	Continuous	-0.5	V_{CC}	V
	Transient (t=200ns)	-2.0[1]	V_{CC}+0.3	
	Transient (t<20ns, f=500kHz)	-2.0[1]	V_{CC}+2.0	

Note:
1. For transient derating beyond the levels indicated, refer to Figure 17 and Figure 18.

Thermal Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature	0		+150	°C
T_{STG}	Storage Temperature	-65		+150	°C
T_L	Lead Soldering Temperature, 10 seconds			+300	°C
T_{VP}	Vapor Phase, 60 seconds			+215	°C
T_{LI}	Infrared, 15 seconds			+220	°C
P_D	Power Dissipation, T_A=25°C			715	mW
θ_{JC}	Thermal Resistance, Junction-to-Case		40		°C/W
θ_{JA}	Thermal Resistance, Junction-to-Ambient		140		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	VCC to GND	10.0	12.0	13.5	V
T_A	Ambient Temperature		0		+85	°C
T_J	Junction Temperature		0		+125	°C

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Electrical Characteristics

V_{CC} and V_{LDRV}=12V, and T_A=25°C using the circuit in Figure 4 unless otherwise noted, each side. The "•" denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Input Supply							
V_{CC}	V_{CC} Voltage Range		•	6.4	12.0	13.5	V
I_{CC}	V_{CC} Current	$\overline{OD}$ =0V	•		2.5	4.0	mA
$\overline{OD}$ **Input**							
$V_{IH\ (OD)}$	Input High Voltage		•	2.0			V
$V_{IL\ (OD)}$	Input Low Voltage		•			0.8	V
$V_{HYS(OD)}$	Input Hysteresis		•		550		mV
I_{OD}	Input Current	$\overline{OD}$ =3.0V	•	–300		+300	nA
$t_{pdl(OD)}$	Propagation Delay[3]	See Figure 5			25	40	ns
$t_{pdh(OD)}$					15	30	ns
PWM Input							
$V_{IH(PWM)}$	Input High Voltage		•	3.5			V
$V_{IL(PWM)}$	Input Low Voltage		•			0.8	V
$I_{IL(PWM)}$	Input Current		•	-1		+1	µA
High-Side Driver							
R_{HUP}	Output Resistance, Sourcing	$V_{BOOT} – V_{SW}$=12V			2.5	3.3	Ω
$I_{SOURCE(LDRV)}$	Source Current[3]	V_{DS}=-10V			2.0		A
R_{HDN}	Output Resistance, Sinking	$V_{BOOT} – V_{SW}$=12V			1.1	1.5	Ω
$I_{SINK(HDRV)}$	Sink Current[3]	V_{DS}=10V			3.0		A
$t_{R(HDRV)}$	Transition Times[3,5]	See Figure 4			25	40	ns
$t_{(HDRV)}$					15	25	ns
$t_{pdh(HDRV)}$	Propagation Delay[3,4]	See Figure 6			40	55	ns
$t_{dl(HDRV)}$					25	40	ns
Low-Side Driver							
R_{LUP}	Output Resistance, Sourcing				2.0	2.6	Ω
$I_{SOURCE(LDRV)}$	Source Current[3]	V_{DS}=-10V			2.7		A
R_{LDN}	Output Resistance, Sinking				0.9	1.2	Ω
$I_{SINK(LDRV)}$	Sink Current[3]	V_{DS}=10V			3.5		A
$t_{R(LDRV)}$	Transition Times[3,5]	See Figure 4			20	30	ns
$t_{F(LDRV)}$					15	25	ns
$t_{pdh(LDRV)}$	Propagation Delay[3,4]	See Figure 6			20	30	ns
$t_{pdl(LDRV)}$					15	25	ns
$t_{pdh(LDF)}$		See *Adaptive Gate Drive Circuit Description*			160		ns

Notes:

2. Limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
3. Specifications guaranteed by design and characterization (not production tested).
4. For propagation delays, t_{pdh} refers to low-to-high signal transition. t_{pdl} refers to high-to-low signal transition.
5. Transition times are defined for 10% and 90% of DC values.

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Test Diagrams

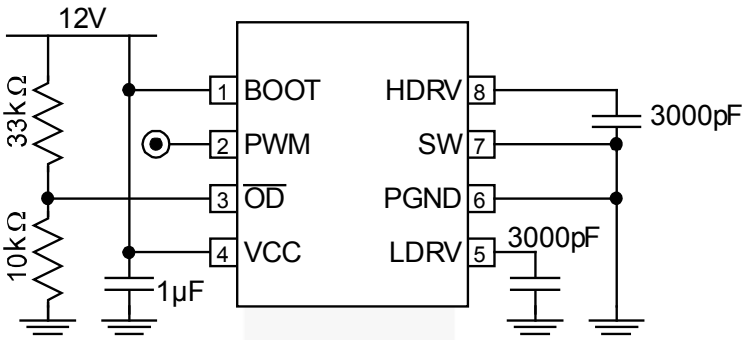


Figure 4. Test Circuit

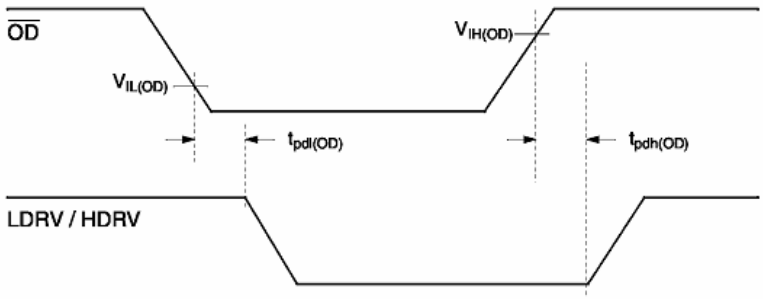


Figure 5. Output Disable Timing

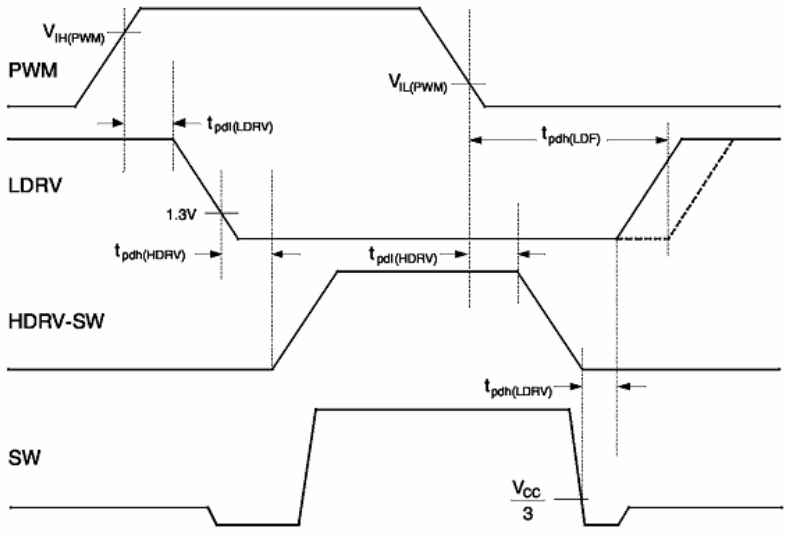


Figure 6. Adaptive Gate Drive Timing

Typical Performance Characteristics

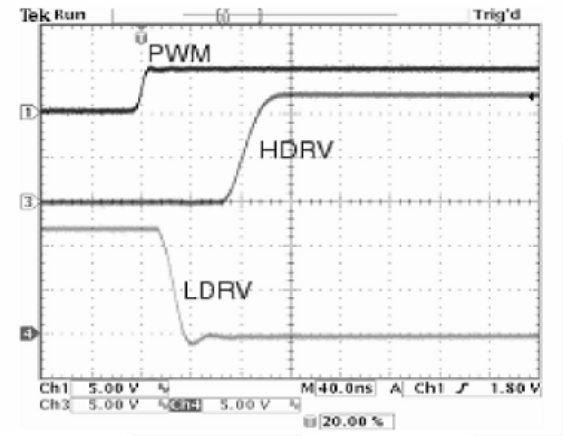


Figure 7. Gate Drive Rise and Fall Times (1)

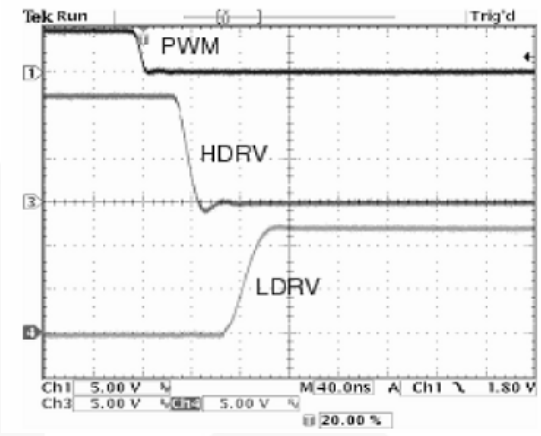


Figure 8. Gate Drive Rise and Fall Times (2)

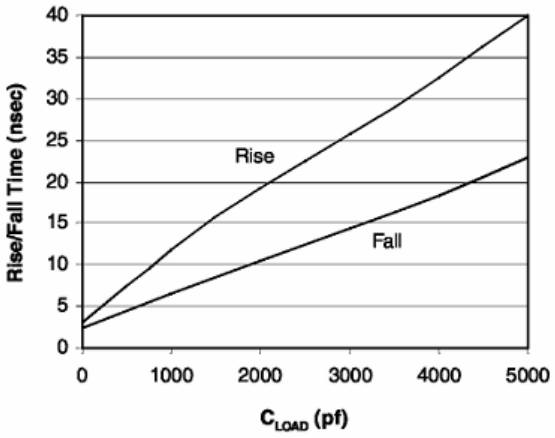


Figure 9. HDRV Rise and Fall Times vs. C_{LOAD}

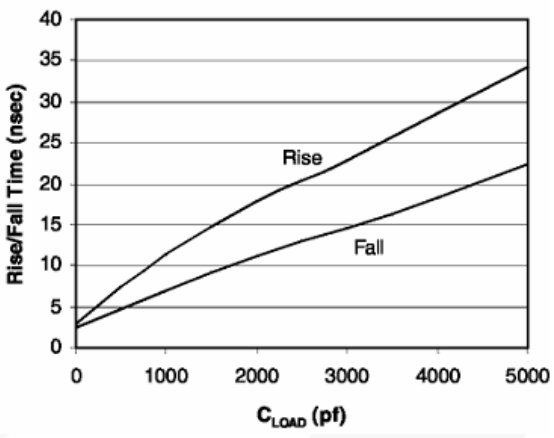


Figure 10. LDRV Rise and Fall Times vs. C_{LOAD}

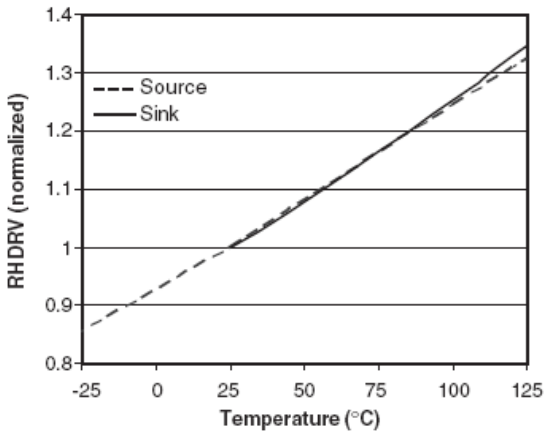


Figure 11. HDRV Normalized Impedance vs. Temperature

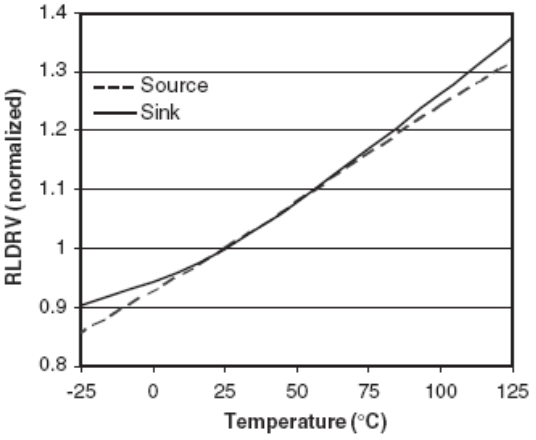


Figure 12. LDRV Normalized Impedance vs. Temperature

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Typical Performance Characteristics (Continued)

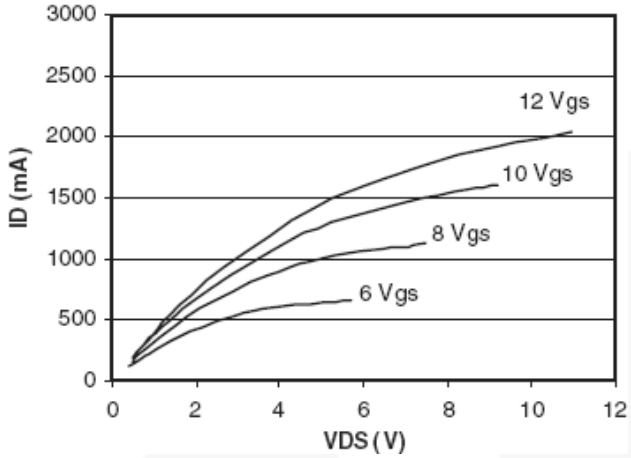


Figure 13. HDRV Pull-Up (Sourcing)

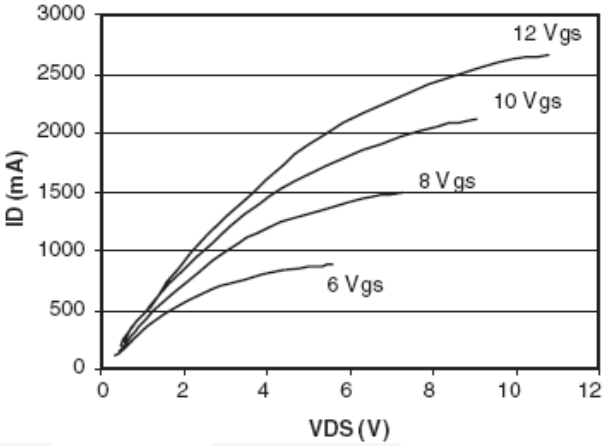


Figure 14. LDRV Pull-Up (Sourcing)

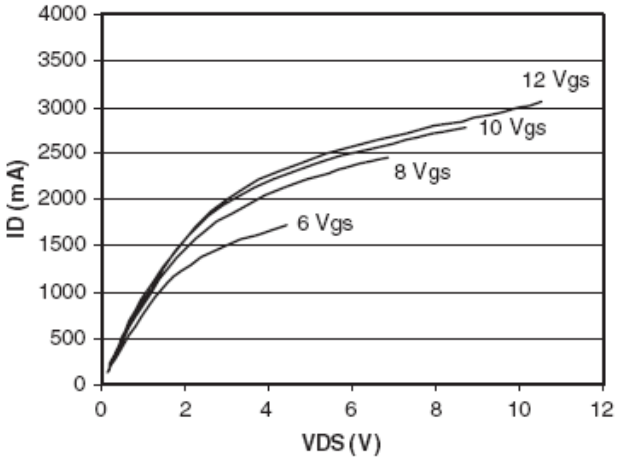


Figure 15. HDRV Pull-Down (Sinking)

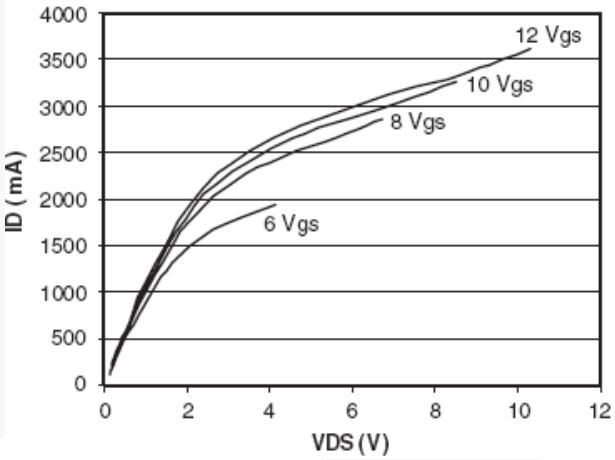


Figure 16. LDRV Pull-Down (Sinking)

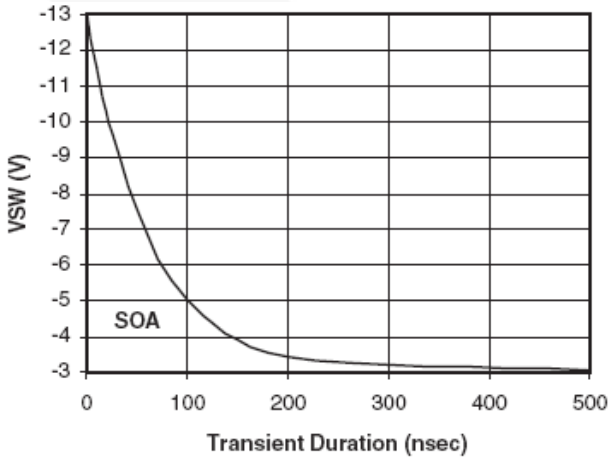


Figure 17. Negative SW Voltage Transient

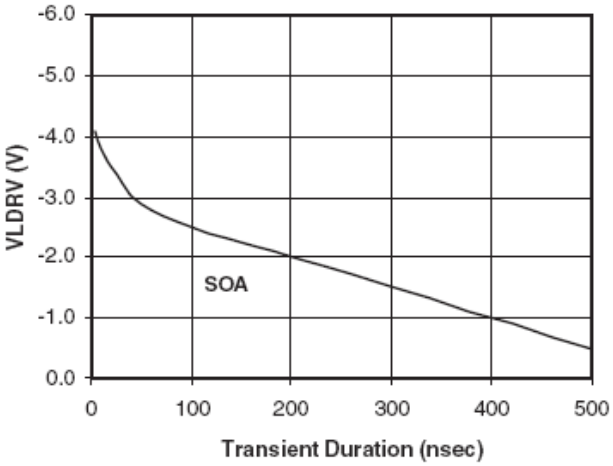


Figure 18. Negative LDRV Voltage Transient

Typical Performance Characteristics (Continued)

I_{CC}{mA}=2 x V_{CC} x (0.26 + 3.38 x f_{SW}), where f_{SW} is in MHz.

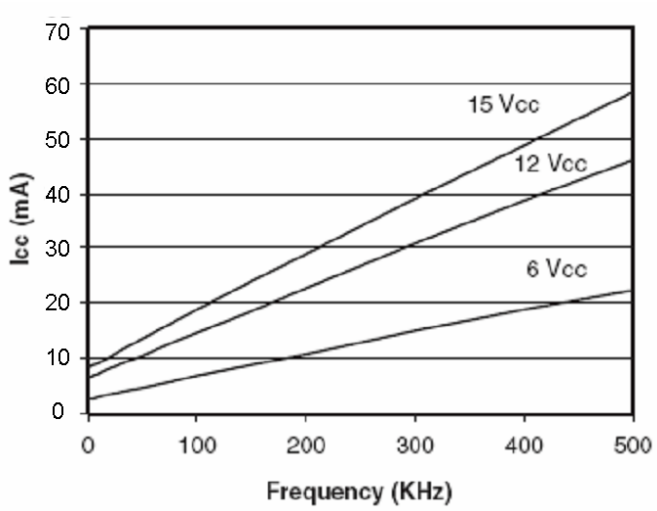


Figure 19. Operating Current vs. Frequency

Circuit Description

The FAN5109 is optimized for driving N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and low-side MOSFETs.

For an illustration of the FAN5109 and its features, refer to the Typical Application diagram in Figure 1 and Functional Block diagram in Figure 2.

Low-Side Driver

The low-side driver (LDRV) is designed to drive ground-referenced, low-$R_{DS(on)}$, N-channel MOSFETs. The bias for LDRV is internally connected between VCC and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the FAN5109 is disabled ($\overline{OD}$ =0V), LDRV is held LOW.

High-Side Driver

The high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of an external diode and bootstrap capacitor (C_{BOOT}).

During start-up, SW is held at PGND, allowing C_{BOOT} to charge to V_{CC} through the diode. When the PWM input goes HIGH, HDRV begins to charge the high-side MOSFET gate (Q1). During this transition, charge is transferred from C_{BOOT} to Q1's gate. As Q1 turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} + $V_{C(BOOT)}$, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. C_{BOOT} is recharged to V_{CC} when SW falls to PGND.

HDRV output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Adaptive Gate Drive Circuit

The FAN5109 advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Refer to the gate drive rise and fall time waveforms in Figure 7 and Figure 8 for the relevant timing information.

To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, Q2 begins to turn OFF after a propagation delay, as defined by $t_{pdl(LDRV)}$ parameter. Once the LDRV pin is discharged below ~1.3V, Q1 begins to turn ON after adaptive delay $t_{pdh(HDRV)}$.

To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, Q1 begins to turn OFF after a propagation delay ($t_{pdl(HDRV)}$). Once the SW pin falls below ~V_{CC}/3, Q2 begins to turn ON after adaptive delay $t_{pdh(LDRV)}$.

Additionally, V_{GS} of Q1 is monitored. When $V_{GS(Q1)}$ is discharged below ~1.3V, a secondary adaptive delay is initiated, which results in Q2 being driven ON after $t_{pdh(LDF)}$, regardless of the SW state. This function is implemented to ensure C_{BOOT} is recharged after each switching cycle, particularly for cases where the power converter is sinking current and the SW voltage does not fall below the V_{CC}/3 adaptive threshold. The secondary delay $t_{pdh(LDF)}$ is longer than $t_{pdh(LDRV)}$.

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Application Information

Supply Capacitor Selection

For the supply input (V_{CC}), a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the VCC and PGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and an external diode, as shown in Figure 1. These components should be selected after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} = \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BOOT} is the voltage droop allowed on the high-side MOSFET drive. For example, the Q_G of the FDD6696 MOSFET is about 35nC at 12V_{GS}. For an allowed droop of ~300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor must be used. The average diode forward current, $I_{F(AVG)}$, can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{SW} \quad (2)$$

where F_{SW} is the switching frequency of the controller.

The peak surge current rating of the diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces.

Thermal Considerations

Total device dissipation:

$$P_D = P_Q + P_{HDRV} + P_{LDRV} \quad (3)$$

P_Q represents quiescent power dissipation:

$$P_Q = V_{CC} \times [4mA + 0.036\ (f_{SW} - 100)] \quad (4)$$

f_{SW} is switching frequency (in kHz).

Q_{G1} is total gate charge of the upper FET (Q1) for its applied V_{GS}.

P_{HDRV} represents internal power dissipation of the upper FET driver.

$$P_{HDRV} = P_{H(R)} + P_{H(F)} \quad (5)$$

$P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges, respectively:

$$P_{H(R)} = P_{Q1} \times \frac{R_{HUP}}{R_{HUP} + R_E + R_G} \quad (6)$$

$$P_{H(F)} = P_{Q1} \times \frac{R_{HDN}}{R_{HDN} + R_E + R_G} \quad (7)$$

$$P_{Q1} = \tfrac{1}{2} \times Q_{G1} \times V_{GS(Q1)} \times f_{SW} \quad (8)$$

As described in Equations 6 and 7, the total power consumed driving the gate is divided in proportion to the resistances in series with the MOSFET's internal gate node, as shown below:

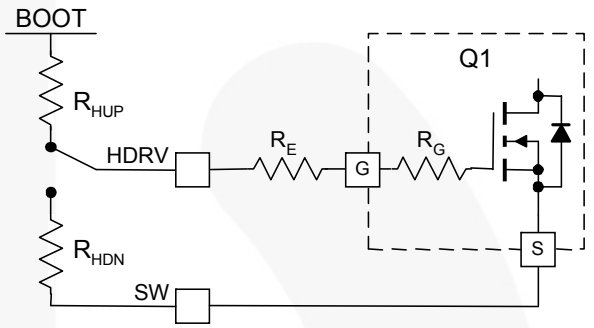


Figure 20. Driver Dissipation Model

R_G is the gate resistance internal to the FET. R_E is the external gate drive resistor implemented in many designs. Note that the introduction of R_E can reduce driver power dissipation, but excess R_E may cause errors in the adaptive gate drive circuitry. For more information, please refer to *Application Note AN-6003, "Shoot-through" in Synchronous Buck Converters*.

P_{LDRV} is dissipation of the lower FET driver:

$$P_{LDRV} = P_{L(R)} + P_{L(F)} \quad (9)$$

where $P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges, respectively:

$$P_{L(R)} = P_{Q2} \times \frac{R_{LUP}}{R_{LUP} + R_E + R_G} \quad (10)$$

$$P_{L(F)} = P_{Q2} \times \frac{R_{LDN}}{R_{HDN} + R_E + R_G} \quad (11)$$

$$P_{Q2} = \tfrac{1}{2} \times Q_{G2} \times V_{GS(Q2)} \times f_{SW} \quad (12)$$

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Layout Considerations

Use the following general guidelines when designing printed circuit boards (*see Figure 21*):

- Trace out the high-current paths and use short, wide (>25 mil) traces to make these connections.
- Connect the PGND pin as close as possible to the source of the lower MOSFET.
- The V_{CC} bypass capacitor should be located as close as possible to the driver's VCC and PGND pins and connected to the top layer.
- Use vias to other layers where possible to maximize thermal conduction away from the IC.

Note!

The further the V_{CC} bypass capacitor is located away from the driver, the less effective it is in limiting V_{CC} spikes. Locate the capacitor as close as possible to the driver and connect it as shown in Figure 21.

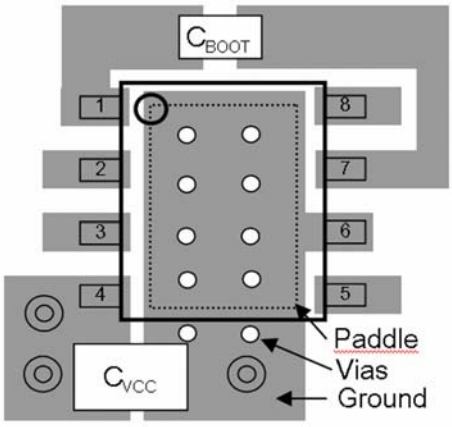


Figure 21. Recommended Layout for SOIC-8 (Not to Scale)

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Physical Dimensions

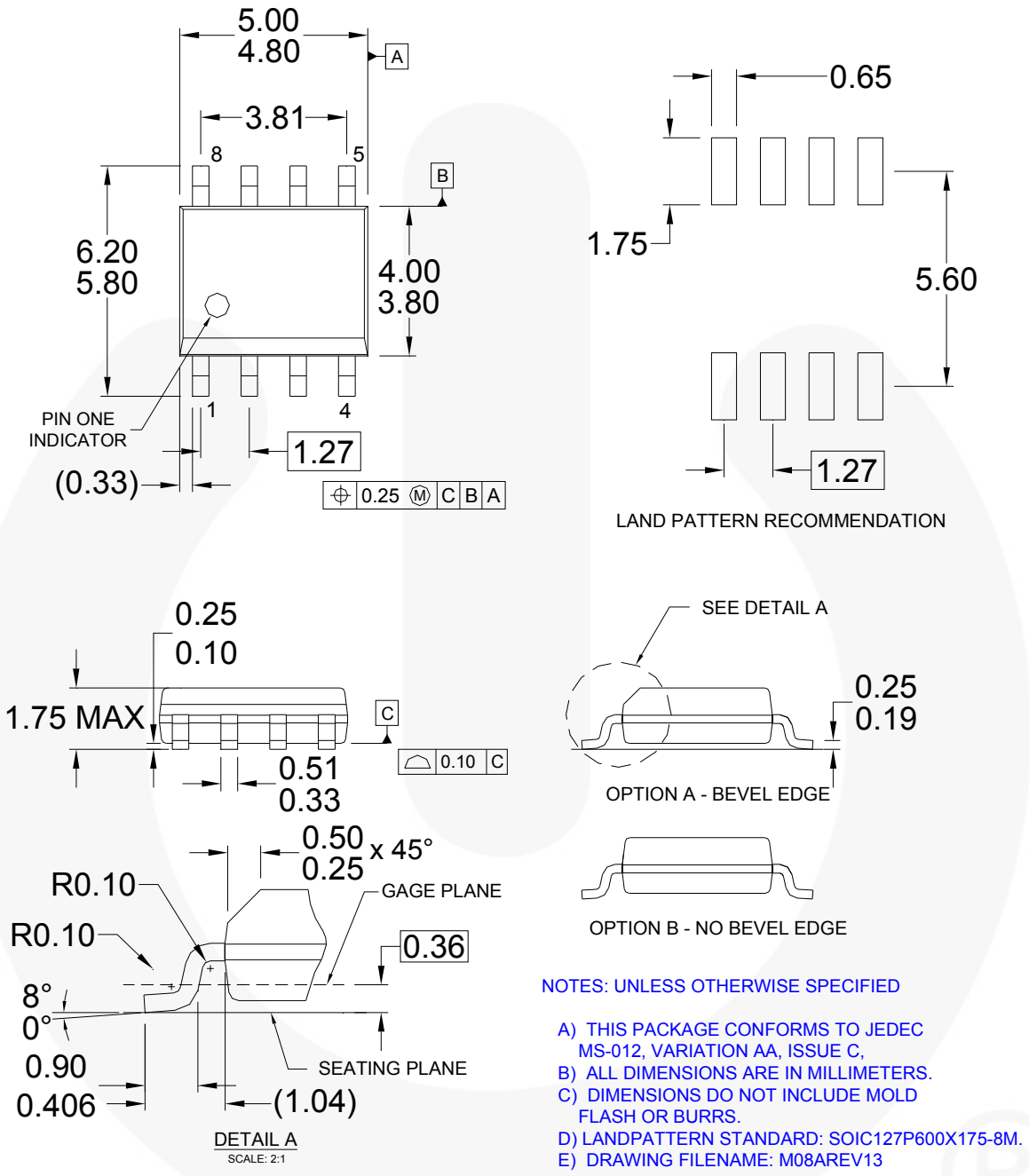


Figure 22. 8-Lead SOIC Package, 0.150mm

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