# Low Power, 350 MHz Voltage Feedback Amplifiers

# AD8038/AD8039

## FEATURES

**Low power: 1 mA supply current/amp**
**High speed**
**350 MHz, −3 dB bandwidth (G = +1)**
**425 V/µs slew rate**
**Low cost**
**Low noise**
**8 nV/√Hz @ 100 kHz**
**600 fA/√Hz @ 100 kHz**
**Low input bias current: 750 nA maximum**
**Low distortion**
**−90 dB SFDR @ 1 MHz**
**−65 dB SFDR @ 5 MHz**
**Wide supply range: 3 V to 12 V**
**Small packaging: 8-lead SOT-23, 5-lead SC70, and 8-lead SOIC**

## APPLICATIONS

**Battery-powered instrumentation**
**Filters**
**A/D drivers**
**Level shifting**
**Buffering**
**Photo multipliers**

## GENERAL DESCRIPTION

The AD8038 (single) and AD8039 (dual) amplifiers are high speed (350 MHz) voltage feedback amplifiers with an exceptionally low quiescent current of 1.0 mA/amplifier typical (1.5 mA maximum). The AD8038 single amplifier in the 8-lead SOIC package has a disable feature. Despite being low power and low cost, the amplifier provides excellent overall performance. Additionally, it offers a high slew rate of 425 V/µs and a low input offset voltage of 3 mV maximum.

The Analog Devices, Inc., proprietary XFCB process allows low noise operation (8 nV/√Hz and 600 fA/√Hz) at extremely low quiescent currents. Given a wide supply voltage range (3 V to 12 V), wide bandwidth, and small packaging, the AD8038 and AD8039 amplifiers are designed to work in a variety of applications where power and space are at a premium.

The AD8038 and AD8039 amplifiers have a wide input common-mode range of 1 V from either rail and swing to within 1 V of each rail on the output. These amplifiers are optimized for driving capacitive loads up to 15 pF. If driving larger capacitive loads, a small series resistor is needed to avoid excessive peaking or overshoot.

## FUNCTIONAL BLOCK DIAGRAM

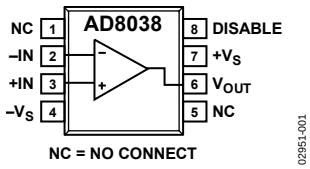



*Figure 1. 8-lead SOIC (R)*

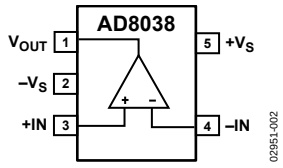



*Figure 2. 5-Lead SC70 (KS)*

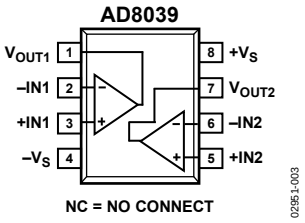



*Figure 3. 8-Lead SOIC (R) and 8-Lead SOT-23 (RJ)*

The AD8039 amplifier is available in a 8-lead SOT-23 package, and the single AD8038 is available in both an 8-lead SOIC and a 5-lead SC70 package. These amplifiers are rated to work over the industrial temperature range of −40°C to +85°C.

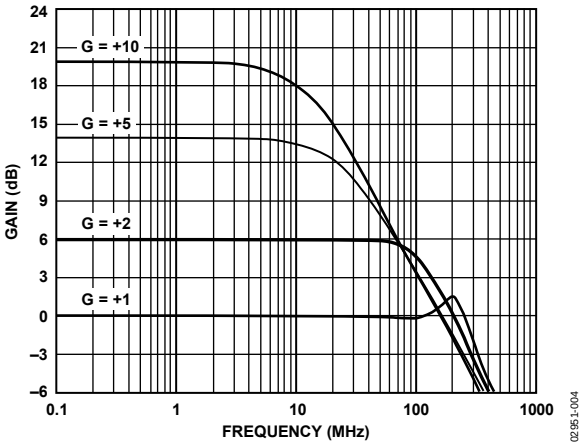



*Figure 4. Small Signal Frequency Response for Various Gains, $V_{OUT}$ = 500 mV p-p, $V_S$ = ±5 V*

**Rev. G**

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# IMPORTANT LINKS for the AD8038_8039*

Last content update 08/19/2013 03:00 am

## DOCUMENTATION

**AN-649:** Using the Analog Devices Active Filter Design Tool

**AN-581:** Biasing and Decoupling Op Amps in Single Supply Applications

**AN-402:** Replacing Output Clamping Op Amps with Input Clamping Amps

**AN-417:** Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems

**MT-060:** Choosing Between Voltage Feedback and Current Feedback Op Amps

**MT-059:** Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters

**MT-058:** Effects of Feedback Capacitance on VFB and CFB Op Amps

**MT-056:** High Speed Voltage Feedback Op Amps

**MT-053:** Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR

**MT-052:** Op Amp Noise Figure: Don't Be Mislead

**MT-050:** Op Amp Total Output Noise Calculations for Second-Order System

**MT-049:** Op Amp Total Output Noise Calculations for Single-Pole System

**MT-048:** Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth

**MT-047:** Op Amp No

**MT-033:** Voltage Feedback Op Amp Gain and Bandwidth

**MT-032:** Ideal Voltage Feedback (VFB) Op Amp

A Stress-Free Method for Choosing High-Speed Op Amps

**FOR THE AD8038**

**UG-112:** Universal Evaluation Board for Single, High Speed Op Amps Offered in SC-70 Packages

**UG-101:** Evaluation Board User Guide

**FOR THE AD8039**

AD8039-EP: Low Power, 350 MHz Voltage Feedback Amplifier

AD8039-DSCC: Microcircuit, Linear, Low Power, 350 MHz Voltage Feedback Amplifier, Monolithic Silicon Military Data sheet

**AN-348:** Avoiding Passive-Component Pitfalls

**AN-356:** User's Guide to Applying and Measuring Operational Amplifier Specifications

**UG-019:** Universal Evaluation Board for Dual, High Speed Op Amps Offered in 8-Lead SOT-23 Packages

## EVALUATION KITS & SYMBOLS & FOOTPRINTS

View the Evaluation Boards and Kits page for the AD8038

View the Evaluation Boards and Kits page for the AD8039

Symbols and Footprints for the AD8038

Symbols and Footprints for the AD8039

## PARAMETRIC SELECTION TABLES

Find Similar Products By Operating Parameters

High Speed Amplifiers Selection Table

## DESIGN TOOLS, MODELS, DRIVERS & SOFTWARE

dBm/dBu/dBv Calculator

Analog Filter Wizard 2.0

Power Dissipation vs Die Temp

**ADIsimOpAmp™**

OpAmp Stability

AD8038/AD8039 SPICE Macro-Model

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## SAMPLE & BUY

**AD8038**

**AD8039**

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# TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 5
Maximum Power Dissipation ... 5
Output Short Circuit ... 5
ESD Caution ... 5
Typical Performance Characteristics ... 6
Layout, Grounding, and Bypassing Considerations ... 13
Disable ... 13
Power Supply Bypassing ... 13
Grounding ... 13
Input Capacitance ... 13
Output Capacitance ... 13
Input-to-Output Coupling ... 13
Applications Information ... 14
Low Power ADC Driver ... 14
Low Power Active Video Filter ... 14
Outline Dimensions ... 15
Ordering Guide ... 16

## REVISION HISTORY

**8/09—Rev. F to Rev. G**

Changes to Applications Section and General Description Section ... 1
Changes to Disable Section and Grounding Section ... 13
Changes to Low Power ADC Driver Section and Low Power Active Video Filter Section ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 16

**8/04—Rev. E to Rev. F**

Changes to Figure 4 ... 10

**8/03—Rev. D to Rev. E**

Change to TPC 34 ... 8

**7/03—Rev. C to Rev. D**

Changes to Ordering Guide ... 4
Updated TPC 35 Caption ... 8

**6/03—Rev. B to Rev. C**

Updated Connection Diagrams ... 1
Updated Ordering Guide ... 4
Updated Outline Dimensions ... 11

**5/02—Rev. A to Rev. B**

Add Part Number AD8038 ... Universal
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Changes to Features ... 1
Changes to Product Description ... 1
Changes to Connection Diagram ... 1
Update to Specifications ... 2
Update to Maximum Power Dissipation ... 4
Update to Output Short Circuit ... 4
Update to Ordering Guide ... 4
Change to Figure 2 ... 4
Change to TPC 2 ... 5
Change to TPC 18 ... 6
Change to TPC 27 ... 7
Change to TPC 29 ... 8
Change to TPC 30 ... 8
Change to TPC 31 ... 8
Added TPC 36 ... 8
Added TPC 37 ... 9
Edits to Low Power Active Video Filter ... 10
Change to Figure 4 ... 10

**4/02—Rev. 0 to Rev. A**

Changes to Features ... 1
Update Specifications ... 2, 3
Edits to TPC 19 ... 7

# SPECIFICATIONS

$T_A$ = 25°C, $V_S$ = ±5 V, $R_L$ = 2 kΩ, Gain = +1, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | G = +1, $V_O$ = 0.5 V p-p | 300 | 350 | | MHz |
| | G = +2, $V_O$ = 0.5 V p-p | | 175 | | MHz |
| | G = +1, $V_O$ = 2 V p-p | | 100 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, $V_O$ = 0.2 V p-p | | 45 | | MHz |
| Slew Rate | G = +1, $V_O$ = 2 V step, $R_L$ = 2 kΩ | 400 | 425 | | V/µs |
| Overdrive Recovery Time | G = +2, 1 V overdrive | | 50 | | ns |
| Settling Time to 0.1% | G = +2, $V_O$ = 2 V step | | 18 | | ns |
| NOISE/HARMONIC PERFORMANCE | | | | | |
| SFDR | | | | | |
| Second Harmonic | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −90 | | dBc |
| Third Harmonic | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −92 | | dBc |
| Second Harmonic | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −65 | | dBc |
| Third Harmonic | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −70 | | dBc |
| Crosstalk, Output-to-Output (AD8039) | f = 5 MHz, G = +2 | | −70 | | dB |
| Input Voltage Noise | f = 100 kHz | | 8 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 600 | | fA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 0.5 | 3 | mV |
| Input Offset Voltage Drift | | | 4.5 | | µV/°C |
| Input Bias Current | | | 400 | 750 | nA |
| Input Bias Current Drift | | | 3 | | nA/°C |
| Input Offset Current | | | ±25 | | nA |
| Open-Loop Gain | $V_O$ = ±2.5 V | | 70 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 10 | | MΩ |
| Input Capacitance | | | 2 | | pF |
| Input Common-Mode Voltage Range | $R_L$ = 1 kΩ | | ±4 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = ±2.5 V | 61 | 67 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| DC Output Voltage Swing | $R_L$ = 2 kΩ, saturated output | | ±4 | | V |
| Capacitive Load Drive | 30% overshoot, G = +2 | | 20 | | pF |
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 12 | V |
| Quiescent Current per Amplifier | | | 1.0 | 1.5 | mA |
| Power Supply Rejection Ratio | −Supply | −71 | −77 | | dB |
| | +Supply | −64 | −70 | | dB |
| POWER-DOWN DISABLE[1] | | | | | |
| Turn-On Time | | | 180 | | ns |
| Turn-Off Time | | | 700 | | ns |
| Disable Voltage—Part is Off | | | $+V_S$ − 4.5 | | V |
| Disable Voltage—Part is On | | | $+V_S$ − 2.5 | | V |
| Disabled Quiescent Current | | | 0.2 | | mA |
| Disabled In/Out Isolation | f = 1 MHz | | −60 | | dB |

[1] Only available in AD8038 8-lead SOIC package.

$T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 2 kΩ to $V_S$/2, Gain = +1, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | G = +1, $V_O$ = 0.2 V p-p | 275 | 300 | | MHz |
| | G = +2, $V_O$ = 0.2 V p-p | | 150 | | MHz |
| | G = +1, $V_O$ = 2 V p-p | | 30 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, $V_O$ = 0.2 V p-p | | 45 | | MHz |
| Slew Rate | G = +1, $V_O$ = 2 V step, $R_L$ = 2 kΩ | 340 | 365 | | V/µs |
| Overdrive Recovery Time | G = +2, 1 V overdrive | | 50 | | ns |
| Settling Time to 0.1% | G = +2, $V_O$ = 2 V step | | 18 | | ns |
| NOISE/HARMONIC PERFORMANCE | | | | | |
| SFDR | | | | | |
| Second Harmonic | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −82 | | dBc |
| Third Harmonic | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −79 | | dBc |
| Second Harmonic | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −60 | | dBc |
| Third Harmonic | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 2 kΩ | | −67 | | dBc |
| Crosstalk, Output-to-Output | f = 5 MHz, G = +2 | | −70 | | dB |
| Input Voltage Noise | f = 100 kHz | | 8 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 600 | | fA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 0.8 | 3 | mV |
| Input Offset Voltage Drift | | | 3 | | µV/°C |
| Input Bias Current | | | 400 | 750 | nA |
| Input Bias Current Drift | | | 3 | | nA/°C |
| Input Offset Current | | | ±30 | | nA |
| Open-Loop Gain | $V_O$ = ±2.5 V | | 70 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 10 | | MΩ |
| Input Capacitance | | | 2 | | pF |
| Input Common-Mode Voltage Range | $R_L$ = 1 kΩ | | 1.0 – 4.0 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = ±1 V | 59 | 65 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| DC Output Voltage Swing | $R_L$ = 2 kΩ, saturated output | | 0.9 – 4.1 | | V |
| Capacitive Load Drive | 30% overshoot | | 20 | | pF |
| POWER SUPPLY | | | | | |
| Operating Range | | 3 | | 12 | V |
| Quiescent Current per Amplifier | | | 0.9 | 1.5 | mA |
| Power Supply Rejection Ratio | | −65 | −71 | | dB |
| POWER-DOWN DISABLE[1] | | | | | |
| Turn-On Time | | | 210 | | ns |
| Turn-Off Time | | | 700 | | ns |
| Disable Voltage—Part is Off | | | $+V_S$ – 4.5 | | V |
| Disable Voltage—Part is On | | | $+V_S$ – 2.5 | | V |
| Disabled Quiescent Current | | | 0.2 | | mA |
| Disabled In/Out Isolation | f = 1 MHz | | −60 | | dB |

[1] Only available in AD8038 8-lead SOIC package.

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 12.6 V |
| Power Dissipation | See Figure 5 |
| Common-Mode Input Voltage | $\pm V_S$ |
| Differential Input Voltage | ±4 V |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8038/AD8039 package is limited by the associated rise in junction temperature ($T_J$) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8038/AD8039. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB ($\theta_{JA}$), ambient temperature ($T_A$), and total power dissipated in the package ($P_D$) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins ($V_S$) multiplied by the quiescent current ($I_S$). Assuming the load ($R_L$) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{quiescent power} + (\textit{total drive power} - \textit{load power})$$

$$P_D = [V_S \times I_S] + [(V_S/2) \times (V_{OUT}/R_L)] - [V_{OUT}^2/R_L]$$

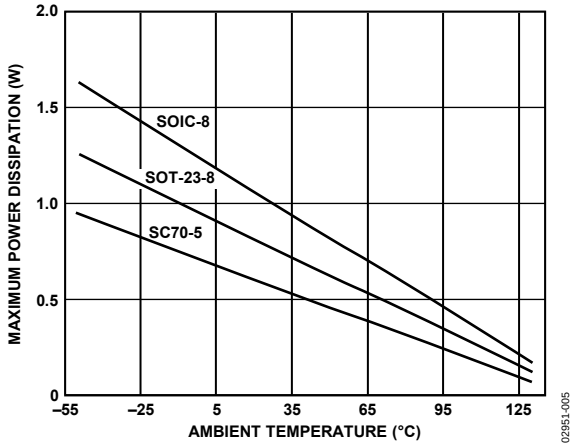



*Figure 5. Maximum Power Dissipation vs. Temperature for a 4-Layer Board*

RMS output voltages should be considered. If $R_L$ is referenced to $V_{S-}$, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for $R_L$ to midsupply

$$P_D = (V_S \times I_S) + (V_S/4)^2/R_L$$

In single-supply operation with $R_L$ referenced to $V_{S-}$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads from metal traces, throughholes, ground, and power planes reduce the $\theta_{JA}$. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Layout, Grounding, and Bypassing Considerations section.

Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (125°C/W), 5-lead SC70 (210°C/W), and 8-lead SOT-23 (160°C/W) packages on a JEDEC standard 4-layer board. $\theta_{JA}$ values are approximations.

## OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current from the AD8038/AD8039 will likely cause a catastrophic failure.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: ±5 V, $C_L$ = 5 pF, G = +2, $R_G$ = $R_F$ = 1 kΩ, $R_L$ = 2 kΩ, $V_O$ = 2 V p-p, Frequency = 1 MHz, $T_A$ = 25°C.

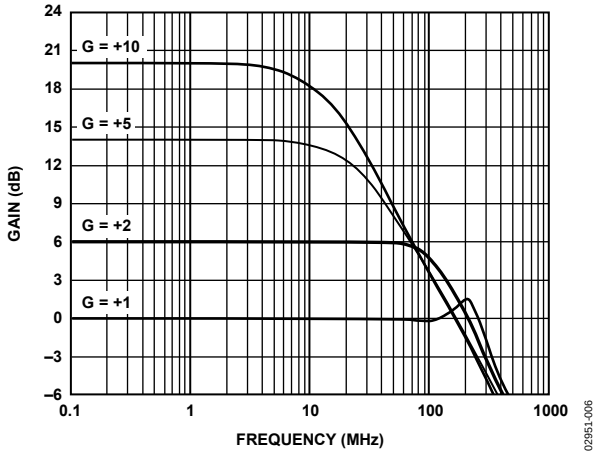



*Figure 6. Small Signal Frequency Response for Various Gains, $V_{OUT}$ = 500 mV p-p*

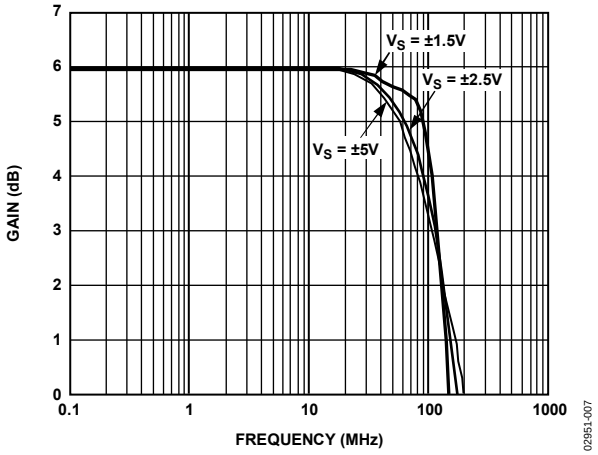



*Figure 7. Small Signal Frequency Response for Various Supplies, $V_{OUT}$ = 500 mV p-p*

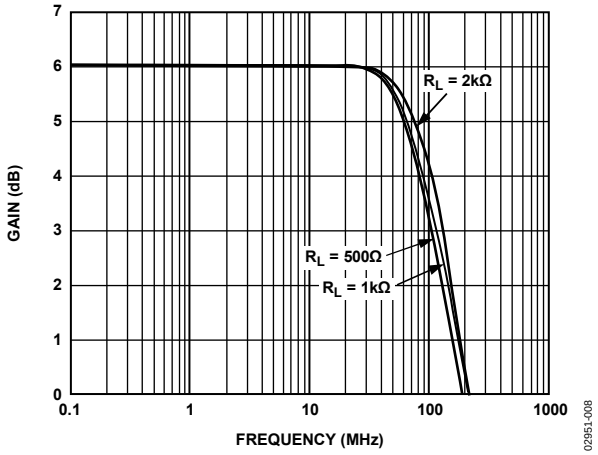



*Figure 8. Small Signal Frequency Response for Various $R_L$, $V_S$ = ±5 V, $V_{OUT}$ = 500 mV p-p*

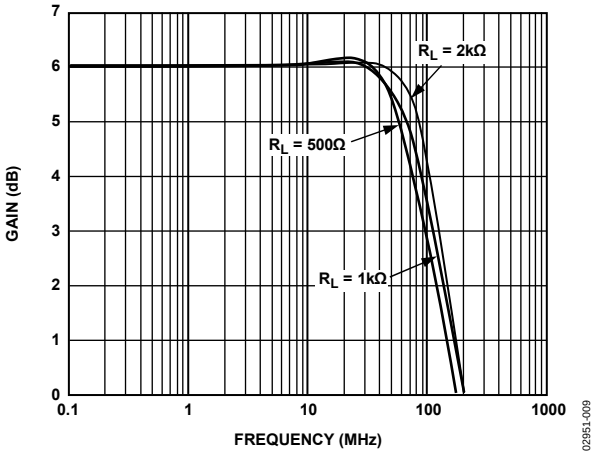



*Figure 9. Small Signal Frequency Response for Various $R_L$, $V_S$ = 5 V, $V_{OUT}$ = 500 mV p-p*

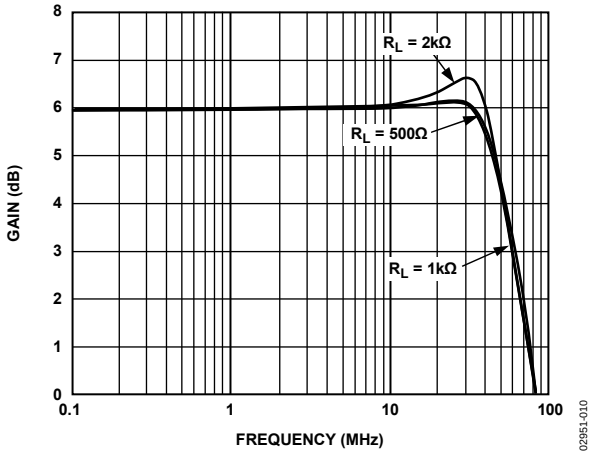



*Figure 10. Large Signal Frequency Response for Various $R_L$, $V_{OUT}$ = 3 V p-p, $V_S$ = 5 V*

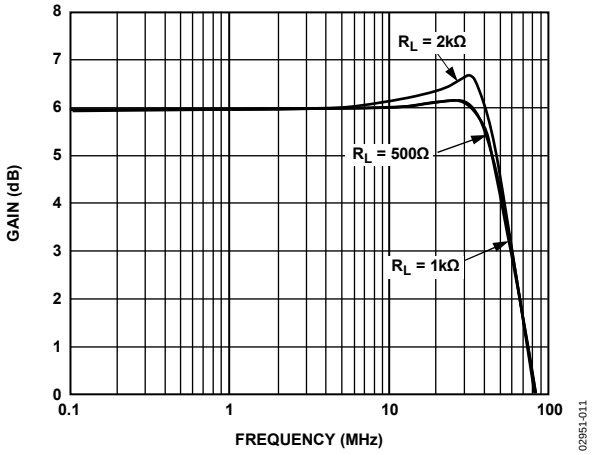



*Figure 11. Large Signal Frequency Response for Various $R_L$, $V_{OUT}$ = 4 V p-p, $V_S$ = ±5 V*

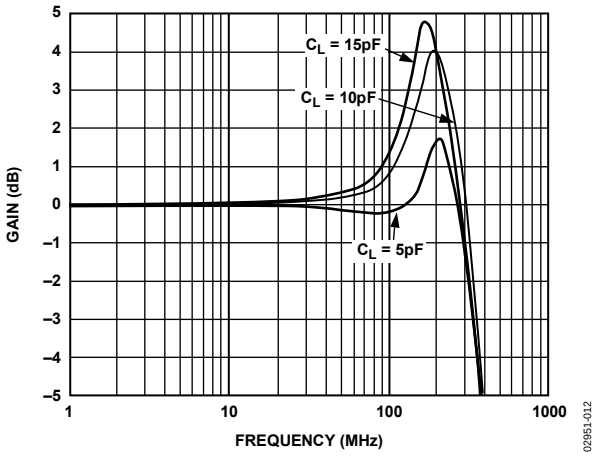



Figure 12. Small Signal Frequency Response for Various $C_L$, $V_{OUT}$ = 500 mV p-p, $V_S$ = ±5 V, G = +1

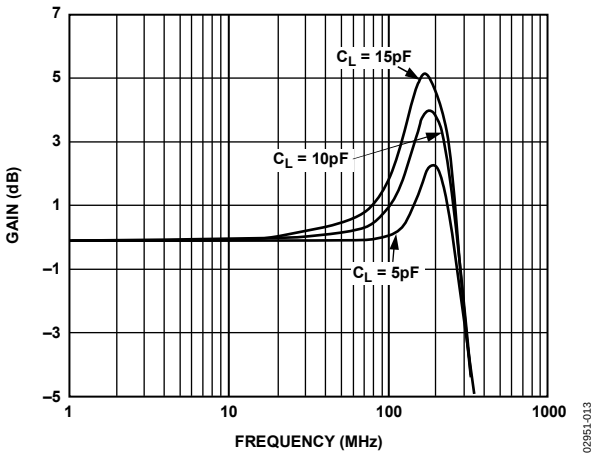



Figure 13. Small Signal Frequency Response for Various $C_L$, $V_{OUT}$ = 500 mV p-p, $V_S$ = 5 V, G = +1

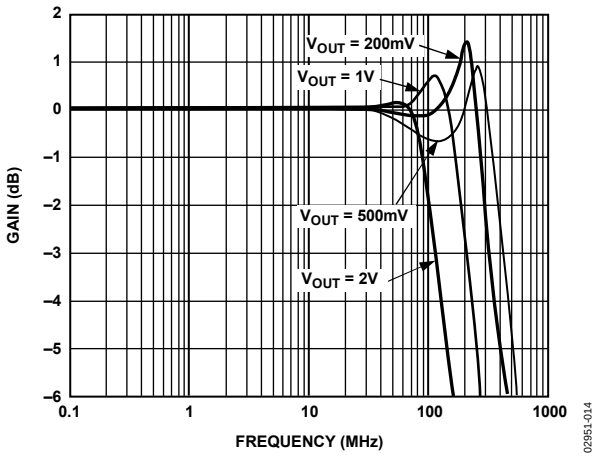



Figure 14. Frequency Response for Various Output Voltage Levels

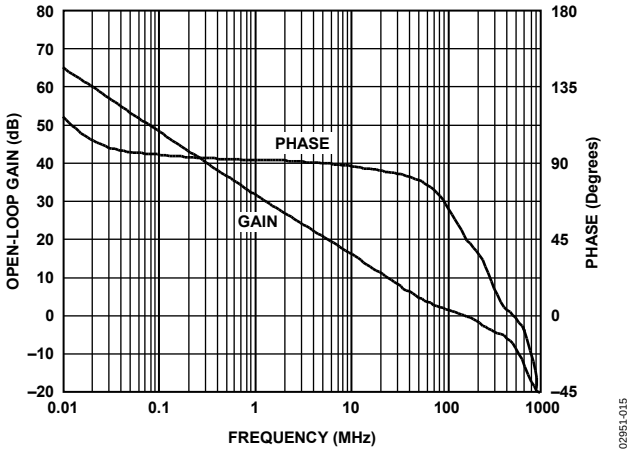



Figure 15. Open-Loop Gain and Phase, $V_S$ = ±5 V

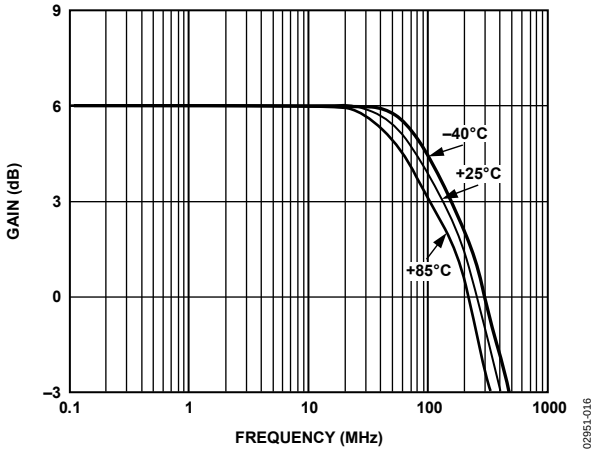



Figure 16. Frequency Response vs. Temperature, Gain = +2, $V_S$ = ±5 V, $V_{OUT}$ = 2 V p-p

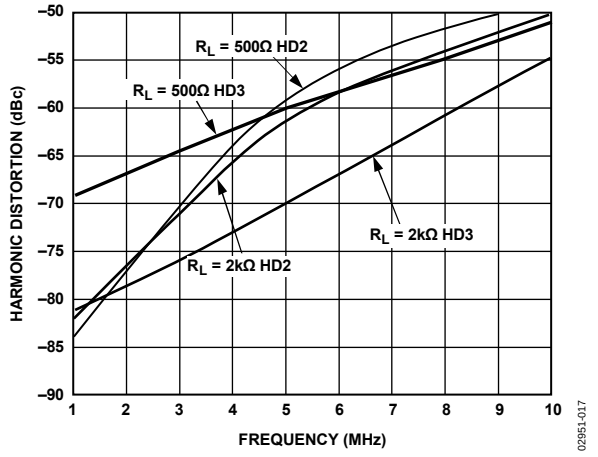



Figure 17. Harmonic Distortion vs. Frequency for Various Loads, $V_S$ = ±5 V, $V_{OUT}$ = 2 V p-p, G = +2

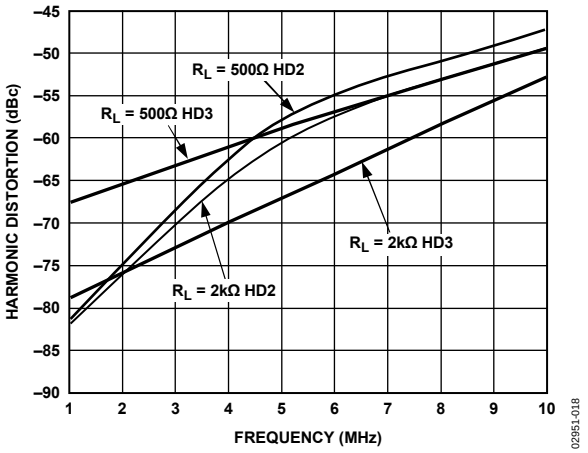



Figure 18. Harmonic Distortion vs. Frequency for Various Loads, $V_S$ = 5 V, $V_{OUT}$ = 2 V p-p, G = +2

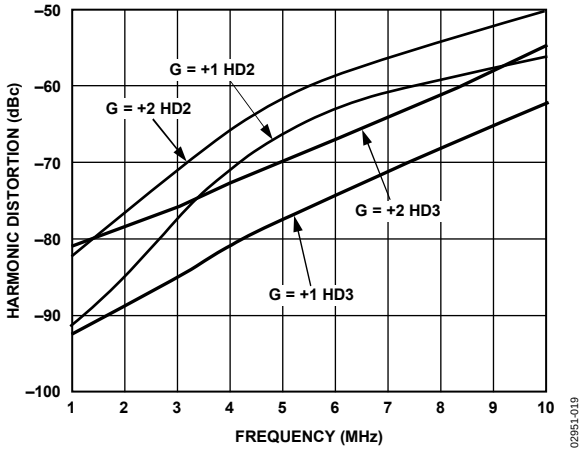



Figure 19. Harmonic Distortion vs. Frequency for Various Gains, $V_S$ = ±5 V, $V_{OUT}$ = 2 V p-p

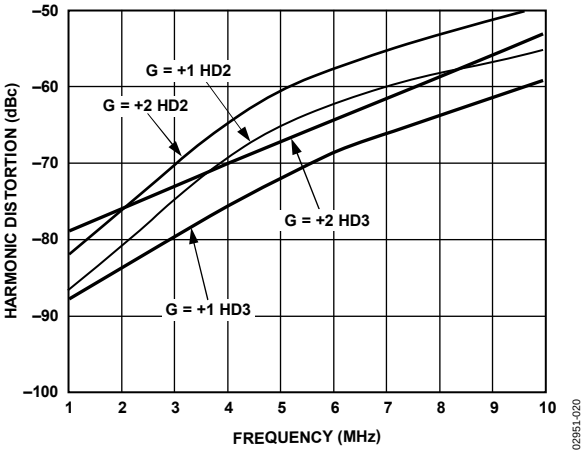



Figure 20. Harmonic Distortion vs. Frequency for Various Gains, $V_S$ = 5 V, $V_{OUT}$ = 2 V p-p

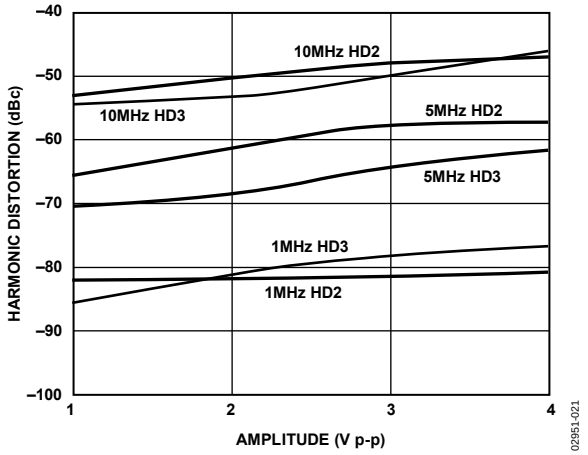



Figure 21. Harmonic Distortion vs. $V_{OUT}$ Amplitude for Various Frequencies, $V_S$ = ±5 V, G = +2

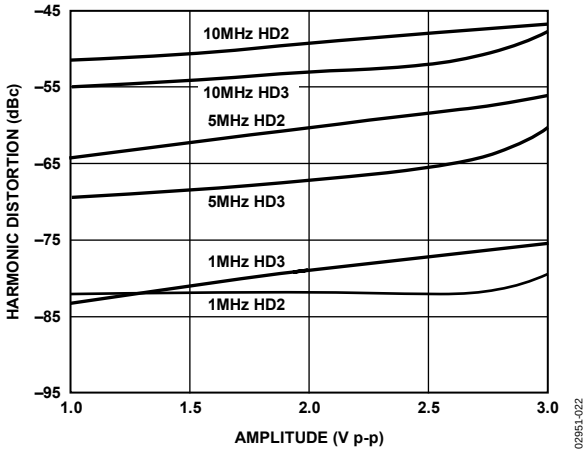



Figure 22. Harmonic Distortion vs. Amplitude for Various Frequencies, $V_S$ = 5 V, G = +2

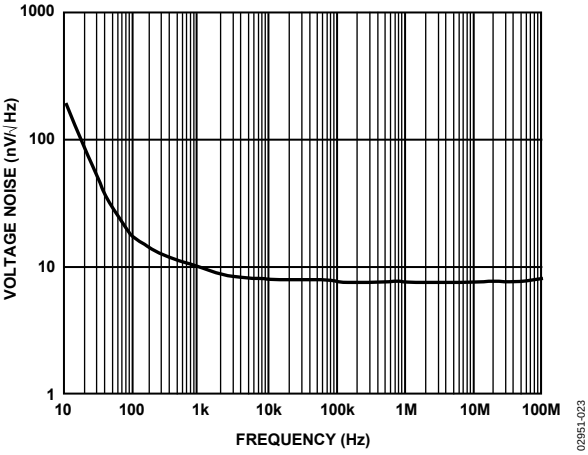



Figure 23. Input Voltage Noise vs. Frequency

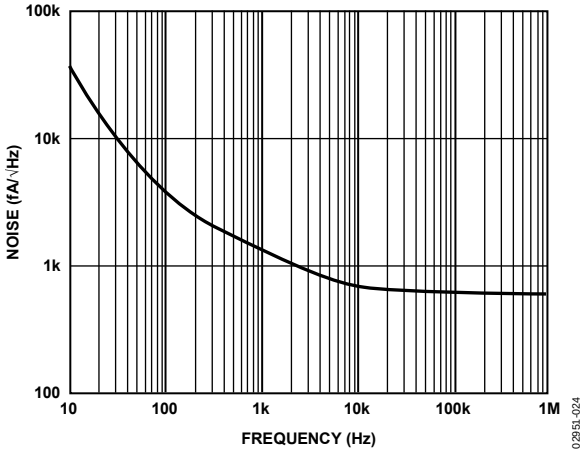



Figure 24. Input Current Noise vs. Frequency

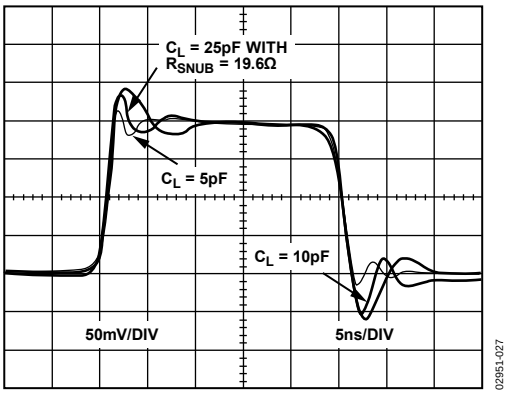



Figure 27. Small Signal Transient Response for Various $C_L$, $V_S$ = 5 V

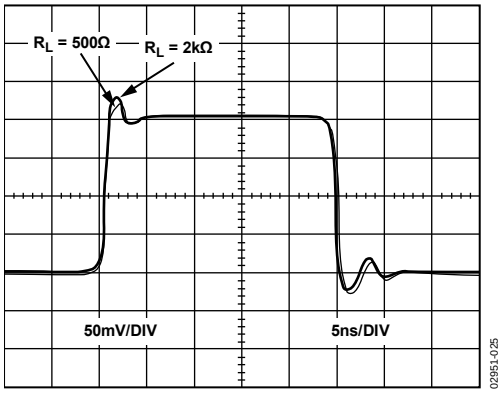



Figure 25. Small Signal Transient Response for Various $R_L$, $V_S$ = 5 V

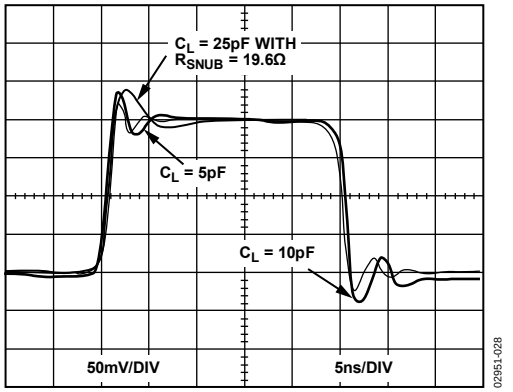



Figure 28. Small Signal Transient Response for Various $C_L$, $V_S$ = ±5 V

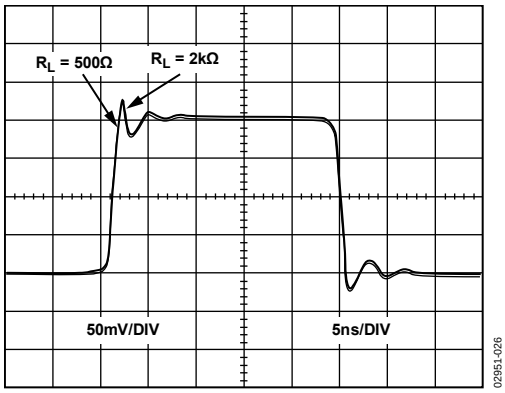



Figure 26. Small Signal Transient Response for Various $R_L$, $V_S$ = ±5 V

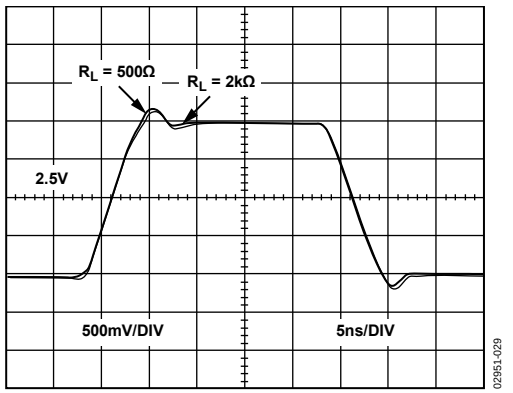



Figure 29. Large Signal Transient Response for Various $R_L$, $V_S$ = 5 V

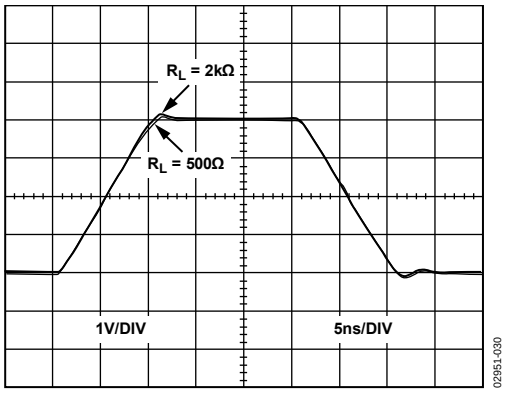



Figure 30. Large Signal Transient Response for Various $R_L$, $V_S$ = ±5 V

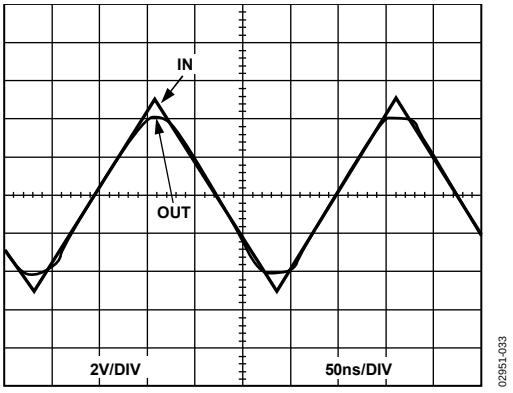



Figure 33. Input Overdrive Recovery, Gain = +1

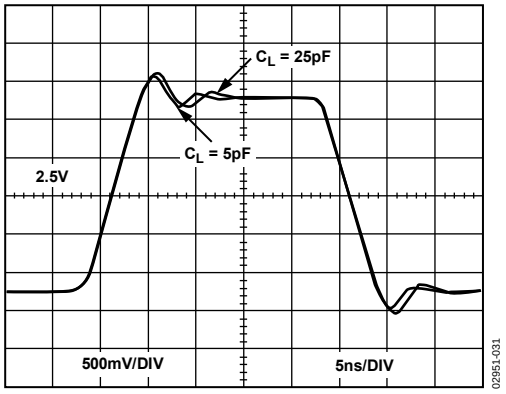



Figure 31. Large Signal Transient Response for Various $C_L$, $V_S$ = 5 V

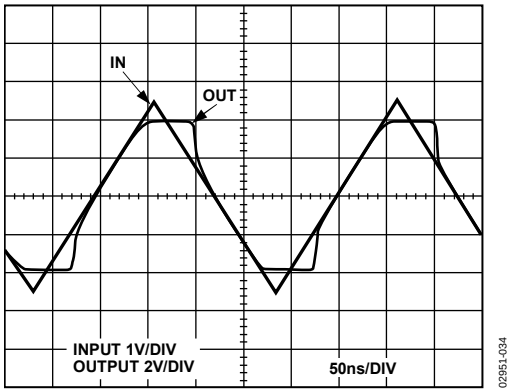



Figure 34. Output Overdrive Recovery, Gain = +2

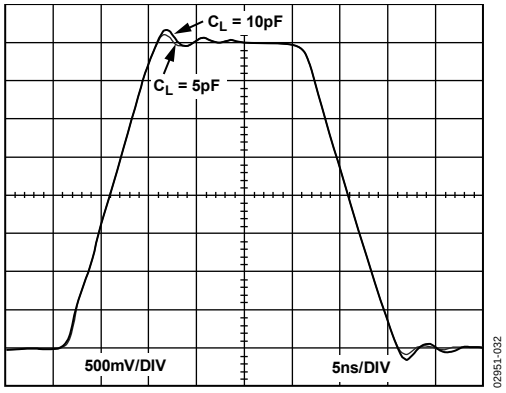



Figure 32. Large Signal Transient Response for Various $C_L$, $V_S$ = ±5 V

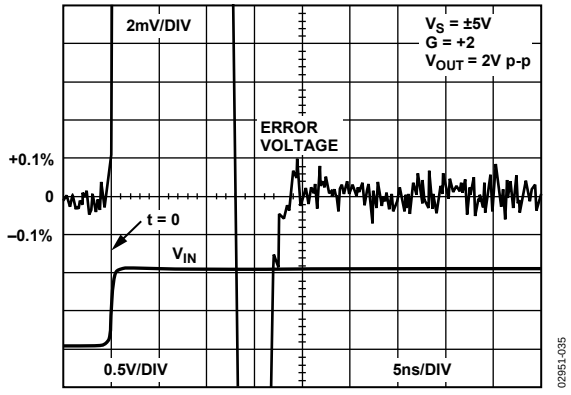



Figure 35. 0.1% Settling Time $V_{OUT}$ = 2 V p-p

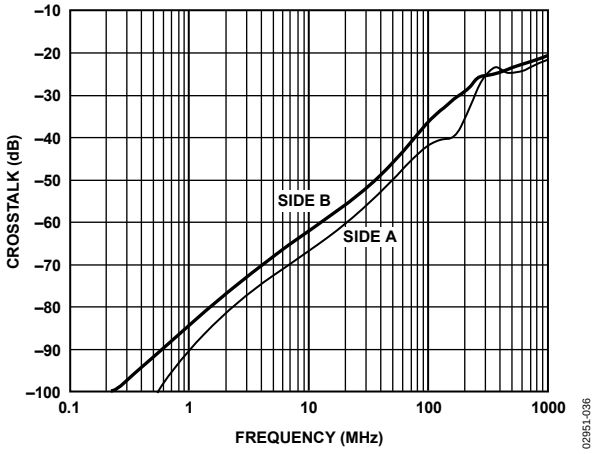



Figure 36. AD8039 Crosstalk, $V_{IN}$ = 1 V p-p, Gain = +1

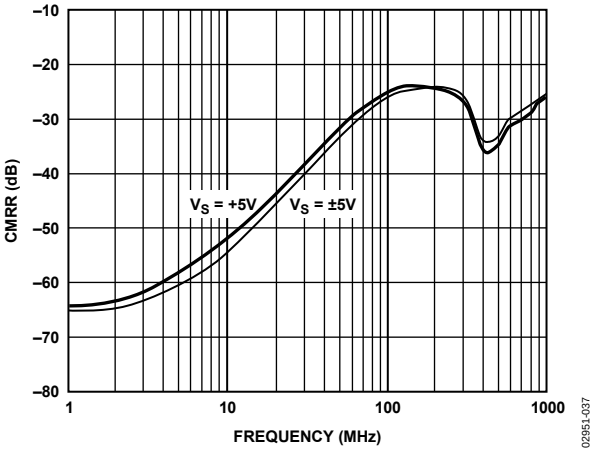



Figure 37. CMRR vs. Frequency, $V_{IN}$ = 1 V p-p

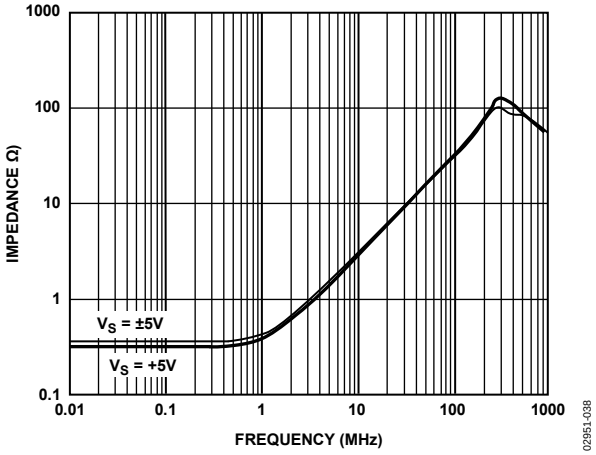



Figure 38. Output Impedance vs. Frequency

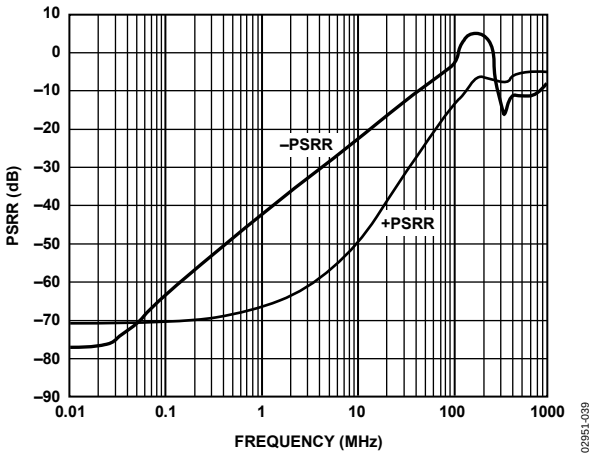



Figure 39. PSRR vs. Frequency

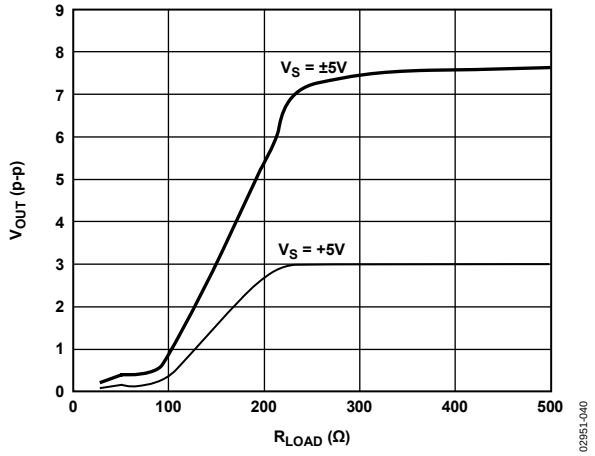



Figure 40. Output Swing vs. Load Resistance

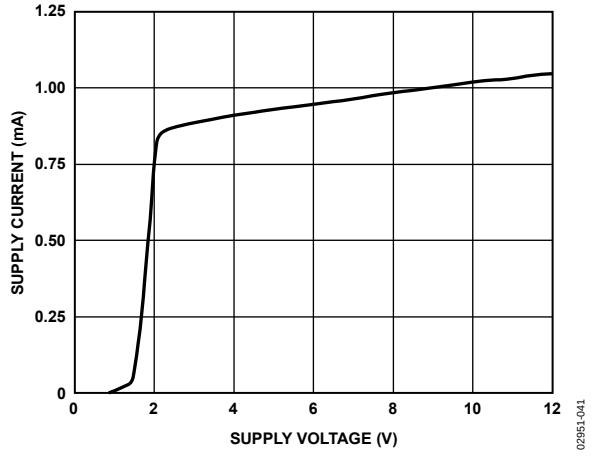



Figure 41. AD8038 Supply Current vs. Supply Voltage

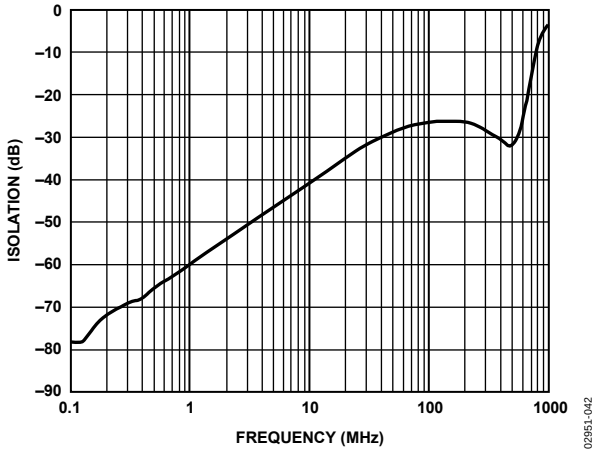



*Figure 42. AD8038 Input-Output Isolation (G = +2, $R_L$ = 2 kΩ, $V_S$ = ±5 V)*

# LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

## DISABLE

The AD8038 in the 8-lead SOIC package provides a disable feature. This feature disables the input from the output (see Figure 42 for input-output isolation) and reduces the quiescent current from typically 1 mA to 0.2 mA. When the $\overline{\text{DISABLE}}$ node is pulled below 4.5 V from the positive supply rail, the part becomes disabled. To enable the part, the $\overline{\text{DISABLE}}$ node needs to be pulled to greater than ($V_S$ – 2.5).

## POWER SUPPLY BYPASSING

Power supply pins are actually inputs, and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise.

Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. The 0.01 μF or 0.001 μF (X7R or NPO) chip capacitors are critical and should be placed as close as possible to the amplifier package. Larger chip capacitors, such as 0.1 μF capacitors, can be shared among a few closely spaced active components in the same signal path. A 10 μF tantalum capacitor is less critical for high frequency bypassing and, in most cases, only one per board is needed at the supply inputs.

## GROUNDING

A ground plane layer is important in densely packed PC boards to spread the current minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise.

The length of the high frequency bypass capacitor leads is most critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

## INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduces the input impedance at high frequencies, in turn increasing the gain of the amplifiers, causing peaking of the frequency response, or even oscillations if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

## OUTPUT CAPACITANCE

To a lesser extent, parasitic capacitances on the output can cause peaking of the frequency response. Two methods to minimize this effect include the following:

- Put a small value resistor in series with the output to isolate the load capacitor from the output stage of the amplifier, see Figure 12, Figure 13, Figure 27, and Figure 28.
- Increase the phase margin with higher noise gains or add a pole with a parallel resistor and capacitor from –IN to the output.

## INPUT-TO-OUTPUT COUPLING

The input and output signal traces should not be parallel to minimize capacitive coupling between the inputs and outputs, avoiding any positive feedback.

# APPLICATIONS INFORMATION

## LOW POWER ADC DRIVER

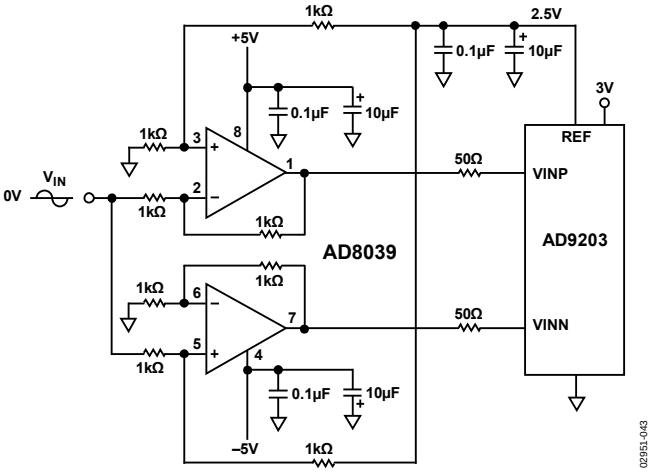



*Figure 43. Schematic to Drive AD9203 with the AD8039*

The AD9203 is a low power (125 mW on a 5 V supply), 40 MSPS 10-bit converter. As such, the low power, high performance AD8039 is an appropriate amplifier choice to drive it.

In low supply voltage applications, differential analog inputs are needed to increase the dynamic range of the ADC inputs. Differential driving can also reduce second and other even-order distortion products. The AD8039 can be used to make a dc-coupled, single-ended-to-differential driver for driving these ADCs. Figure 43 is a schematic of such a circuit for driving the AD9203, 10-bit, 40 MSPS ADC.

The AD9203 works best when the common-mode voltage at the input is at the midsupply or 2.5 V. The output stage design of the AD8039 makes it ideal for driving these types of ADCs.

In this circuit, one of the op amps is configured in the inverting mode, and the other is in the noninverting mode. However, to provide better bandwidth matching, each op amp is configured for a noise gain of +2. The inverting op amp is configured for a gain of −1, and the noninverting op amp is configured for a gain of +2. Each has a very similar ac response. The input signal to the noninverting op amp is divided by 2 to normalize its voltage level and make it equal to the inverting output.

The outputs of the op amps are centered at 2.5 V, which is the midsupply level of the ADC. This is accomplished by first taking the 2.5 V reference output of the ADC and dividing it by 2 with a pair of 1 kΩ resistors. The resulting 1.25 V is applied to the positive input of each op amp. This voltage is then multiplied by the gain of the op amps to provide a 2.5 V level at each output.

## LOW POWER ACTIVE VIDEO FILTER

Some composite video signals derived from a digital source contain clock feedthrough that can limit picture quality. Active filters made from op amps can be used in this application, but they consume 25 mW to 30 mW for each channel. In power-sensitive applications, this can be too much, requiring the use of passive filters that can create impedance matching problems when driving any significant load.

The AD8038 can be used to make an effective low-pass active filter that consumes one-fifth of the power consumed by an active filter made from an op amp. Figure 44 shows a circuit that uses a AD8038 with ±2.5 V supplies to create a three-pole Sallen-Key filter. This circuit uses a single RC pole in front of a standard 2-pole active section.

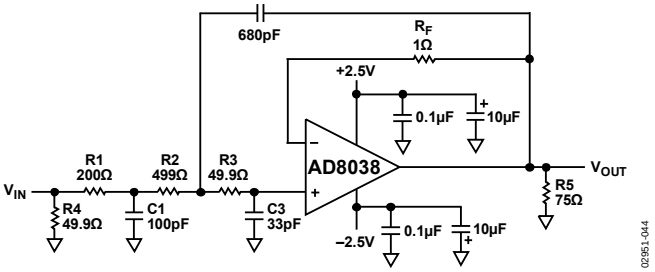



*Figure 44. Low-Pass Filter for Video*

Figure 45 shows the frequency response of this filter. The response is down 3 dB at 6 MHz; therefore, it passes the video band with little attenuation. The rejection at 27 MHz is 45 dB, which provides more than a factor of 100 in suppression of the clock components at this frequency.

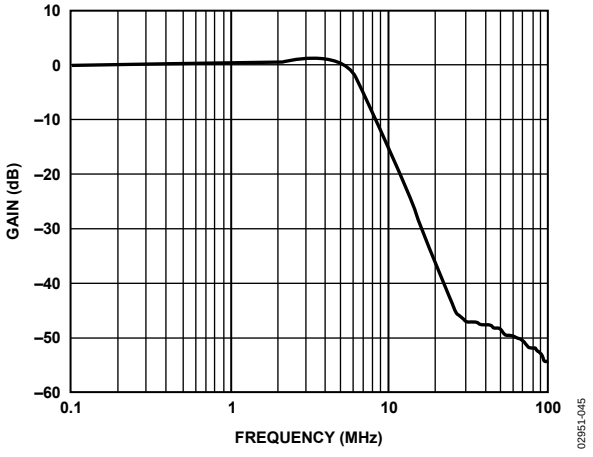



*Figure 45. Video Filter Response*

# OUTLINE DIMENSIONS

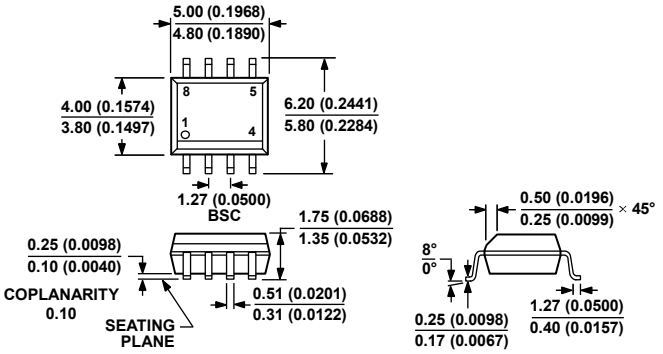



*Figure 46. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

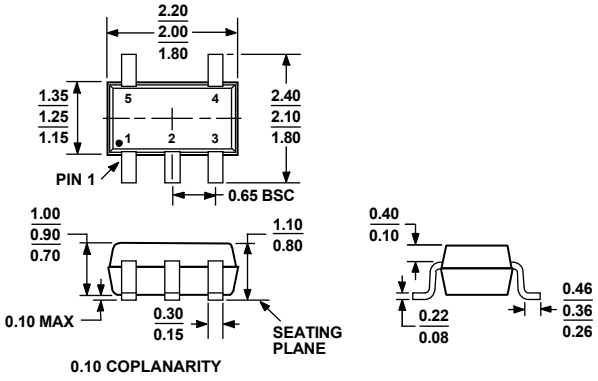
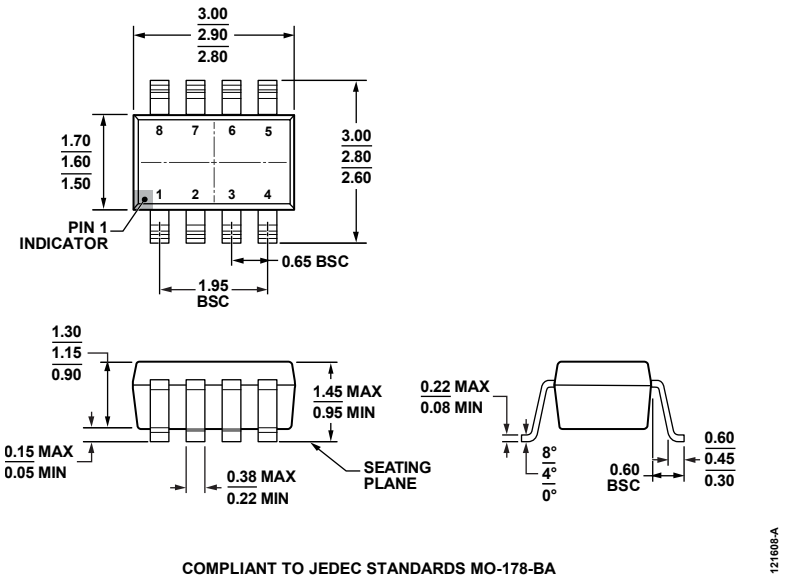



*Figure 47. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]*
*(KS-5)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-178-BA

*Figure 48. 8-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8038AR | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038AR-REEL | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038AR-REEL7 | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038ARZ[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038ARZ-REEL[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038ARZ-REEL7[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8038AKSZ-R2[1] | −40°C to +85°C | 5-Lead Thin Shrink Small Outline Transistor Package [SC70] | KS-5 | H1C |
| AD8038AKSZ-REEL[1] | −40°C to +85°C | 5-Lead Thin Shrink Small Outline Transistor Package [SC70] | KS-5 | H1C |
| AD8038AKSZ-REEL7[1] | −40°C to +85°C | 5-Lead Thin Shrink Small Outline Transistor Package [SC70] | KS-5 | H1C |
| AD8039AR | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039AR-REEL | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039AR-REEL7 | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039ARZ[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039ARZ-REEL[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039ARZ-REEL7[1] | −40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| AD8039ART-R2 | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA |
| AD8039ART-REEL | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA |
| AD8039ART-REEL7 | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA |
| AD8039ARTZ-R2[1] | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA# |
| AD8039ARTZ-REEL[1] | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA# |
| AD8039ARTZ-REEL7[1] | −40°C to +85°C | 8-Lead Small Outline Transistor Package [SOT-23] | RJ-8 | HYA# |

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked..

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