

# **IGBT/MOSFET Applications based on**

## **Coreless Transformer Driver IC 2ED020I12-F**

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Driver IC's either for IGBT's or MOSFET's are commonly used in several power electronics applications. Here the problem of isolating the high and low side driver stages occurs. Currently almost all of these applications are based on optocouplers, discrete transformers or level-shifters for either safety or functional isolation. This paper presents a new approach based on the coreless transformer driver IC 2ED020I12-F and, furthermore, gives an outlook on upcoming developments.

### **Coreless Transformer Technology (CLT)**

Nowadays the common solution to realize either functional or safety isolation for low and medium power applications is the usage of optocouplers, discrete transformers, or monolithic level-shifters. All of them have their typical advantages and disadvantages which are well known. The primary goal of the coreless transformer technology is to combine these advantages by avoiding at the same time the disadvantages. This means in detail a high insulation capability, no ageing and therefore constant reliability over the projected lifetime, small package size, easy integration of additional logic functions, and cost effective production. The basic principle of the CLT is the implementation of a microplanar transformer embedded within the semiconductor process. The transformer provides the galvanic isolation and signal transmission between input and output stage.

### **Half-bridge driver 2ED020I12-F**

The development of the driver IC 2ED020I12-F was driven by the idea to improve today's driver solutions based on integrated circuits like monolithic level shifters or multiple component scenarios of separate driver IC's and optocouplers or discrete transformers.

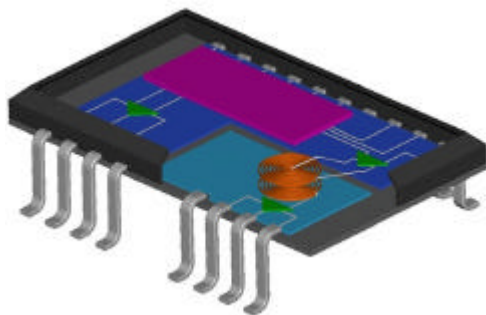


Figure 1: Simplified schematic of 2ED020I12-F

The 2ED020I12-F contains two drivers for an IGBT or MOSFET half-bridge, whereby the high side is galvanically isolated from the low side part through a coreless transformer system as described before. The main features of the IC are:

- Fully operational up to 1200V<sub>DC</sub>
- Drive supply range from 0V to +18V
- Drive peak output current of +1A / -2A

Due to the used CLT and SPT5 technology short propagation delays of 50ns and a delay mismatch of  $\pm 10$ ns can be achieved. As an additional feature a general purpose operational amplifier and a comparator with open collector output are implemented.

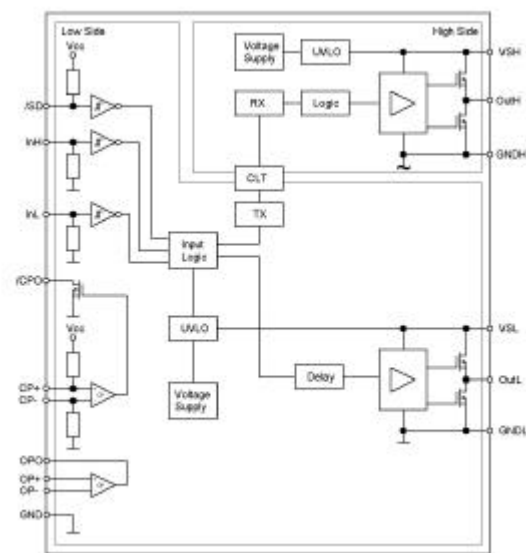


Figure 2: Block diagram of 2ED020I12-F

## Driver EMI ruggedness

Besides the insulation capability, a further key point necessary for the usage as a driver in an industrial environment is important: The ruggedness against high  $dV/dt$  disturbance and an overall immunity against the change of external magnetic fields. Concerning the 2ED020I12-F the critical component in terms of EMI seems to be the coreless transformer and associated receiver circuitry. Tests conducted have proved that the 2ED020I12-F is immune against  $dV/dt$  of at least  $50\text{ kV}/\mu\text{s}$  as well as  $dH/dt$  greater than  $100 \frac{\text{A}}{\text{m} \cdot \text{ns}}$ . Among other things this

is attained by a small coupling capacitance of less than  $0.2\text{pF}$ , reduced internal parasitic capacitances and the magnetic shielding of the lead frame.

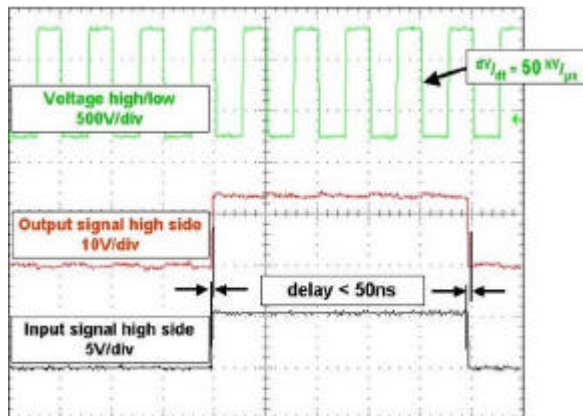


Figure 3: Immunity against  $dV/dt$  disturbance

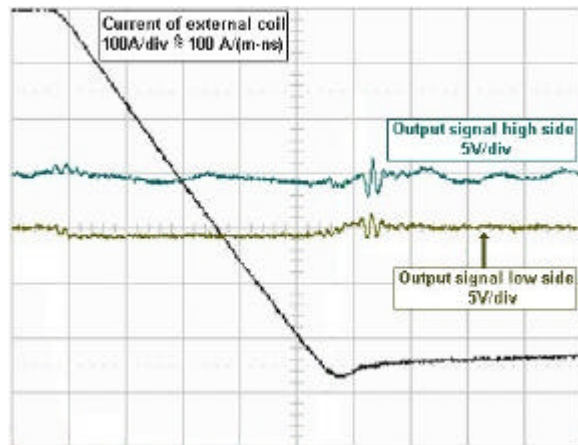


Figure 4: Immunity against  $dH/dt$  disturbance

## Considerations for unipolar driver stages

Generally datasheets of IGBT modules refer to a gate drive voltage from  $-15\text{V}$  to  $+15\text{V}$ . However, the 2ED020I12-F provides a gate voltage  $0\text{V}$  to

$+15\text{V}$ . This requires a closer look at how values like the gate resistor  $R_G$ , turn-on losses  $E_{\text{on}}$ , turn-off losses  $E_{\text{off}}$ , turn-on delay times  $t_{\text{d,on}}$ , and turn-off delay times  $t_{\text{d,off}}$  depend on the driving gate voltage.

The gate resistor – as one of the main factors – in general determines the turn-off losses of an IGBT. To calculate the gate resistor for a specific turn-off loss at unipolar switching the following

rule of thumb applies:  $R_{0/15} \approx \frac{1}{3} R_{-15/15}$ . The

factor  $\frac{1}{3}$  is derived from the relation

of  $\frac{V_{\text{MP}} - 0\text{V}}{V_{\text{MP}} - (-15\text{V})}$  and assumes that the Miller-

Plateau voltage  $V_{\text{MP}}$  has a value between  $+8\text{V}$  and  $+10\text{V}$  depending on several factors like the IGBT chip and collector current.

Figure 5 proves the rule to be sufficiently accurate by a measurement of the losses  $E_{\text{off}} = f(R_G)$  at different gate voltages for an IGBT. It can be seen that for the same losses of

$E_{\text{off}} \approx 1,55\text{mJ}$  the factor of  $\frac{1}{3}$  matches quite well to  $R_{0/15} = 62\Omega$  and  $R_{-15/15} = 180\Omega$ .

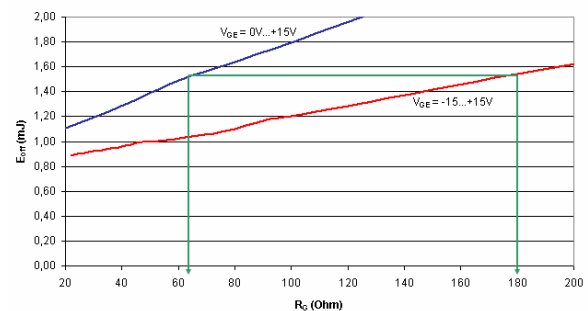


Figure 5: Comparison  $E_{\text{off}} = f(R_G)$

In contrast to the turn-off losses there are no differences for the specific turn-on losses between a driver stage providing  $-15\text{V}$  to  $+15\text{V}$  or  $0\text{V}$  to  $+15\text{V}$ . The reason for this is that the losses depend on the collector current  $I_c$  of the IGBT. Hence,  $I_c$  itself depends on the provided gate voltage, i.e. according to the transfer characteristic as shown in Figure 6 the collector current will only flow in case the gate voltage is above  $0\text{V}$ . Therefore, it makes no difference whether that starting point of the driving gate voltage source is at  $-15\text{V}$  or  $0\text{V}$ .

The benefit of bipolar gate voltages is the suppression of transient EMI voltages during switched-off IGBT's. This is a major concern in

medium to high power applications, but negligible for low to medium power applications.

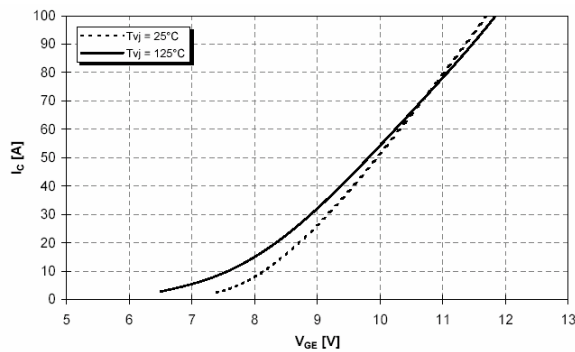


Figure 6: Transfer characteristic

Comparing the turn-on delay times with 0V to +15V and -15V to +15V switching the IGBT has in general lower delay times as shown in a measurement for several values of  $R_G$  in Figure 7.

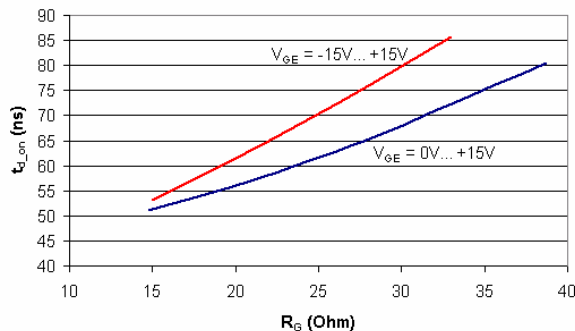


Figure 7: Comparison  $t_{d,on} = f(R_G)$

On the other hand concerning the turn-off delay times with 0V to +15V gate voltage the IGBT has larger delay times than with a -15V to +15V driver stage as shown in Figure 8.

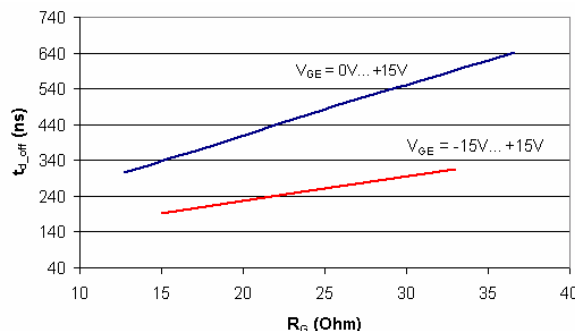


Figure 8: Comparison  $t_{d,off} = f(R_G)$

## Applications

The 2ED020I12-F is a driver IC not only for IGBT's, but due to the rated maximum switching frequency of up to 60kHz without degradation also suitable for MOSFET's. This opens the way for applications like:

- 3-phase low and medium power converters for AC and BLDC drives
- H-Bridges for DC drives or SMPS

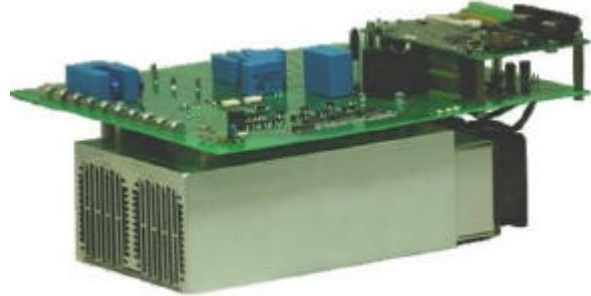


Figure 9: 15kVA converter with 2ED020I12-F

## External circuitry

A convenient solution for the power supply of the high side of the driver is realized by a bootstrap circuit. As an alternative a separate floating power supply provided by an SMPS might be used. The simple bootstrap circuit contains a suitable diode and capacitor. The selection of these devices is determined by several factors:

- The blocking voltage of the diode must withstand the DC-Link voltage. Thus, for 800V systems a 1200V diode is the proper choice.
- The voltage provided by the capacitor has to be maintained at a value greater than the UVLO threshold of the driver. The value of the bootstrap capacitor can be estimated with enough safety by the following rule of thumb:

$$C \geq 30 \frac{2Q_G + \frac{I_q + I_L}{f_S}}{V_{DD} - V_F - V_{CE}}$$

$Q_G$ : Gate charge of driven IGBT or MOSFET

$I_q$ : Quiescent current of driver IC

$I_L$ : Leakage current of capacitor (only relevant for electrolytic capacitors)

$f_S$ : Switching frequency

$V_{DD}$ : Supply voltage

$V_F$ : Bootstrap diode forward voltage drop

$V_{CE}$ : Collector-emitter voltage drop of low side IGBT (source-drain voltage for MOSFET)

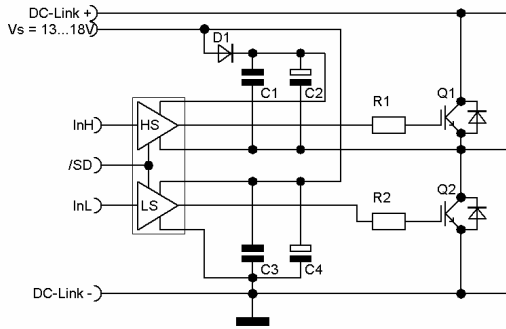


Figure 10: Bootstrap circuit

The low side driver is able to manage ground bounces of typical medium power inverters. Nevertheless, the ground pins GND and GNDL of the IC have to be connected externally in the shortest possible way (see Figure 11). In this way any voltage drop due to ground bounce is reduced. Thereby, the reference ground of the driver has to be defined in accordance with the applications. For instance:

- In case no shunt resistor is used, the driver ground is equal to the low side IGBT emitter or MOSFET source respectively.
- When using a shunt resistor the ground of the driver has to be connected either to the low side emitter or source. In this case the ground of the driver and for instance the  $\mu$ Controller are separated by the shunt resistor. This assures that the current through the shunt resistor does not contain any gate current.

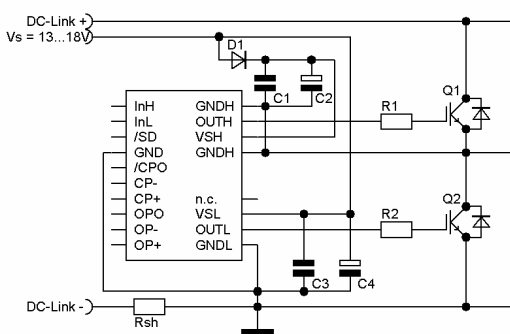


Figure 11: Ground reference at low side emitter

- In another scenario the ground of the driver is on the same level as the  $\mu$ Controller and the shunt resistor will

work as an additional common low side emitter or source resistor.

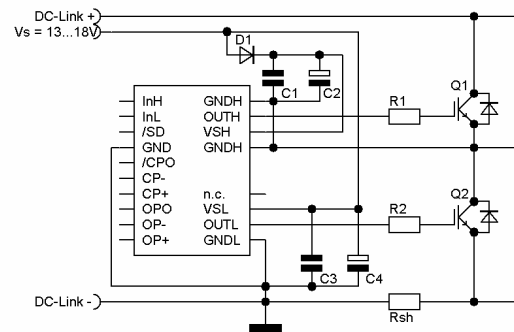


Figure 12: Ground reference at negative DC-Link

For low and even several medium power applications it is basically sufficient to connect an IGBT or MOSFET with the 2ED020112-F through a gate resistor, of which the value is determined

$$\text{by the formula } R_{G(\min)} = \frac{\Delta V_{GE}}{I_{G(\max)}}.$$

$R_{G(\min)}$ : Minimum gate resistor value. Considering also any internal resistor values within the driver and IGBT/MOSFET itself.

$\Delta V_{GE}$ : Maximum voltage level. For 0V/15V driver stage is  $\Delta V_{GE} = 15V$ . Voltage drops at bootstrap circuits (like  $V_F$  and  $V_{CE}$ ) decreasing the resulting maximum voltage accordingly.

$I_{G(\max)}$ : Maximum allowable peak gate current.

Some medium power applications might have the requirement for higher source and/or sink currents than +1A / -2A. In such applications an additional booster can be used as illustrated in Figure 13.

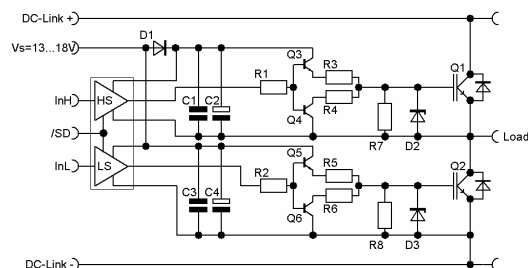


Figure 13: Booster

The integrated operational amplifier (OpAmp) and comparator are suitable to detect over- (OC) and/or short circuit current (SC). Figure 14 shows an example for open-emitter modules where in each half-bridge low-side a shunt resistor might be located. In case of a positive OC or SC the circuitry signals a fault if the

threshold – set by R7 and R8 – of the comparator is reached. The benefit of this circuit is that one driver IC handles one half-bridge not only for switching the power semiconductors, but also for measurement tasks. No further discrete OpAmps or comparators are needed.

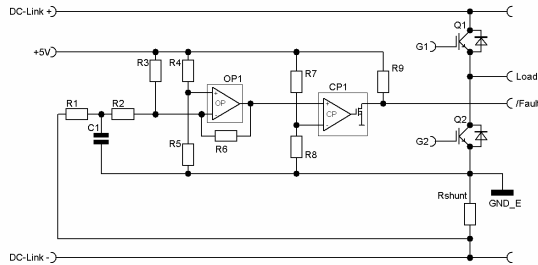


Figure 14: Positive OC/SC detection

Another, more complex possibility would be combining the OpAmps and comparators of several driver IC's (for example in 3-phase converters with a shunt resistor placed in the negative DC-Link). Figure 15 shows an example where one comparator is detecting OC and the other SC events. The different assignment is basically defined by the time constants set by R6, C2 and R7, C3 respectively.

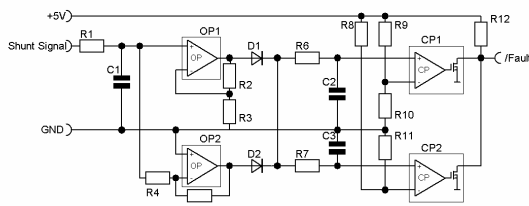


Figure 15: Positive/Negative OC/SC detection

### Integrated protective measures

To avoid the simultaneous switching of the high and low side of a half-bridge either by erroneously generated input signals from the  $\mu$ Controller or EMI the 2ED020112-F has an interlocking function at the primary side implemented that prevents any halfbridge short circuit.

As another feature it houses an under-voltage lockout circuit (UVLO) which inhibits the high or low side to drive an IGBT or MOSFET with insufficient supply voltage, which prevents the power semiconductor from operating in a high dissipation mode.

Furthermore, the driver IC contains low pass digital filters at the logic inputs. This allows the

safe handling of spikes without increasing the propagation delay time.

Last but not least the 2ED020112-F has a shutdown input, which enables or disables both the high and low side driver stages. This shutdown input could be controlled for instance by a fault timer circuitry as shown in Figure 16, which extends any trigger input signal to  $t = R3 \cdot C4$ . The input signal for pin "/Trigger in" could be provided, for example, from the circuitry shown in Figure 14 or Figure 15.

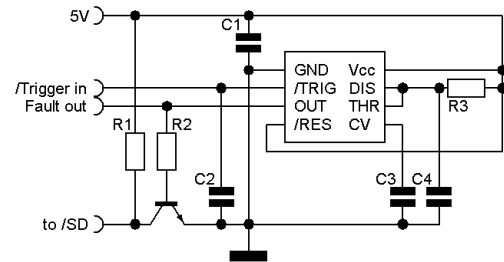


Figure 16: Fault Timer circuitry with LMC555

### External protective measures

Additionally to the implemented protective measures also some external measures might be advisable for certain applications. These are for example:

- A resistor  $R_{GE}$  between gate and emitter avoids uncontrolled charging of the input capacitance  $C_{ies}$  of the IGBT or MOSFET.
- A transient suppressor Zener diode between gate and emitter limits the maximum gate-emitter voltage  $V_{GE}$ .

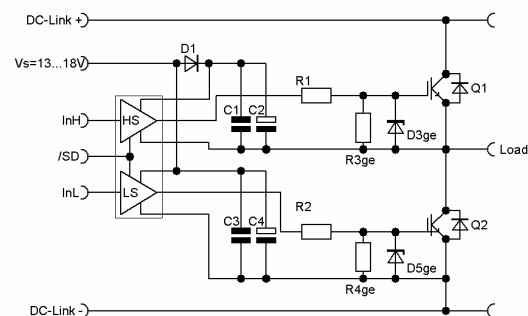


Figure 17: External protective measures

### Outlook

Ongoing developments are focusing on single IGBT and MOSFET driver IC's based on the coreless transformer technology which have an

isolation of up to 1200V. Furthermore, the demand for the combination of safety isolation, high reliability, and low production costs for analog-to-digital converters (ADC) leads to the development of a sigma-delta ADC with coreless transformer. Target applications will be shunt current measurements for instance in individual phases of 3-phase converters, potential free measurement of PIM NTC resistors, and DC-link voltages. Figure 18 shows an application with six CLT single driver IC's and six CLT ADC. All of them with safety isolation to drive and control a 3 phase motor.

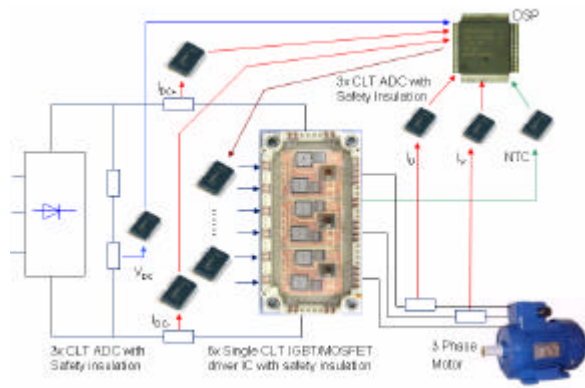


Figure 18: Application with ADC's and driver IC's of eupec EiceDRIVER™ family

## Conclusion

The potential of the coreless transformer technology implemented in the driver IC 2ED020112-F – and soon also in driver and analog-digital-converters with safety isolation – offers developers a convenient usage in a wide range of low and medium power applications due to its simple and reliable way of integration.

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