CompactFlash™ Disk
INDUSTRIAL GRADE
W7CFxxxA-H Series

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Revision History

Revision	Month	Year	History
2.0	February	2006	-ROHS Spec Release
2.1	June	2006	-Add Title Page & Revision History -Update Table 28: Identify Drive Information -Update Table 37: Attribute Memory Read AC Characteristics -Update Table 38: Attribute Memory Write AC Characteristics
2.2	June	2006	-Update Table 28: Identify Drive Information -Update Tables 37~42 -Update Table 43: True IDE Mode I/O Read/Write Timing -Update Table 44: True IDE DMA Mode I/O Read/Write Timing -Update Figures 14~19 -Update Figure 20: True IDE Mode I/O Timing Diagram -Update Figure 21: True IDE DMA Mode I/O Timing Diagram
2.3	December	2006	-Update Table 37 Attribute Memory Read Timing -Update Table 38 Attribute Memory Write Timing -Update Table 39 I/O Access Read Timing -Update Table 41 Common Memory Access Read Timing
2.4	May	2007	-Update DMA pins' description, Pin 43 DMARQ and 44 DMACK -Update Table 7 Layout
2.5	March	2008	-Update new naming scheme for the CF card
2.6	May	2008	-Update Table 48 Ordering Information and naming guide
2.7	October	2008	-Add section 4.1 Labeling and Marking
2.8	November	2008	-Add 16GB capacity to the specification
2.9	January	2009	-Update table 48 with 8GB Real Capacity -Update table 48 key with firmware options
2.10	January	2010	-Update the ordering information with firmware options

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CompactFlash™ Card
INDUSTRIAL GRADE

WxCFxxxA-H Series ROHS 6/6 Compliant

Features

GENERAL
- Type I Density up to 16-GB
- 32-bit RISC/DSP Controller
- Solid State Data Storage
- Dual 3.3V / 5V Interface
- Industry Standard Compatibility
- Specialized for High-Reliability
- ROHS 6/6 Compliant

PERFORMANCE
- True IDE Mode Capable
  - PIO Mode 0-4
  - DMA Mode 0-2 (Optional)
- High Performance 16.7 MB/s Burst
- Low Power Consumption
- ATA-2 Compliant (w/DMA Enable)

RELIABILITY
- > 2,000,000 Program/Erase Cycles
- Industrial Wear Leveling
  - Includes Static Block Management
- Spares & Bad Block Management
- On-Board ECC
  - Corrects up to 6-bytes/Sector
- High Environmental Tolerance
- 10-Year Data Retention
- Unlimited Reads

COMPATIBILITY
- CFA Spec, Revision 4.1, Feb 2007
- PCMCIA PC Card Standard, 7.0, February 1999
- PCMCIA PC Card ATA Spec, 7.0, Feb 1999



Wintec Type I CompactFlash™ Card

Configuration Options

- Industrial Temperature
- Fixed / Removable Disk
- DMA Mode Enable
- Data Programming Service
- Custom Labeling

NOTE:
1. See Section 5.0 for Configuration & Ordering Guide

DESCRIPTION

The Wintec Industries W7CFxxxA-H series of ROHS Compliant Industrial Grade CompactFlash™ Memory Cards are constructed with Samsung NAND-type single-level-cell (SLC) flash memory devices paired to a powerful 32-bit RISC/DSP-based system controller for virtual-to-physical address mapping and other flash management functions.

Wintec Industrial CompactFlash™ Cards employ a variety of sophisticated error checking and flash management utilities allowing for maximum levels of data reliability and card endurance. Patented wear-leveling methods ensure even wear of flash blocks across the entire card capacity. Background operations track erase counts, prioritize new writes to blocks with lower wear, and relocate static data to blocks with higher wear. Bad-block Management routines replace worn blocks with spare blocks reserved by the controller on card initialization. Reed-Solomon based ECC algorithms capable of detecting and correcting up to 6 bytes per 512 byte sector are implemented on the fly without performance degradation to ensure data reliability through user data transfers and background wear-leveling operations. Additional information regarding the specifics of wear leveling, ECC methods, and application-specific card life calculations are available upon request and under NDA.

Industrial grade reliability, industry standard compatibility, and the ability to emulate IDE hard disk drives make Wintec CompactFlash™ Cards ideal for industrial, military, and other high endurance applications.

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1.0 General Product Specification

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

Table 1: Performance Specifications

Parameter		Spec
Burst Transfer Rate To/From Host		16.6 MB/s
Burst Transfer Rate To/From Flash		20.0 MB/s
Sustained Read (Typical)		8.0 MB/s
Sustained Write (Typical)		6.0 MB/s
Active-to-Sleep Delay		Programmable
Command-to-DRQ (Max.)		50.0 ms
Startup Times	**Sleep-to-Write (Max.)**	2.5 ms
	Sleep-to-Read (Max.)	20 ms
	Reset-to-Ready (Typical)	50.0 ms
	Reset-to-Ready (Max.)	400.0 ms

NOTE:
1. All performance figures are based on testing done in True IDE PIO Mode 4.

Table 2: Card Endurance

Parameter	Spec
Program/Erase Cycles	> 2,000,000 Cycles
Read Cycles	Unlimited
Data Retention	10 Years (Min.)
MTBF	> 4,000,000 Hours

Table 3: Card Data Reliability

Parameter	Spec
Non-Recoverable Errors	< 1 in 10^{14} Bytes Read
Erroneous Correction	< 1 in 10^{20} Bytes Read
ECC Correctability	6 Bytes/Sector
ECC Detectability	6 Bytes/Sector

Table 4: Environmental Specifications

Parameters		Operating	Non-Operating
Temperature	**Standard Temp.**	0°C to 70°C	-55°C to 95°C
	Industrial Temp.	-40°C to 85°C	-55°C to 95°C
Humidity		8% to 95% (Non-Condensing)	8% to 95% (Non-Condensing)
Vibration		16.3 G rms	N/A
Altitude		80,000 ft. (Max.)	
Shock		2,000 G (Max.)	
Acoustic		0 db	

Table 5: Power Consumption

Capacity	Sleep (Max)	Read/Write (Typical)	Read/Write (Max)
32MB	300 µ	40 mA	50 mA
64MB	300 µ	40 mA	50 mA
128MB	300 µ	40 mA	50 mA
256MB	300 µ	40 mA	50 mA
512MB	450 µ	45.02mA	60.10mA
1-GB	450 µ	45.02mA	60.10mA
2-GB	600 µ	45.06mA	60.30mA
4-GB	600 µ	45.06mA	60.30mA
8-GB	600 µ	45.06mA	60.30mA

NOTE:
1. Input voltage 3.3V (±5%) or 5V (±10%) with a maximum ripple of 100mV peak-to-peak.
2. All values listed are at 25°C and nominal supply voltage.
3. Stated figures are based on primary configurations and may vary as larger density component NAND flashes are released.

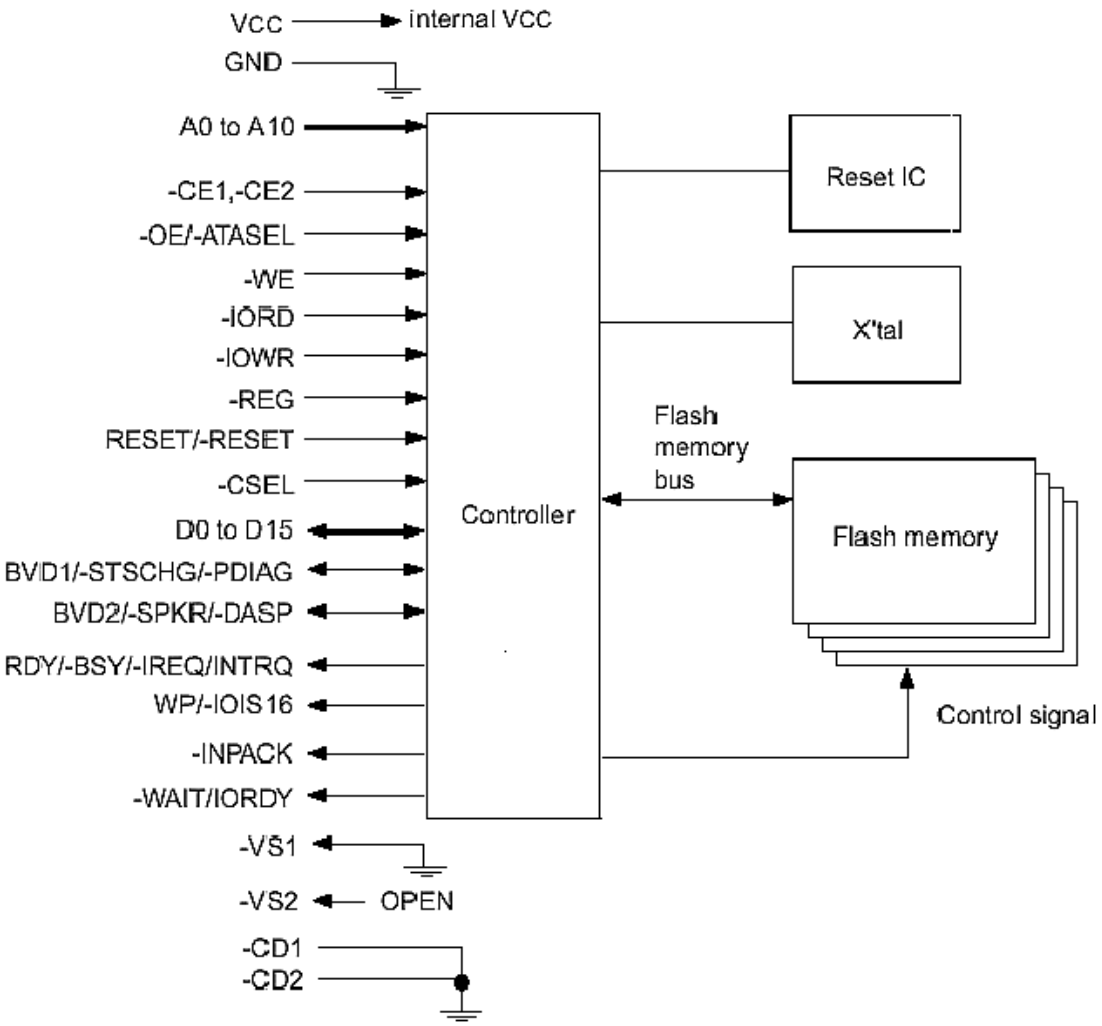


Figure 1: Card Block Diagram

NOTE: -CE1, -CE2, -OE, -WE –IORD, -IOWR, -REG, -RESET, -CSEL, -PDIAG, -DASP pins are pulled up in card. –CE1, -CE2, -OE, -WE, -IORD, -IOWR, -REG pins are Schmitt trigger type input buffer.

Table 6: Card Pin Assignment

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin	**Signal**	**Type**	**Pin**	**Signal**	**Type**	**Pin**	**Signal**	**Type**
1	GND	Ground	**1**	GND	Ground	**1**	GND	Ground
2	D03	I/O	**2**	D03	I/O	**2**	D03	I/O
3	D04	I/O	**3**	D04	I/O	**3**	D04	I/O
4	D05	I/O	**4**	D05	I/O	**4**	D05	I/O
5	D06	I/O	**5**	D06	I/O	**5**	D06	I/O
6	D07	I/O	**6**	D07	I/O	**6**	D07	I/O
7	-CE1	I	**7**	-CE1	I	**7**	-CS0	I
8	A10	I	**8**	A10	I	**8**	A10[2]	I
9	-OE	I	**9**	-OE	I	**9**	-ATA SEL	I
10	A09	I	**10**	A09	I	**10**	A09[2]	I
11	A08	I	**11**	A08	I	**11**	A08[2]	I
12	A07	I	**12**	A07	I	**12**	A07[2]	I
13	VCC	Power	**13**	VCC	Power	**13**	VCC	Power
14	A06	I	**14**	A06	I	**14**	A06[2]	I
15	A05	I	**15**	A05	I	**15**	A05[2]	I
16	A04	I	**16**	A04	I	**16**	A04[2]	I
17	A03	I	**17**	A03	I	**17**	A03[2]	I
18	A02	I	**18**	A02	I	**18**	A02	I
19	A01	I	**19**	A01	I	**19**	A01	I
20	A00	I	**20**	A00	I	**20**	A00	I
21	D00	I/O	**21**	D00	I/O	**21**	D00	I/O
22	D01	I/O	**22**	D01	I/O	**22**	D01	I/O
23	D02	I/O	**23**	D02	I/O	**23**	D02	I/O
24	WP	O	**24**	-IOIS16	O	**24**	-IOCS16	O
25	-CD2	O	**25**	-CD2	O	**25**	-CD2	O
26	-CD1	O	**26**	-CD1	O	**26**	-CD1	O
27	D11[1]	I/O	**27**	D11[1]	I/O	**27**	D11[1]	I/O
28	D12[1]	I/O	**28**	D12[1]	I/O	**28**	D12[1]	I/O
29	D13[1]	I/O	**29**	D13[1]	I/O	**29**	D13[1]	I/O
30	D14[1]	I/O	**30**	D14[1]	I/O	**30**	D14[1]	I/O
31	D15[1]	I/O	**31**	D15[1]	I/O	**31**	D15[1]	I/O
32	-CE2[1]	I	**32**	-CE2[1]	I	**32**	-CS1[1]	I
33	-VS1	O	**33**	-VS1	O	**33**	-VS1	O
34	-IORD	I	**34**	-IORD	I	**34**	-IORD	I
35	-IOWR	I	**35**	-IOWR	I	**35**	-IOWR	I
36	-WE	I	**36**	-WE	I	**36**	-WE[3]	I
37	RDY/BSY	O	**37**	IREQ	O	**37**	INTRQ	O
38	VCC	Power	**38**	VCC	Power	**38**	VCC	Power
39	-CSEL	I	**39**	-CSEL	I	**39**	-CSEL	I
40	-VS2	O	**40**	-VS2	O	**40**	-VS2	O
41	RESET	I	**41**	RESET	I	**41**	RESET	I
42	-WAIT	O	**42**	-WAIT	O	**42**	IORDY	O
43	-INPACK	O	**43**	-INPACK	O	**43**	DMARQ	O
44	-REG	I	**44**	-REG	I	**44**	-DMACK	I
45	BVD2	I/O	**45**	-SPKR	I/O	**45**	-DASP	I/O
46	BVD1	I/O	**46**	-STSCHG	I/O	**46**	-PDIAG	I/O
47	D08[1]	I/O	**47**	D08[1]	I/O	**47**	D08[1]	I/O
48	D09[1]	I/O	**48**	D09[1]	I/O	**48**	D09[1]	I/O
49	D10[1]	I/O	**49**	D10[1]	I/O	**49**	D10[1]	I/O
50	GND	Ground	**50**	GND	Ground	**50**	GND	Ground

NOTE:

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.

Table 7: Card Pin Explanation

Signal Name	Type	Pin #	Description
A10 - A0 (PC Card Memory Mode)	I	8, 10, 11, 12, 14 -20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the Compact Flash Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode) A10 - A3 (True IDE Mode)		18, 19, 20	In True IDE Mode only A[2:0] is used to select the one of eight registers in the Task File. In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/ -BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	25, 26	These Card Detect pins are connected to ground on the Compact Flash Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.

Table 7: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0 -D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode –CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When this pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	2-6, 21, 22, 23, 27-31, 47, 48, 49	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			These signals are the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode all Task File operations occur in byte mode on the low order bus D00 -D07 while all data transfers are 16 bits using D00 -D15.
GND (PC Card Memory Mode)	-	1, 50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the Compact Flash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-.This signal is used in a handshake manner with DMACK- before negating DMAREQ, and reasserting DMAREQ if there is more data to transfer. DMAREQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host .In this case, the BIOS must report that DMA mode is not supported by the host so that the device driver will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and true-IDE modes of operation need not alter the PCMICIA mode connections while in True-IED mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Compact Flash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Table 7: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
- IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Compact Flash controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
- IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the Compact Flash Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the Compact Flash Card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the Compact Flash Card has completed its power up or reset function. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The Compact Flash Card has been powered up with +RESET continuously disconnected or asserted.
- IREQ (PC Card I/O Mode)			I/O Operation – After the Compact Flash Card has been configured for I/O operation, this signal is used as – Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
-INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high Interrupt Request to the host.

Table 7: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMAREQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DAM operation is not supported by a True-IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
-RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal resets the Compact Flash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
-RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	-	13, 38	+5, +3.3V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1, -VS2 (PC Card Memory Mode)	O	33, 40	Voltage Sense Signals. –VS1 is grounded so that the Compact Flash Card CIS can be read at 3.3 volts and –VS2 is open and reserved by PCMCIA for a secondary voltage.
-VS1, -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1, -VS2 (True IDE Mode)			This signal is the same for all modes.

Table 7: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-WAIT (PC Card Memory Mode)	O	42	This signal is not asserted for all modes.
-WAIT (PC Card I/O Mode)			This signal is not asserted for all modes.
-IORDY (True IDE Mode)			This signal is not asserted for all modes.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the Compact Flash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
-WP (PC Card Memory Mode)	O	24	Memory Mode – The Compact Flash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the Compact Flash Card is configured for I/O Operation, Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

2.0 Card Function Explanation

2.1 Attribute Access Specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG = "L" as follows. That region can be accessed by Byte/Word/Odd-byte modes, which are defined by PC card standard specifications.

Table 8: Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H					High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	High-Z	Even byte
	L	H	L	H	L	H	High-Z	Invalid
Word access (16-bit)	L	L	L		L	H	Invalid	Even byte
Odd byte access (8-bit)	L	L	H		L	H	Invalid	High-Z

Table 9: Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H					Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	Don't care	Even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16-bit)	L	L	L		H	L	Don't care	Even byte
Odd byte access (8-bit)	L	L	H		H	L	Don't care	Don't care

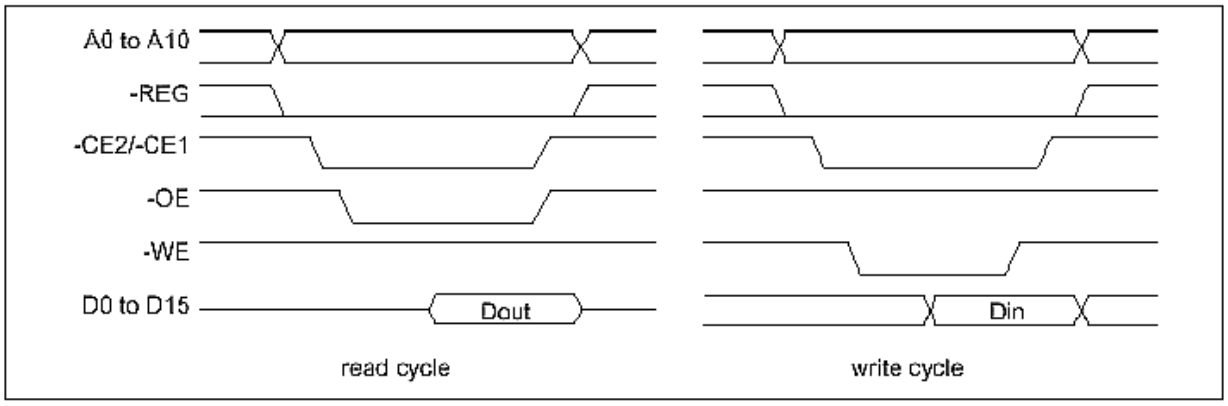


Figure 2: Attribute Access Timing Example

2.2 Task File Register Access Specifications

There are two cases of Task File register mapping, one is mapped I/O address area, and the other is mapped Memory address area. Each case of Task File register read and write operations are executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte modes, which are defined by PC card standard specifications.

2.2.1 I/O Address Map

Table 10: Task File Register Read Access Mode (i)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	H	H	High-Z	Even byte
	L	H	L	H	L	H	H	H	High-Z	Odd byte
Word access (16-bit)	L	L	L		L	H	H	H	Odd byte	Even byte
Odd byte access (8-bit)	L	L	H		L	H	H	H	Odd byte	High-Z

Table 11: Task File Register Write Access Mode (i)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	H	H	Don't care	Even byte
	L	H	L	H	H	L	H	H	Don't care	Odd byte
Word access (16-bit)	L	L	L		H	L	H	H	Odd byte	Even byte
Odd byte access (8-bit)	L	L	H		H	L	H	H	Odd byte	Don't care

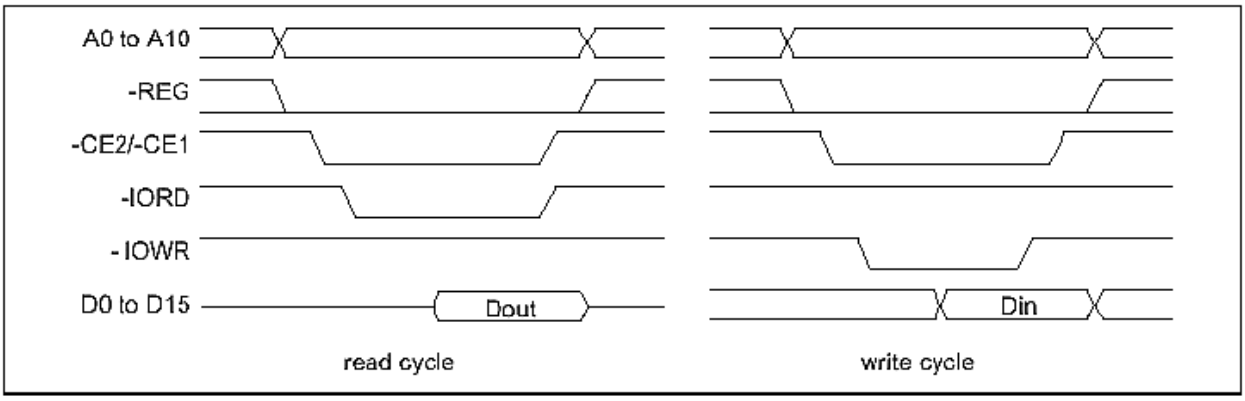


Figure 3: Task File Register Access Timing Example (i)

2.2.2 Memory Address Map

Task File Register Read Access Mode (ii)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							High-Z	High-Z
Byte access (8-bit)	H	H	L	L	L	H	H	H	High-Z	Even byte
	H	H	L	H	L	H	H	H	High-Z	Odd byte
Word access (16-bit)	H	L	L		L	H	H	H	Odd byte	Even byte
Odd byte access (8-bit)	H	L	H		L	H	H	H	Odd byte	High-Z

Table 13: Task File Register Write Access Mode (ii)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							Don't care	Don't care
Byte access (8-bit)	H	H	L	L	H	L	H	H	Don't care	Even byte
	H	H	L	H	H	L	H	H	Don't care	Odd byte
Word access (16-bit)	H	L	L		H	L	H	H	Odd byte	Even byte
Odd byte access (8-bit)	H	L	H		H	L	H	H	Odd byte	Don't care

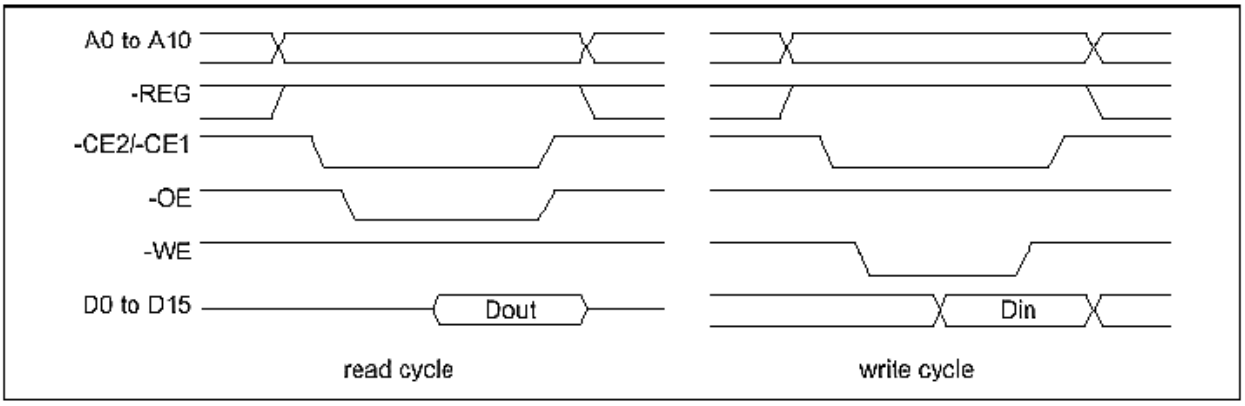


Figure 4: Task File Register Access Timing Example (ii)

2.2.3 True IDE Mode

The card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the –OE input signal is asserted GND by the host. In this True IDE Mode Attribute Registers are not accessible from the host. Only I/O operation to the task files and data registers are allowed. If this card is configured during power on sequence, data registers are accessed in word (16-bit). The card permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

Table 14: True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 -A2	-IORD	-IOWR	D8 -D15	D0 -D7
Invalid mode	L	L				High-Z	High-Z
Standby mode	H	H				High-Z	High-Z
Data register access	H	L	0	L	H	Odd byte	Even byte
Alternate status access	L	H	6H	L	H	High-Z	Status out
Other task file access	H	L	1-7H	L	H	High-Z	Data

Table 15: True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 -A2	-IORD	-IOWR	D8 -D15	D0 -D7
Invalid mode	L	L				Don't care	Don't care
Standby mode	H	H				Don't care	Don't care
Data register access	H	L	0	L	H	Odd byte	Even byte
Alternate status access	L	H	6H	L	H	Don't care	Control in
Other task file access	H	L	1-7H	L	H	Don't care	Data

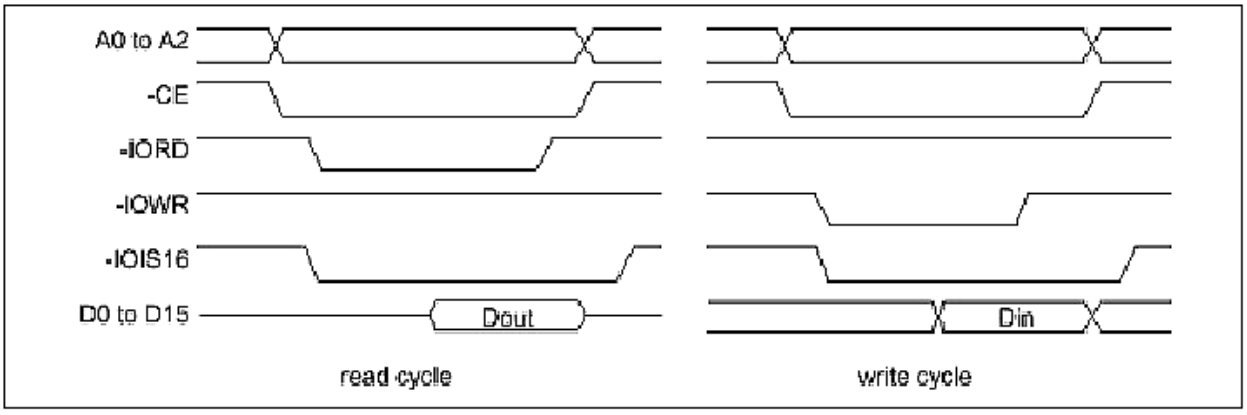


Figure 5: True IDE Mode I/O Access Timing Example

2.3 Configuration Register Specification

This card supports four configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers cannot be used.

2.3.1 Configuration Option register (Address 200H)

This register is used for setting the card configuration status and for issuing soft reset to the card.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRESET	LevlREQ	INDEX					

NOTE:
1. Initial value: 00H

Table 17: Option Register Function

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevlREQ (HOST->)	R/W	This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bit is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.

Table 18: INDEX bit assignment

INDEX Bit						Task File register address	Mapping mode
5	4	3	2	1	0		
0	0	0	0	0	0	0H to FH, 400H to 7FFH	Memory Mapped
0	0	0	0	0	1	xx0H to xxFH	Contiguous I/O Mapped
0	0	0	0	1	0	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O Mapped
0	0	0	0	1	1	170H to 177H, 376H to 377H	Secondary I/O Mapped

2.3.2 Configuration and Status Register (Address 202H)

This register is used for observing the card state.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

NOTE:
1. 1initial value: 00H

Table 19: Configuration and Status Register Function

Name	R/W	Function
CHGED (HOST->)	R	This bit indicates that CRDY/-BSY bit on Pin Replacement register is set to "1". When CHGED bit is set to "1", -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with one 8-bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters sleep stat (Power Down mode). When this bit is reset to "0", the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (HOST->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero.

2.3.3 Pin Replacement Register (Address 204H)

This register is used for providing the signal state of –IREQ signal when the card configured I/O card interface.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

NOTE:
1. Initial value 0CH

Table 20: Pin Replacement Register Function

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-BSY bit masking

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2.3.4 Socket and Copy Register (Address 206H)

This register is used for identification of the card from the other cards. Host can read and write this register. This register should be set by host before Configuration Option register is set.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	DRV#	0	0	0	0

NOTE:
1. Initial value: 00H

Table 21: Socket and Copy Register Function

Name	R/W	Function
DRV# (HOST->)	R/W	This field are used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization.

2.4 Task File Register Specification

These registers are used for reading and writing the storage data in the card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

Table 22: Memory map (INDEX=0)

-REG	A10	A9 -A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0		0	0	0	0	0H	Data register	Data register
1	0		0	0	0	1	1H	Error register	Feature register
1	0		0	0	0	0	2H	Sector count register	Sector count register
1	0		0	0	0	1	3H	Sector number register	Sector number register
1	0		0	1	1	0	4H	Cylinder low register	Cylinder low register
1	0		0	1	1	1	5H	Cylinder high register	Cylinder high register
1	0		0	1	1	0	6H	Drive head register	Drive head register
1	0		1	1	1	1	7H	Status register	Command register
1	0		1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0		1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0		1	1	1	1	DH	Dup. error register	Dup. feature register
1	0		1	1	1	0	EH	Alt. status register	Device control register
1	0		1	1	1	1	FH	Drive address register	Reserved
1	1					0	8H	Even data register	Even data register
1	1					1	9H	Odd data register	Odd data register

Table 23: Contiguous I/O map (INDEX=1)

-REG	A10 -A4	A3	A2	A1	A0	Offset	-IORD=L	-IOWR=L
0		0	0	0	0	0H	Data register	Data register
0		0	0	0	1	1H	Error register	Feature register
0		0	0	1	0	2H	Sector count register	Sector count register
0		0	0	1	1	3H	Sector number register	Sector number register
0		0	1	0	0	4H	Cylinder low register	Cylinder low register
0		0	1	0	1	5H	Cylinder high register	Cylinder high register
0		0	1	1	0	6H	Drive head register	Drive head register
0		0	1	1	1	7H	Status register	Command register
0		1	0	0	0	8H	Dup. even data register	Dup. even data register
0		1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0		1	1	0	1	DH	Dup. error register	Dup. feature register
0		1	1	1	0	EH	Alt. status register	Device control register
0		1	1	1	1	FH	Drive address register	Reserved

Table 24: Primary I/O Map (INDEX=2)

-REG	A10	A9 -A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0		1FH	0	0	0	0	Data register	Data register
0		1FH	0	0	0	1	Error register	Feature register
0		1FH	0	0	1	0	Sector count register	Sector count register
0		1FH	0	0	1	1	Sector number register	Sector number register
0		1FH	0	1	0	0	Cylinder low register	Cylinder low register
0		1FH	0	1	0	1	Cylinder high register	Cylinder high register
0		1FH	0	1	1	0	Drive head register	Drive head register
0		1FH	0	1	1	1	Status register	Command register
0		3FH	0	1	1	0	Alt. status register	Device control register
0		3FH	0	1	1	1	Drive address register	Reserved

Table 25: Secondary I/O Map (INDEX=3)

-REG	A10	A9 -A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0		17H	0	0	0	0	Data register	Data register
0		17H	0	0	0	1	Error register	Feature register
0		17H	0	0	1	0	Sector count register	Sector count register
0		17H	0	0	1	1	Sector number register	Sector number register
0		17H	0	1	0	0	Cylinder low register	Cylinder low register
0		17H	0	1	0	1	Cylinder high register	Cylinder high register
0		17H	0	1	1	0	Drive head register	Drive head register
0		17H	0	1	1	1	Status register	Command register
0		37H	0	1	1	0	Alt. status register	Device control register
0		37H	0	1	1	1	Drive address register	Reserved

Table 26: True IDE Mode I/O Map

-CE2	-CE1	A2	A1	A0	-IORD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

2.4.1 Data Register

This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error and Feature register.

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D0 to D15															

2.4.2 Error Register

This register is a read only register, and is used for analyzing the error content during card accessing. This register is valid when the BSY bit in Status Register and Alternate Status Register are set to "0" (Ready).

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BBK	UNC	"0"	IDNF	"0"	ABRT	'0'	AMNF

bit	Name	Function
7	BBK (Bad BlocK detected)	This bit is set when a Bad Block is detected in requested ID field.
6	UNC (Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (AboRTed command)	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

2.4.3 Feature Register

This register is a write only register, and provides information regarding features of the drive, which the host wishes to utilize.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Feature byte							

2.4.4 Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request. This register's initial value is "01H".

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Sector count byte							

2.4.5 Sector Number Register

This register contains the starting sector number, which is started by following sector transfer command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Sector number byte							

2.4.6 Cylinder Low Register

This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Cylinder low byte							

2.4.7 Cylinder High Register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Cylinder high byte							

2.4.8 Drive Head Register

This register is used for selecting the Drive number and head number for the following command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	LBA	1	DRV	Head #			

NOTE:
1. DRV: Drive number

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA = 1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07 - LBA00: Sector Number Register D7 - D0. LBA15 - LBA08: Cylinder Low Register D7 - D0. LBA23 - LBA16: Cylinder High Register D7 - D0. LBA27 - LBA24: Drive / Head Register bits HS3 - HS0.
5	1	This bit is set to "1".
4	DRV (DRiVe select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3 -0	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

2.4.9 Status Register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX = 1, 2, 3) and level interrupt mode, -IREQ is negated. This register should be accessed in byte mode. In word mode, it is recommended that Alternate status register may be used as this register.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF (Drive Write Full)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

2.4.10 Alternate Status Register

This register is the same as Status register in physically, so the it assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

2.4.11 Command Register

This register is write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card is Ready state.

Command	Command Code	Used Parameter						
		FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

NOTE:

FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command
N: The register does not contain a valid parameter for this command.

2.4.12 Device Control Register

This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				1	SRST	nIEN	0

bit	Name	Function
7 -4		Don't care
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling –IREQ. When this bit is set to "0", –IREQ is enabled. When this bit is set to "1", –IREQ is disabled.
0	0	This bit is set to "0".

2.4.13 Drive Address Register

This register is read only register, and it is used for confirming the drive status. This register is provided for compatibility with the AT disk drive interface. It is recommended that this register be not mapped into the host's I/O space because of potential conflicts on bit7.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7		This bit is unknown.
6	nWTG (WriTing Gate)	This bit is unknown.
5 -2	nHS3 -0(Head Select3 - 0)	These bits are the negative value of Head Select bits (bit 3 to 0) in Drive/Head register.
1	nDS1 (Idrive Select1)	This bit is unknown.
0	nDS0 (Idrive Select0)	This bit is unknown.

2.5 ATA Command Specification

This table summarizes the ATA command set with the paragraphs. Following shows the support commands and command codes, which are written in, command registers.

Table 27: ATA Command Set

No.	Command	Command Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H or 98H	-	-	-	-	Y	-	-
2	Execute drive diagnostic	90H	-	-	-	-	Y	-	-
3	Erase sector	C0H	-	Y	Y	Y	Y	Y	Y
4	Format track	50H	-	Y	-	Y	Y	Y	Y
5	Identify Drive	ECH	-	-	-	-	Y	-	-
6	Idle	E3H or 97H	-	Y	-	-	Y	-	-
7	Idle immediate	E1H or 95H	-	-	-	-	Y	-	-
8	Initialize drive parameters	91H	-	Y	-	-	Y	Y	-
9	Read buffer	E4H	-	-	-	-	Y	-	-
10	Read multiple	C4H	-	Y	Y	Y	Y	Y	Y
11	Read long sector	22H, 23H	-	-	Y	Y	Y	Y	Y
12	Read sector	20H, 21H	-	Y	Y	Y	Y	Y	Y
13	Read verify sector	40H, 41H	-	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	-	-	-	-	Y	-	-
15	Request sense	03H	-	-	-	-	Y	-	-
16	Seek	7XH	-	-	Y	Y	Y	Y	Y
17	Set features	EFH	Y	-	-	Y	Y	-	-
18	Set multiple mode	C6H	-	Y	-	-	Y	-	-
19	Set sleep mode	E6H or 99H	-	-	-	-	Y	-	-
20	Stand by	E2H or 96H	-	-	-	-	Y	-	-
21	Stand by immediate	E0H or 94H	-	-	-	-	Y	-	-
22	Translate sector	87H	-	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	-	-	-	-	Y	Y	-
24	Write buffer	E8H	-	-	-	-	Y	-	-
25	Write long sector	32H or 33H	-	-	Y	Y	Y	Y	Y
26	Write multiple	C5H	-	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	-	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	-	Y	Y	Y	Y	Y	Y
29	Write sector w/o erase	38H	-	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	-	Y	Y	Y	Y	Y	Y

NOTE:

FR: Feature register
SC: Sector Count register (00H to FFH)
SN: Sector Number register (01H to 20H)
CY: Cylinder register (to)
DR: DRV bit of Drive Head register
HD: Head No. (0 to 3) of Drive Head register
NH: No. of Heads
Y: Set up
- : Not Set up

2.5.1 ATA Command Set Description

1. Check Power Mode (code: E5H or 98H): This command checks the power mode.
2. Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the Card.
3. Erase Sector(s) (code: C0H): This command is used to erase data sectors.
4. Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive. But selected sector data is not exchanged. This card accepts a sector buffer of data from the host to follow the command with same protocol as the Write Sector command.
5. Identify Drive (code: ECH): This command enables the host to receive parameter information from the Card.

Table 28: Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General Configuration: 848Ah: Removable Disk (Default) 044Ah: Fixed Disk (Option)
1	XXXX	2	Number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of heads
4	0000h	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Number of sectors per track
7 -8	XXXX	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Reserved
10 -19	aaaa	20	Serial Number in ASCII (Right Justified)
20	0002h	2	Buffer type: Dual ported multi-sector
21	0002h	2	Buffer size in 512 byte increments
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23 -26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	0001h	2	Maximum of 1 sector on Read/Write Multiple command
48	0000h	2	Double Word not supported
49	0200h	2	Capabilities: Bit 9: LBA Supported
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	DMA data transfer cycle timing mode (Not Supported)
53	0003h	2	Field validity
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple Sector Setting is valid
60 -61	XXXX	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0000h	2	Multiword DMA Transfer: 0000h: Not Supported
64	0003h	2	Advanced PIO Modes supported
65	0000h	2	Minimum DMA transfer cycle time per word

66	0000h	2	Recommended DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-127	XXXXh	130	Reserved
128-159	0000h	64	Reserved Vendor Unique Bytes
160-255	0000h	192	Reserved

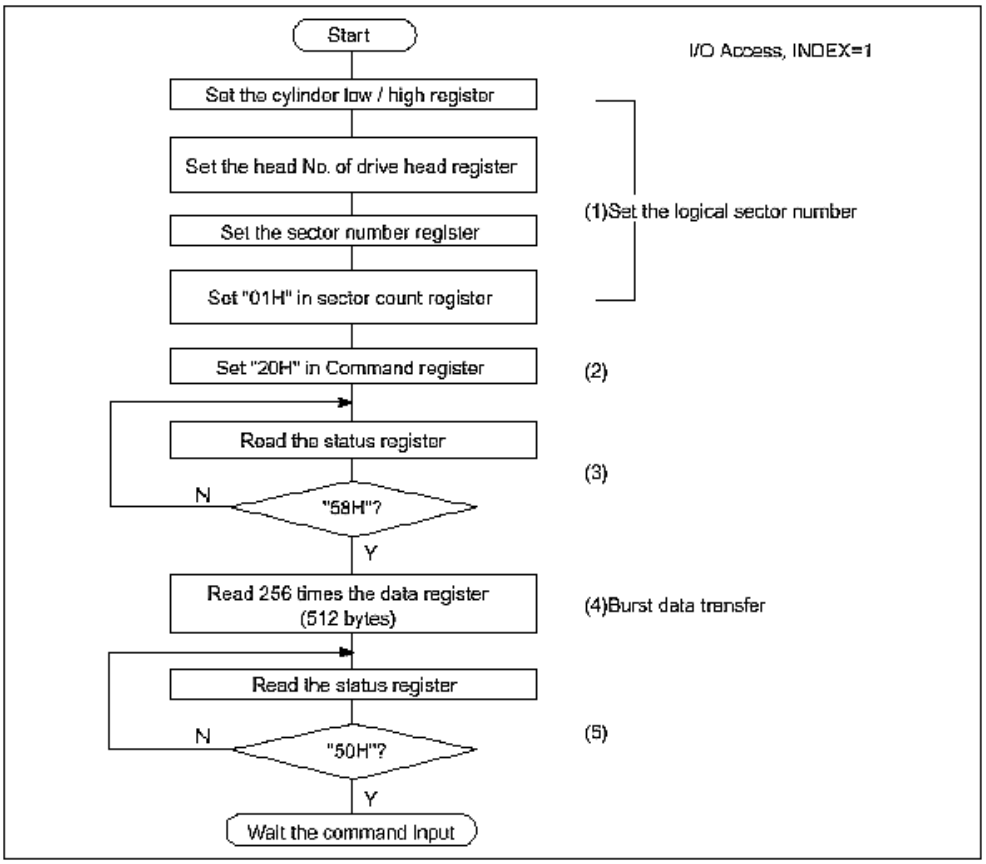
6. Idle (code: E3H or 97H): This command causes the PC Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
7. Idle Immediate (code: E1H or 95H): This command causes the Card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.
8. Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cylinder.
9. Read Buffer (code: E4H): This command enables the host to read the current contents of the PC card's sector buffer.
10. Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.
11. Read Long Sector (code: 22H, 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
12. Read Sector(s) (code: 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
13. Read Verify Sector(s) (code: 40H, 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
14. Recalibrate (code: 1XH): This command is effectively a NOP command to the Card and is provided for compatibility purposes.
15. Request Sense (code: 03H): This command requests an extended error code after command ends with an error.
16. Seek (code: 7XH): This command is effectively a NOP command to the Card although it does perform a range check.
17. Set Features (code: EFH): This command is used by the host to establish or select certain features.

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Disable 8-bit data transfer.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

18. Set Multiple Mode (code: C6H): This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.
19. Set Sleep Mode (code: E6H or 99H): This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
20. Stand By (code: E2H or 96H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
21. Stand By Immediate (code: E0H or 94H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
22. Translate Sector (code: 87H): This command allows the host a method of determining the exact number of times a user sector has been erased and programmed.
23. Wear level (code: F5H): This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00H indicating Wear Level is not needed.

24. Write Buffer (code: E8H): This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.
25. Write Long Sector (code: 32H or 33H): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
26. Write Multiple (code: C5H): This command is similar to the Write Sector command. Interrupts are not presented on each sector, but on the transfer of a block, which contains the number of sectors defined by Set Multiple command.
27. Write Multiple without Erase (code: CDH): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.
28. Write Sector(s) (code: 30H or 31H): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
29. Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.
30. Write Verify (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

2.5.2 Sector Transfer Protocol



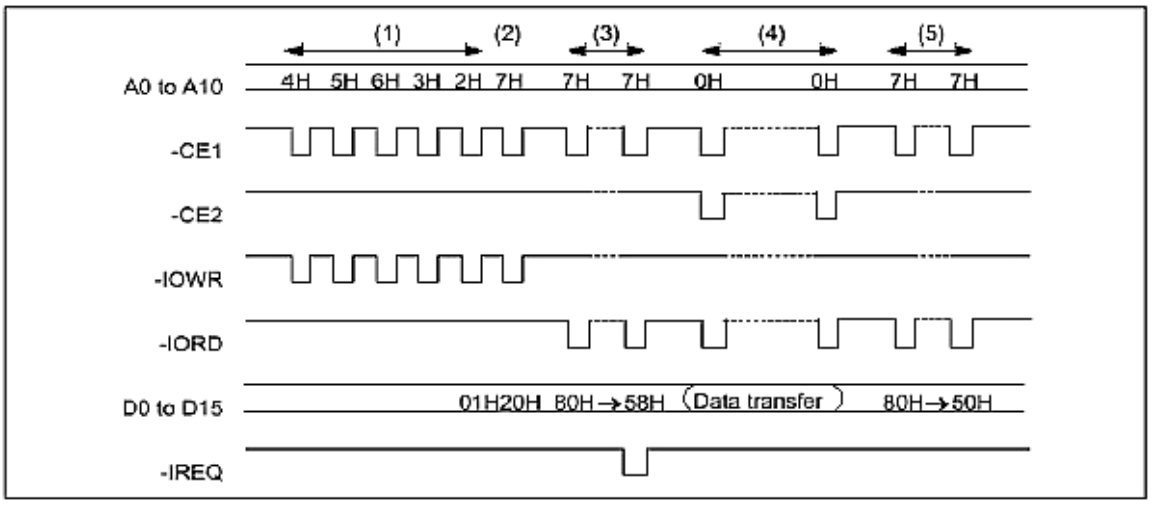
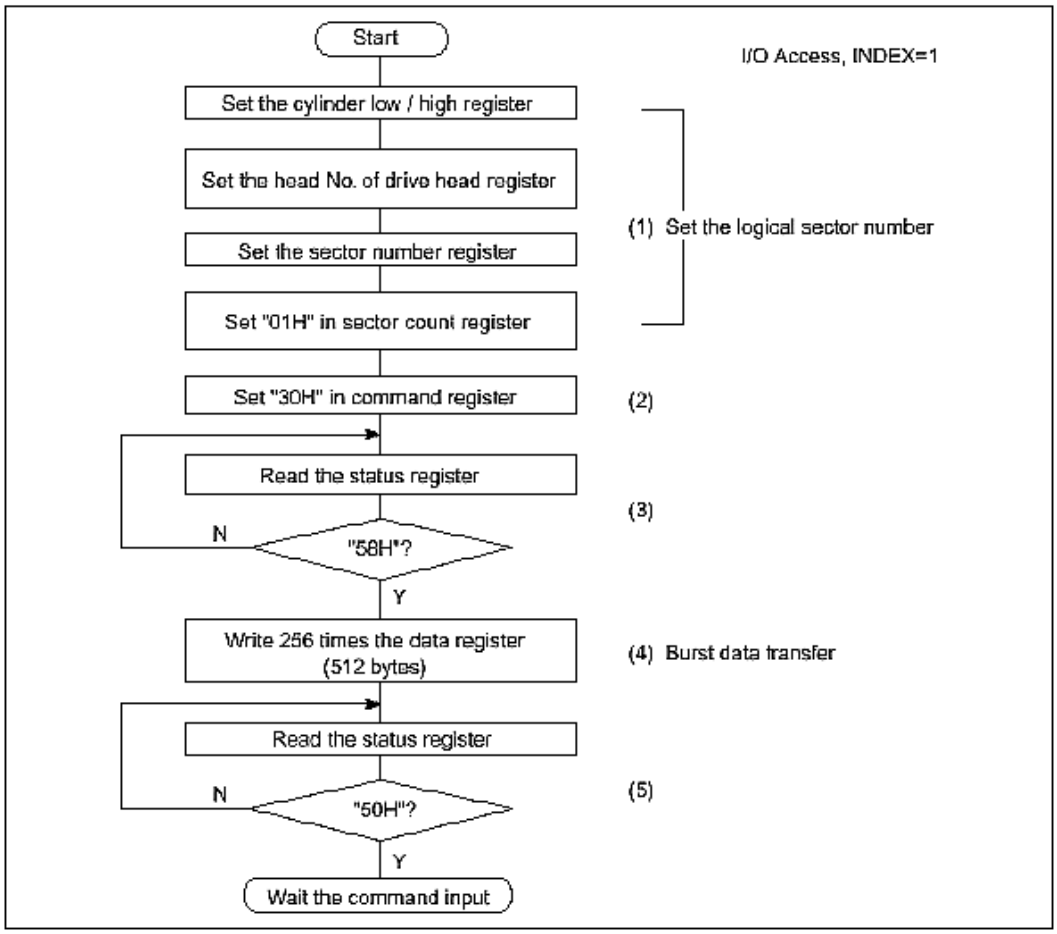


Figure 6: Sector Read

NOTE: 1 sector read procedure after the card configured I/O interface is shown as follows.



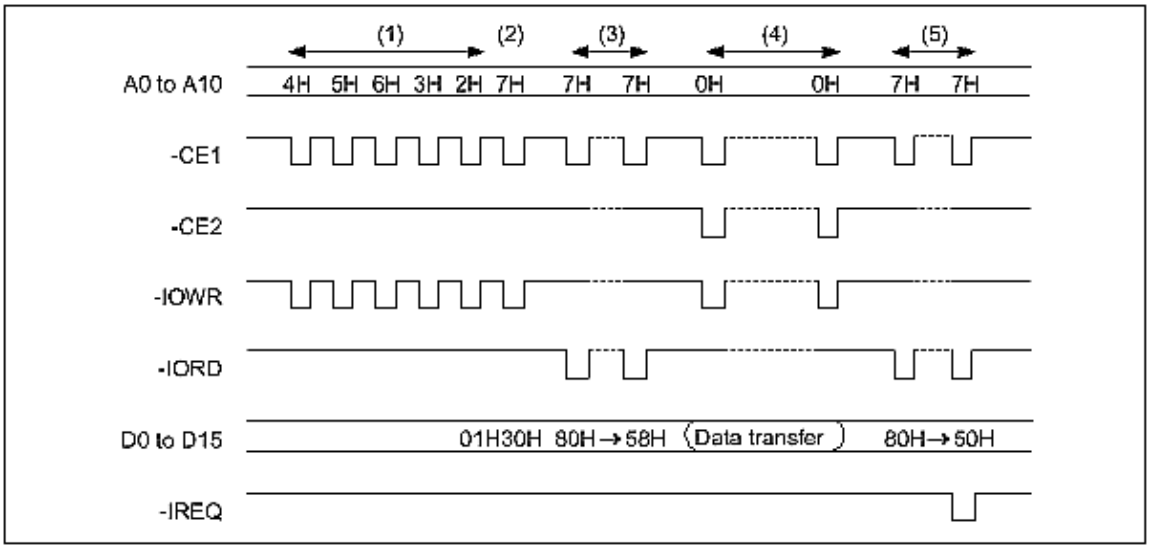


Figure 7: Sector Write

NOTE: 1 sector write procedure after the card configured I/O interface is shown as follows.

3.0 Electrical Specification

3.1 General

Table 29: Absolute Maximum Ratings (V_{CC}=3.3V ± 5% or V_{CC}=5V ± 10%)

Symbol	Parameter	Min	Max	Units
V_{CC}	V_{CC} With Respect to GND	-0.3	6.5	V
V_{IN} / V_{OUT}	All Input/Output Voltages[1]	-0.3	V_{CC} + 0.3	V
T_A	Operating Temperature (Standard Temp)	0	70	°C
T_A	Operating Temperature (Industrial Temp)	-40	85	°C
T_S	Storage Temperature	-55	125	°C
V*	Voltage on any Pin Except V_{CC} with Respect to GND	-0.5	0.5	V

NOTE:
1. V_{IN} / V_{OUT} Min. = -2.0V for Pulse Width 0.20ns

Table 30: Input Leakage Control

Symbol	Parameter	Type	Conditions	MIN	MAX	Units
IL	Input Leakage Current	IxZ	Vih = Vcc/Vil = Gnd	-1	1	µA
RPU1	Pull Up Resistor	IxU	Vcc = 5.0V	50k	500k	Ohm
RPD1	Pull Down Resistor	IxD	Vcc = 5.0V	50k	500k	Ohm

NOTE: The minimum pull-up resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the Compact Flash Memory Card to reduce power use.

Table 31: Input Characteristics

Type	Parameter	Symbol	Vcc = 3.3 V			Vcc = 5.0 V			Units
			MIN	TYP	MAX	MIN	TYP	MAX	
1	Input Voltage CMOS	Vih Vil	2.4		 0.6	2.4		 0.8	V
2	Input Voltage CMOS	Vih Vil	1.5		 0.6	2.0		 0.8	V
3	Input Voltage CMOS Schmitt Trigger	Vih Vil		1.8 1.0			2.8 2.0		V

Table 32: Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh only
ONx	N-Channel Only	Iol only

Table 33: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 GND +0.4V	V
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 GND +0.4V	V
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 GND +0.4V	V
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

Table 34: Capacitance (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Condition	Min	Max	Unit
Input capacitance	Cin	Vin = 0V	-	35	pF
Output capacitance	Cout	Vout = 0V	-	35	pF

Table 35: Power-up/Power-down Timing

The timing specification was defined to retain data in the Flash Card during power-up or power-down cycles and to permit peripheral cards to perform power-up initialization.

Item	Symbol	Condition	Value		
			Min	Max	Unit
CE signal level[1]	Vi (CE)	0V < Vcc < 2.0V	0	ViMAX	V
		2.0V < Vcc < V_{IH}	<Vcc – 0.1	ViMAX	
		< V_{IH} < Vcc	V_{IH}	ViMAX	
CE Setup Time	Tsu (Vcc)		20		ms
	Tsu (RESET)		20		ms
CE Recover Time	Trec (Vcc)		0.001		ms
Vcc Rising Time[2]	tpr	10% → 90% of (Vcc + 5%)	0.1	300	ms
	tpf	90% of (Vcc – 5%) → 10%	3.0	300	ms
Reset Width	Tw (RESET)		10		µs
	Th (Hi-z Reset)		1		ms
	Ts (Hi-z Reset)		0		ms

NOTE:

1. ViMAX means Absolute Maximum Voltage for Input in the period of 0V < Vcc < 2.0V, Vi (CE) is only 0V - ViMAX.
2. The tpr and tpf are defined as "linear waveform" in the period of 10% to 90% or vice-versa. Even if the waveform is not "linear waveform," its rising and falling time must be met by this specification.

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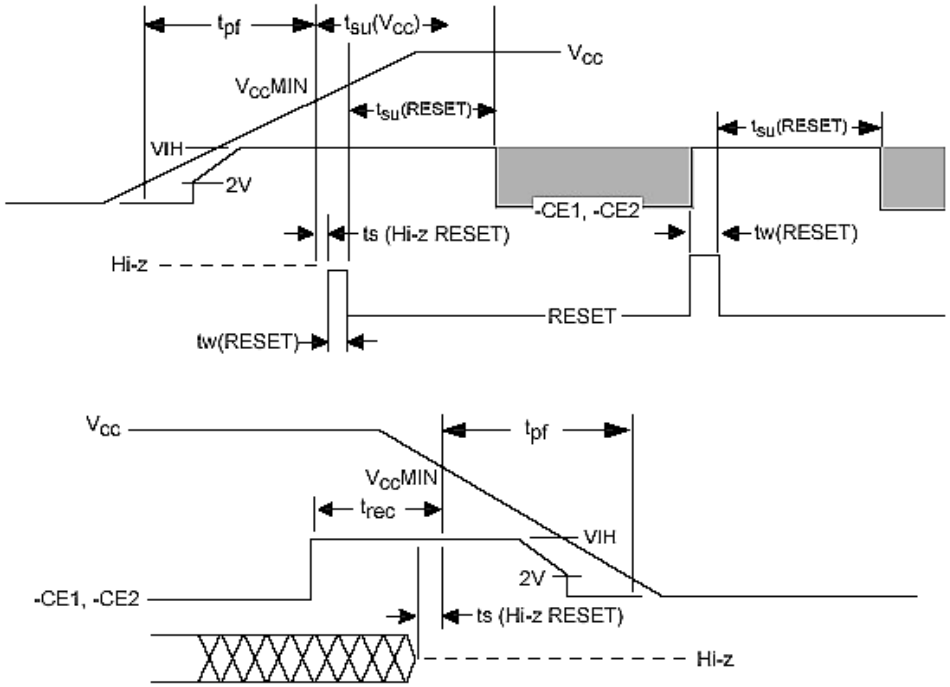


Figure 8: Power Up/Power Down Timing

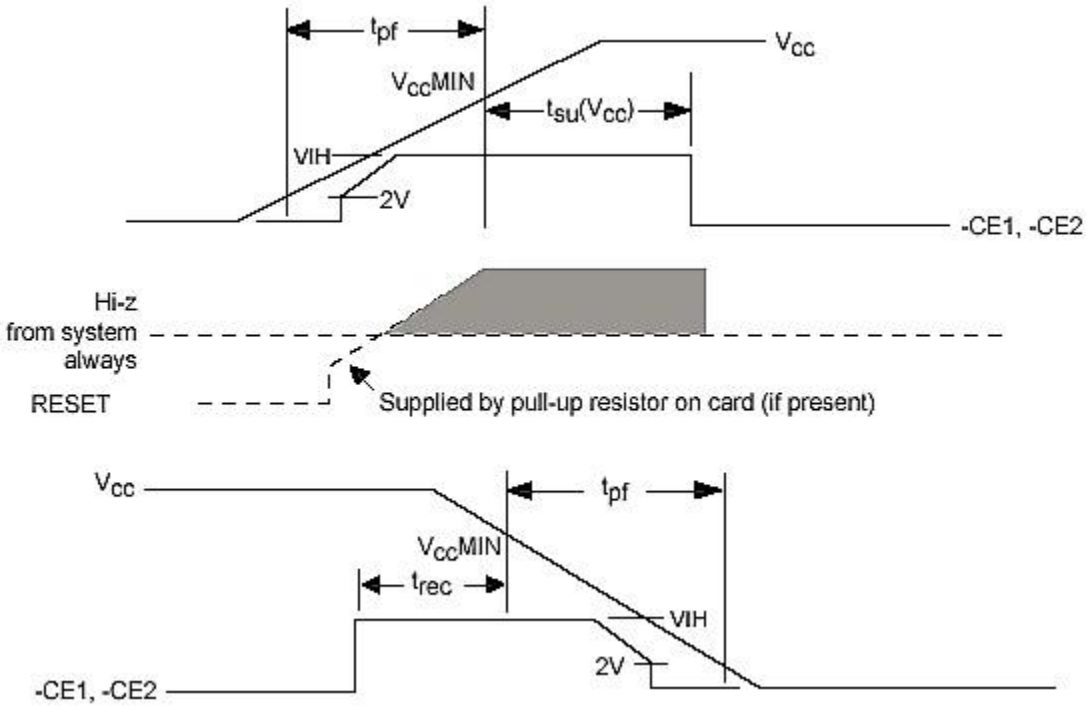


Figure 9: Power Up/Power Down Timing for Systems Not Supporting RESET

3.2 DC Characteristics

Table 36: (Ta = 0 to +70°C, Vcc = 5V ± 10%, 3.3V ± 5%)

Parameter	Symbol	Conditions	V_{CC} = 3.3V ± 5%			V_{CC} = 5V ± 10%			Unit
			Min	Typ	Max	Min	Typ	Max	
Input leakage current[1]	I_{LI}	V_{IN} = GND to V_{CC}	-	-	0.1	-	-	0.1	mA
Output voltage	V_{OL}	I_{OL} = 8 mA	-	-	0.4	-	-	0.4	V
	V_{OH}	I_{OL} = -8 mA	V_{CC}-0.8	-	-		-	-	V_I
Input voltage (CMOS)	V_{IL}	-	-	-	0.6	-	-	0.8	V
	V_{IH}	-	2.4	-	-	4.0	-	-	V
Input voltage (Schmitt trigger)	V_{IL}	-	-	1.0	-	-	2.0	-	V
	V_{IH}	-	-	1.8	-	-	2.8	-	V
Sleep/Standby Current	I_{SP1}	Ctrl = Vcc-0.2V[2]	-	-	0.3	-	0.5	1.0	mA
Sector Read Current	I_{CCR}(DC)	Ctrl = Vcc-0.2V[2]	-	25	50	-	40	75	mA
	I_{CCR}(Max)		-	50	80	-	80	120	
Sector Write Spec	I_{CCR}(DC)	Ctrl = Vcc-0.2V[2]	-	25	50	-	45	75	mA
	I_{CCR}(Max)		-	50	80	-	80	120	

NOTE:
1. Except Pulled-Up Input Pin
2. CMOS Level in Memory Card & I/O Mode

3.2.1 Current Waveform (Vcc = 5V, Ta = 25°C)

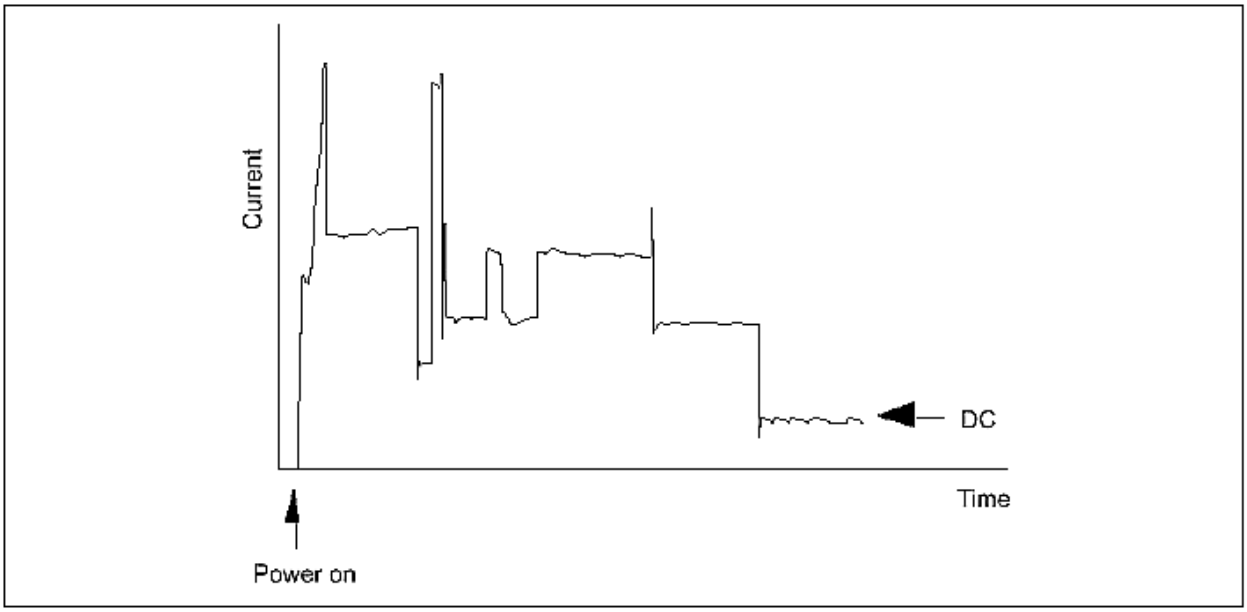


Figure 11: Power on Operation (Reference Only)

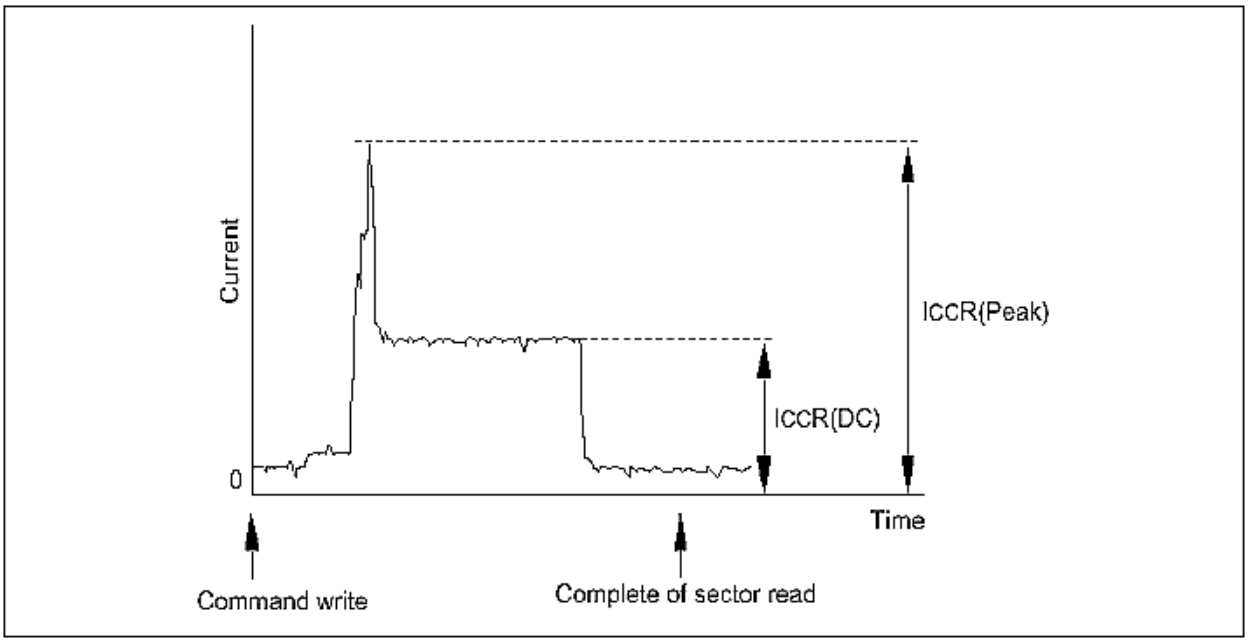


Figure 12: Sector Read

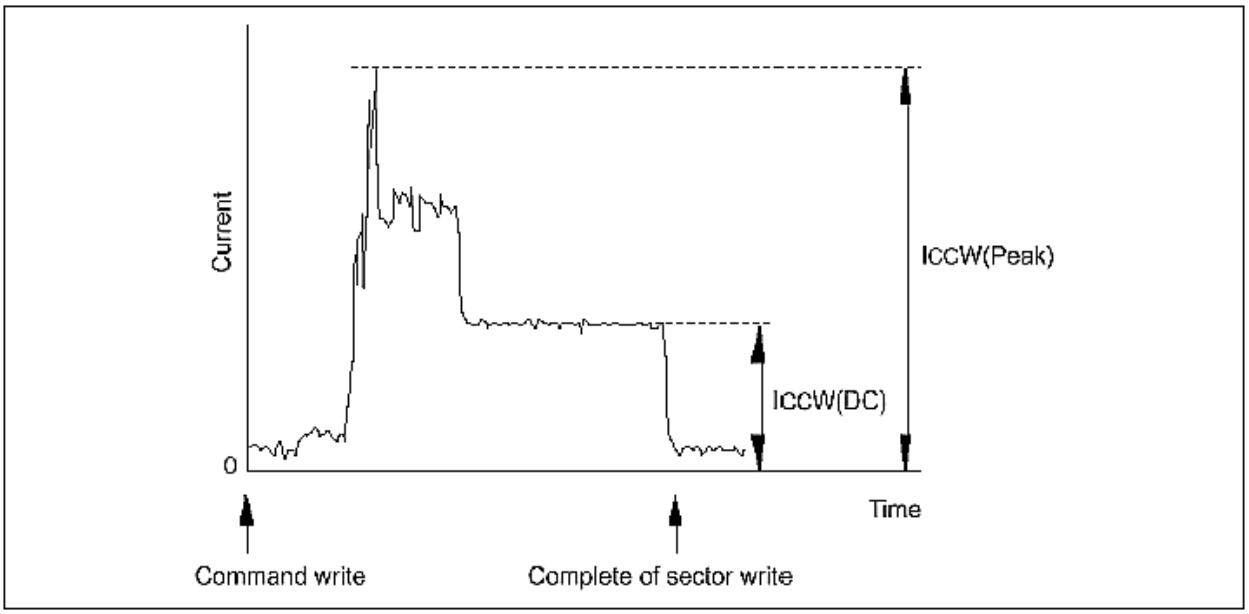


Figure 13: Sector Write

3.3 AC Characteristics

(Ta = 0 to +70℃, Vcc = 5V±10%, 3.3V±5%)

3.3.1 General

Attribute Memory access time is defined as 300 ns. Detailed timing specifications are shown in Table 37.

Table 37: Attribute Memory Read Timing

Speed Version			300ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns)**	**Max (ns)**
Read cycle time	tCR	tAVAV	120	-
Address access time	ta(A)	tAVQV	-	75
Card Enable access time	ta(CE)	tELQV	-	75
Output Enable access time	ta(OE)	tGLQV	-	50
Output disable time (-CE)	tdis(CE)	tEHQZ	-	30
Output disable time (-OE)	tdis(OE)	tGHQZ	-	30
Address setup time	tsu(A)	tAVGL	30	-
Output enable time (-CE)	ten(CE)	tELQNZ	5	-
Output enable time (-OE)	ten(OE)	tGLQNZ	5	-
Data valid from Address Change	tv(A)	tAXQX	0	-

Note: All times are in nanaseconds. Dout signifies data provided by the CompactFlash Card to the system. The –CE signal or both the –OE signal and the –WE signal shall be de-asserted between consecutive cycle operations.

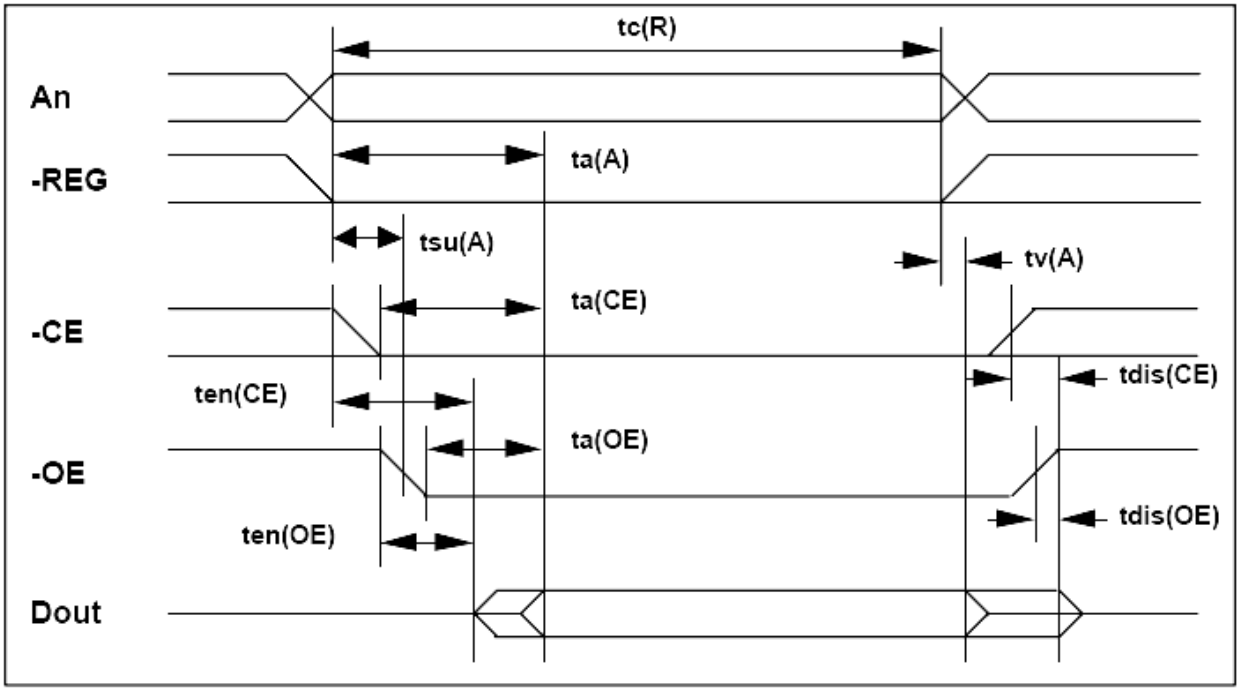


Figure 14: Attribute Memory Read Timing Diagram

The Card Configuration Register (Attribute Memory) write access time is defined as 250ns. Detailed timing specifications are shown in Table 38.

Table 38: Attribute Memory Write Timing

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns)**	**Max (ns)**
Write cycle time	tCW	tAVAV	120	-
Write pulse width	tw(WE)	tWLWH	70	-
Address setup time	tsu(A)	tAVWL	30	-
Write recover time	trec(WE)	tWMAX	30	-
Data setup time for WE	tsu(D-WEH)	tDVWH	20	-
Data hold time	th(D)	tWMDX	10	-

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Card.

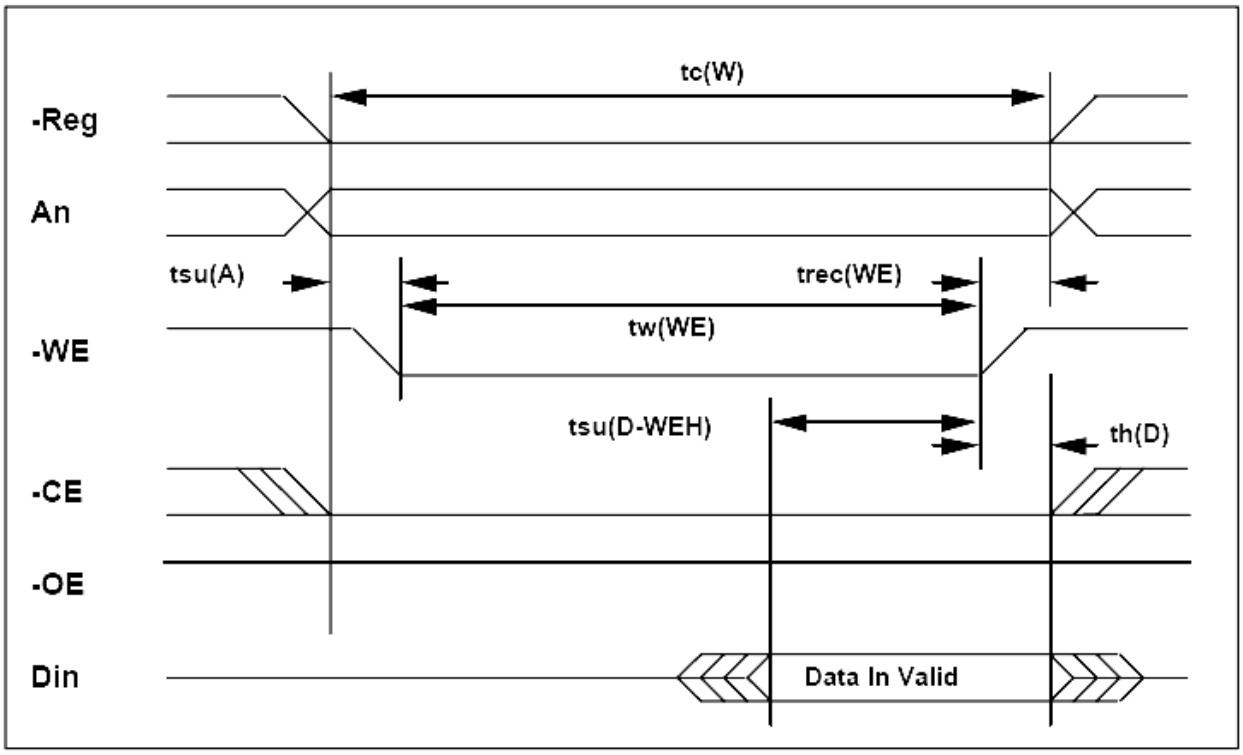


Figure 15: Attribute Memory Write Timing Diagram

Table 39: I/O Access Read Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Data delay after –IORD	td(IORD)	tIGLQV	-	100
Data hold following –IORD	th(IORD)	tIGHQX	0	-
-IORD pulse width	tw(IORD)	tIGLIGH	165	-
Address setup before –IORD	tsuA(IORD)	tAVIGL	70	-
Address hold following –IORD	thA(IORD)	tIGHAX	20	-
-CE setup before –IORD	tsuCE(IORD)	tELIGL	5	-
-CE hold following –IORD	thCE(IORD)	tIGHEH	20	-
-REG setup before –IORD	tsuREG(IORD)	tRGLIGL	5	-
-REG hold following –IORD	thREG(IORD)	tIGHRGH	0	-
-INPACK delay falling from –IORD	tdfINPACK(IORD)	tIGLIAL	-	45
-INPACK delay rising from –IORD	tdrINPACK(IORD)	tIGHIAH	-	45
-IOIS16 delay falling from address	tdfIOIS16(ADR)	tAVISL	-	35
-IOIS16 delay rising from address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL	-	35
Data Delay from Wait Rising	td(WT)	tWTHQV	-	0
Wait pulse width	tw(WT)	tWTLWTH	-	350

Note: Maximum load on –WAIT, -INPACK, and –IOIS16 is 1 LSTTL with 50 pF total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0 nsec, but minimum –IORD width shall be met. Dout signifies data provided by the CompactFlash Card to the system. Wait pulse width meets PCMCIA specifications of 12µs but is intentionally less in this specification.

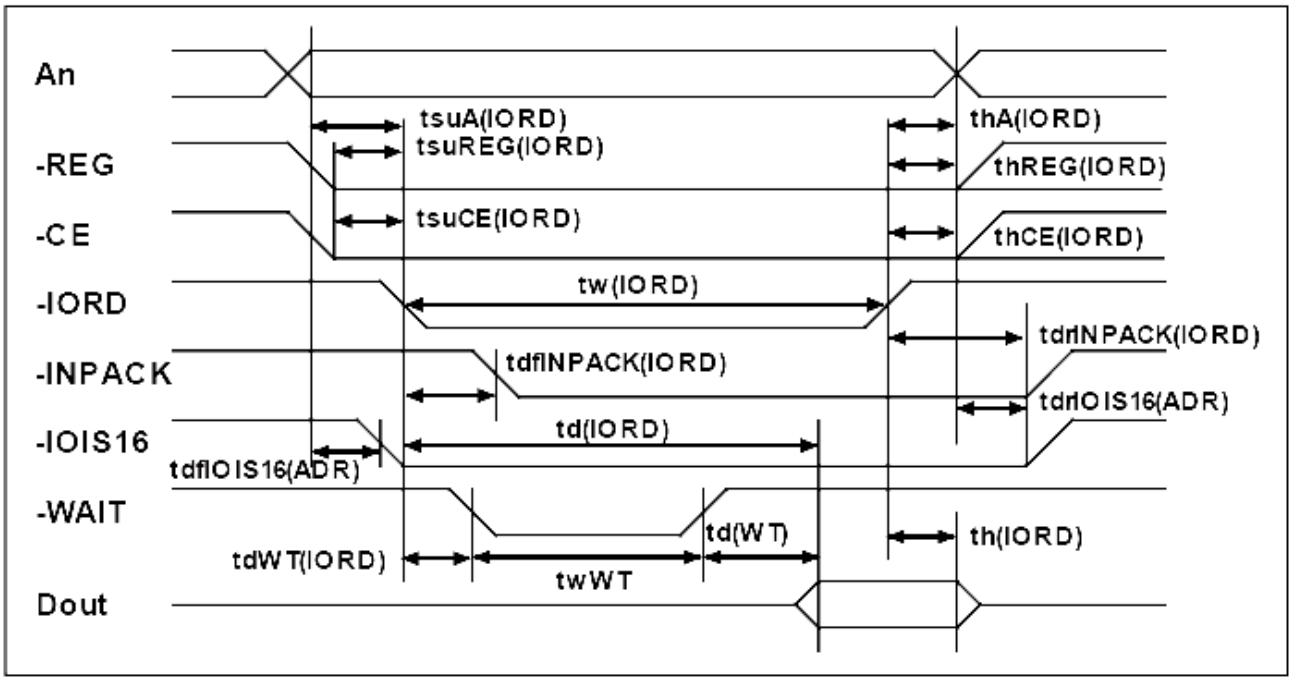


Figure 16: I/O Access Read Timing Diagram

Table 40: I/O Access Write Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Data setup before – IOWR	tsu(IOWR)	tDVIWH	60	-
Data hold following – IOWR	th(IOWR)	tIWHDX	30	-
- IOWR pulse width	tw(IOWR)	tIWLIWH	165	-
Address setup before – IOWR	tsuA(IOWR)	tAVIWL	70	-
Address hold following – IOWR	thA(IOWR)	tIWHAX	20	-
-CE setup before – IOWR	tsuCE(IOWR)	tELIWL	5	-
-CE hold following – IOWR	thCE(IOWR)	tIWHEH	20	-
-REG setup before – IOWR	tsuREG(IOWR)	tRGLIWL	5	-
-REG hold following – IOWR	thREG(IOWR)	tIWHRGH	0	-
-IOIS16 delay falling from address	tdfIOIS16(ADR)	tAVISL	-	35
-IOIS16 delay rising from address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL	-	35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	-
Wait pulse width	tw(WT)	tWTLWTH	-	350

Note: Maximum load on –WAIT, -INPACK, and –IOIS16 is 1 LSTTL with 50 pF total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0 nsec, but minimum –IORD width shall be met. Din signifies data provided by the CompactFlash Card to the system. Wait pulse width meets PCMCIA specifications of 12µs but is intentionally less in this specification.

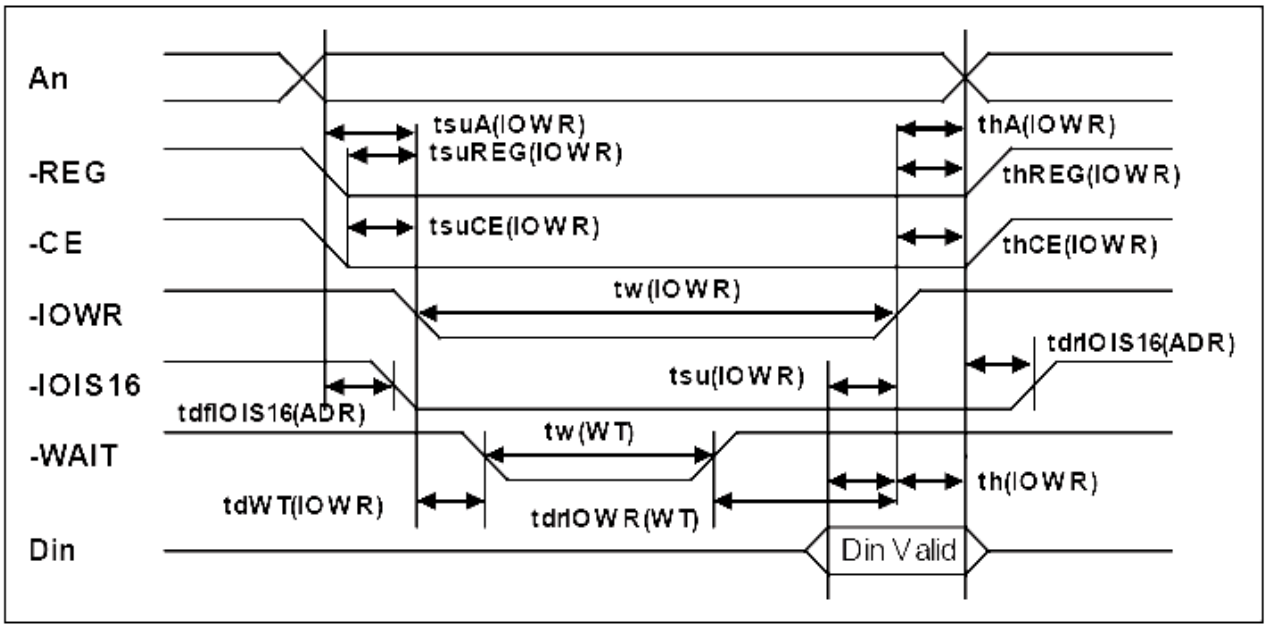


Figure 17: I/O Access Write Timing Diagram

Table 41: Common Memory Access Read Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Output Enable access time	ta(OE)	tGLQV	-	50
Output disable time (-OE)	tdis(OE)	tGHQZ	-	30
Address setup time	tsu (A)	tAVGL	30	-
Address hold time	th(A)	tGHAX	20	-
-CE setup time	tsu(CE)	tELGL	0	-
-CE hold time	th(CE)	tGHEH	20	-
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV	-	35
Data Setup for Wait Release	tv(WT)	tQVWTH	-	0
Wait pulse width	tw(WT)	tWTLWTH	-	350

Note: Maximum load on –WAIT is 1 LSTTL with 50 pF total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait pulse width. The Wait pulse width meets PCMCIA specifications of 12µs but is intentionally less in this specification.

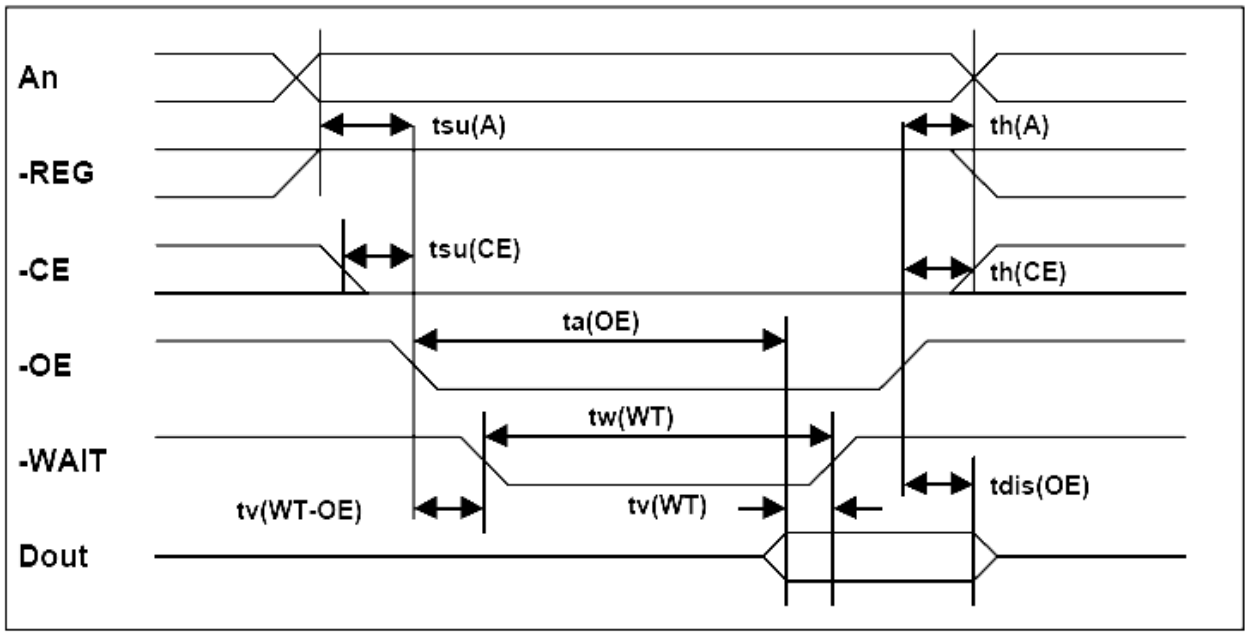


Figure 18: Common Memory Access Read Timing Diagram

Table 42: Common Memory Access Write Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Data setup time (-WE)	tsu(D-WEH)	tDVWH	20	-
Data hold time	th(D)	tWMDX	10	-
WE pulse time	tw(WE)	tWLWH	70	-
Address setup time	tsu (A)	tAVWL	30	-
-CE setup time	tsu(CE)	tELWL	0	-
Write recover time	trec(WE)	tWMAX	30	-
Address hold time	th(A)	tGHAX	20	-
-CE Hold following WE	th(CE)	tGHEH	20	-
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV	-	35
WE High from Wait Release	tv(WT)	tWTHWH	0	-
Wait pulse width	tw(WT)	tWTLWTH	-	350

Note: Maximum load on –WAIT is 1 LSTTL with 50 pF total load. All times are in nanoseconds. Din signifies data provided by the CompactFlash Card to the system. The –WAIT signal may be ignored if the –WE cycle to cycle time is greater than the Wait pulse width. The Max Wait pulse width can be determined from the Card Information Structure. The Wait pulse width meets PCMCIA specifications of 12µs but is intentionally less in this specification.

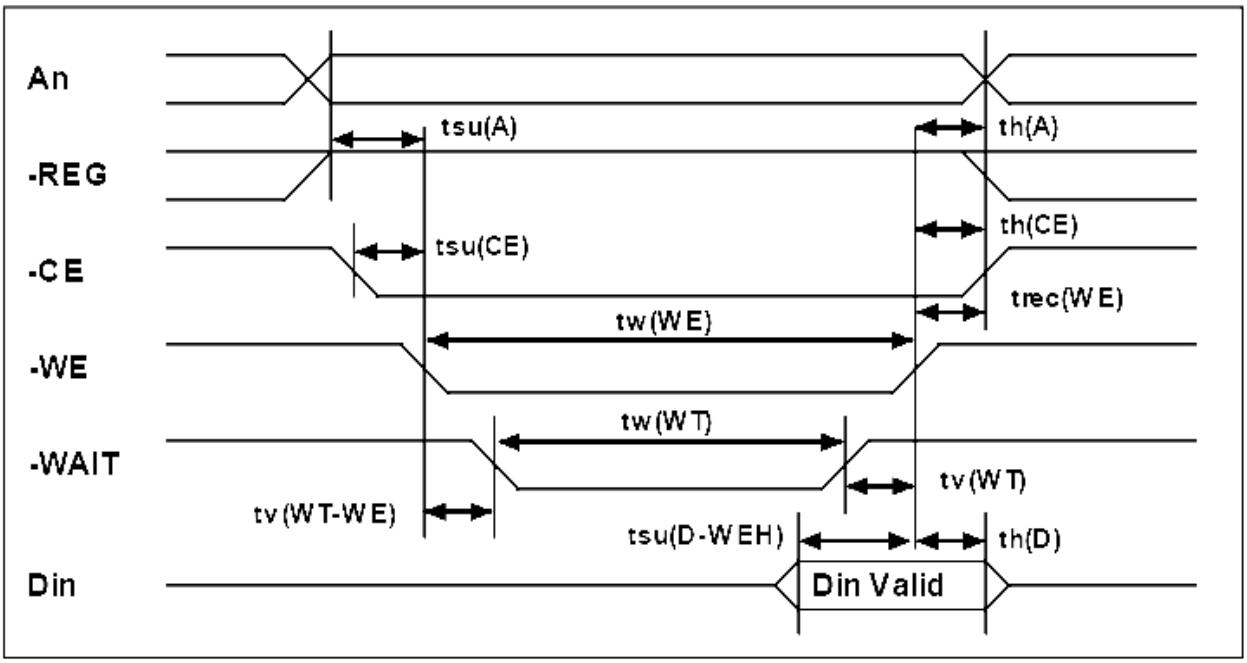


Figure 19: Common Memory Access Write Timing Diagram

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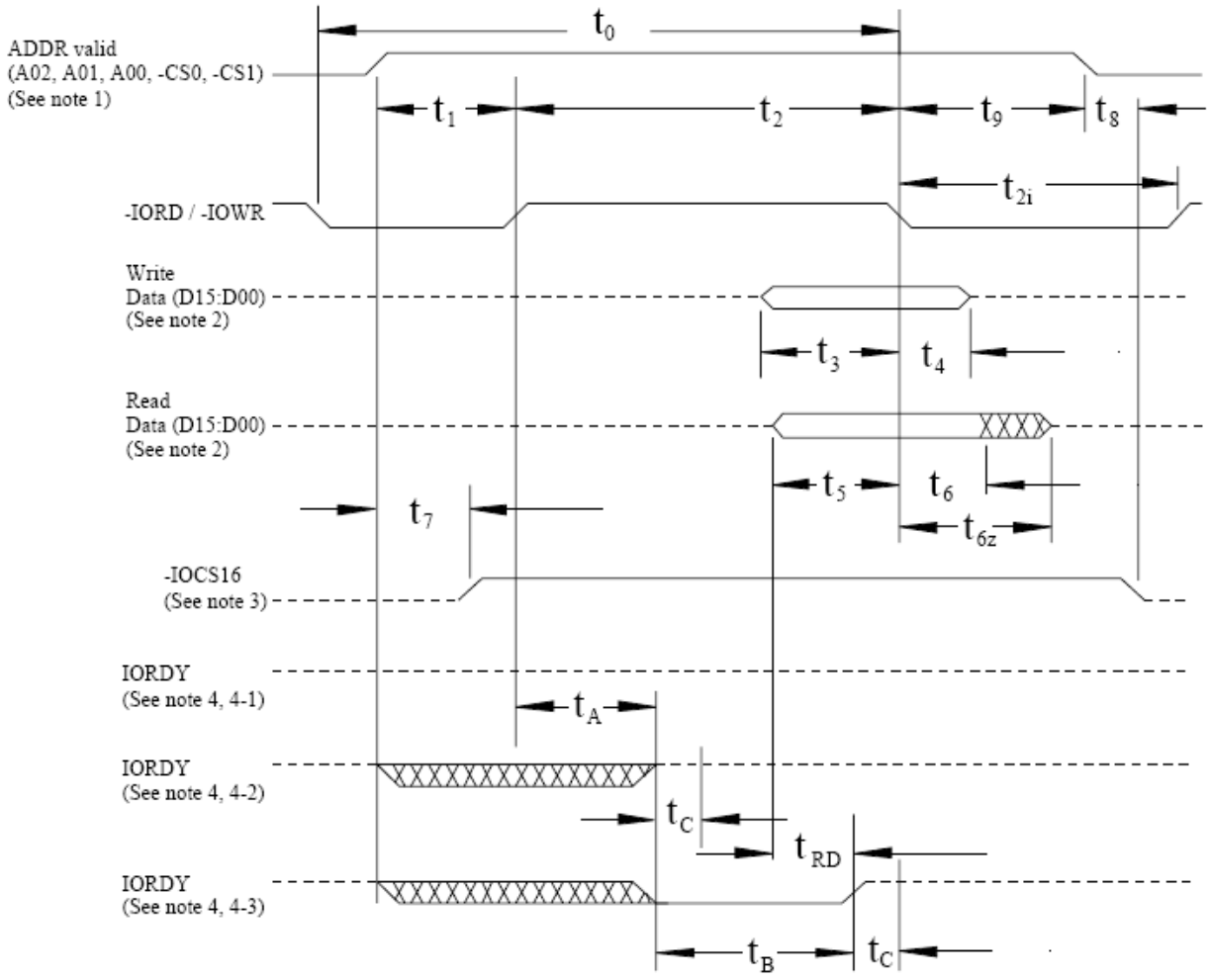
The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR, and the –IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 43: True IDE Mode I/O Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t0	Cycle time (min)	600	383	240	180	120	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	
t2	-IORD/-IOWR (min)	165	125	100	80	70	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	1
t3	-IOWR data setup (min)	60	45	30	30	20	
t4	-IOWR data hold (min)	30	20	15	10	10	
t5	-IORD data setup (min)	50	35	20	20	20	
t6	-IORD data hold (min)	50	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	2
t7	Address valid to –IOCS16 assertion (max)	90	50	40	n/a	n/a	4
t8	Address valid to –IOCS16 released (max)	60	45	30	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
tC	IORDY assertion to release (max)	5	5	5	5	5	

Notes: The maximum load on –IOCS16 is 1 LSTTL with a 50 pF total load. All times are in nanoseconds. Minimum time from –IORDY high to –IORD high is 0 nsec, but minimum –IORD width shall still be met.

1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify drive data. A CompactFlash Card implementation shall support any legal host implementation.
2) This parameter specifies the time from the negation edge of –IORD to the time that the data bus is no longer driven by the CompactFlash Card (tri-state).
3) The delay from the activation of –IORD or –IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Card is not driving IORDY negated at tA after the activation of –IORD or –IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Card is driving IORDY negated at the time tA after the activation of –IORD or –IOWR, then tRD shall be met and t5 is not applicable.
4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.



Notes:

(1) Device address consists of –CS0, -CS1, and A[02::00]

(2) Data consists of D[15::00] (16-bit) or D[07::00] (8-bit)

(3) –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of –IORD or –IOWR. The assertion and negation of IORDY is described in the following three cases:

(4-1) Device never negates IORDY: No wait is generated.

(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.

(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and –IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

ALL WAVEFORMS IN HIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 20: True IDE Mode I/O Timing Diagram

The timing diagram for True IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR, and the –IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

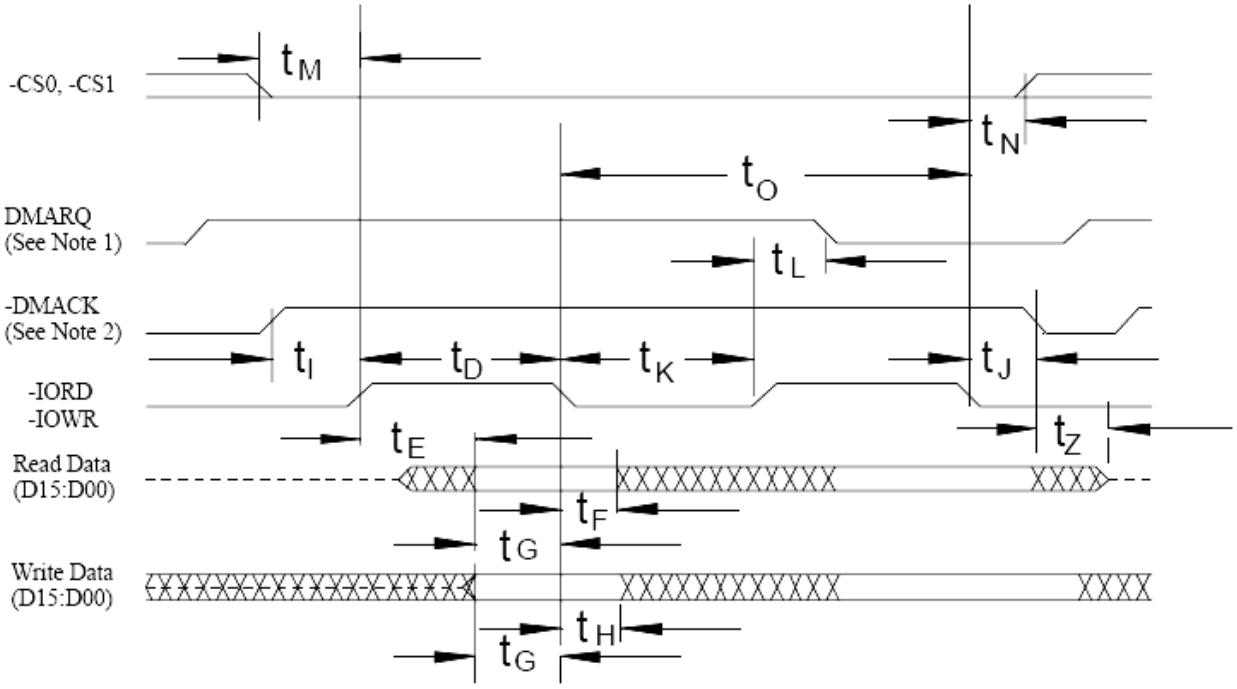
Table 44: True IDE DMA Mode I/O Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Note
t_O	Cycle time (min)	480	150	120	1
t_D	-IORD/-IOWR asserted width (min)	215	80	70	1
t_E	-IORD data access (max)	150	60	50	
t_F	-IORD data hold (min)	5	5	50	
t_G	-IORD/-IOWR data setup (min)	100	30	20	
t_H	-IOWR data hold (min)	20	15	10	
t_I	DMACK to -IORD/-IOWR setup (min)	0	0	0	
t_J	-IORD/-IOWR to –DMACK hold (min)	20	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	1
t_{KW}	-IOWR negated width (min)	215	50	25	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	
t_M	CS(1:0) valid to -IORD/-IOWR	50	30	25	
t_N	CS(1:0) hold	15	10	10	
t_Z	-DMACK	20	25	25	

Notes:

1) t_O is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_O, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_O is equal to or greater than the value reported in the device's identify drive data. A CompactFlash Card implementation shall support any legal host implementation.

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Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN HIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 21: True IDE DMA Mode I/O Timing Diagram

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3.4 Reset Characteristics (Memory Card Mode & I/O Card Mode)

Table 45: Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Reset setup time	tsu(RESET)	100	-	-	ms
-CE recover time	trec(VCC)	1	-	-	µs
VCC rising up time	tpr	0.1	-	100	ms
VCC falling down time	tpf	3	-	300	ms
Reset pulse width	tw(RESET)	10	-	-	µs
	th(Hi-Z RESET)	1	-	-	ms
	ts(Hi-Z RESET)	0	-	-	ms

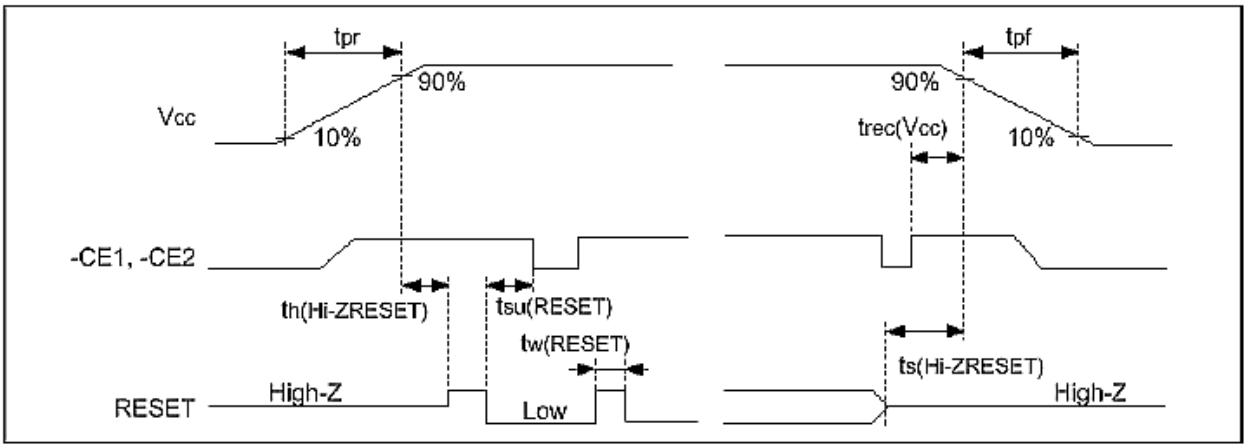


Figure 22: Hard Reset Timing

Table 46: Power on Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
-CE setup time	tsu(VCC)	100	-	-	ms
VCC rising up time	tpr	0.1	-	100	ms

NOTE:
1. All card status is reset automatically when Vcc goes over 2.3V.

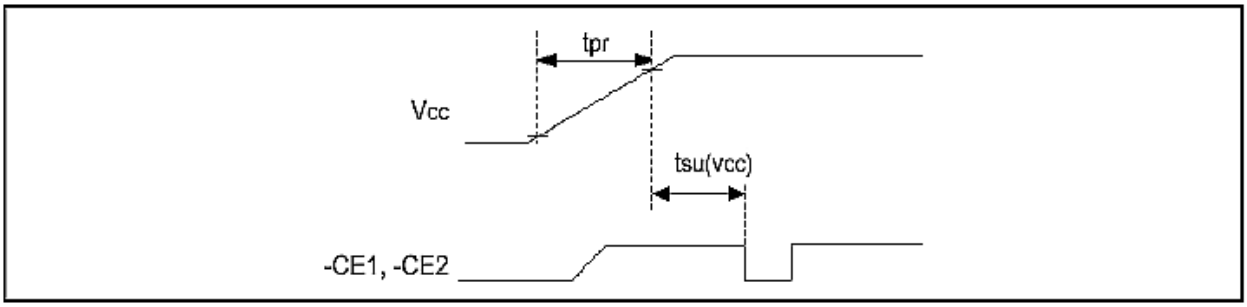


Figure 23: Power on Reset Timing

3.5 User Notes

In the reset or power off, all register information is cleared. All card status is cleared automatically when Vcc voltage turns below about 2.5V. Notice that the card insertion/removal should not be executed when host is active in True IDE Mode. After card hard reset, soft reset, power-on reset, or ATA reset, the card cannot be operated until +RDY/-BSY pin is moved from "low". Notice that the card removal should be executed after card internal operations are completed. Before the card insertion, Vcc cannot be supplied to the card. After confirmation that –CD1, -CD2 pins are inserted, supply Vcc to the card. –OE must be kept at the Vcc level during power on reset in memory card mode and I/O card mode. –OE must be kept constantly at the GND level in True IDE Mode.

4.0 Physical Specifications

Table 47: Physical Specifications

Weight:	11.4 g (0.40 oz) typical, 14.2 g (0.50 oz) maximum
Length:	36.40 ± 0.15 mm (1.433 ± 0.006 in)
Width:	42.80 ± 0.10 mm (1.685 ± 0.004 in)
Thickness:	3.3 ± 0.10 mm (0.13 ± 0.004 in) – Excluding Lip

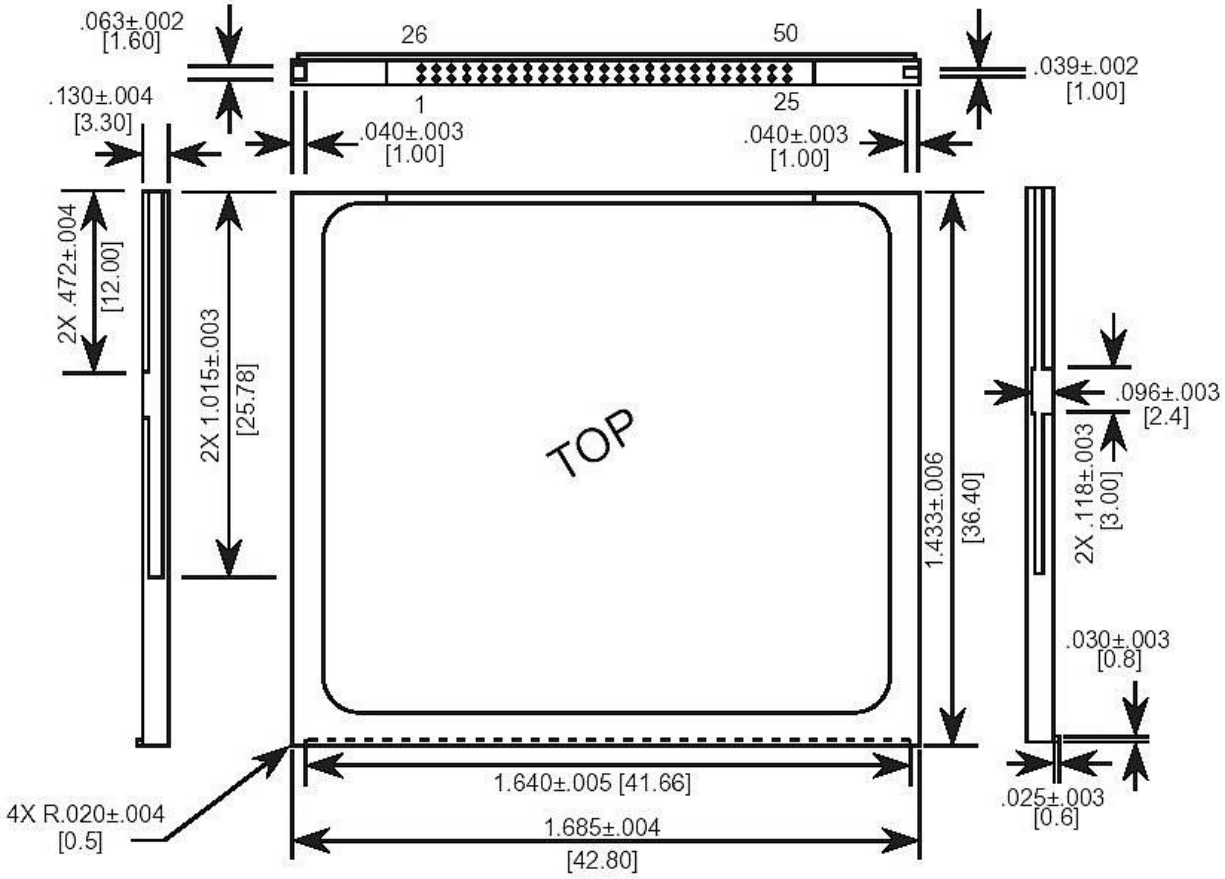


Figure 24: Physical Dimensions

4.1 Labelling and Marking

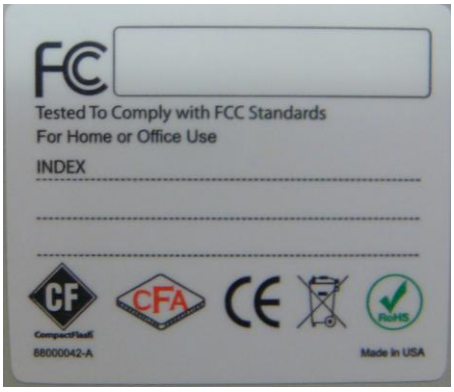




Fig 25 & 26 CF Card Back and Front Labels

The standard labels used for Wintec Industrial CF cards are shown in figs 25 & 26. The front label will indicate the capacity of the card and will indicate if the card is Industrial Temperature (no marking if not). The back label will contain the various logos indicating compliance with appropriate bodies and regulations. The back label will also be inked in marked area with the part number and lot numbers of the cards. Customized labeling is available upon request.

5.0 Ordering Information

Table 48: Product Availability List & Naming

Card Capacity	Part Number	Real Capacity	Total Sectors/Card (Max LBA+1)	Cylinders	Heads	Sectors
32 MB	W7CF032M1vA(I)-w0Px-yyy.z	32,636,928	63,744	498	4	32
64 MB	W7CF064M1vA(I)-w0Px-yyy.z	65,536,000	128,000	1,000	4	32
128 MB	W7CF128M1vA(I)-w0Px-yyy.z	131,334,144	256,512	1,002	8	32
256 MB	W7CF256M1vA(I)-w0Px-yyy.z	262,930,432	513,536	1,003	16	32
512 MB	W7CF512M1vA(I)-w0Px-yyy.z	526,417,920	1,028,160	1,020	16	63
1 – GB	W7CF001G1vA(I)-w0Px-yyy.z	1,054,900,224	2,060,352	2,044	16	63
2 – GB	W7CF002G1vA(I)-w0Px-yyy.z	2,118,057,984	4,136,832	4,104	16	63
4 – GB	W7CF004G1vA(I)-w0Px-yyy.z	4,244,889,600	8,290,800	8,225	16	63
8 – GB	W7CF008G1vA(I)-w0Px-yyy.z	8,455,200,768	16,435,440	16305	16	63
16 – GB	W2CF016G1vA(I)-w0Px-yyy.z	TBD	32,014,080	31760	16	63

NOTE:
1. Total Sectors/Card = Sectors/Track * # Heads * # Cylinders
2. Real Capacity = The logical address capacity including the area used for file system and controller overhead.
3. Cards default with DMA disabled. For DMA Enable use "w1Px" Suffix.
4. (I) denotes Industrial Temperature option, leave blank for standard Commercial Temp.

(v) Disk/Interface Options
X : Removable Disk True IDE Capable
P : SPI Interface
T : Fixed Disk True IDE

(w) Controller Options
H2 : Hyperstone F2
H3 : Hyperstone F3
S : SMI
T : Toshiba

(x) Component Flash IC Die Revision
A : A- die
B : B- die
C : C- die
D : D- die

(yyy) Component Flash type
001: 1-Nand Flash chip
01D: 1-Nand, Dual Die, 1-CE
1D2: 1-Nand, Dual Die, 2-CE
1Q2: 1-Nand, Quad Die, 2-CE
002: 2-Nand Flash chips
02D: 2-Nand, Dual Die, 1-CE
2D2: 2-Nand, Dual Die, 2-CE
2Q2: 2-Nand, Quad Die, 2-CE
4D2: 4-Nand, Dual Die, 2-CE
4Q2: 4-Nand, Quad Die, 2-CE

(z) Firmware Options
.00 : 060729
.01 : 080112
.02 : 090720
.03 : 100924

Firmware Revision/Options (Optional)
Please contact the factory for the latest firmware revisions and/or custom labeling and programming identification.

Contact Us (US & Int'l):

Wintec Industries OEM Sales
675 Sycamore Drive
Milpitas, CA 95035
Ph: 408-856-0663
Fax: 408-856-0518

oemsales@wintecind.com
http://www.wintecind.com/oem

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ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
ОГРН: 1167746717709