Complete 14-Bit CCD/CIS Signal Processor

AD9814

FEATURES

14-Bit 10 MSPS A/D Converter
No Missing Codes Guaranteed
3-Channel Operation Up to 10 MSPS
1-Channel Operation Up to 7 MSPS
Correlated Double Sampling
1-6x Programmable Gain
±300 mV Programmable Offset
Input Clamp Circuitry
Internal Voltage Reference
Multiplexed Byte-Wide Output (8+6 Format)
3-Wire Serial Digital Interface
+3/+5 V Digital I/O Compatibility
28-Lead SOIC Package
Low Power CMOS: 330 mW (Typ)
Power-Down Mode: <1 mW

APPLICATIONS

Flatbed Document Scanners
Film Scanners
Digital Color Copiers
Multifunction Peripherals

PRODUCT DESCRIPTION

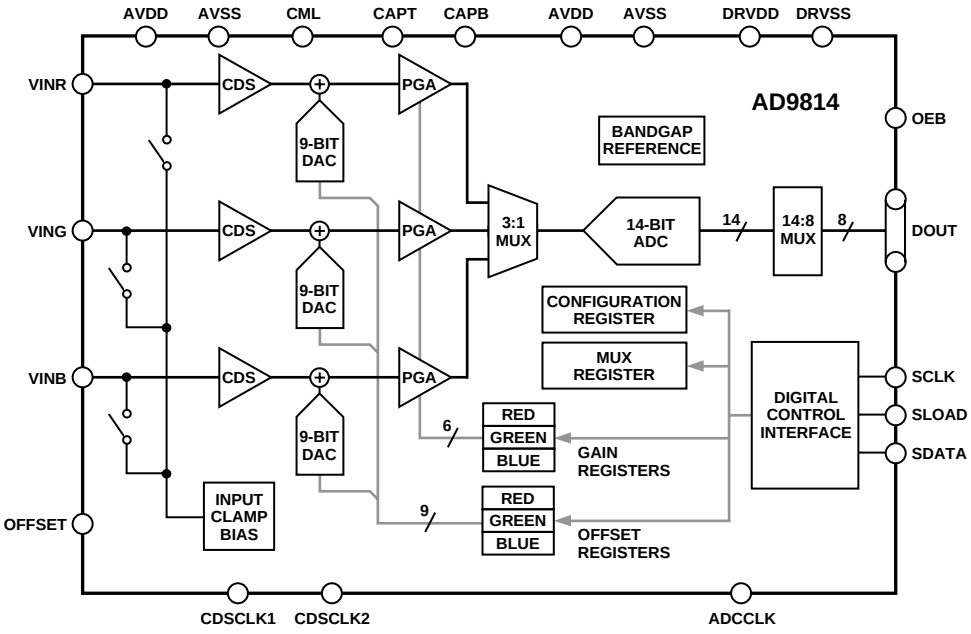
The AD9814 is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of trilinear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), multiplexed to a high performance 14-bit A/D converter.

The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 14-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, and provide adjustment of the gain, offset, and operating mode.

The AD9814 operates from a single +5 V power supply, typically consumes 330 mW of power, and is packaged in a 28-lead SOIC.

FUNCTIONAL BLOCK DIAGRAM



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AD9814–SPECIFICATIONS

ANALOG SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DRVDD = +5 V, 3-Channel CDS Mode, f_{ADCCLK} = 6 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 2 MHz, PGA Gain = 1, Input Range = 4 V, unless otherwise noted.)

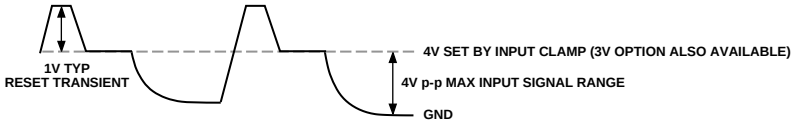
Parameter	J-Grade Min	J-Grade Typ	J-Grade Max	K-Grade Min	K-Grade Typ	K-Grade Max	Units
CONVERSION RATE							
3-Channel Mode with CDS		6	10		6	10	MSPS
1-Channel Mode with CDS		6	7		6	7	MSPS
ACCURACY (Entire Signal Path)							
ADC Resolution		14			14		Bits
Integral Nonlinearity[1] (INL)		+2.5/–6.0			+2.5/–6.0	±11.0	LSB
INL @ 10 MHz		+4.0/–7.0			+4.0/–7.0		LSB
Differential Nonlinearity (DNL)		+0.6/–0.5			+0.6/–0.5	±1.0	LSB
DNL @ 10 MHz		+0.8/–0.6			+0.8/–0.6		LSB
No Missing Codes Guaranteed	13			14			Bits
Offset Error		–12			–12	±104	mV
Gain Error[2]		2.2			2.2	±5.3	% FSR
ANALOG INPUTS							
Input Signal Range[3]		4.0			4.0		V p-p
Allowable Reset Transient[3]		1.0			1.0		V
Input Limits[4]	AVSS – 0.3		AVDD + 0.3	AVSS – 0.3		AVDD + 0.3	V
Input Capacitance		10			10		pF
Input Bias Current		10			10		nA
AMPLIFIERS							
PGA Gain at Minimum		1			1		V/V
PGA Gain at Maximum		5.8			5.8		V/V
PGA Resolution		64			64		Steps
PGA Monotonicity		Guaranteed			Guaranteed		
Programmable Offset at Minimum		–300			–300		mV
Programmable Offset at Maximum		+300			+300		mV
Programmable Offset Resolution		512			512		Steps
Programmable Offset Monotonicity		Guaranteed			Guaranteed		
NOISE AND CROSSTALK							
Input Referred Noise @ PGA Min		130			130		µV rms
Total Output Noise @ PGA Min		0.55			0.55		LSB rms
Input Referred Noise @ PGA Max		84			84		µV rms
Total Output Noise @ PGA Max		2.0			2.0		LSB rms
Channel-Channel Crosstalk		<1			<1		LSB
POWER SUPPLY REJECTION							
AVDD = +5 V ± 0.25 V		0.07			0.07	0.3	% FSR
Differential VREF (@ +25°C)							
CAPT-CAPB (4 V Input Range)		2.0		1.9	2.0	2.1	V
CAPT-CAPB (2 V Input Range)		1.0		0.94	1.0	1.06	V
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	–65		+150	–65		+150	°C
POWER SUPPLIES							
AVDD	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
DRVDD	+3.0	+5.0	+5.25	+3.0	+5.0	+5.25	V
Total Operating Current							
AVDD		64			64	80	mA
DRVDD		1.8			1.8	10	mA
Power-Down Mode Current		150			150		µA
Power Dissipation		330			330	450	mW
Power Dissipation @ 10 MHz		355			355		mW
Power Dissipation (1-Channel Mode)		220			220	265	mW

NOTES

[1]The Integral Nonlinearity in measured using the "fixed endpoint" method, NOT using a "best-fit" calculation. See Definitions of Specifications.

[2]The Gain Error specification is dominated by the tolerance of the internal differential voltage reference.

[3]Linear input signal range is from 0 V to 4 V when the CCD's reference level is clamped to 4 V by the AD9814's input clamp. A larger reset transient can be tolerated by using the 3 V clamp level instead of the nominal 4 V clamp level. Linear input signal range will be from 0 V to 3 V when using the 3 V clamp level.



[4]The input limits are defined as the maximum tolerable voltage levels into the AD9814. These levels are not intended to be in the linear input range of the device. Signals beyond the input limits will turn on the overvoltage protection diodes.

[5]The PGA Gain is approximately "linear in dB" and follows the equation: $Gain = \left[\frac{5.8}{1 + 4.8\left[\frac{63 - G}{63}\right]}\right]$ where G is the register value. See Figure 13.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DRVDD = +5 V, CDS Mode, f_{ADCCLK} = 6 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 2 MHz, C_L = 10 pF, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.6			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	4.5			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Output Current	I_{OH}		50		µA
Low Level Output Current	I_{OL}		50		µA

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DRVDD = +5 V)

Parameter	Symbol	Min	Typ	Max	Units
CLOCK PARAMETERS					
3-Channel Pixel Rate	t_{PRA}	300	500		ns
1-Channel Pixel Rate	t_{PRB}	140			ns
ADCCLK Pulsewidth	t_{ADCLK}	45			ns
CDSCLK1 Pulsewidth	t_{C1}	20			ns
CDSCLK2 Pulsewidth	t_{C2}	40			ns
CDSCLK1 Falling to CDSCLK2 Rising	t_{C1C2}	0			ns
ADCCLK Falling to CDSCLK2 Rising	t_{ADC2}	10			ns
CDSCLK2 Rising to ADCCLK Rising	t_{C2ADR}	10			ns
CDSCLK2 Falling to ADCCLK Falling	t_{C2ADF}	50			ns
CDSCLK2 Falling to CDSCLK1 Rising	t_{C2C1}	50			ns
ADCCLK Falling to CDSCLK1 Rising	t_{ADC1}	0			ns
Aperture Delay for CDS Clocks	t_{AD}		3		ns
SERIAL INTERFACE					
Maximum SCLK Frequency	f_{SCLK}	10			MHz
SLOAD to SCLK Set-Up Time	t_{LS}	10			ns
SCLK to SLOAD Hold Time	t_{LH}	10			ns
SDATA to SCLK Rising Set-Up Time	t_{DS}	10			ns
SCLK Rising to SDATA Hold Time	t_{DH}	10			ns
SCLK Falling to SDATA Valid	t_{RDV}	10			ns
DATA OUTPUT					
Output Delay	t_{OD}		6		ns
3-State to Data Valid	t_{DV}		16		ns
Output Enable High to 3-State	t_{HZ}		5		ns
Latency (Pipeline Delay)			3 (Fixed)		Cycles

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Units
VIN, CAPT, CAPB	AVSS	–0.3	AVDD + 0.3	V
Digital Inputs	AVSS	–0.3	AVDD + 0.3	V
AVDD	AVSS	–0.5	+6.5	V
DRVDD	DRVSS	–0.5	+6.5	V
AVSS	DRVSS	–0.3	+0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD9814JR	0°C to +70°C	28-Lead 300 Mil SOIC
AD9814KR	0°C to +70°C	28-Lead 300 Mil SOIC

THERMAL CHARACTERISTICS

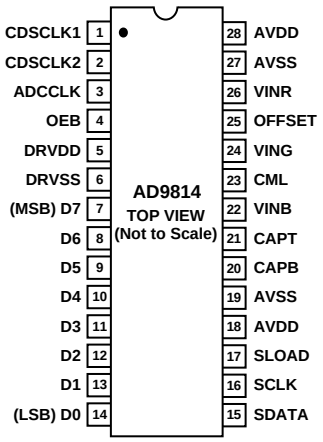
Thermal Resistance

28-Lead 300 Mil SOIC

θ_{JA} = 71.4°C/W

θ_{JC} = 23°C/W

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Type	Description
1	CDSCLK1	DI	CDS Reference Level Sampling Clock
2	CDSCLK2	DI	CDS Data Level Sampling Clock
3	ADCCLK	DI	A/D Converter Sampling Clock
4	OEB	DI	Output Enable, Active Low
5	DRVDD	P	Digital Output Driver Supply
6	DRVSS	P	Digital Output Driver Ground
7	D7	DO	Data Output MSB. ADC DB13 High Byte, ADC DB5 Low Byte
8	D6	DO	Data Output. ADC DB12 High Byte, ADC DB4 Low Byte
9	D5	DO	Data Output. ADC DB11 High Byte, ADC DB3 Low Byte
10	D4	DO	Data Output. ADC DB10 High Byte, ADC DB2 Low Byte
11	D3	DO	Data Output. ADC DB9 High Byte, ADC DB1 Low Byte
12	D2	DO	Data Output. ADC DB8 High Byte, ADC DB0 Low Byte
13	D1	DO	Data Output. ADC DB7 High Byte, Don't Care Low Byte
14	D0	DO	Data Output LSB. ADC DB6 High Byte, Don't Care Low Byte
15	SDATA	DI/DO	Serial Interface Data Input/Output
16	SCLK	DI	Serial Interface Clock Input
17	SLOAD	DI	Serial Interface Load Pulse
18	AVDD	P	+5 V Analog Supply
19	AVSS	P	Analog Ground
20	CAPB	AO	ADC Bottom Reference Voltage Decoupling
21	CAPT	AO	ADC Top Reference Voltage Decoupling
22	VINB	AI	Analog Input, Blue Channel
23	CML	AO	Internal Bias Level Decoupling
24	VING	AI	Analog Input, Green Channel
25	OFFSET	AO	Clamp Bias Level Decoupling
26	VINR	AI	Analog Input, Red Channel
27	AVSS	P	Analog Ground
28	AVDD	P	+5 V Analog Supply

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9814 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity error refers to the deviation of each individual code from a line drawn from "zero scale" through "positive full scale." The point used as "zero scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

OFFSET ERROR

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

GAIN ERROR

The last code transition should occur for an analog value 1 1/2 LSB below the nominal full-scale voltage. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

INPUT REFERRED NOISE

The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and converted to an equivalent voltage, using the relationship 1 LSB = 4 V/16384 = 244 mV. The noise is then referred to the input of the AD9814 by dividing by the PGA gain.

CHANNEL-TO-CHANNEL CROSSTALK

In an ideal three channel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel crosstalk specification is a measure of the change that occurs in one channel as the other two channels are varied. In the AD9814, one channel is grounded and the other two channels are exercised with full-scale input signals. The change in the output codes from the first channel is measured and compared with the result when all three channels are grounded. The difference is the channel-to-channel crosstalk, stated in LSB.

APERTURE DELAY

The aperture delay is the time delay that occurs from when a sampling edge is applied to the AD9814 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

POWER SUPPLY REJECTION

Power Supply Rejection specifies the maximum full-scale change that occurs from the initial value when the supplies are varied over the specified limits.

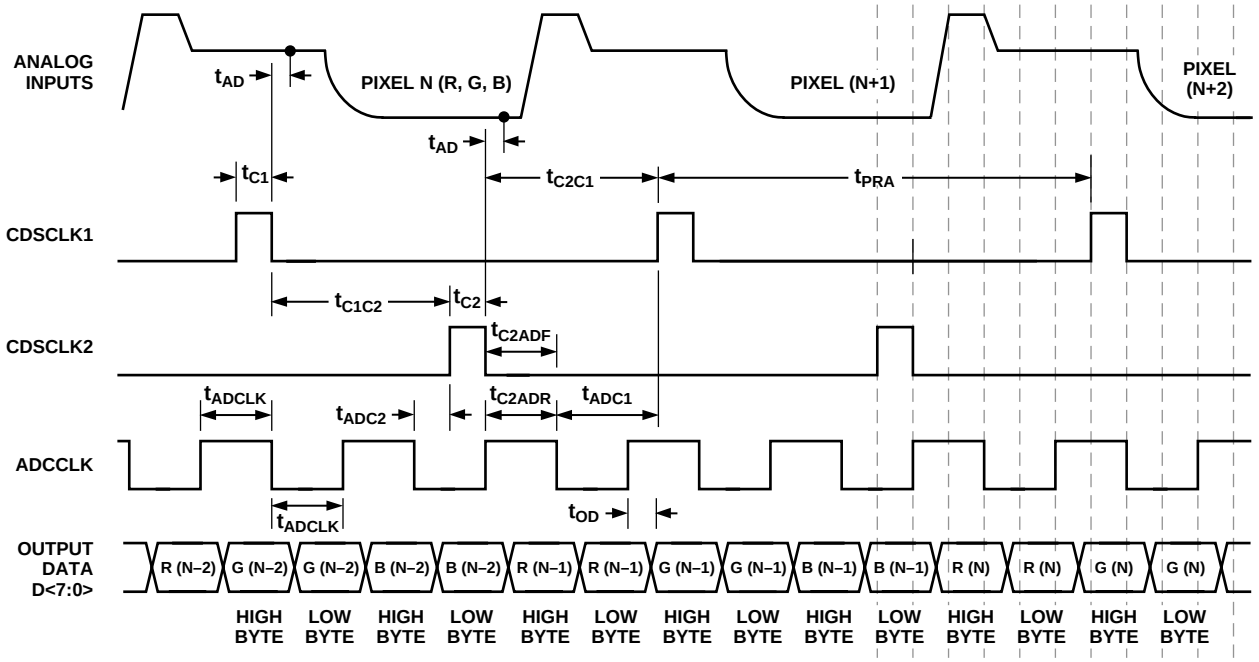


Figure 1. 3-Channel CDS Mode Timing

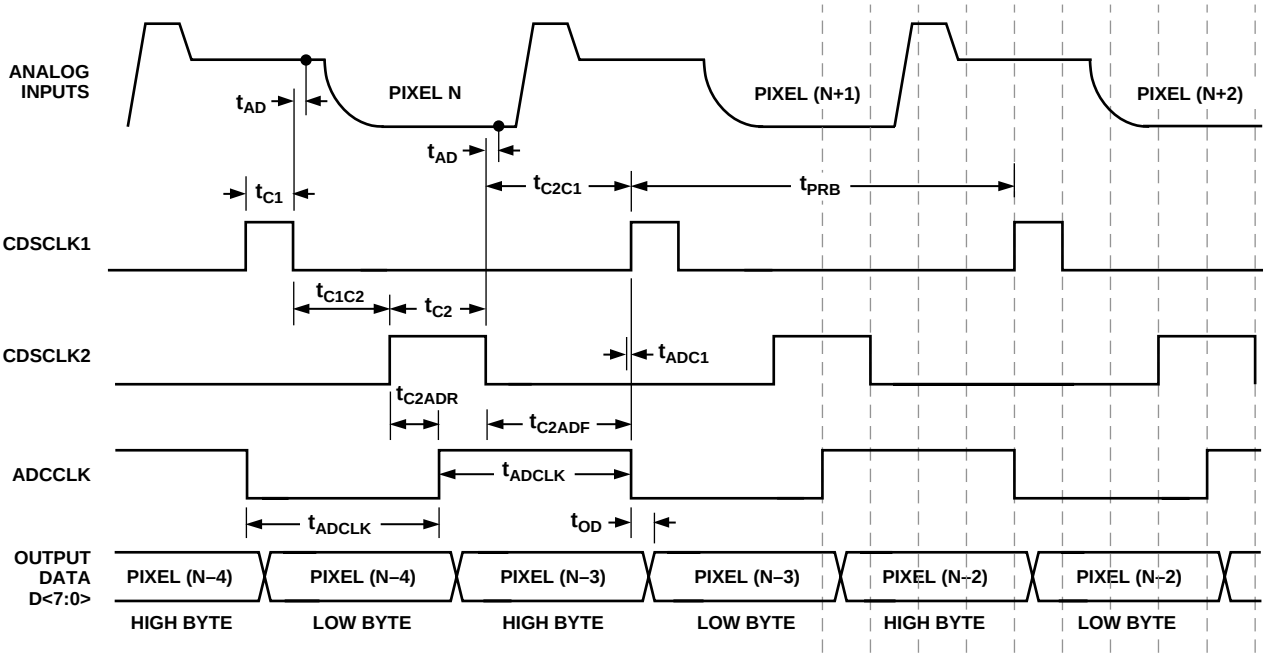


Figure 2. 1-Channel CDS Mode Timing

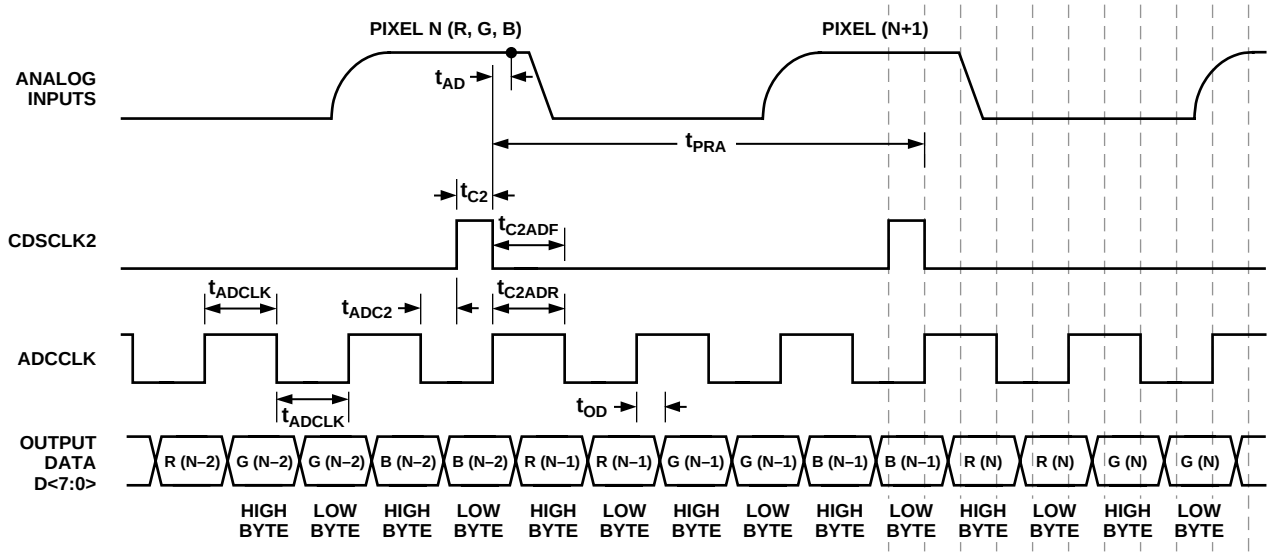


Figure 3. 3-Channel SHA Mode Timing

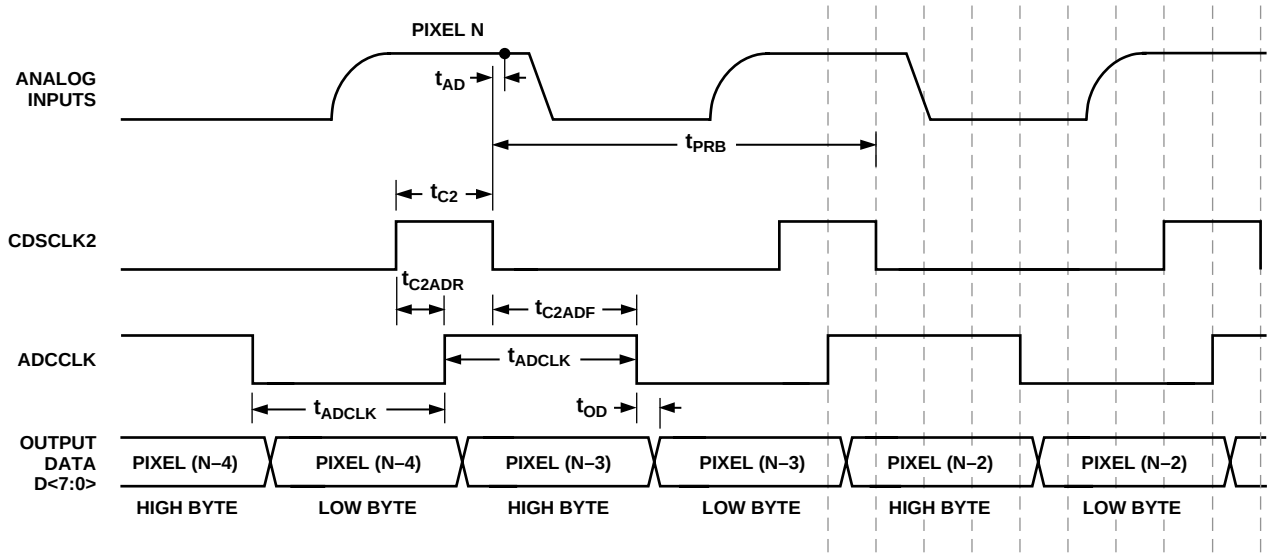


Figure 4. 1-Channel SHA Mode Timing

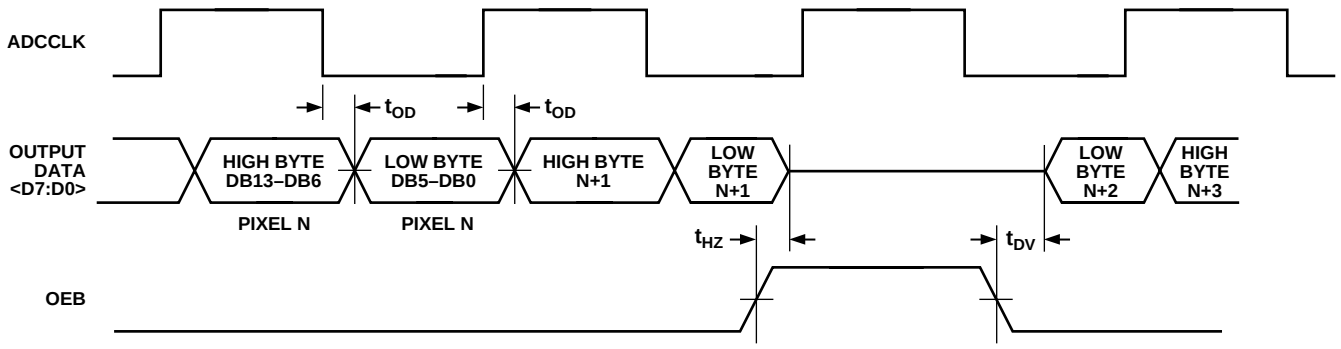


Figure 5. Digital Output Data Timing

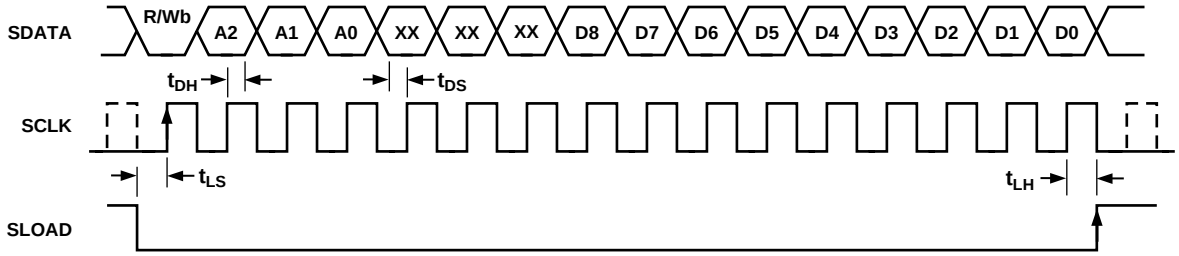


Figure 6. Serial Write Operating Timing

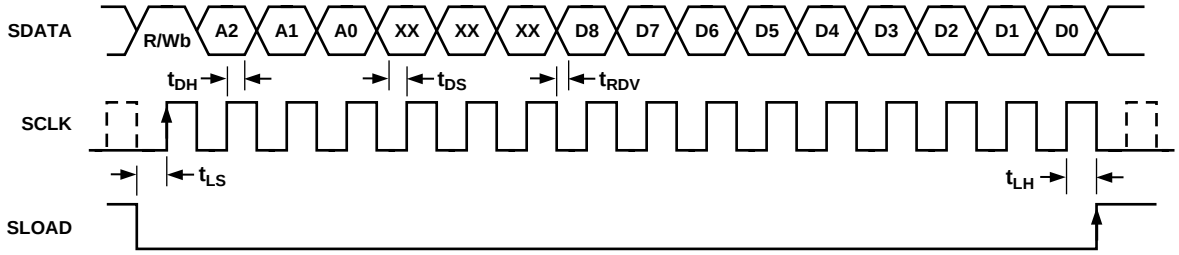


Figure 7. Serial Read Operation Timing

FUNCTIONAL DESCRIPTION

The AD9814 can be operated in four different modes: 3-Channel CDS Mode, 3-Channel SHA Mode, 1-Channel CDS Mode, and 1-Channel SHA Mode. Each mode is selected by programming the Configuration Register through the serial interface. For more detail on CDS or SHA mode operation, see the Circuit Operation section.

3-Channel CDS Mode

In 3-Channel CDS Mode, the AD9814 simultaneously samples the red, green and blue input voltages from the CCD outputs. The sampling points for each Correlated Double Sampler (CDS) are controlled by CDSCLK1 and CDSCLK2 (see Figures 8 and 9). CDSCLK1's falling edge samples the reference level of the CCD waveform. CDSCLK2's falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD's reference and data levels. Next, the output voltage of each CDS amplifier is level-shifted by an Offset DAC. The voltages are then scaled by the three Programmable Gain Amplifiers before being multiplexed through the 14-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The offset and gain values for the red, green and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register.

Timing for this mode is shown in Figure 1. It is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK, although this is not required to satisfy the minimum timing constraints. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three clock cycles.

3-Channel SHA Mode

In 3-Channel SHA Mode, the AD9814 simultaneously samples the red, green and blue input voltages. The sampling point is controlled by CDSCLK2. CDSCLK2's falling edge samples the input waveforms on each channel. The output voltages from the three SHAs are modified by the offset DACs and then scaled by the three PGAs. The outputs of the PGAs are then multiplexed through the 14-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin (see Figure 10). With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero-scale output. The OFFSET pin may also be used as a coarse offset adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the red, green and blue inputs in the first amplifier stage of the AD9814. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 2. CDSCLK1 should be grounded in this mode. Although not required, it is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three ADCCLK cycles.

The offset and gain values for the red, green and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register.

1-Channel CDS Mode

This mode operates in the same way as the 3-Channel CDS mode. The difference is that the multiplexer remains fixed in this mode, so only the channel specified in the MUX register is processed.

Timing for this mode is shown in Figure 3. Although not required, it is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK.

1-Channel SHA Mode

This mode operates in the same way as the 3-Channel SHA mode, except that the multiplexer remains stationary. Only the channel specified in the MUX register is processed.

The input signal is sampled with respect to the voltage applied to the OFFSET pin. With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero scale output. The OFFSET pin may also be used as a coarse offset adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the red, green and blue inputs in the first amplifier stage of the AD9814. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 4. CDSCLK1 should be grounded in this mode of operation. Although not required, it is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK.

INTERNAL REGISTER DESCRIPTIONS

Table I. Internal Register Map

Register Name	Address A2	A1	A0	Data Bits D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	Input Rng	VREF	3Ch/1Ch	CDS On	Clamp	Pwr Dn	0	0
MUX	0	0	1	0	RGB/BGR	Red	Green	Blue	0	0	0	0
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Configuration Register

The Configuration Register controls the AD9814's operating mode and bias levels. Bits D8, D1 and D0 should always be set low. Bit D7 sets the full-scale voltage range of the AD9814's A/D converter to either 4 V (high) or 2 V (low). Bit D6 controls the internal voltage reference. If the AD9814's internal voltage reference is used, this bit is set high. Setting Bit D6 low will disable the internal voltage reference, allowing an external voltage reference to be used. Bit D5 will configure the AD9814 for either the 3-Channel (high) or 1-Channel (low) mode of operation. Setting Bit D4 high will enable the CDS mode of operation, and setting this bit low will enable the SHA mode of operation. Bit D3 sets the dc bias level of the AD9814's input clamp. This bit should always be set high for the 4 V clamp bias, unless a CCD with a reset feedthrough transient exceeding 2 V is used. If the 3 V clamp bias level is used, the peak-to-peak input signal range to the AD9814 is reduced to 3 V maximum. Bit D2 controls the power-down mode. Setting Bit D2 high will place the AD9814 into a very low power "sleep" mode. All register contents are retained while the AD9814 is in the powered-down state.

Table II. Configuration Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Input Range	Internal VREF	# of Channels	CDS Operation	Input Clamp Bias	Power-Down	Set to 0	Set to 0
	1 = 4 V* 0 = 2 V	1 = Enabled* 0 = Disabled	1 = 3-Ch Mode* 0 = 1-Ch Mode	1 = CDS Mode* 0 = SHA Mode	1 = 4 V* 0 = 3 V	1 = On 0 = Off (Normal)*		

*Power-on default value.

MUX Register

The MUX Register controls the sampling channel order in the AD9814. Bits D8, D3, D2, D1, and D0 should always be set low. Bit D7 is used when operating in 3-Channel Mode. Setting Bit D7 high will sequence the MUX to sample the red channel first, then the green channel and then the blue channel. When in this mode, the CDSCLK2 pulse always resets the MUX to sample the red channel first (see Timing Figure 1). When Bit D7 is set low, the channel order is reversed to blue first, green second and red third. The CDSCLK2 pulse will always reset the MUX to sample the blue channel first. Bits D6, D5, and D4 are used when operating in 1-Channel Mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX will remain stationary during 1-Channel Mode.

Table III. MUX Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	3-Channel Select	1-Channel Select	1-Channel Select	1-Channel Select	Set to 0	Set to 0	Set to 0	Set to 0
	1 = R-G-B* 0 = B-G-R	1 = RED* 0 = Off	1 = GREEN 0 = Off*	1 = BLUE 0 = Off*				

*Power-on default value.

PGA Gain Registers

There are three PGA registers for individually programming the gain in the red, green and blue channels. Bits D8, D7 and D6 in each register must be set low, and bits D5 through D0 control the gain range in 64 increments. See Figure 13 for a graph of the PGA Gain versus PGA register code. The coding for the PGA registers is straight binary, with an all "zeros" word corresponding to the minimum gain setting (1x) and an all "ones" word corresponding to the maximum gain setting (5.8x).

Table IV. PGA Gain Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
					•				•	•
					•				•	•
					•				•	•
0	0	0	1	1	1	1	1	0	5.4	14.6
0	0	0	1	1	1	1	1	1	5.8	15.25

*Power-on default value.

Offset Registers

There are three PGA registers for individually programming the offset in the red, green and blue channels. Bits D8 through D0 control the offset range from –300 mV to +300 mV in 512 increments. The coding for the offset registers is sign magnitude, with D8 as the sign bit. Table V shows the offset range as a function of the Bits D8 through D0.

Table V. Offset Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	+1.2
					•				•
					•				•
					•				•
0	1	1	1	1	1	1	1	1	+300
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	–1.2
					•				•
					•				•
					•				•
1	1	1	1	1	1	1	1	1	–300

*Power-on default value.

CIRCUIT OPERATION

Analog Inputs—CDS Mode

Figure 8 shows the analog input configuration for the CDS mode of operation. Figure 9 shows the internal timing for the sampling switches. The CCD reference level is sampled when CDSCLK1 transitions from high to low, opening S1. The CCD data level is sampled when CDSCLK2 transitions from high to low, opening S2. S3 is then closed, generating a differential output voltage representing the difference between the two sampled levels.

The input clamp is controlled by CDSCLK1. When CDSCLK1 is high, S4 closes and the internal bias voltage is connected to the analog input. The bias voltage charges the external 0.1 µF input capacitor, level-shifting the CCD signal into the AD9814's input common-mode range. The time constant of the input clamp is determined by the internal 5 kΩ resistance and the external 0.1 µF input capacitance.

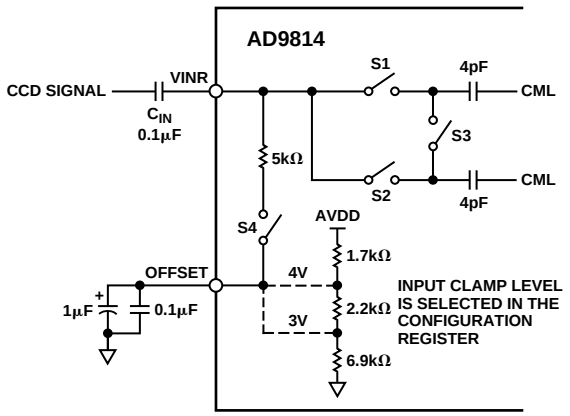


Figure 8. CDS-Mode Input Configuration (All Three Channels Are Identical)

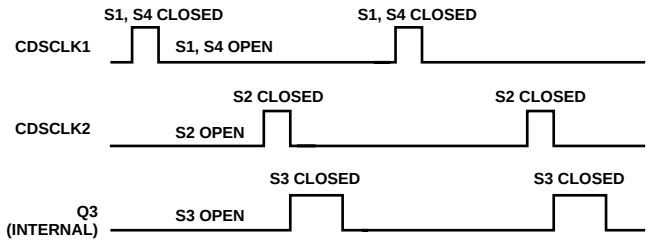


Figure 9. CDS-Mode Internal Switch Timing

External Input Coupling Capacitors

The recommended value for the input coupling capacitors is 0.1 µF. While it is possible to use a smaller capacitor, this larger value is chosen for several reasons:

1. **Signal Attenuation**. The input coupling capacitor creates a capacitive divider with a CMOS integrated circuit's input capacitance, attenuating the CCD signal level. C_{IN} should be large relative to the IC's 10 pF input capacitance in order to minimize this effect.
2. **Linearity**. Some of the input capacitance of a CMOS IC is junction capacitance, which varies nonlinearly with applied voltage. If the input coupling capacitor is too small, then the attenuation of the CCD signal will vary nonlinearly with signal level. This will degrade the system linearity performance.
3. **Sampling Errors**. The internal 4 pF sample capacitors have a "memory" of the previously sampled pixel. There is a charge redistribution error between C_{IN} and the internal sample capacitors for larger pixel-to-pixel voltage swings. As the value of C_{IN} is reduced, the resulting error in the sampled voltage will increase. With a C_{IN} value of 0.1 µF, the charge redistribution error will be less than 1 LSB for a full-scale pixel-to-pixel voltage swing.

Analog Inputs—SHA Mode

Figure 10 shows the analog input configuration for the SHA mode of operation. Figure 11 shows the internal timing for the sampling switches. The input signal is sampled when CDSCLK2 transitions from high to low, opening S1. The voltage on the OFFSET pin is also sampled on the falling edge of CDSCLK2, when S2 opens. S3 is then closed, generating a differential output voltage representing the difference between the sampled input voltage and the OFFSET voltage. The input clamp is disabled during SHA mode operation.

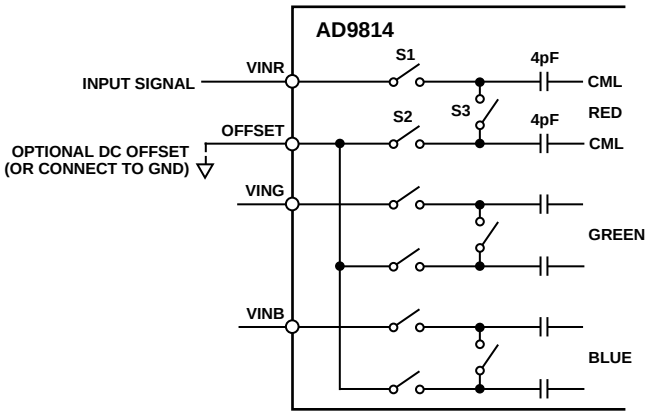


Figure 10. SHA-Mode Input Configuration (All Three Channels Are Identical)

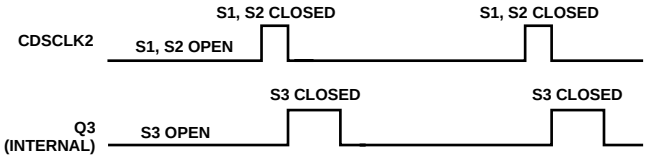


Figure 11. SHA-Mode Internal Switch Timing

Figure 12 shows how the OFFSET pin may be used in a CIS application for coarse offset adjustment. Many CIS signals have dc offsets ranging from several hundred millivolts to more than 1 V. By connecting the appropriate dc voltage to the OFFSET pin, the CIS signal will be restored to "zero." After the large dc offset is removed, the signal can be scaled using the PGA to maximize the ADC's dynamic range.

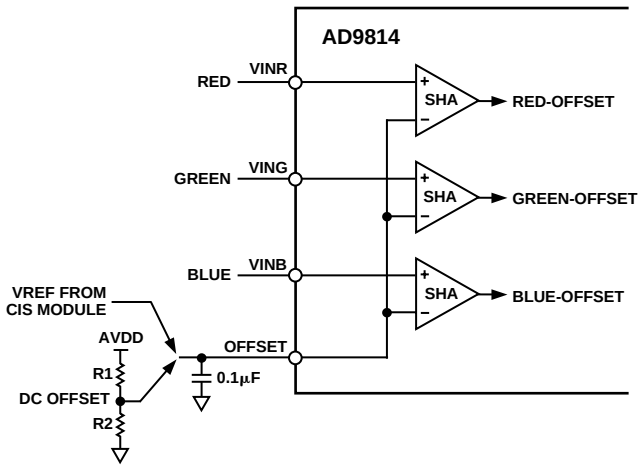


Figure 12. SHA-Mode Used with External DC Offset

Programmable Gain Amplifiers

The AD9814 uses one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1x (0 dB) to 5.8x (15.5 dB), adjustable in 64 steps. Figure 6 shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately "linear in dB", the gain in V/V varies nonlinearly with register code, following the equation:

$$Gain = \frac{5.8}{1 + 4.8\left[\frac{63 - G}{63}\right]}$$

where G is the decimal value of the gain register contents, and varies from 0 to 63.

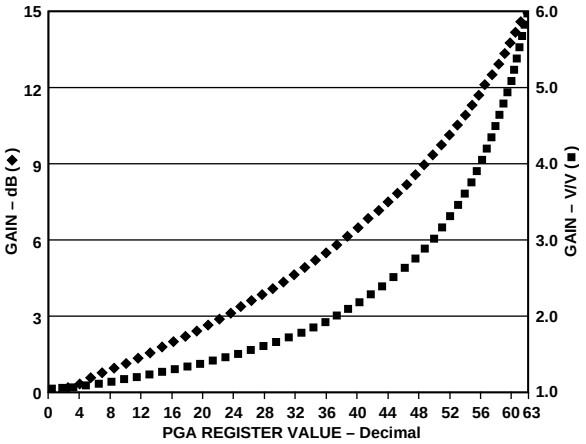


Figure 13. PGA Gain Transfer Function

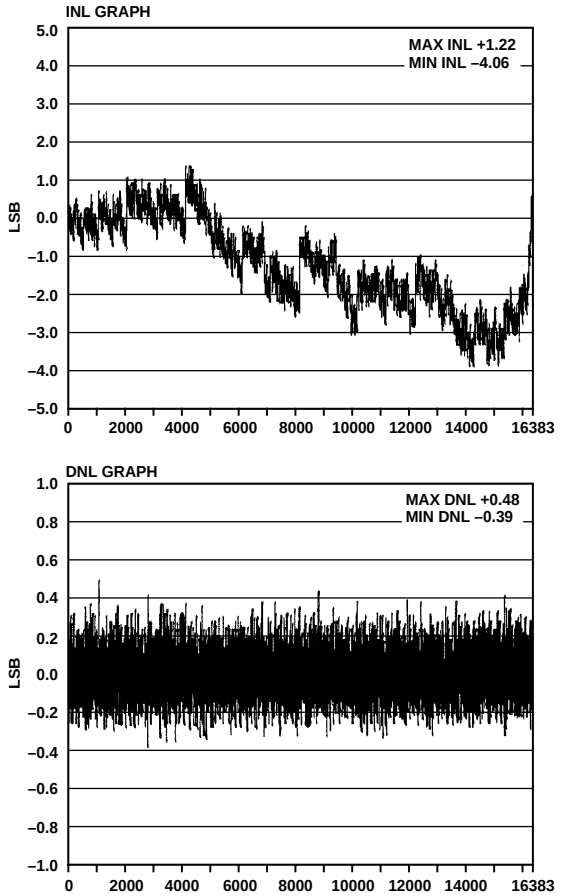


Figure 14. Typical Linearity Performance

APPLICATIONS INFORMATION

Circuit and Layout Recommendations

The recommended circuit configuration for 3-Channel CDS mode operation is shown in Figure 15. The recommended input coupling capacitor value is 0.1 µF (see Circuit Operation section for more details). A single ground plane is recommended for the AD9814. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the AD9814. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK (see Figures 1 through 4 for timing). All 0.1 µF decoupling capacitors should be located as close as possible to the AD9814 pins. When operating in single channel mode, the unused analog inputs should be grounded.

Figure 16 shows the recommended circuit configuration for 3-Channel SHA mode. All of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the AD9814 without the use of coupling capacitors. The analog input signals must already be dc-biased between 0 V and 4 V (see the Circuit Operation section for more details).

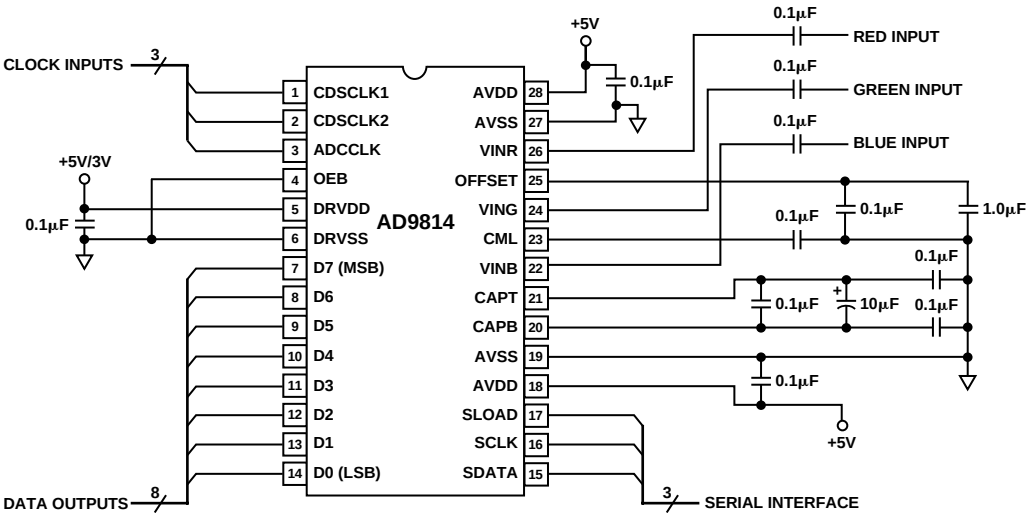


Figure 15. Recommended Circuit Configuration, 3-Channel CDS Mode

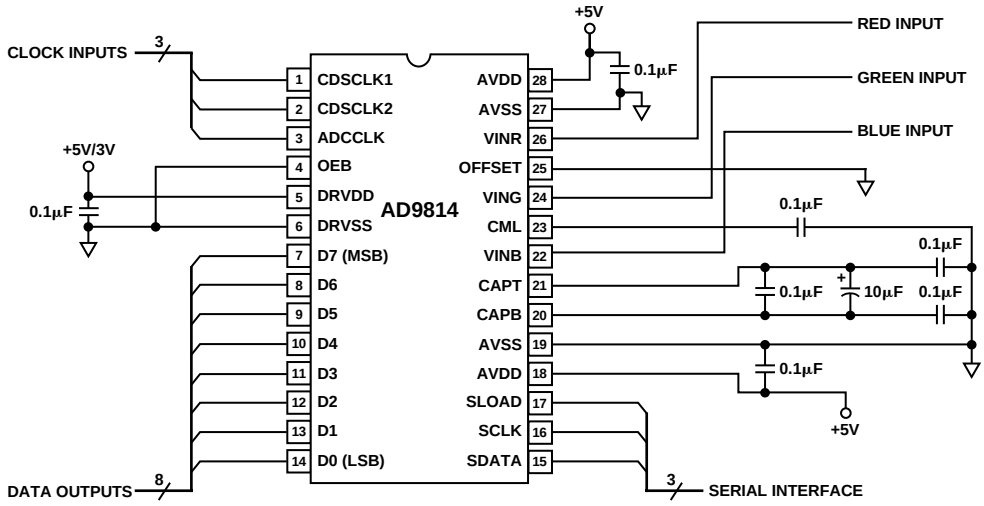
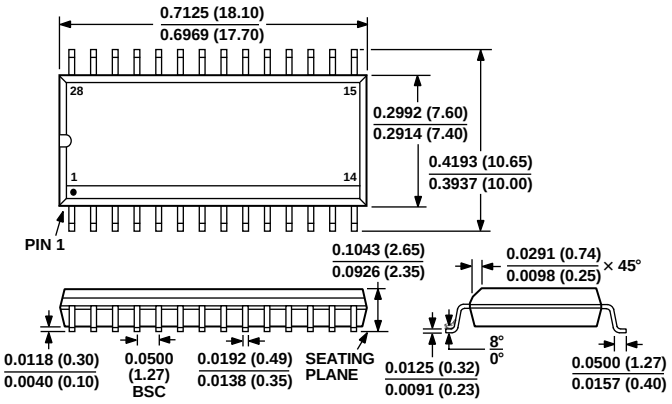


Figure 16. Recommended Circuit Configuration, 3-Channel SHA Mode (Analog Inputs Sampled with Respect to Ground)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead, 300 Mil SOIC (R-28)



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