

## GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W



RoHS Compliant



### Applications

- 48V<sub>DC</sub> distributed power architectures
- Routers/ VoIP/Soft and other Telecom Switches
- LAN/WAN/MAN applications
- File servers, Enterprise Networks, Indoor wireless
- SAN/NAS/iSCSI applications
- Semiconductor Manufacturing

### Features

- Efficiency 96.5% typical, exceeds 80plus Titanium levels
- Compact 1RU form factor with 30 W/in<sup>3</sup> density
- Constant power from 48 – 58V<sub>DC</sub>
- 6000W from nominal 3 $\Phi$ -380/480V<sub>AC</sub>
- Output voltage programmable from 42V – 58V<sub>DC</sub>
- PMBus compliant dual, redundant I<sup>2</sup>C serial bus
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- SEMI-F47 Tested and Compliant at 480V<sub>AC</sub>
- Output overvoltage and overload protection
- AC Input overvoltage and undervoltage protection
- Over-temperature warning and protection
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 2A Aux power
- Remote ON/OFF
- Internally controlled Variable-speed fan
- Hot insertion/removal (hot plug)
- Three front panel LED indicators
- EN/IEC/UL/CSA C22.2 60950-1 2<sup>nd</sup> edition +A1
- CE mark§
- Meets FCC part 15, EN55022 Class A standards
- Meets EN61000 immunity and transient standards
- Shock & vibration: Meets IPC 9592 Class II standards

### Description

The GP100 series of rectifiers provide significant efficiency improvements in the Global Platform of Power supplies. High-density front-to-back airflow is designed for minimal space utilization and is highly expandable for future growth. The 3 $\Phi$  - 380/480Vrms input product is designed to be deployed internationally. It is configured with dual-redundant PMBus™ compliant I<sup>2</sup>C communications busses that allow it to be used in a broad range of applications. Feature set flexibility makes these rectifiers an excellent choice for applications requiring modular, very-high-efficiency AC to - 48V<sub>DC</sub> intermediate voltages, such as in distributed power.

\* UL is a registered trademark of Underwriters Laboratories, Inc.  
 † CSA is a registered trademark of Canadian Standards Association.

‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.

§ This product is intended for integration into end-user equipment. All CE marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)

\*\* ISO is a registered trademark of the International Organization of Standards

\* The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)



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## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	V <sub>IN</sub>	0	600	V <sub>AC</sub>
Operating Ambient Temperature <sup>1</sup>	T <sub>A</sub>	-10	75	°C
Storage Temperature	T <sub>stg</sub>	-40	85	°C
I/O Isolation voltage to Frame (100% factory Hi-Pot tested)			2087	V <sub>AC</sub>

## Electrical Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, V<sub>o</sub>=54V<sub>DC</sub>, resistive load, and temperature conditions. To meet measurement accuracy a warm up time of 1hr may be required.

INPUT					
Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range (3Φ delta with safety frame ground)	V <sub>IN</sub>	320	380/480	530	V <sub>AC</sub>
Low voltage	Turn-OFF	(300)		320	
	Turn-ON	(315)		330	
	Hysteresis	5			
High voltage	Turn-OFF	530		(550)	
	Turn-ON	520		(540)	
	Hysteresis	5			
Input voltage phase unbalance	V <sub>IN</sub>	-15		10	%
Frequency	F <sub>IN</sub>	47		63	Hz
Operating Current (3Φ - all phases operational)	I <sub>IN</sub>			15	A <sub>AC</sub>
Input current phase unbalance [load > 50% of FL]				1	%
Inrush Transient (per Φ at 480V <sub>RMS</sub> , 25°C, excluding X-Capacitor charging)	I <sub>IN</sub>		25	30	A <sub>PK</sub>
Source Impedance (NEC allows 2.5% of source voltage drop inside a building)		0.20	0.25		Ω
Idle Power (at 480V <sub>AC</sub> , 25°C)	Main output OFF		15		W
	Main output ON @ I <sub>o</sub> =0		25		
Leakage Current (per Φ, 530V <sub>AC</sub> , 60Hz)	I <sub>IN</sub>		2.5	3.5	mA
Power Factor (50 – 100% load)	PF	0.96	0.995		
Efficiency (380/480V <sub>AC</sub> @ 25°C)	10% load 20% load 50% load 100% load		90/91 93/94 96/96.5 95/96		%
Holdup time (V <sub>IN</sub> = 320V <sub>RMS</sub> , V <sub>OUT</sub> ≥ 42V <sub>DC</sub> , constant power load)	T	10	12		ms
Ride through (at 480V <sub>AC</sub> , 25°C, constant power load)	T	1/2	1		cycle
Power Fail Warning <sup>2</sup> (V <sub>OUT</sub> ≥ 42V <sub>DC</sub> , P <sub>OUT</sub> = constant power)	PFW	5	8	12	ms
Isolation (per EN60950)	Input – Output	3000			V <sub>AC</sub>
	Input-Chassis/Signals	2000			V <sub>AC</sub>

<sup>1</sup> See the derating guidelines under the Environmental Specifications section

<sup>2</sup> Internal protection circuits may override the PFW signal and may trigger an immediate shutdown.

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3Φ-380/480V<sub>AC</sub> Input; Default Outputs: ±54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

## Electrical Specifications (continued)

54/52/48V <sub>DC</sub> MAIN OUTPUT					
Parameter	Symbol	Min	Typ	Max	Unit
Output Power ( 320 – 530V <sub>AC</sub> – 3Φ, T <sub>AMB</sub> = 0 – 45°C )	W	6000			W <sub>DC</sub>
Factory set default set point V <sub>IN</sub> = 480V, I = 10% FL, 25°C I <sup>2</sup> C/RS485	V <sub>OUT</sub>	-50	54/52/48	450	V <sub>DC</sub>
Nominal set point (droop regulation; max-no load, min-full load)					mV <sub>DC</sub>
Overall regulation (load, temperature, aging) 0 – 45°C LOAD > 2.5A		-0.5		+0.5	%
T <sub>AMB</sub> > 45°C		-2		+2	%
Output Voltage Set Range		42	0.012	58	V <sub>DC</sub>
Programmable voltage resolution					V <sub>DC</sub>
Programmed voltage retention		30			days
Output Current ( 54 /, T <sub>AMB</sub> = 45°C )	I <sub>OUT</sub>	1		111	A <sub>DC</sub>
V <sub>OUT</sub> = 54V <sub>DC</sub>		1		115	
V <sub>OUT</sub> = 52V <sub>DC</sub>		1		125	
V <sub>OUT</sub> = 48V <sub>DC</sub>					
Current Share ( > 50% FL) active current share		-5		5	%FL
remotely controlled I <sub>SHARE</sub> is employed		-2		2	%FL
Max units parallelable active current share/ remotely controlled				20/100	units
Proportional Current Share between different power supplies ( > 50% FL)			<7		%FL
Output Ripple RMS (5Hz to 20MHz)	V <sub>OUT</sub>			100	mV <sub>rms</sub>
( 20MHz bandwidth, load > 10%FL) Peak-to-Peak (5Hz to 20MHz)				250	mV <sub>p-p</sub>
Load < 10%FL				400	mV <sub>p-p</sub>
Voice Band Output Noise	V <sub>OUT</sub>	With 880Ahr battery in system		45	dBrnC
		Without battery		55	
		Psophometric Noise			2 <sup>3</sup>
External Bulk Load Capacitance	C <sub>OUT</sub>	0		1,700	μF/A
Turn-On ( <b>monotonic turn-ON</b> from 30 – 100% of V <sub>nom</sub> , above -5°C <sup>4</sup> )	T				
Delay			5		s
Rise Time – PMBus or Analog mode			100		ms
Rise Time – RS-485 mode		2.5			s
		5			
	8				
55A (50% load )					
83A (75% load)					
100A (90% load)					
Output Overshoot	V <sub>OUT</sub>			2	%
Load Step Response	I <sub>OUT</sub>				
ΔI [V <sub>IN</sub> = 380/480V <sub>AC</sub> , 25°C, load step 20% ↔ 80%, di/dt = 1A/μs ]				60	%FL
ΔV, ( 380/480 V <sub>AC</sub> , 25°C)		-5		5	%
Settling Time to normal regulation	T			2	ms
Overload <sup>5</sup> - Power limit when V <sub>OUT</sub> ≥ 48V <sub>DC</sub>	P <sub>OUT</sub>	6050			W <sub>DC</sub>
recoverable current limit when 40V <sub>DC</sub> < V <sub>OUT</sub> < 48V <sub>DC</sub>	I <sub>OUT</sub>	110		120	%FL
Output shutdown (one retry after a 2 – 10 second delay)	V <sub>OUT</sub>			36	V <sub>DC</sub>
Short circuit protection	No damage				
System power up	Upon startup, delay overload shutdown for 20 seconds to allow the insertion and startup of multiple modules within a system.				
Overvoltage	V <sub>OUT</sub>	59	59.5	60	V <sub>DC</sub>
		> 65			
		44		59.5	
	Latched shutdown If 3 restart attempted within a 30 sec window unit latches OFF				
Restart delay		3.5	4	5	sec
Over-temperature warning (prior to commencement of shutdown)	T		5		°C
Shutdown (below the max device rating being protected)			20		
Restart attempt Hysteresis (below shutdown level)			10		
Isolation Output-Chassis	V	500			V <sub>DC</sub>
Restart/Reset conditions	Loss of input > 100ms or Output OFF followed by ON command				

<sup>3</sup> Complies with ANSI TI.523-2001 section 4.9.2 emissions max limit of 20mV flat unweighted wideband noise limits<sup>4</sup> Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.<sup>5</sup> Overload retries must incorporate normal soft-start turn-ON.

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5V <sub>DC</sub> Auxiliary output					
Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint	V <sub>OUT</sub>		5		V <sub>DC</sub>
Overall Regulation		-5		+5	%
Output Current		0		2	A
Ripple and Noise (20mHz bandwidth)			50	100	mV <sub>p-p</sub>
Over-voltage Clamp				7	V <sub>DC</sub>
Over-current Limit		110		230	%FL

## General Specifications

Parameter	Min	Typ	Max	Units	Notes
Reliability Calculated		560,000 190,000		Hours	Full load, 25°C; Full load, 55°C; - MTBF per Telecordia SR232 Reliability protection for electronic equipment, issue 3, method I, case III,
Service Life		10		Years	80% load, 35°C ambient, excluding fans
Unpacked Weight		4.3/9.5		kg/lb	
Packed Weight		4.9/10.8		kg/lb	
Heat Dissipation	200 Watts or 682 BTUs @ 80% load, 250 Watts or 853 BTUs @ 100% load				

## Signal Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. Signals are referenced to Logic\_GRD unless noted otherwise.. See the Signal Definitions table for additional information.

Parameter	Symbol	Min	Typ	Max	Unit
<b>Remote ON/OFF</b> (should be connected to Logic_GRD) 54V output OFF	V <sub>OUT</sub>	2.5	—	12	V <sub>DC</sub>
54V output ON	V <sub>OUT</sub>	0	—	0.8	V <sub>DC</sub>
<b>Vprog Margining</b>		44		58	V <sub>DC</sub>
Voltage control range	V <sub>control</sub>	0		5	V <sub>DC</sub>
Programmed output voltage range	V <sub>OUT</sub>	44		58	V <sub>DC</sub>
Voltage adjustment resolution (8-bit A/D)	V <sub>control</sub>		3.3		mV <sub>DC</sub>
Output configured to 54V <sub>DC</sub>	V <sub>control</sub>	3.0		3.3	V <sub>DC</sub>
Output configured to 44V <sub>DC</sub>	V <sub>control</sub>	0		0.1	V <sub>DC</sub>
<b>Interlock</b> [Connected externally to Vout ( - )]	V	—		0.4	V <sub>DC</sub>
<b>Module Present</b> [Internally shorted to Logic_GRD]					
Normal operation	V	—		0.4	V <sub>DC</sub>
<b>Fault</b> (pulled up internally to V <sub>stdby</sub> by a 10k $\Omega$ resistor)					
Logic HI (No fault is present)	V	0.7 V <sub>stdby</sub>	—	V <sub>stdby</sub>	V <sub>DC</sub>
Sink current	I	—	—	5	mA
Logic LO (Fault is present)	V	0	—	0.4	V <sub>DC</sub>
<b>SMBAlert#</b> (pulled up internally to V <sub>stdby</sub> by a 10k $\Omega$ resistor)					
Logic HI (No Alert – normal)	V	0.7V <sub>stdby</sub>	—	V <sub>stdby</sub>	V <sub>DC</sub>
Logic LO (Alert is set)	V	0	—	0.4	V <sub>DC</sub>
<b>8V_INT</b> (no components should be connected to this pin) Interconnected between power supplies to back-bias the internal secondary processor					

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3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52V_{DC}$  @ 6000W, 5V<sub>DC</sub> @ 10W

## Feature Specifications (continued)

## Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>PMBus Signal Interface Characteristics<sup>6</sup></b>						
Input Logic High Voltage (CLK, DATA)		V	1.5		3.6	V <sub>DC</sub>
Input Logic Low Voltage (CLK, DATA)		V	0		0.8	V <sub>DC</sub>
Input high sourced current (CLK, DATA)		I	0		10	$\mu$ A
Output Low sink Voltage (CLK, DATA, SMBALERT#)	I <sub>OUT</sub> =3.5mA	V			0.4	V <sub>DC</sub>
Output Low sink current (CLK, DATA, SMBALERT#)		I	3.5			mA
Output High open drain leakage current (CLK, DATA, SMBALERT#)	V <sub>OUT</sub> =3.6V	I	0		10	$\mu$ A
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz
<b>Measurement System Characteristics</b>						
Clock stretching		T <sub>stretch</sub>			25	ms
Standard measurement parameters	Update frequency				1	Hz
	Report delay after 25% step				2	sec
	Report delay to accuracy				10	sec
I <sub>OUT</sub> measurement range	Linear	I <sub>MR</sub>	0		130	A <sub>DC</sub>
I <sub>OUT</sub> measurement accuracy 25°C	> 25A	I <sub>OUT(ACC)</sub>	-1		+1	% of FL
	< 25A		2.5		2.5	A <sub>DC</sub>
V <sub>OUT</sub> measurement range	Linear	V <sub>OUT(rMR)</sub>	0		70	V <sub>DC</sub>
V <sub>OUT</sub> measurement accuracy <sup>7</sup>		V <sub>OUT(ACC)</sub>	-1		+1	%
P <sub>OUT</sub> measurement range	Linear	P <sub>OUT(rMR)</sub>	0		6100	W <sub>DC</sub>
P <sub>OUT</sub> measurement accuracy	30°C	P <sub>OUT(ACC)</sub>	-30		30	W <sub>DC</sub>
	-5°C – 55°C		TBD		TBD	
Temp measurement range	Linear	Temp <sub>(rMG)</sub>	0		150	°C
Temp measurement accuracy <sup>8</sup>		Temp <sub>(ACC)</sub>	-5		+5	%
V <sub>IN</sub> measurement range, each phase	Linear	V <sub>IN(rMG)</sub>	0		600	V <sub>AC</sub>
V <sub>IN</sub> measurement accuracy		V <sub>IN(ACC)</sub>	-1.5		+1.5	%
I <sub>IN</sub> measurement range, each phase	Linear	I <sub>IN(MR)</sub>	0		20	A <sub>DC</sub>
I <sub>IN</sub> measurement accuracy		I <sub>IN(ACC)</sub>	-5		5	% of FL
P <sub>IN</sub> measurement range, computed 3 $\Phi$ result	Linear	P <sub>IN(rng)</sub>	0		6750	W <sub>in</sub>
P <sub>IN</sub> measurement accuracy	10-100% Load	P <sub>IN(ACC)</sub>	-150		150	W
F <sub>IN</sub> measurement range	Linear	F <sub>IN(MR)</sub>	45		65	Hz
F <sub>IN</sub> measurement accuracy		F <sub>IN(ACC)</sub>				
Fan Speed measurement range	Linear		0		30k	RPM
Fan Speed measurement accuracy			-10		10	%
Fan speed control – duty cycle	Direct		0		100	%

<sup>6</sup> Clock, Data, and SMBAlert need to be pulled up to V<sub>DD</sub> externally.<sup>7</sup> Above 2.5A of load current<sup>8</sup> Temperature accuracy reduces non-linearly with decreasing temperature

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3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

## Environmental Specifications

Parameter		Min	Typ	Max	Units	Notes
Ambient Temperature		-5 <sup>9</sup>		55	°C	Air inlet from sea level to 5,000 feet.
Storage Temperature		-40		85	°C	
Operating Altitude				1524/5000	m / ft	
Non-operating Altitude				8200/30k	m / ft	
Power Derating with Temperature				2.0	%/°C	55°C to 75°C <sup>10</sup>
Power Derating with Altitude				2.0	°C/305 m °C/1000 ft	Above 1524/5000 m/ft; 3962/13000 m/ft max
Humidity	Operating Storage	5 5		95 95	% %	Relative humidity, non-condensing
Shock and Vibration	Operational	Meets IPC 9592 Class II, Section 5 and GR-63_CORE requirements				
	Packaged	0.02	0.01	0.02	g <sup>2</sup> /Hz	Modified IASTM-D-4728-91 8 hour duration on each axis
Acoustic Noise			55	58	dBA	
Earthquake Rating		4			Zone	Meet GR-63_CORE requirements

## EMC [Surges and sags applied one $\Phi$ at a time and all 3 $\Phi$ 's simultaneously; phase angles 0, 90, 270°]

Parameter	Function	Standard	Level	Criteria	Test
AC input	Conducted emissions	EN55022, FCC part 15 EN61000-3-2, Telcordia GR1089-CORE	A – 6dB margin		0.15 – 30MHz 0 – 2 KHz
	Radiated emissions	EN55022	A – 6dB margin		30 – 10000MHz
AC Input Immunity	Line surge		3 x V <sub>NOM</sub> 480V	B	1 $\Phi$ only or all 3 $\Phi$
	Line sags and interruptions	EN61000-4-11  Output will stay above 40V <sub>DC</sub> @ full load  Sag must be higher than 80Vrms.		A	-30%, 10ms
				B	-60%, 100ms
				B	-100%, 5sec
				A	25% sag for 2 sec
				A	1 cycle interruption
		SEMI-F47 Compliant at 480Vac Output will Stay at Full Power	50% Sag	Any Phase	10 cycles @ 50Hz 12 cycles @ 60Hz
			70% Sag		25 cycles @ 50Hz 30 cycles @ 60Hz
			80% Sag		50 cycles @ 50Hz 60 cycles @ 60Hz
	Lightning surge	EN61000-4-5, Level 4, 1.2/50 $\mu$ s – error free		A	4kV, comm
				A	2kV, diff
		ANSI C62.41-2002 100kHz ring wave 1.2/50 $\mu$ s-8/20 $\mu$ s 550ns EFT burst	3, Category B 3, Category B	B, Table 2 B, Table 3 B, Table 7	6kV/0.5kA 6kV, 3kA 2kV, severity II
	Fast transients	EN61000-4-4	3	A	5/50ns, 2kV (common mode)
Enclosure immunity	Conducted RF fields	EN61000-4-6	3	A	130dB $\mu$ V, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3	3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140		A	
	ESD	EN61000-4-2	4	A	8kV contact, 15kV air

Criteria	Performance
A	No performance degradation
B	Temporary loss of function or degradation not requiring manual intervention
C	Temporary loss of function or degradation that may require manual intervention
D	Loss of function with possible permanent damage

<sup>9</sup> Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -5°C

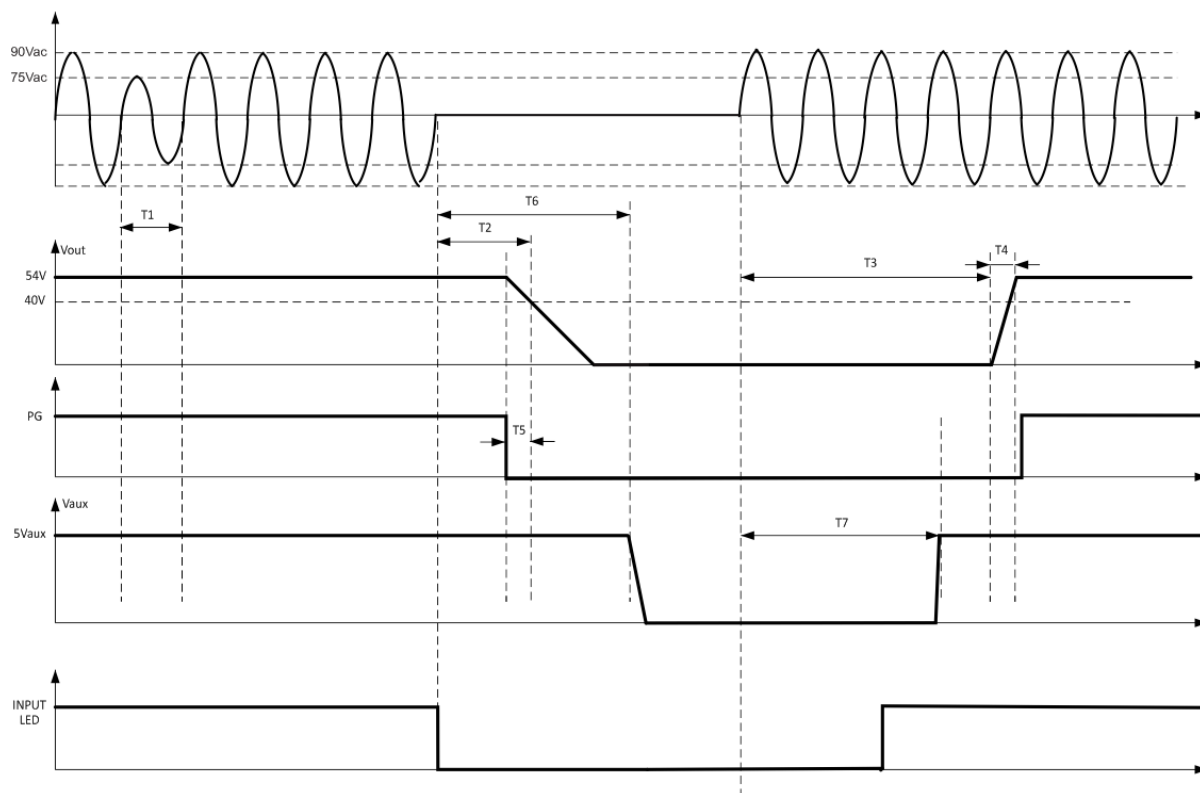
<sup>10</sup> The maximum operational ambient is reduced in Europe in order to meet certain power cord maximum ratings of 70°C. The maximum operational ambient where 70°C rated power cords are utilized is reduced to 60°C until testing demonstrates that a higher level is acceptable. At high input voltage (530V<sub>AC</sub>), the maximum temperature rating is reduced to 70°C.

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### Timing diagrams

#### Response to input fluctuations



T1 – ride through time – 0.5 to 1 cycles [ 10 – 20ms]  $V_{OUT}$  remains within regulation – load dependent

T2 – hold up time - 15ms –  $V_{OUT}$  stays above 40V<sub>DC</sub>

T3 – delay time – 10s – from when the AC returns within regulation to when the output starts rising in I<sup>2</sup>C mode

T4 – rise time - 120ms – the time it takes for  $V_{OUT}$  to rise from 10% to 90% of regulation in I<sup>2</sup>C mode

T5 – power good warning – 3ms – the time between assertion of the PG signal and the output decaying below 40V<sub>DC</sub>.

T6 – hold up time of the 5VAUX output @ full load – 1s – from the time AC input failed

T7 – rise time of the 5VAUX output - 3.65ms – 5VAUX is available at least 450ms before the main output is within regulation

Blinking of the input/AC LED –  $V_{IN} < 80V_{AC}$  (the low transitioned signal represents blinking of the input LED).

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3 $\Phi$ -380/480V<sub>AC</sub> input; Default Outputs:  $\pm 54$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

## Control and Status

The Rectifier provides three means for monitor/control: analog, PMBus™, or the GE Galaxy-based RS485 protocol.

Details of analog control and the PMBus™ based protocol are provided in this data sheet. GE will provide separate application notes on the Galaxy RS485 based protocol for users to interface to the rectifier. Contact your local GE representative for details.

**Control hierarchy:** Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (V<sub>prog</sub>) and a PMBus command, (OPERATION) .

Using output voltage as an example; the V<sub>prog</sub> signal pin has ultimate control of the output voltage until the V<sub>prog</sub> is either > 3V<sub>DC</sub> or a no connect. When the programming signal via V<sub>prog</sub> is either a no connect or > 3V<sub>DC</sub>, it is ignored, the output voltage is set at its nominal 54V<sub>DC</sub>.

Unless otherwise noted, the V<sub>prog</sub> signal pin controls the output voltage set point (if it is connected) until a firmware command is executed. Once a firmware command to change the output voltage has been executed, the signal pin is ignored. [ In the above example, the rectifier will no longer 'listen' to the V<sub>prog</sub> pin if the OPERATION command has been executed.]

In summary, V<sub>prog</sub> is utilized for initialized configuration of the output voltage and to change the output voltage when PMBus is not used for that function.

**Analog controls:** Details of analog controls are provided in this data sheet under Feature Specifications.

**Signal Reference:** Unless otherwise noted, all signals, the standby output, and I<sup>2</sup>C communications are referenced to Logic\_GRD. See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic\_GRD is capacitively coupled to Frame\_GRD inside the rectifier. The maximum voltage differential between Logic\_GRD and Frame\_GRD should be less than 100V<sub>DC</sub>. It is assumed that the end user will connect Logic\_GRD to his digital ground reference in his system.

Logic\_GRD is isolated from the main output of the rectifier.

(Note that RS485 communications is referenced to Vout(-), main power return of the rectifier).

## Control Signals

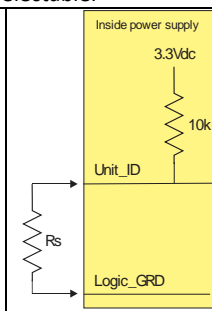
**Protocol:** This signal pin defines the communications mode setting of the rectifier. Two different states can be configured. State #1 is the I<sup>2</sup>C application in which case the protocol pin should be left a no-connect. State #2 is the RS485 mode application in which case a resistor value between 1k $\Omega$  and 5k $\Omega$  should be present between this pin and Vout ( - ).

**Device address in I<sup>2</sup>C mode:** Address bits A3, A2, A1, A0 set the specific address of the  $\mu$ P in the rectifier. With these four bits, up to sixteen (16) rectifiers can be independently addressed on a single I<sup>2</sup>C bus. These four bits are configured by two signal pins, Unit\_ID and Rack\_ID. The least significant bit x (LSB) of the address byte is set to either **write [0]** or **read [1]**. A **write** command instructs the rectifier. A **read** command accesses information from the rectifier.

Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
$\mu$ P	40 – 4F	1	0	0	A3	A2	A1	A0	R/W
Broadcast	00	0	0	0	0	0	0	0	0
ARA <sup>11</sup>	C	0	0	0	1	1	0	0	1
		MSB <span style="float:right">LSB</span>							

**Unit\_ID:** Up to 10 different units are selectable.

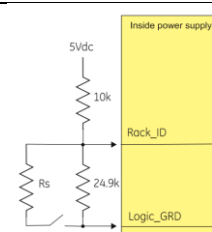
A voltage divider between 3.3V and Logic\_GRD configures Unit\_ID. Internally a 10k $\Omega$  resistor is pulled up to 3.3VDC. A pull down resistor R<sub>s</sub> needs to be connected between pin Unit\_ID and Logic\_GRD.



Unit_ID	Voltage level	R <sub>s</sub> ( $\pm 0.1\%$ )
Invalid	3.30	
1	3.00	100k
2	2.67	45.3k
3	2.34	24.9k
4	2.01	15.4k
5	1.68	10.5k
6	1.35	7.15k
7	1.02	4.99k
8	0.69	2.49k
9	0.36	1.27k
10	0	0

**Rack\_ID:** Up to 8 different combinations are selectable.

A voltage divider between 5V<sub>DC</sub> and Logic\_GRD configures Rack\_ID. A switch between each R<sub>s</sub> value changes the Rack\_ID level according to the table below.



<sup>11</sup> Implement if feasible, this is a 'read' only address



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3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52V_{DC}$  @ 6000W, 5V<sub>DC</sub> @ 10W

Rack_ID	Voltage level <sup>12</sup>	5% tolerance	
1	3.31	3.15	3.48
2	1.07	1.02	1.13
3	1.89	1.80	1.99
4	0.58	0.55	0.60
5	1.66	1.57	1.74
6	0.84	0.80	0.88
7	1.42	1.35	1.49
8	2.86	2.71	3.00

**Configuration of the A3 – A0 bits:** The rectifier will determine the configured address based on the Unit\_ID and Rack\_ID voltage levels as follows (the order is A3 – A0):

		Unit_ID				
		1	2	3	4	5
Rack_ID	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
	4	1100	1101	1110	1111	
	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

Unit x Shelf: 4 x 4 and 5 x 3

		Unit_ID				
		6	7	8	9	10
Rack_ID	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
	4	0110	0111	0000	0001	0010
	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

Unit x Shelf: 2 x 8 and 3 x 5

**Address detection:** The Slot\_ID pin must be shorted to Vout(-) in order to deliver output power. This connection provides a second interlock feature. (In RS485 mode the slot\_ID resistance to Vout(-) is sufficient to sense the interlock feature)

**Bay\_ID:** The Unit\_ID definition in I<sup>2</sup>C mode becomes the bay id in RS485 mode.

**Slot\_ID:** Up to 10 different modules could be positioned across a 19" shelf if the modules are located vertically within the shelf. The resistor below needs to be placed between Slot\_ID and Vout (-). Internal pull-up to 3.3V is 10k $\Omega$ .

Slot	Resistor	Voltage	Slot	Resistor	Voltage
invalid	none	3.3V	6	7.15k	1.35V
1	100k	3V	7	4.99k	1.02V
2	45.3k	2.67V	8	2.49k	0.69V
3	24.9k	2.34V	9	1.27k	0.36V
4	15.4k	2.01V	10	0	0
5	10.5k	1.68V			

**Shelf\_ID:** When placed horizontally up to 20 shelves can be stacked on top of each other in a fully configured rack. The shelf will generate the precision voltage level tabulated below referenced to Vout (-).

Shelf	V <sub>MIN</sub>	V <sub>NOM</sub>	V <sub>MAX</sub>
Fault	0	0	0
1	1.21	1.23	1.24
2	2.42	2.45	2.48
3	3.63	3.68	3.72
4	4.84	4.90	4.96
5	6.06	6.13	6.20
6	7.27	7.35	7.43
7	8.48	8.58	8.67
8	9.69	9.80	9.91
9	10.90	11.03	11.15
10	12.11	12.25	12.39
11	13.32	13.48	13.63
12	14.53	14.70	14.87
13	15.74	15.93	16.11
14	16.95	17.15	17.35
15	18.17	18.38	18.59
16	19.38	19.60	19.82
17	20.59	20.83	21.06
18	21.80	22.05	22.30
19	23.01	23.28	23.54
20	24.22	24.50	24.78

**Global Broadcast:** This is a powerful command because it instruct all power supplies to respond simultaneously. A **read** instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled power supplies change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all power supplies simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth *acknowledge* bit. To be certain that each rectifier responded to the global instruction, a **READ** instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

<sup>12</sup> Accuracy  $\pm 5\%$  (+5V accuracy  $\pm 4\%$ )

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3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**Alert Response Address (ARA):** This feature enables the 'master' to rapidly determine which 'slave' rectifier triggered the SMBAlert signal without having to poll each rectifier one at a time. During normal operation the rectifier activates (pulls down LO) the Alert signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the alert-response-address, address 12b, with a 'read' instruction. If the rectifier triggered the 'alert' it should respond back with its address. The instruction takes the form below;

1	8		1	8	1	8	1	1
S	ARA address	Rd	A	My address	A	PEC	A	P

If during the ARA response multiple power supplies send out their addresses, then the actual address received by the master is the lowest address from the combinations of those power supplies that responded.

The 'my address' field contains the address of the rectifier in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification

The  $\mu$ C needs to read the actual **my address** data byte that is sent back to the master. If the **my address** data byte agrees with the address of this unit, then, and only then, the  $\mu$ C needs to clear (de-assert) its Alert# signal. Thus, the rectifier whose address has been sent out gets de-asserted from the joint Alert# line.

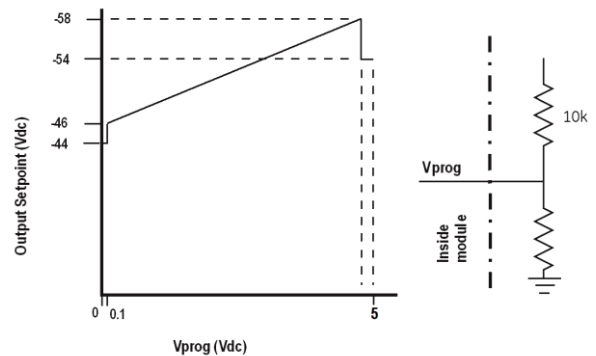
If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all rectifiers that asserted Alert# have had their status states read back.

**Voltage programming ( $V_{prog}$ ):** Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Software voltage programming permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

When bias power is recycled to the controller the controller restarts into its default configuration, programmed to set the output as instructed by the  $V_{prog}$  pin. Again, subsequent software commanded settings permanently override the margin setting. As an example, adding a resistor between  $V_{prog}$  and Logic\_GRD is an effective way of changing the factory set point of the rectifier to whatever voltage level is desired by the user during initial start-up.

The  $V_{prog}$  pin level should be set by a divider from 3.3Vdc to Logic\_GRD external to the rectifier as shown in the graph. Programming can be accomplished either by a resistor divider or by a voltage source injecting a precision voltage level into the  $V_{prog}$  pin. Above 3Vdc the rectifier sets the output to its default state. If  $V_{prog}$  feature is not used, this signal should be pulled up to the 5VA output with a 10k resistor.

An analog voltage on this signal can vary the output voltage from 44Vdc to 58Vdc.



Factory default setting driven by  $V_{prog}$

**Load share ( $I_{share}$ ):** This is a single wire analog signal that is generated and acted upon automatically by power supplies connected in parallel.  $I_{share}$  pins should be connected to each other for power supplies, if active current share among the power supplies is desired. No resistors or capacitors should get connected to this pin.

**ON/OFF:** Controls the main 54V<sub>DC</sub> output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn **ON** the rectifier. The rectifier will turn **OFF** if either the **ON/OFF** or the **Interlock** pin is released. This signal is referenced to Logic\_GRD. Note that in RS485 mode this pin is ignored.

**Interlock:** This is a shorter pin utilized for hot-plug applications to ensure that the rectifier turns **OFF** before the power pins are disengaged. It also ensures that the rectifier turns **ON** only after the power pins have been engaged. Must be connected to  $V_{OUT}$  (-) for the rectifier to be ON.

**8V\_INT:** Single wire connection between modules, provides redundant bias to the DC/DC control circuitry of an unpowered module.

## Status Signals

**Module Present:** This signal is used as an OUTPUT signal by the rectifier to notify the system controller that a rectifier is physically present in the slot. This signal pin is pulled down to Logic\_GRD by the rectifier

**Power Good Warning (PG#):** This signal is HI when the main output is being delivered and goes LO if the main output is about to decay below regulation. Note that should a catastrophic failure occur, the signal may not be fast enough to provide a meaningful warning. PG# also pulses at a 1ms duty cycle if the unit is in overload.

**Fault#:** A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Fan failure

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- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

## Serial Bus Communications

The I<sup>2</sup>C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I<sup>2</sup>C Serial bus.

All signals are referenced to 'Logic\_GRD'.

**Pull-up resistors:** The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I<sup>2</sup>C and SMBus standards.

**Serial Clock (SCL):** The clock pulses on this line are generated by the host that initiates communications across the I<sup>2</sup>C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I<sup>2</sup>C /SMBus specifications.

**Serial Data (SDA):** This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I<sup>2</sup>C /SMBus specifications.

## Digital Feature Descriptions

**PMBus™ compliance:** The rectifier is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from [www.pmbus.org](http://www.pmbus.org).

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

The Alert# response protocol (ARA) whereby the PMBus Master can inquire who activated the Alert# signal is also supported. This feature is described in more detail later on.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

**Non-supported commands:** Non supported commands are flagged by setting the appropriate STATUS bit and issuing an

SMBAlert# to the 'host' controller. If a non-supported read is requested the rectifier will return 0x00h for data.

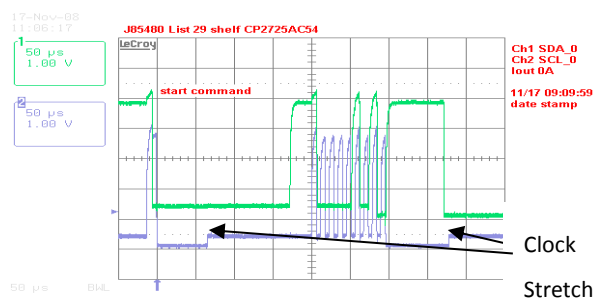
**Data out-of-range:** The rectifier validates data settings and sets the data out-of-range bit and SMBAlert# if the data is not within acceptable range.

**Master/Slave:** The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

**Clock stretching:** The 'slave'  $\mu$ Controller inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier.

Note that clock stretching can only be performed after completion of transmission of the 9<sup>th</sup> ACK bit, the exception being the START command.



Example waveforms showing clock stretching.

**I<sup>2</sup>C Bus Lock-Up detection:** The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

**Communications speed:** Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate.

**Packet Error Checking (PEC):** The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the correct command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial  $C(x) = x^8 + x^2 + x + 1$ , in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

**Alert#:** The rectifier can issue Alert# driven from either its internal micro controller ( $\mu$ C) or from the I<sup>2</sup>C bus master

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selector stage. That is, the Alert# signal of the internal  $\mu$ C funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the rectifier. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The  $\mu$ C driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear\_faults' instruction.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOU over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults
- Both Alert#\_0 and -1 are asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR\_FAULTS command
- Bias power to the processor is recycled

The rectifier will re-assert the Alert line if the internal state of the rectifier has changed, even if that information cannot be reported by the status registers until a clear\_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear\_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the rectifier. The host is now able to read the latest reported status register information and issue a clear\_faults to retire the Alert signal.

**Re-initialization:** The I<sup>2</sup>C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I<sup>2</sup>C  $\mu$ Controller does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few  $\mu$ seconds required to accomplish re-initialization the I<sup>2</sup>C  $\mu$ Controller may not recognize a command sent to it. (i.e. a start condition).

**Read back delay:** The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning

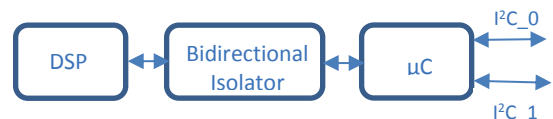
state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

**Successive read backs:** Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

### Dual Master Control:

Two independent I<sup>2</sup>C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I<sup>2</sup>C lines does not affect communications capability on the other I<sup>2</sup>C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time.

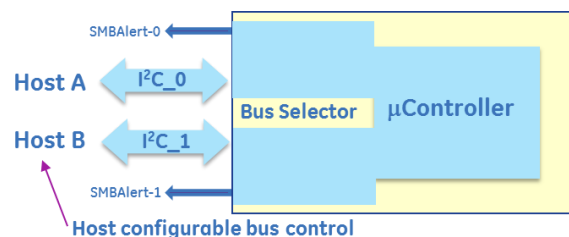
Conceptually a Digital Signal Processor (DSP) referenced to Vout(-) of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power GRD, Vout(-) and signal GRD (Logic\_GRD). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I<sup>2</sup>C lines to two independent system controllers.



The secondary micro controller is designed to default to I2C\_0 when powered up. If only a single system controller is utilized, it should be connected to I2C\_0. In this case the I2C\_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I2C\_0 and the other to I2C\_1.

At power up the master connected to I2C\_0 has control of the bus. See the section on Dual Master Control for further description of this feature.



Conceptual representation of the dual I<sup>2</sup>C bus system.

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## PMBus™ Commands

**Standard instruction:** Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8	1	8	1
S	Slave address	Wr	A	Command Code

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

☐ Master to Slave ☐ Slave to Master

SMBUS annotations; S – Start, Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

**Standard READ:** Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	No-ack	P

**Block communications:** When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1
Byte count = N	A	Data 1	A	Data 2	A

8	1	8	1	8	1	1
.....	A	Data 48	A	PEC	A	P

Block read format:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte count = N	A	Data 1	A	Data 2	A

8	1	8	1	8	1	1
.....	A	Data 48	A	PEC	NoAck	P

**Linear Data Format:** The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the

exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^E$$

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent

## Standard features

**Supported features that are not readable:** The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both CNTL pin and the OPERATION are supported.
CAPABILITY (0x19)	400KHz, SMBALERT
PMBus revision (0x98)	1.2

**Status and Alarm registers:** The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear\_faults command is received from the host. For example, the shutdown or OC\_fault bits stay in their alarmed state until the host clears the registers.

A clear\_faults clears all registers. If a fault still persists after the clear\_faults is commanded, the register bit annunciating the fault is reset again.

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## PMBus™ Command set:

Command	Hex Code	Data Field	Non-Volatile Memory Storage
Operation	0x01	1	yes
Clear_Faults	0x03	-	
Write_Protect	0x10	1	no
Restore_default_all	0x12	-	
Restore_user_all	0x16	-	
Restore_default_code	0x14	1	
Store_user_code	0x17	1	yes
Restore_user_code	0x18	1	
Vout_mode	0x20	1	
Vout_command	0x21	2	yes
Vin_ON	0x35	2	no
Vin_OFF	0x36	2	no
Fan_config_1_2	0x3A	1	Yes / 99
Fan_command_1	0x3B	2	
Vout_OV_fault_limit	0x40	2	Yes / 60
Vout_OV_fault_response	0x41	1	Yes / 80
Vout_OV_warn_limit	0x42	2	Yes / 59
Vout_UV_warn_limit	0x43	2	Yes / 42
Vout_UV_fault_limit	0x44	2	Yes / 41
Vout_UV_fault_response <sup>13</sup>	0x45	1	No / C0
Iout_OC_fault_limit	0x46	2	Yes /
Iout_OC_fault_response	0x47	1	Yes / C0
Iout_OC_LV_fault_limit	0x48	2	Yes/36
Iout_OC_warn_limit	0x4A	2	Yes /
OT_fault_limit	0x4F	2	Yes/TBD
OT_fault_response <sup>14</sup>	0x50	1	Yes / C0
OT_warn_limit	0x51	2	Yes/TBD
Vin_OV_fault_limit	0x55	2	yes
Vin_OV_fault-response	0x56	1	No / C0
Vin_OV_warn_limit	0x57	2	yes
Vin_UV_warn_limit	0x58	2	yes
Vin_UV_fault_limit	0x59	2	No /
Vin_UV_fault_response	0x5A	1	No / C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_Vout	0x7A	1	
Status_Iout	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Status_fan_1_2	0x81	1	
Read_Vin	0x88	2	
Read_Iin	0x89	2	
Read_Vout	0x8B	2	
Read_Iout	0x8C	2	
Read_temp_PFC	0x8D	2	
Read_temp_DC+PRI	0x8E	2	

Command	Hex Code	Data Field	Non-Volatile Memory Storage
Read_temp_DC_SEC	0x8F	2	
Read_fan_speed_1	0x90	2	
Read_fan_speed_2	0x91	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	6	
Mfr_model	0x9A	16	
Mfr_revision	0x9B	8	
Mfr_serial	0x9E	16	
Status_summary	0xD0	12	
Status_unit	0xD1	2	
Status_alarm	0xD2	4	
Read_fan_speed	0xD3	7	
Read_input	0xD4	14	
Read_firmware_rev	0xD5	7	
Read_run_timer	0xD6	4	
Status_bus	0xD7	1	
Take over bus control	0xD8		yes
EEPROM Record	0xD9	128	yes
Read_temp_exhaust	0xDA	2	
Read_temp_inlet	0xDB	2	
Reserved for factory use	0xDC		
Reserved for factory use	0xDD		
Reserved for factory use	0xDE		
Test Function	0xDF	1	
<b>Upgrade commands</b>			
Password	0xE0	4	
Target list	0xE1	4	
Compatibility code	0xE2	16	
Software version	0xE3	7	
Memory capability	0xE4	7	
Application status	0xE5	1	
Boot loader	0xE6	1	
Data transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

<sup>13</sup> Only latched (0x80) or restart (0xC0) are supported

<sup>14</sup> Only latched (0x80) or restart (0xC0) are supported



# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

## Command Descriptions

**Operation (0x01)** : By default the Rectifier is turned **ON** at power up as long as *Power ON/OFF* is active LO. The Operation command is used to turn the Rectifier ON or OFF via the PMBus. The data byte below follows the OPERATION command.

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To **RESET** the rectifier cycle the rectifier OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

**Clear\_faults (0x03)**: Clears all STATUS and FAULT registers and resets the Alert# line of the I<sup>2</sup>C side in control. The I<sup>2</sup>C side not in control cannot clear registers in the rectifier. This command is always executable.

If a fault still persists after the issuance of the clear\_faults command, the specific registers indicating the fault first clears but then get set again to indicate that the unit is still in the fault state.

**WRITE\_PROTECT register (0x10)**: Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write\_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store\_user\_code command. The default setting of this register is enable\_all\_writes, write\_protect 0x00h. The write\_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

**Restore\_Default\_All (0x12)**: Restores all register values and responses to the default parameters set in the rectifier. The factory default cannot be changed.

**Restore\_default\_code (0x14)**: Restore only a specific register parameter to the factory default parameters set in the rectifier.

**Store\_user\_code (0x17)**: Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

**Restore\_user\_code (0x18)**: Restores the user default setting of a single register.

**Vout\_mode (0x20)**: This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout\_command. These commands have a 16 bit mantissa. The exponent is fixed by the module and is returned by this command.

Mode	Bits [7:5]	Bits [4:0] (exponent)
Linear	000b	xxxxxb

**Vout\_Command (0x21)** : Used to dynamically change the output voltage of the rectifier. This command can also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all power supplies using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the Vprog signal pin. The program no longer looks at the 'Vprog pin' and will not respond to any hardware voltage settings. If power is removed from the  $\mu$ Controller it will reset itself into its default configuration looking at the Vprog signal for output voltage control. In many applications, the Vprog pin is used for setting initial conditions, if different than the factory setting. Software programming then takes over once I<sup>2</sup>C communications are established.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the margin pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Voltage margin range: 42V<sub>DC</sub> – 58 V<sub>DC</sub>.

**A voltage programming example**: The task: set the output voltage to 50.45V<sub>DC</sub>

This rectifier supports the linear mode of conversion specified in the PMBus™ specification. The supported output voltage exponent is documented in the Vout\_mode (0x20) command. The exponent for output voltage setting is 2<sup>-9</sup> (see the PMBus™ specification for reading this command). Calculate the required voltage setting to be sent; 50.45 x 2<sup>9</sup> = 25830. Convert this decimal number into its hex equivalent: 64E6 and send it across the bus LSB first and then MSB; E664 with the trailing PEC.

**Vin\_ON (0x35)**: This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low\_line or high\_line mode.

**Vin\_OFF (0x36)**: This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low\_line or high\_line mode.

## GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**Fan\_config\_1\_2 (0x3A)** : This command requires that the fan speed be commanded by duty cycle. Both fans must be commanded simultaneously. The tachometer pulses per revolution is not used. Default is duty cycle control.

**Fan\_command\_1 (0x3B)**: This command instructs the rectifier to increase the speed of both fans above what is internally required. The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e. 100% = 0 x 64h. The command can increase or decrease fan speed. An incorrect value will result in a 'data error'. Sending 00h tells the rectifier to revert back to its internal control.

**Vout\_OV\_fault\_limit (0x40)**: Sets the value at which the main output voltage will shut down. The default OV\_fault value is set at 60Vdc. This level can be permanently changed and stored in non-volatile memory.

**Vout\_OV\_fault\_response (0x41)**: This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

**Restart after a latched state**: Either of four restart mechanisms is available;

- The hardware pin **ON/OFF** may be cycled OFF and then ON.
- The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON.
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the **ON/OFF** signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

**Vout\_OV\_warn\_limit (0x42)**: Sets the value at which a warning will be issued that the output voltage is too high. The default OV\_warn limit is set at 56Vdc. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

**Vout\_UV\_warn\_limit (0x43)**: Sets the value at which a warning will be issued that the output voltage is too low. The default UV\_warning limit is set at 41Vdc. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

**Vout\_UV\_fault\_limit (0x44)**: Sets the value at which the rectifier will shut down if the output gets below this level. The default UV\_fault limit is set at 39Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

**Vout\_UV\_fault\_response (0x45)**: Sets the response if the output voltage falls below the UV\_fault\_limit. The default UV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

**Iout\_OC\_fault\_limit (0x46)**: Sets the value at which the rectifier will shut down. The default OC\_fault\_limit is contingent on whether the rectifier operates in the low\_line or high\_line mode. The default level can be permanently changed and stored in non-volatile memory. Which level is changed is contingent on the input voltage applied to the rectifier at the time the change takes place.

**Iout\_OC\_fault\_response (0x47)**: Sets the response if the output overload exceeds the OC\_Fault\_limit value. The default OC\_fault\_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state can be permanently changed and stored in non-volatile memory. The response is the same for both low\_line and high\_line operations.

**Iout\_OC\_warn\_limit (0x4A)**: Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level. The default level can be permanently changed and stored in non-volatile memory. Which level is changed is contingent on the input voltage applied to the rectifier at the time the change takes place.

**OT\_fault\_limit (0x4F)**: Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT\_fault\_response register.



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3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**OT\_fault\_response (0x50):** Sets the response if the output overtemperature exceeds the OT\_Fault\_limit value. The default OT\_fault\_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

**OT\_warn\_limit (0x51):** Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

**Vin\_OV\_fault\_limit (0x55):** Sets the value at which the rectifier shuts down because the input voltage exceeds the allowable operational limit. The default Vin\_OV\_fault\_limit is set at 300Vac. This level can be permanently lowered and stored in non-volatile memory.

**Vin\_OV\_fault\_response (0x56):** Sets the response if the input voltage level exceeds the Vin\_OV\_fault\_limit value. The default Vin\_OV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

**Vin\_UV\_warn\_limit (0x58):** This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV\_fault\_limit is 90Vac. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

**Vin\_UV\_fault\_limit (0x59):** Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin\_UV\_fault\_limit is set at 85Vac. This level can be permanently raised and stored in non-volatile memory.

**Vin\_UV\_fault\_response (0x5A):** Sets the response if the input voltage level falls below the Vin\_UV\_fault\_limit value. The default Vin\_UV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

**STATUS\_BYTE (0x78) :** Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	VOUT Overvoltage	0
4	IOUT Overcurrent	0
3	VIN Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

**STATUS\_WORD (0x79):** Returns status\_byte as the low byte and the following high\_byte.

Bit Position	Flag	Default Value
7	VOUT fault or warning	0
6	IOUT fault or warning	0
5	INPUT	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0

2	FANS	0
1	OTHER	0
0	UNKNOWN	0

**STATUS\_VOUT (0x7A):** Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	VOUT_OV_WARNING	0
5	VOUT_UV_WARNING	0
4	VOUT UV Fault	0
3 – 0	X	0

**STATUS\_IOUT (0x7B):** Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	X	0
5	IOUT OC Warning	0
4	X	0
3	CURRENT SHARE FAULT	0
2	IN POWER LIMITING MODE	0
1 – 0	X	0

The OC Fault limit sets where current limit is set. The rectifier actually shuts down below the LV fault limit setting.

**STATUS\_INPUT (0x7C):** Returns one byte of information of input voltage related faults.

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1 – 0	X	0

**STATUS\_TEMPERATURE (0x7D):** Returns one byte of information of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 – 0	X	0

**STATUS\_CML (0x7E):** Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 – 2	X	0
1	Other Communication Fault	0
0	X	0

# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**STATUS\_FAN\_1\_2 (0x81)** : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Fan 1 Fault	0
6	Fan 2 Fault	0
5 – 4	Not supported	0
3	Fan 1 speed overwritten	0
2	Fan 2 speed overwritten	0
1 – 0	Not supported	0

## Read back Descriptions

**Single parameter read back:** Functions (except V<sub>IN</sub>, I<sub>IN</sub>) can be read back one at a time using the read\_word\_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer. Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8	1	8	1
S	Slave address	Wr	A	Command Code

1	8	1
Sr	Slave address	Rd

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	No-Ack	P

**Read back error:** If the  $\mu$ C does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

**Read Vin, Iin (0x88,0x99):** Returns the reading of phase 1.

**Read\_fan\_speed 1 & 2 (0x90, 0x91):** Reading the fan speed is in Direct Mode returning the RPM value of the fan.

**Read\_FRU\_ID (0x99,0x9A, 0x9B 0x9E):** Returns FRU information. Must be executed one register at a time.

1	8	1	8	1
S	Slave address	Wr	A	Command 0x9x

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = x

8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	NA	P

**Mfr\_ID (0x99):** Manufacturer in ASCII – 6 characters maximum,  
General Electric – Critical Power represented as,  
GE-CP

**Mfr\_model (0x9A):** Manufacturer model-number in ASCII – 16 characters, for this unit: GP100H3M54TExxx

**Mfr\_revision (0x9B):** Total 8 bytes, provides the product series number when the product was manufactured.

**Mfr\_serial (0x9E):** Product serial number includes the manufacturing date, manufacturing location in up to 16 characters. For example:

13KZ51018193xxx, is decoded as;

13 – year of manufacture, 2013

KZ – manufacturing location, in this case Matamoros

51 – week of manufacture

018193xxx – serial #, mfr choice

## Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

**Mfr\_Specific Status and alarm registers:** The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

**Status\_summary (0xD0) :** This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

1	8	1	8	1
S	Slave address	Wr	A	Command Code

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 11

8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1
Current-LSB	A	Current-MSB	A

8	1	8	1
Temperature-LSB	A	Temperature-MSB	A

8	1	1
PEC	No-Ack	P

# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3Φ-380/480V<sub>AC</sub> Input; Default Outputs: ±54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**Status\_unit(0xD1):** This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

## Status-2

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	Power_Capacity [HL = 1]	x
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	x

**Oring fault:** Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the rectifier. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus, a non-destructive or'ing fault does not trigger a shutdown.

## Status-1

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	Service LED ON	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	x

**Status\_alarm (0xD2):** This command returns the ALARM-3 - ALARM-1 register values.

## Alarm-3

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i2c communications fault	0
3	AC monitor communications fault	0
2	x	0
1	x	0
0	Or'ing fault	0

## Alarm-2

Bit	Flag	Default
7	FAN_Fault	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	Vo lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

**Power Delivery:** If the difference between sourced current and current share is > 10A, a fault is issued.

## Alarm-1

Bit	Flag	Default
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

**Over temperature warning:** This flag is set 5°C prior to the commencement of an over temperature shutdown.

**Read\_Fan\_speed (0 x D3) :** Returns the commanded speed in percent and the measured speed in RPM. If a fan does not exist, or if the command is not supported the unit return 0x00.

1	8	1	8	1
S	Slave address	Wr	A	Command 0xE1

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 6

8	1	8	1	8	1	8	1
Adj%-LSB	A	Adj%-MSB	A	Fan1-LSB	A	Fan1-MSB	A

8	1	8	1	8	1	1
Fan2-LSB	A	Fan2-MSB	A	PEC	No-Ack	P

**Read input string (0xD4):** Reads back the input voltage, input current and total input power consumed by the rectifier.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDC	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = 14	A	Voltage – LSB-Φ1	A	Voltage – MSB-Φ1	A

8	1	8	1
Voltage – LSB-Φ3	A	Voltage – MSB-Φ3	A

8	1	8	1
Current – LSB-Φ1	A	Current – MSB-Φ1	A

8	1	8	1
Current – LSB-Φ3	A	Current – MSB-Φ3	A

8	1	8	1	8	1	1
Power – LSB	A	Power – MSB	A	PEC	No-ack	P

**Read\_firmware\_rev [0 x D5]:** Reads back the firmware revision of all three μC in the module.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDD	A

1	1	7	1	1	8	1
---	---	---	---	---	---	---

# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

A	Sr	Slave Address	Rd	A	Byte Count = 6	A
---	----	---------------	----	---	----------------	---

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
i2c major rev	A	i2c revision	A	PEC	No-ack	P

**Read\_run\_timer [0xD6]:** Reads the operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is 10 years

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 4	A

8	1	8	1	8	1
Time – LSB	A	Time	A	Time – MSB	A

8	1	1
PEC	No-ack	P

**EEPROM record (0xD9):** The  $\mu$ C contains 128 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xD9	A

8	1	8	1
Start location	A	Byte count	A

8	1	8	1
first_byte	A	.....	A
		.....	

8	1	1
PEC	A	P

To read contents from the EEPROM section

1	7	1	1	8	1
S	Slave address	Wr	A	Command 0xD9	A

8	1	8	1
Memory location	A	Byte count $\leq 32$	A

1	7	1	1
Sr	Slave address	Rd	A

8	1	8	1
Byte 1	A	.....	A
		.....	

8	1	1
PEC	No-ack	P

## Test Function (0xDF)

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	Service LED	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

**LEDS test ON:** Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

**LEDS test OFF:** Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

**Service LED ON:** Requests the rectifier to **flash**-ON the Service (ok-to-remove) LED. The **flash** sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

**Service LED OFF:** Requests the rectifier to turn OFF the Service (ok-to-remove) LED.

**OR'ing Test:** This command verifies functioning of output OR'ing. At least two paralleled rectifiers are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one rectifier should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

## General performance descriptions

**Default state:** Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store\_user\_code).

**Delayed overcurrent shutdown during startup:** Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection.

## GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**Unit in Power Limit or in Current Limit:** When output voltage is  $> 36$ V<sub>DC</sub> the Output LED will continue blinking.

When output voltage is  $< 36$ V<sub>DC</sub>, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

**Restart after a latchoff:** PMBus™ fault\_response commands can be configured to direct the rectifier to remain latched off for over\_voltage, over\_temperature and over\_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON.
2. The unit may be commanded to restart via I<sup>2</sup>C through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart**.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the **Status\_2** register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

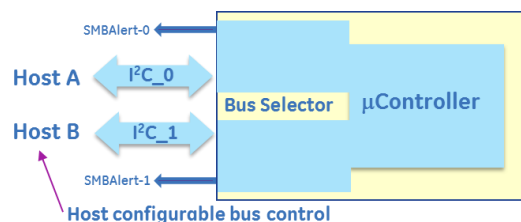
The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

**Auto\_restart:** Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the PMBus™ fault\_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

Two independent I<sup>2</sup>C lines and Alert# signals provide true communications redundancy allowing two independent controllers to sequentially control the rectifier.

A short or an open connection in one of the I<sup>2</sup>C lines does not affect communications capability on the other I<sup>2</sup>C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time when the bus is idle.



**Conceptual representation of the dual I<sup>2</sup>C bus system.**

The Alert# line exiting the rectifier combines the Alert# functions of rectifier control and dual\_bus\_control.

**Status\_bus (0xD7):** Bus\_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The  $\mu$ C may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Bit	Flag	Default
7	Bus 1 command error	0
6	Bus 1 SMBAlert enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 SMBAlert enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	1

**Command Execution:** The master not in control can issue two commands on the bus, take\_over\_bus\_control and clear\_faults

**Take\_over\_Bus\_Control(0xD8):** This command instructs the internal  $\mu$ C to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I<sup>2</sup>C selector section of the  $\mu$ C. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Control can be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note; The  $\mu$ C can handle read instructions from both busses simultaneously.

### Dual Master Control:

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The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

**Status Notifications:** Once control is transferred both SMBAlert lines should get asserted by the I2C selector section of the μC. The released 'master' is notified that a STATUS change occurred and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the rectifier. Each master must issue a clear\_faults command to clear his SMBAlert signal.

If the SMBAlert signal was actually triggered by the rectifier and not the I<sup>2</sup>C selector section of the μC, then only the 'master' in control can clear the rectifier registers. Incomplete transmissions should not occur on either bus.

**EEPROM record (0xD9):** The μC contains 128 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xD9	A

8	1	8	1
Start location	A	Byte count	A

8	1	8	1
first_byte	A	last_byte	A

8	1	1
PEC	A	P

To read contents from the EEPROM section

1	7	1	1	8	1
S	Slave address	Wr	A	Command 0xD9	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1	8	1
Byte 1	A	Byte ≤ 32	A

8	1	1
PEC	No-ack	P

## Test Function (0xDF)

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	Service LED	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

**LEDs test ON:** Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds

OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

**LEDs test OFF:** Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

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Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

## General performance descriptions

**Default state:** Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store\_user\_code).

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1. The hardware pin **ON/OFF** may be cycled OFF and then ON.



## GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

2. The unit may be commanded to restart via I<sup>2</sup>C through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart**.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the **Status\_2** register.

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**Auto\_restart:** Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault\_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

### Fault Management

Certain transitional states can occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear\_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

All fault information is sticky. If the fault still persists after a clear\_faults has been issued, then the fault state will reassert. All operational state information is not sticky.

The rectifier differentiates between **internal faults** that are within the rectifier and **external faults** that the rectifier protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed

by looking at the input LEDs. These fault categorizations are predictive in nature. Therefore, there is a likelihood that a categorization may not have been made correctly.

**Input voltage out of range:** The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

### State Change Definition

A **state\_change** is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a **state\_change**;

- Initial power-up of the system when INPUT gets turned ON. This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each rectifier to reset the system\_interrupt. If the rectifier is back-biased through the 8V\_INT or the 5VSTB it will not issue an SMBALERT# when INPUT power is turned back ON.
- Whenever the rectifier gets hot-plugged into a working system. This is the indicator to the system (MASTER) that a new rectifier is on line.
- Any changes in the bit patterns of the STATUS and ALARM registers are a STATUS change which triggers the SMBALERT# flag. Note that a host-issued command such as CLEAR\_FAULTS will not trigger an SMBALERT#

### Hot plug procedures

Careful system control is recommended when hot plugging a rectifier into a live system. It takes about 15 seconds for a rectifier to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple power supplies may respond to specific instructions because the address of the hot plugged rectifier always defaults to xxx0000 (depending on which device is being addressed within the rectifier) until the rectifier configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which rectifier is to be removed. The controller turns the service LED ON, thus informing the installer that the identified rectifier can be removed from the system. The system controller should then poll the module\_present signal to verify when the rectifier is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

### Hot plug configuration

During hot plug the rectifier attempts to configure itself to the bus voltage of a working system. The following are the turn-ON steps implemented within the rectifier:

- Prior to turning ON the main output the rectifier reads the bus voltage present on the bus. If the bus voltage and the commanded voltage (either default or Vmargin) are

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the same, the power supply proceeds to turn ON into its commanded value.

- If the bus voltage and the commanded voltage do not agree, the rectifier ignores the commanded voltage and waits for the external controller to command it to set its output voltage. This step is required to ensure that the plugged in rectifier does not attempt to source an entire system at an uncontrolled voltage level.
- If the bus voltage is below 40V<sub>dc</sub> the rectifier proceeds to turn ON into its commanded value.

### Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the rectifier. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the rectifier is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same rectifier. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the rectifier out of service.

**Information only alarms:** The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- V<sub>out</sub> out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stby out of limits
- Communication errors

### LEDs

Three LEDs are located on the front faceplate. The AC\_OK LED provides visual indication of the INPUT signal function. When the LED is ON GREEN the rectifier input is within normal design limits.

The second LED is the DC\_OK LED. When GREEN the DC output is present. When 'blinking' a power limit or overload condition exists. When OFF the output is not present.

The third LED is the FAULT LED. A continuous RED condition indicates that a fault exists and the rectifier has been shut down. Blinking of the RED LED in RS485 mode indicates that communications with the controller was not established. In I2C mode, blinking of the FAULT LED indicates an OTW.

### Remote upgrade

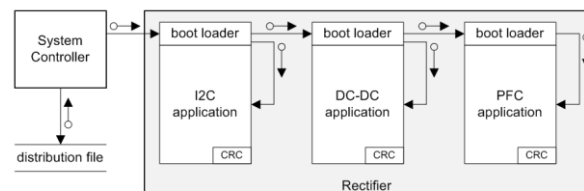
This section describes at a high-level the recommended re-programming process for the three internal micro controllers inside the rectifier when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by GE Critical Power for controller based systems positioned primarily for the telecommunications industry. GE Critical Power will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

For some customers internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from GE Critical Power. This kit contains a turn-key package with the re-program firmware.

**Conceptual Description:** The rectifier contains three independent  $\mu$ Controllers. The boost (PFC) section is controlled by the primary  $\mu$ Controller. The secondary DC-DC converter is controlled by the secondary  $\mu$ Controller, and I<sup>2</sup>C communications are being handled by the I<sup>2</sup>C Interface  $\mu$ Controller.

Each of the  $\mu$ Controllers contains a **boot loader** section and an **application** section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the rectifier.



The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

**The Upgrade Package:** This package contains the following files;

- **Manifest.txt** – The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary



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This file contains the version number and the compatibility code of the upgraded program for each of the three processors

- **Program.bin** - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file GP100H3R54TEZ.zip
- Unzipping the contents shows the following files  
GP100H3R54TEZ.pfc.bin  
GP100H3R54TEZ.sec.bin  
manifest.txt
- Opening manifest.txt shows the following  
# Upgrade manifest file  
# Targets: GP100H3R54TEZ PFC and SEC  
# Date: Tue 01/14/2014 14:25:09.37  
# Notes:
- Program contents  
>p,GP100H3R54TE\_P01,GP100H3R54TEZ\_PFC.bin,1.18  
>s,GP100H3R54TE\_S01,GP100H3R54TEZ\_SEC.bin,1.1  
compatibility code, new program, revision number

**Upgrade Status Indication:** The FAULT LED is utilized for indicating the status of the re-programming process.

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or programming in progress
Fault	ON	Erase or re-program failed

Wink: 0.25 seconds ON, 0.75 seconds OFF

Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

## Upgrade procedure

1. Initialization: To execute the re-programming/upgrade in the system, the module to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the module is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation.

Note: Make sure that sufficient power is provided by the remaining on-line power supplies so that system functionality is not jeopardized.

2. Unzip the distribution file
3. Unlock upgrade execution protection by issuing the command below;

**Password(0xE0):** This command unlocks the upgrade commands feature of the module by sending the characters 'UPGD'.

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE0	A	Byte count - 4

8	1	8	1	8	1	1
Byte 0 - U	A	Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

**Target list(0xE1) :** This command returns the upgradable processors within the module. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE1

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count - n

8	1	8	1	8	1	1
Byte 0	A	Byte n	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)  
s – secondary (DC-DC)  
i – I<sup>2</sup>C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the module compatibility code of the target processor.

**Compatibility code (0xE2):** The compatibility code consists of up to 16 characters defining the hardware configuration. To read the compatibility codes of each processor in the module execute the following read:

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 16	A	Byte 0

8	1	8	1	1
Byte 15	A	PEC	No-Ack	P

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)  
s – secondary (DC-DC)  
i – I<sup>2</sup>C

6. Check the software revision of the target processor and compare it to the revision in the upgrade. If the revisions are the same, or the module has a higher revision then no upgrade is required for the target processor.

**Software revision(0xE3):** This command returns the software revision of the target.

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1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE3	A	Target-x

1	8	1	8	1
Sr	Slave addr	Rd	A	Major revision

8	1	8	1	1
Minor revision	A	PEC	No-Ack	P

7. Verify the capability of each processor

**Memory capability (0xE4):** Provides the specifics of the capability of the device to be reprogrammed

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count=7	A	Max bytes

8	1	8	1	8	1	8	1
ET-LSB	A	ET-MSB	A	BT-LSB	A	BT-MSB	A

8	1	8	1	8	1	1
App_CRC_LSB	A	App_CRC_MSB	A	PEC	No-Ack	P

Where the fields definition are shown as below:

<b>Max Bytes</b>	Maximum number of bytes in a data packet
<b>ET</b>	Erase time for entire application space (in mS)
<b>BT</b>	Data packet write execution time (uS)
<b>APP_CRC</b>	Returns the application CRC-16 calculation. If the calculation returns invalid, the reprogram failed. (See application status(0xE5) command)

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

**Application status (0xE5):** Returns the Boot Loader's present status

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE5	A	Target-x

1	8	1	8	1	8	1	1
Sr	Slave addr	Rd	A	Status	A	PEC	No-Ack

Status bits:

0x00	Processor is available	0x10	Reserved
0x01	Application erased	0x20	Reserved
0x02	CRC-16 invalid	0x40	Manages downstream μC
0x04	Sequence out of order	0x80	In boot loader
0x08	Address out of range		

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

9. Issue a Boot Loader command with the *enter boot block* instruction

**Boot loader (0xE6):** This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

1	7	7	7	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE6	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

Data:

1=enter boot block (software reboot)

2=erase

3=done

4=exit<sup>15</sup> boot block (watchdog reboot)

**Note:** The target μC field is ignored for enter and exit commands. During this process if the output of the module was not turned OFF the boot loader will turn OFF the output

10. Erase and program each μC using the Boot Loader command, starting with the PFC.

11. Wait at least 1 second after issuing an *erase* command to allow the μC to complete its task.

12. Use command 0xE5 to verify that the PFC μC is erased. The returned status byte should be 0x81.

13. Use the Data Transfer command to update the application of the target μC.

**Data transfer (0xE7):** The process starts with uploading data packets with the first sequence number (0x0000).

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE7	A	Target-x

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count = n	A

8	1	8	1	1
Byte 0	A	.....	Byte n-1	A

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

<sup>15</sup> The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

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1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE4

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 3

1	8	1	8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Status	A	PEC	No-Ack	P

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

- Execute a Boot loader command to tell the PFC μC that the transfer is done.

At the completion signal, the PFC μC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

Wait for at least 1 second to allow time for the PFC μC to calculate the error checking value.

- Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.
- Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC μC will transfer to the uploaded application code.
- Wait for at least 1 second.
- Use command 0xE1 to verify that the PFC μC is now in the application code. The returned status data bte should be 0x00.
- Repeat the program upgrade for the Secondary and I<sup>2</sup>C μC's, if included in the upgrade package.

## Product comcode

Although the comcode number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

### Product comcode (0xE8):

1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE8

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 11

8	1	8	1	8	1	8	1
Byte 0	A	.....	Byte 10	A	PEC	No-Ack	P

**Error handling:** The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending module from service.

## Black box

Contents of the black box and more detailed information about the specifics of the feature are described in a separate document. The intent here is to provide a high level summary. This feature includes the following;

- A rolling event Recorder
- Operational Use Statistics

### The rolling event recorder

The purpose of the black box is to provide operational statistics as well as fault retention for diagnostics following either recoverable or non-recoverable fault events. Sufficient memory exists to store up to 5 time-stamped snapshot records (pages) that include the state of the status and alarm registers and numerous internal measurement points within the rectifier. Each record is stored into nonvolatile memory at the time when a black box trigger event occurs. Once five records are stored, additional records over-write the oldest record.

The memory locations will be cleared, when the product is shipped from the GE factory.

### Operational use statistics

This feature of the black box includes information on the repetition and duration of certain events in order to understand the long-term operational state of the rectifier. The events are placed into defined buckets for further analysis. For example; the rectifier records how long was the output current provided in certain load ranges.

### Accessing the event records

The event records are accessed by uploading the entire contents of the black box of the rectifier into a folder assigned by the user. Within the I<sup>2</sup>C protocol this upload is accomplished by the upload\_black\_box (0xF0) command described below. GE provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

**Upload black box(0xF0):** This command executes the upload from the rectifier to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the rectifier to gather the required data from the secondary DSP controller.

1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xF0

8	1	8	1
Start address - msb	A	Start address - lsb	A

8	1
Length = N (≤ 32)	A

..... delay 100ms

GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3Φ-380/480V<sub>AC</sub> Input; Default Outputs: ±54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Length ≤ 32	A	Byte 0

8	1	8	1	1
Byte N-1	A	PEC	No-Ack	P

If a transmission error occurs, or if the uC did not receive the data from the DSP, the uC may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by rev 1.3 of the GE Interface Adapter is 32 x 64 comprising 2048 bytes of data.

Start  
Address    0 ..... Byte ..... 31  
0000h  
0020h  
0040h  
.  
.  
.  
.  
.  
.  
.  
.  
07E0h

# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm 54/52$ V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

**Table 2: Alarm and LED state summary**

Condition	Rectifier LED State				Monitoring Signals <sup>18</sup>		
	AC OK Green	DC OK Green	Fault Red		Fault	PFW	Module Present
OK	1	1	0		HI	HI	LO
Thermal Alarm (5°C before shutdown)	1	1	Blinks		HI	HI	LO
Thermal Shutdown	1	0	1		LO	LO	LO
Defective Fan	1	0	1		LO	?	LO
Blown AC Fuse in Unit	1	0	1		LO	LO	LO
AC Present but not within limits	Blinks	0	0		HI	HI	LO
AC not present <sup>16</sup>	0	0	0		HI	LO	LO
Boost Stage Failure	1	0	1		LO	LO	LO
Over Voltage Latched Shutdown	1	0	1		LO	LO	LO
Over Current	1	Blinks	0		HI	Pulsing <sup>19</sup>	LO
Non-catastrophic Internal Failure <sup>17</sup>	1	1	1		LO	HI	LO
Missing Module							HI
Standby (remote)	1	0	0		HI	LO	LO

<sup>16</sup>This signal is correct if the rectifier is back biased from other power supplies in the shelf.

<sup>17</sup> Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.

<sup>18</sup> Signal transition from HI to LO is output load dependent

<sup>19</sup> Pulsing at a duty cycle of 1ms as long as the unit is in overload.

**Table 3: Signal Definitions**

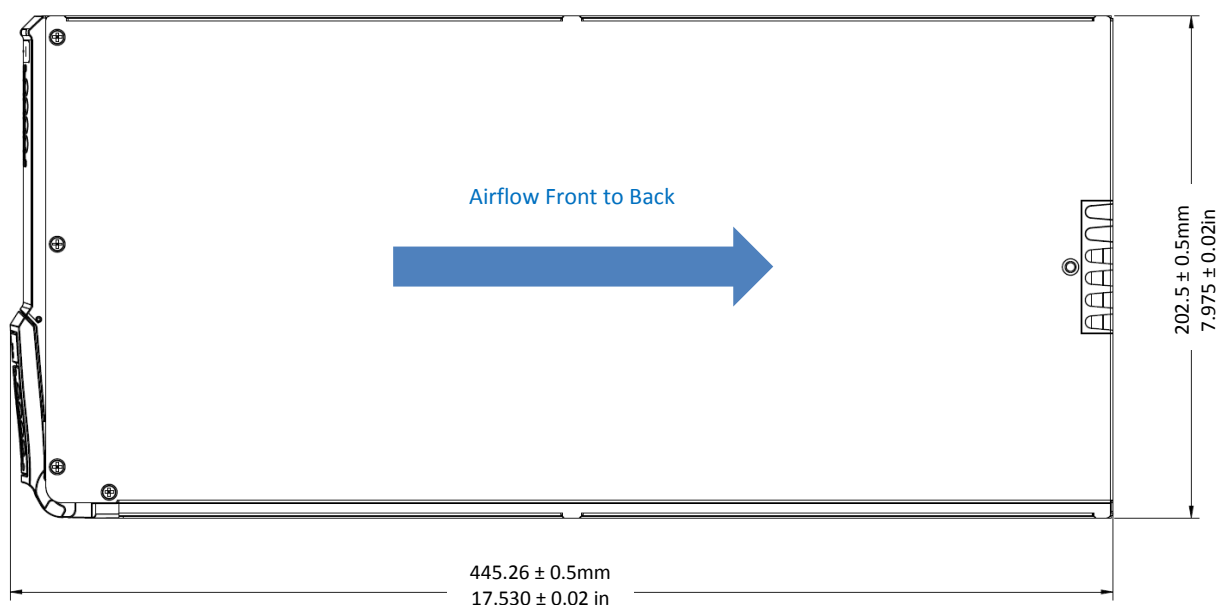
Signals (Fault, PFW, OTW, Power Capacity) are open drain FETs. An active LO signal (< 0.4V<sub>DC</sub>) state. Signals are referenced to Logic\_GRD unless otherwise stated.

Function	Label	Type	Description
Remote ON/OFF	ON/OFF	Input	When shorted to Logic_GRD turns ON the main output.
Output voltage adjust	Vprog	Input	Changes the output voltage (see table).
Power Fail Warning	PFW	Output	Open drain FET; Changes to LO $\cong$ 5msec before the output $\leq$ 40V <sub>DC</sub> .
Internal failure	Fault	Output	An open drain FET; normally HI, changes to LO.
Module Present	MOD_PRES	Output	Short pin, Connected to Logic_GRD notifies the system that module is present.
Defines communications	Protocol	Input	no-connect
Slot Address/Interlock	Slot_ID INTERLOCK	Input	Short pin referenced to Vout( - ). This signal provides the last-to-make and first-to-break function to properly control the rectifier for hot plug and hot disengagement. Connected to Vout( - ).
Unit Address	Unit_ID	Input	A resistor to Logic_GRD (see definition in spec).
Rack Address	Rack_ID	Input	An external resistor divider from 5VA to Logic_GRD (see definition I spec).
DC-DC Back bias	8V_INT	Bi-direct	Used to back bias the DSP from other operating Power supplies. Ref: Vout( - ).
Standby power	5VA	Output	5V @ 2A provided for external use. This output is always ON and or'ed isolated.
Current Share	Ishare	Bi-direct	A single wire active-current-share interconnect between modules Ref: Vout( - ).
I <sup>2</sup> C Line 0, I <sup>2</sup> C Line 1	SCL_0, SCL_1	Input	Clock signal pins of the two redundant buses. No internal pull ups are present.
I <sup>2</sup> C Line 0, I <sup>2</sup> C Line 1	SDA_0, SDA_1	Bi-direct	Data signal pins of the two redundant buses. No internal pull ups are present.
SMBALERT# Line 0, Line 1	ALERT#_0, ALERT#_1	Output	Interrupt signal pins of the two redundant buses. This signal is pulled to 3.3V via a 10k $\Omega$ resistor. Active LO.

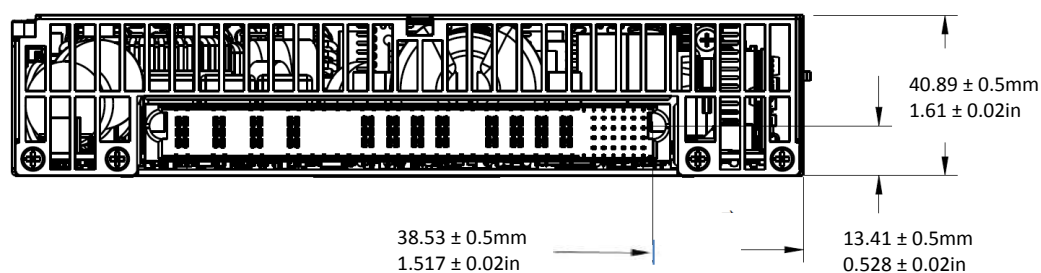
# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

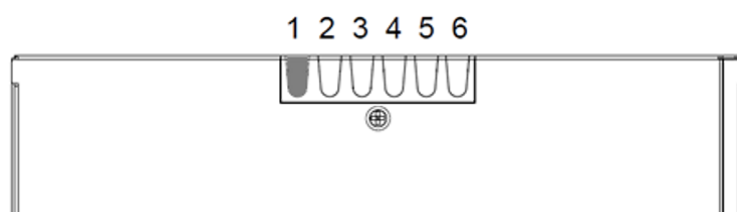
## Mechanical Outline



**Top View** [Note: add safety label to side of unit per UL, EC directives, TUV, Power Systems Practices]



**Rear View**

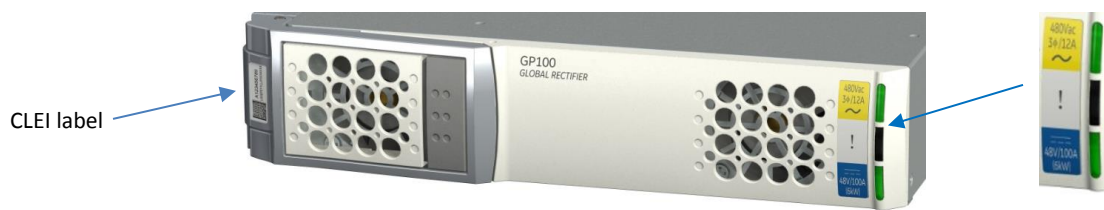


**Keying**

Product	Keying Location Knotched
I2C communications	1

# GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W



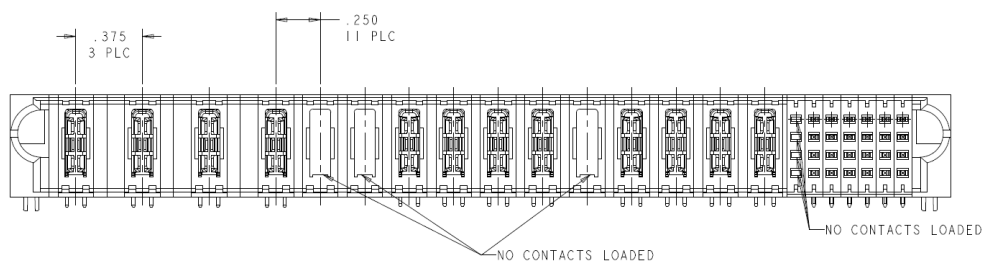
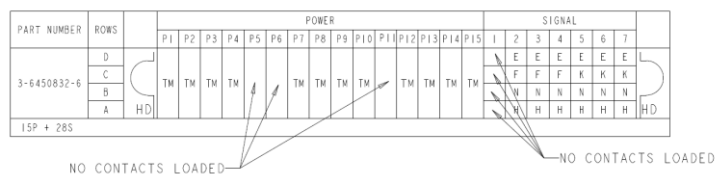
Front View: Faceplate Color: Spattered Finish CO White (OS11148)

## Front Panel LEDs

Symbol	Color	Function
~	Green	<b>ON:</b> Input ok <b>Blinking:</b> Input out of limits
!	Red	<b>ON:</b> Fault <b>Blinking:</b> Impending failure warning
≡	Green	<b>ON:</b> Output ok <b>Blinking:</b> Overload

## Mating Connector

Rectifier side: Tyco 3-6450832-6



AC INPUT				DC OUTPUT											SIGNALS							
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	1	2	3	4	5	6	7	
L1	L2	L3	Frame GND	Empty	Empty	Vout +	Vout +	Vout +	Vout +	Empty	Vout -	Vout -	Vout -	Vout -	Empty	SLOT_ID INTERLOCK	PROTOCOL	Unit_ID	ALERT1#	SDA1	SCL1	D
															Empty	NO CONNECT	NO CONNECT	Rack_ID	MOD_PRES	FAULT#	LOGIC_GND	C
															Empty	8V_INT	NO CONNECT	NO CONNECT	Vprog	PFW#	5VA	B
															Empty	ISHARE	NO CONNECT	REMOTE ON/OFF	ALERT0#	SDA0	SCL0	A
PWB																						

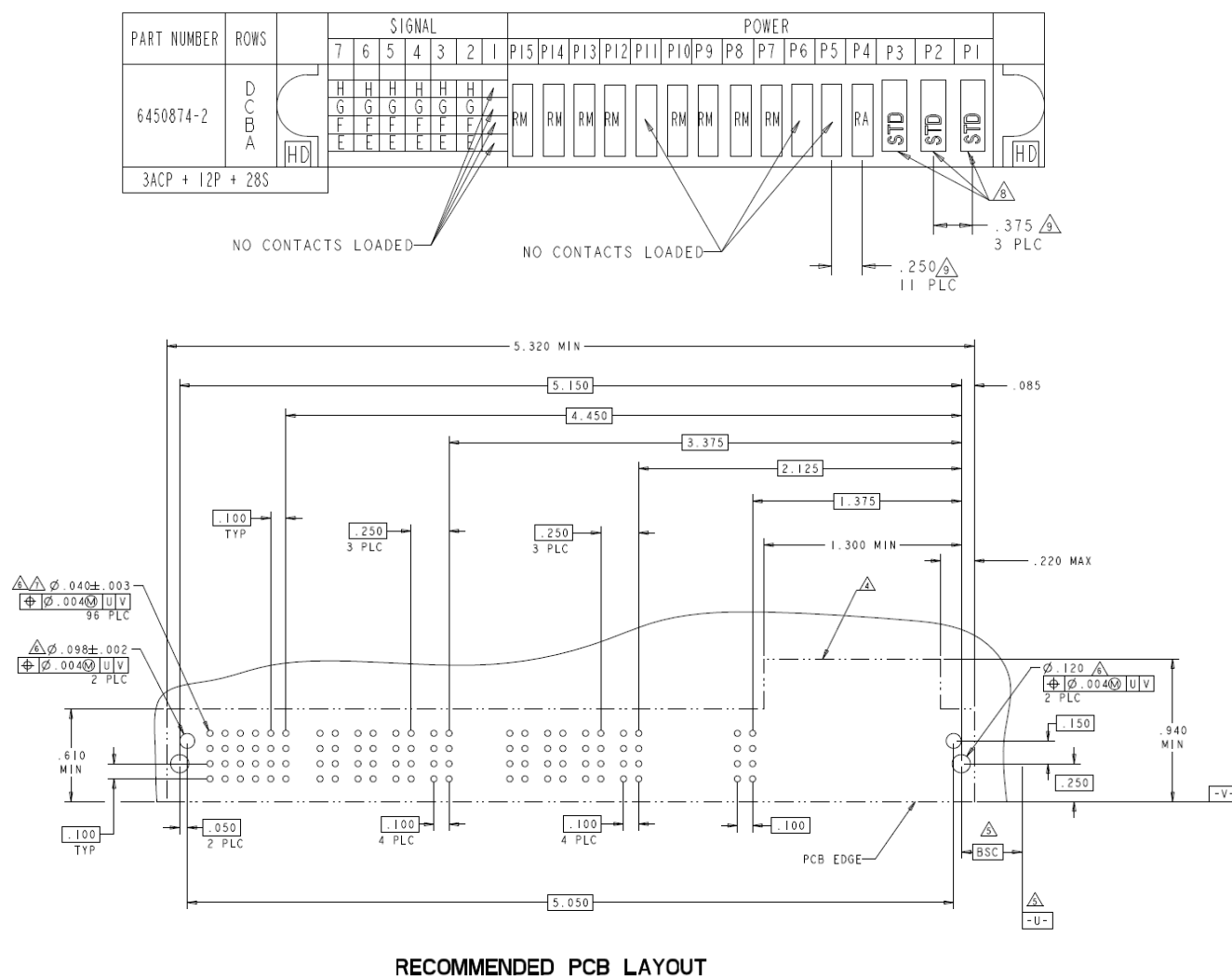
### Notes:

- = Short Pin
- = System side mating connector must have its Frame GND pin the longest to ensure that it is mating first.
- = Slot location

SIGNALS							
1	2	3	4	5	6	7	
Empty	SLOT_ID INTERLOCK	PROTOCOL	Unit_ID	ALERT1#	SDA1	SCL1	D
Empty	NO CONNECT	NO CONNECT	Rack_ID	MOD_PRES	FAULT#	LOGIC_GND	C
Empty	8V_INT	NO CONNECT	NO CONNECT	Vprog	PFW#	5VA	B
Empty	ISHARE	NO CONNECT	REMOTE ON/OFF	ALERT0#	SDA0	SCL0	A

**3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W**

**System side receptacle:** Tyco soldered version: 6450874-2  
press-fit version: 6450884-2  
AC power contact: 1-1600961-8 (3X)  
AC power contact secondary lock: 1600903-1 (3X)





## GP100H3M54TEZ Global Platform Line High Efficiency Rectifier

3 $\Phi$ -380/480V<sub>AC</sub> Input; Default Outputs:  $\pm$ 54/52V<sub>DC</sub> @ 6000W, 5V<sub>DC</sub> @ 10W

### Ordering Information

Please contact your GE Sales Representative for pricing, availability and optional features.

Item	Description	Comcode
GP100H3M54TEZ	110A rectifier with isolated dual I <sup>2</sup> C communications	150039274

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