Model 357

Voltage Controlled Crystal Oscillator

FEATURES

- Standard 7x5mm Surface Mount Footprint
- HCMOS/TTL Compatible Output
- Frequency Range 1.5 – 77.76 MHz
- Frequency Stability, ±50 ppm Standard (±25 ppm and ±20 ppm available)
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable Standard
- Low Phase Jitter, ***NON-Multiplied***
- Tape & Reel Packaging
- **RoHS/Green Compliant**

DESCRIPTION

The Model 357 is a ceramic packaged Voltage Controlled oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

ORDERING INFORMATION

357 □□□□□□□ M □□□□

SUPPLY VOLTAGE
L = +3.3 Vdc, Pin 2 Enable (standard)
S = +5.0 Vdc, Pin 2 Enable (standard)
V = +3.3 Vdc, Pin 5 Enable
W = +5.0 Vdc, Pin 5 Enable

FREQUENCY IN MHz
M - indicates MHz and decimal point. Frequency is recorded with minimum 4 significant digits to the right of the "M".

ABSOLUTE PULL RANGE (APR)
B = ± 50 ppm APR (standard)
C = ± 80 ppm APR
D = ± 100 ppm APR

OPERATING TEMPERATURE RANGE
C = -20°C to +70°C (standard)
I = -40°C to +85°C *

FREQUENCY STABILITY
3 = ± 50 ppm (standard)
5 = ± 25 ppm
6 = ± 20 ppm *

* Consult factory for 6I availability.

Example Part Number: 357LB3C019M4400

• • • CTS Electronic Components, Inc. • 171 Covington Drive • Bloomingdale, IL 60108 • • •
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ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
	Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range	f_O	-	1.5	-	77.76	MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_O$	-	-	-	20, 25 or 50	± ppm
	Absolute Pull Range (See Note 2 and Ordering Information)	APR	-	50, 80 or 100	-	-	± ppm
	Operating Temperature Commercial Industrial	T_A	-	 -20 -40	 25	 70 85	°C
Electrical and Waveform Parameters	Supply Voltage Model 357S, 357W Model 357L, 357V	V_{CC}	± 10 %	 4.5 2.97	 5.0 3.3	 5.5 3.63	V
	Supply Current	I_{CC}	C_L = 15 pF 1.5 MHz to 20 MHz 20.1 MHz to 40 MHz 40.1 MHz to 60 MHz 60.1 MHz to 80 MHz	 - - - -	 5 8 10 12	 20 30 40 45	mA
	Output Load	C_L		-	-	30	pF
	Control Voltage Model 357S, 357W Model 357L, 357V	V_C	 V_{CC} = 5.0V V_{CC} = 3.3V	 0.5 0.3	 2.5 1.65	 4.5 3.0	V
	Frequency Deviation	Δf	25°C at Time of Shipment, over V_C range	-	135	-	± ppm
	Linearity Best Straight Line Fit	L	< 52 MHz > 52 MHz	-	5 8	10 15	%
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 CMOS Load CMOS Load	 90%V_{CC} -	 - -	 - 10%V_{CC}	V
	Output Current Levels Logic '1' Level Logic '0' Level	 I_{OH} I_{OL}	 CMOS Load CMOS Load	 - -	 - -	 -14 14	mA
	Rise and Fall Time	T_R, T_F	@ 10% - 90% Levels	-	3.5	5.0	ns
	Input Impedance	Z_C	-	50	-	-	kOhms
	Transfer Function	-	-	-	Positive	-	-
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
	Modulation Roll-off	-	@ -3dB	10	-	-	kHz
	Phase Jitter	tjms	Bandwidth 12 kHz - 20 MHz	-	-	1	ps RMS
	Enable Function Enable Input Voltage Disable Input Voltage	 V_{IH} V_{IL}	 Pin 2 or Pin 5 Logic '1', Output Enabled Pin 2 or Pin 5 Logic '0', Output Disabled	 2.5 -	 - -	 - 0.5	V
	Enable Time	T_{PLZ}	Pin 2 or Pin 5 Logic '1'	-	-	100	ns

Notes:

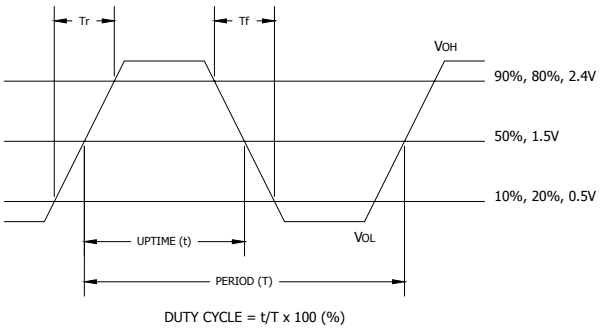
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 10 year aging at an average operating temperature of +40 °C.
2. Minimum guaranteed frequency shift from f_O over variations in temperature, aging, power supply and load at an average operating temperature of +40°C for 10 years.

SINGLE SIDE BAND PHASE NOISE
(typical maximum)

Frequency Offset	Phase Noise (dBc/Hz) *	Frequency Offset	Phase Noise (dBc/Hz) *
10 Hz	-60	10k Hz	-130
100 Hz	-90	100k Hz	-150
1k Hz	-112	≥ 100k Hz	-150

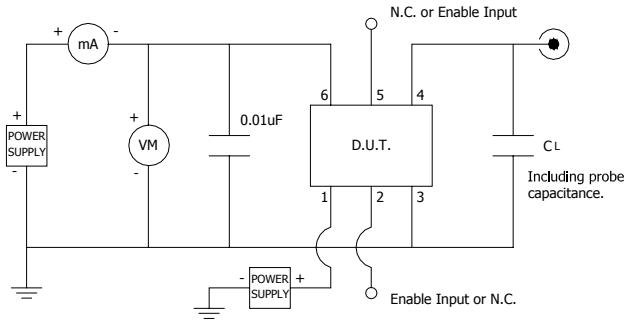
* Results may vary depending on frequency.

CMOS/TTL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, CMOS LOAD



D.U.T. PIN ASSIGNMENTS

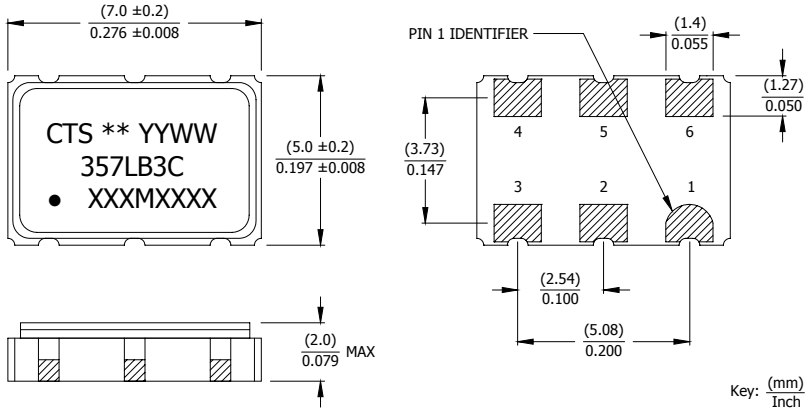
PIN	SYMBOL	DESCRIPTION
1	V_C	Control Voltage
2	EOH or N.C.	Enable or No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C. or EOH	No Connect or Enable
6	V_{CC}	Supply Voltage

ENABLE TRUTH TABLE

PIN 2 or PIN 5	PIN 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



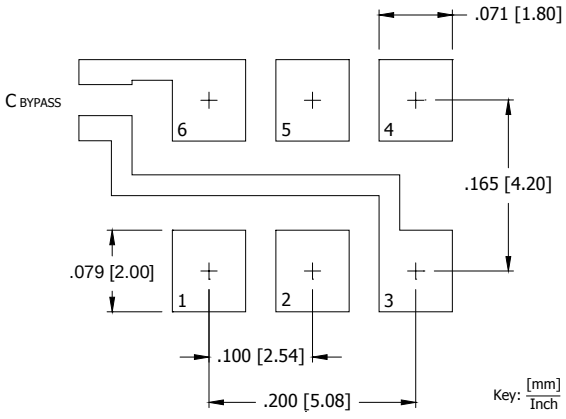
MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. Truncated CTS part number.
4. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.

NOTES

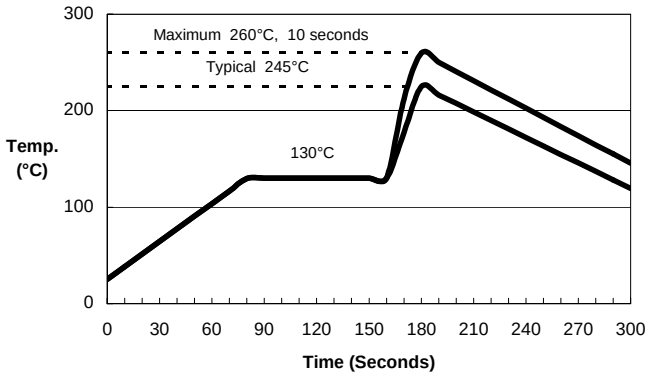
1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

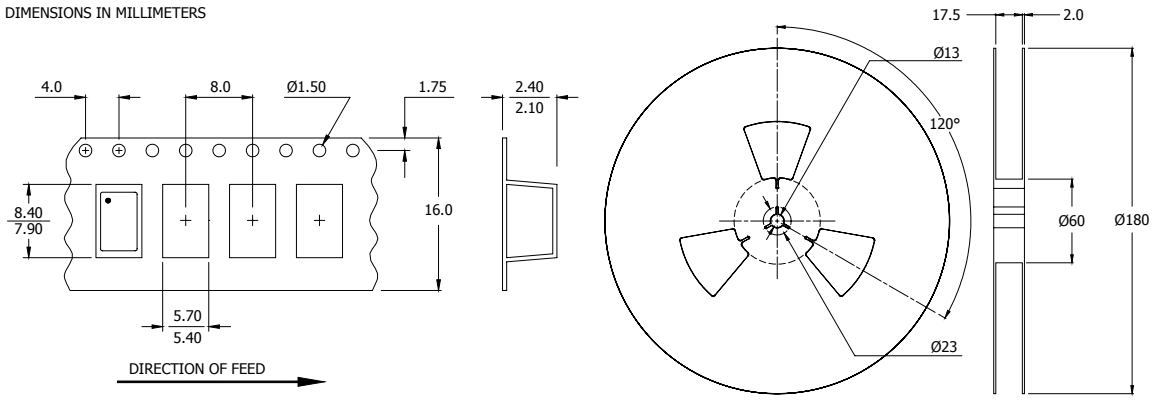


C_{BYPASS} should be ≥ 0.01 uF.

SUGGESTED REFLOW PROFILE



TAPE AND REEL INFORMATION



Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.

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ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
ОГРН: 1167746717709