FAIRCHILD SEMICONDUCTOR®

December 2012

FDD10AN06A0

N-Channel PowerTrench® MOSFET
60V, 50A, 10.5mΩ

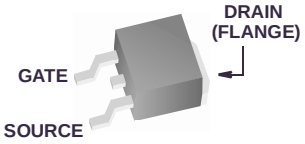
Features

- $r_{DS(ON)}$ = 9.4mΩ (Typ.), V_{GS} = 10V, I_D = 50A
- Q_g(tot) = 28nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Qrr Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

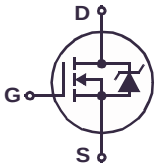
Applications

- Motor Load Control
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs

Formerly developmental type 82560



TO-252AA
FDD SERIES



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C < 115°C, V_{GS} = 10V)	50	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 52°C/W)	11	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	429	mJ
P_D	Power dissipation	135	W
	Derate above 25°C	0.9	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	1.11	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	52	°C/W

©2012 Fairchild Semiconductor Corporation

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD10AN06A0	FDD10AN06A0	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 50V, V_{GS} = 0V, T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 50A, V_{GS} = 10V	-	0.0094	0.0105	Ω
		I_D = 25A, V_{GS} = 6V	-	0.015	0.027	
		I_D = 50A, V_{GS} = 10V, T_J = 175°C	-	0.020	0.023	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	1840	-	pF
C_{OSS}	Output Capacitance		-	340	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	110	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 30V, I_D = 50A, I_g = 1.0mA		28	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V, V_{DD} = 30V, I_D = 50A, I_g = 1.0mA	-	3.5	4.6	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 30V, I_D = 50A, I_g = 1.0mA	-	9.8	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 30V, I_D = 50A, I_g = 1.0mA	-	6.4	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 30V, I_D = 50A, I_g = 1.0mA	-	7.8	-	nC
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 50A, V_{GS} = 10V, R_{GS} = 10Ω	-	-	131	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	79	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	32	-	ns
t_f	Fall Time		-	32	-	ns
t_{OFF}	Turn-Off Time		-	-	97	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 50A	-	-	1.25	V
		I_{SD} = 25A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	-	27	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	-	23	nC

Notes:
1: Starting T_J = 25°C, L = 8.58mH, I_{AS} = 10A.

Typical Characteristics T_C = 25°C unless otherwise noted

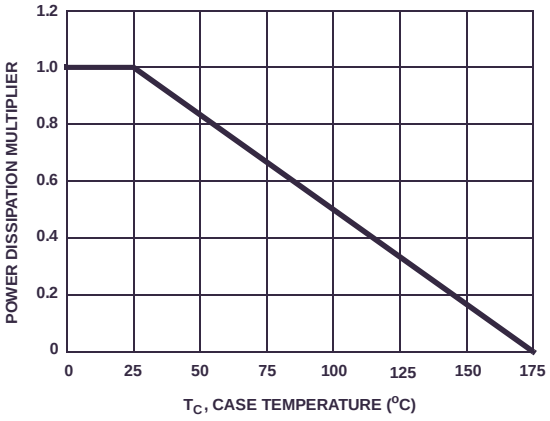


Figure 1. Normalized Power Dissipation vs Ambient Temperature

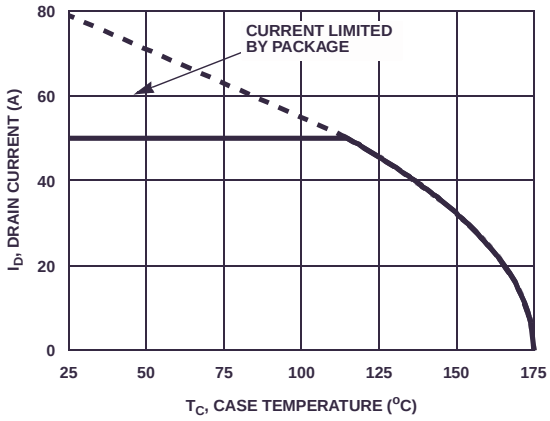


Figure 2. Maximum Continuous Drain Current vs Case Temperature

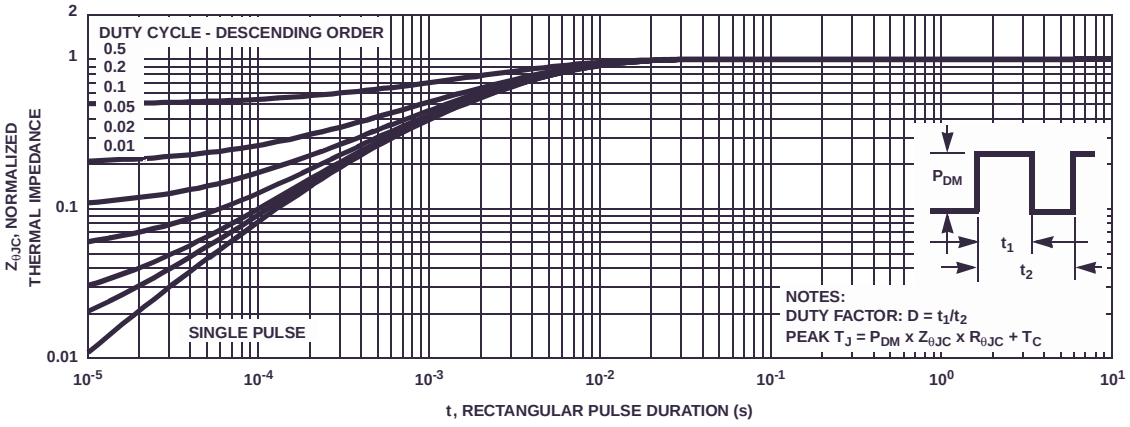


Figure 3. Normalized Maximum Transient Thermal Impedance

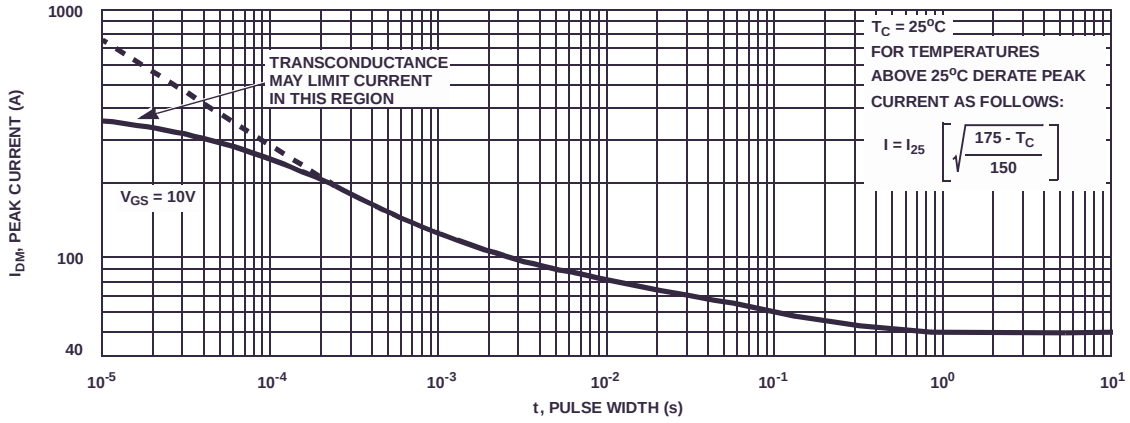


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

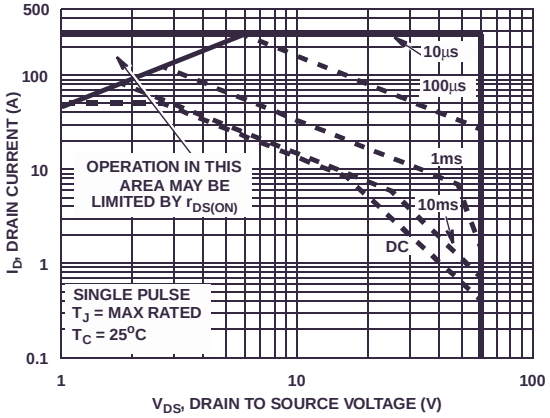
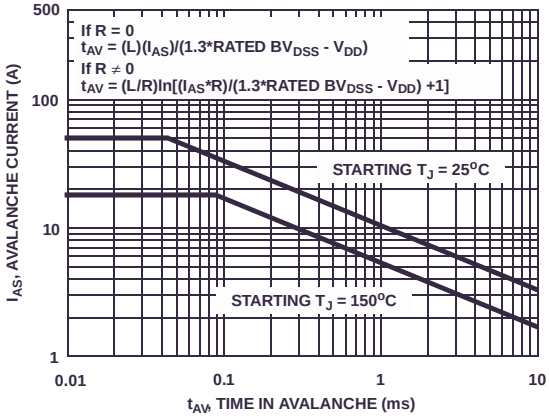


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

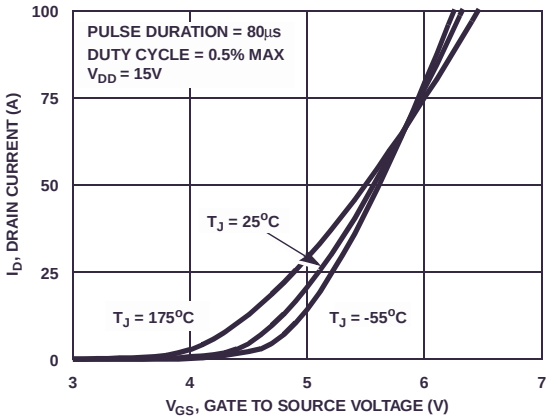


Figure 7. Transfer Characteristics

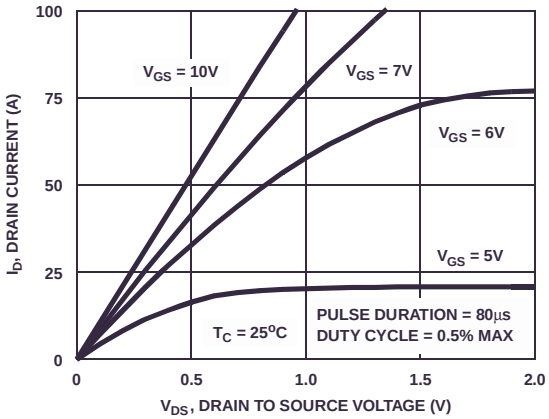


Figure 8. Saturation Characteristics

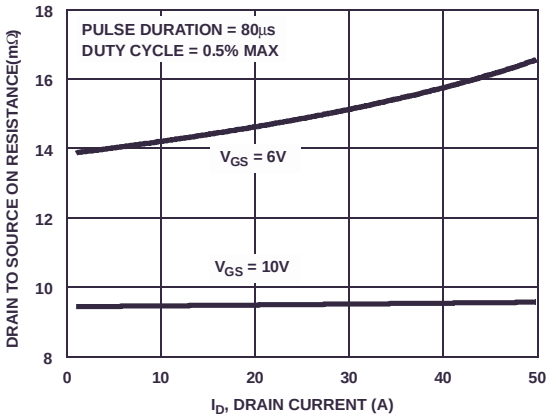


Figure 9. Drain to Source On Resistance vs Drain Current

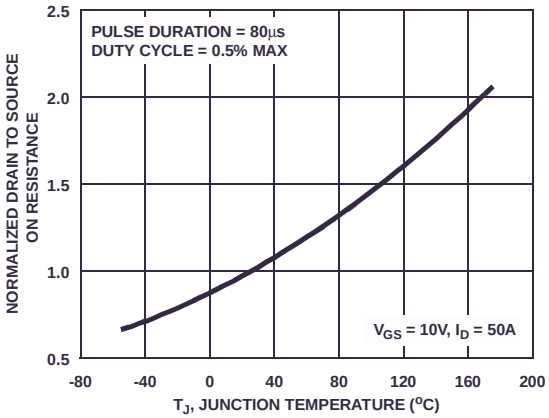


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

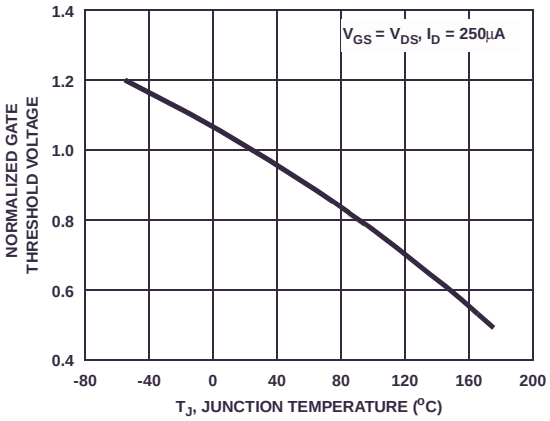


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

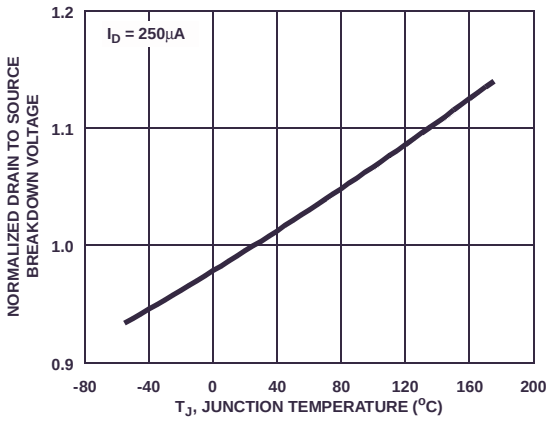


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

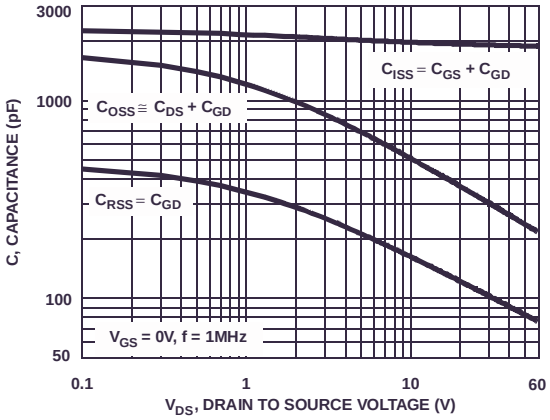


Figure 13. Capacitance vs Drain to Source Voltage

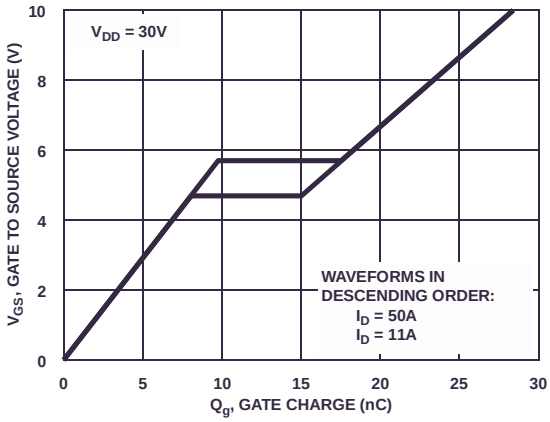


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

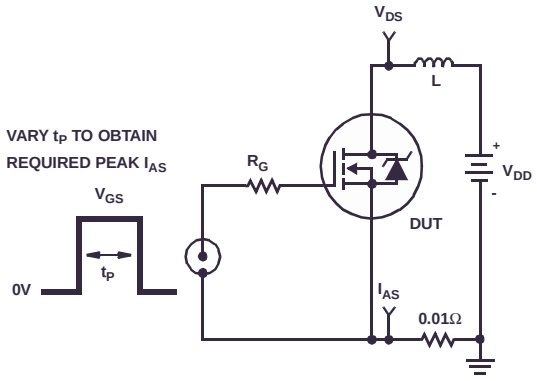


Figure 15. Unclamped Energy Test Circuit

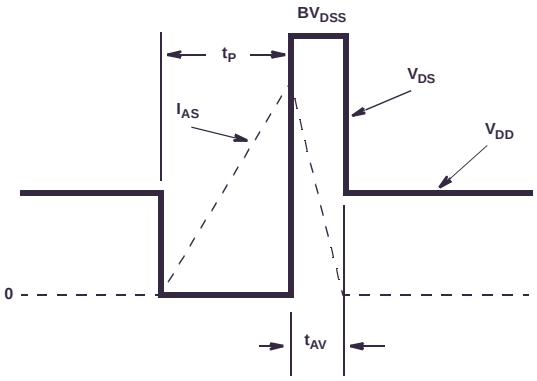


Figure 16. Unclamped Energy Waveforms

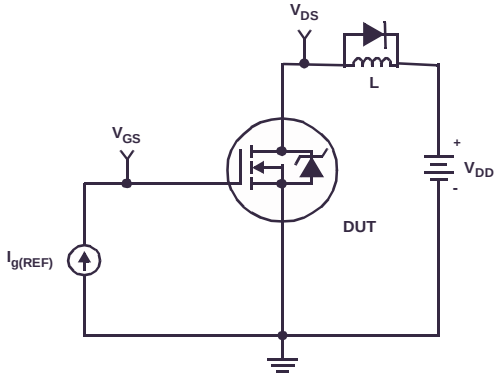


Figure 17. Gate Charge Test Circuit

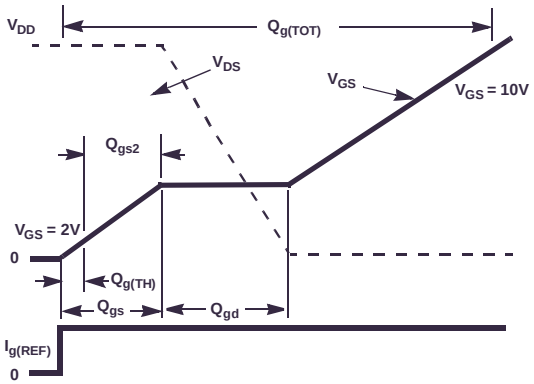


Figure 18. Gate Charge Waveforms

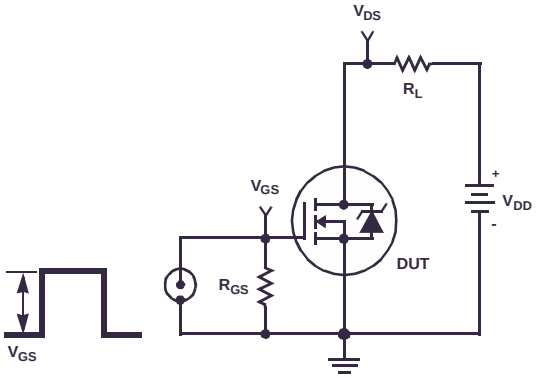


Figure 19. Switching Time Test Circuit

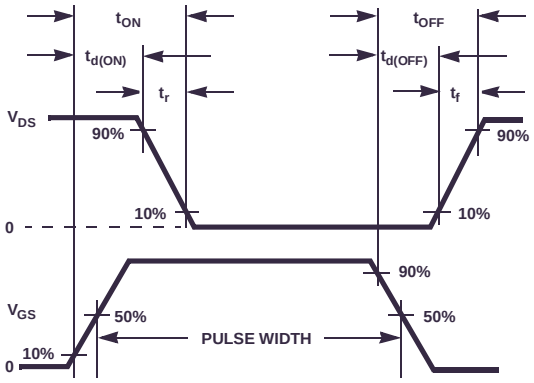


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad \text{(EQ. 3)}$$

Area in Centimeters Squared

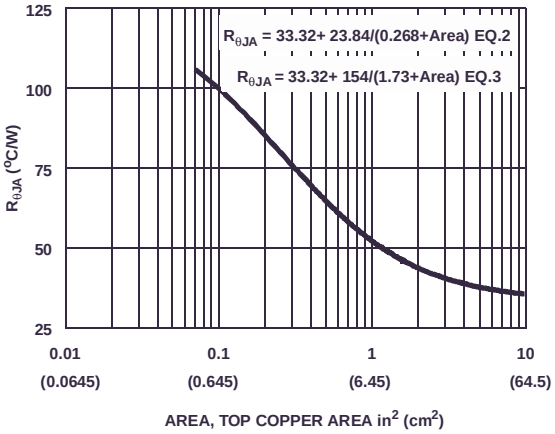


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

```
.SUBCKT FDD10AN06A0 2 1 3 ;       rev July 2002
Ca 12 8 7e-10
Cb 15 14 7e-10
Cin 6 8 1.8e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 67.2
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 3.2e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 1.2e-9

RLgate 1 9 32
RLdrain 2 5 10
RLsource 3 7 12

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 1.35e-3
Rgate 9 20 3.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 6e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

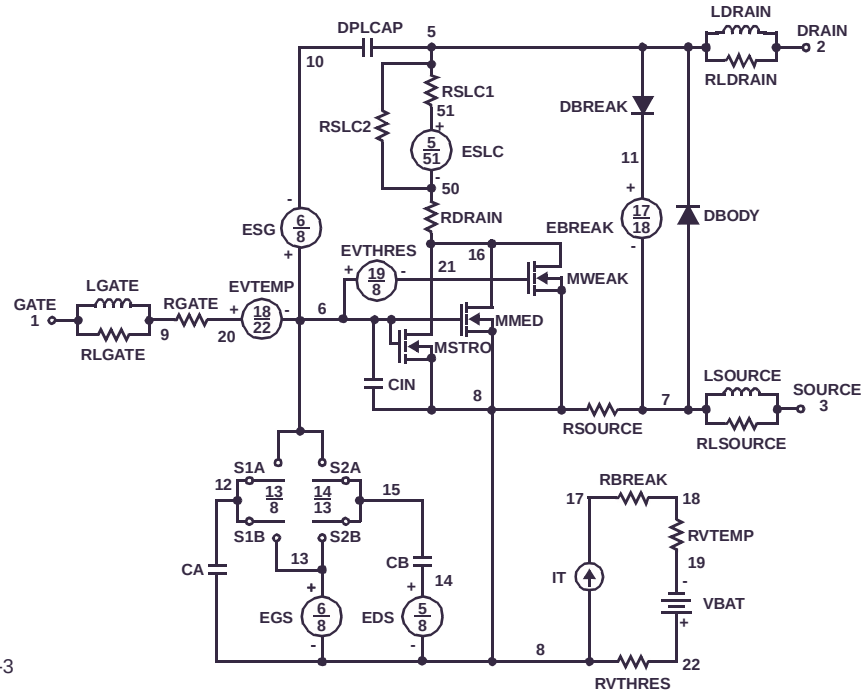
Vbat 22 19 DC 1
ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),7))}

.MODEL DbodyMOD D (IS=2E-11 N=1.06 RS=3.3e-3 TRS1=2.4e-3 TRS2=1.1e-6
+ CJO=1.25e-9 M=5.3e-1 TT=4.2e-8 XTI=3.9)
.MODEL DbreakMOD D (RS=2.7e-1 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=4.7e-10 IS=1e-30 N=10 M=0.44)

.MODEL MmedMOD NMOS (VTO=3.5 KP=5.5 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.6)
.MODEL MstroMOD NMOS (VTO=4.25 KP=80 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=2.92 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=36 RS=0.1)

.MODEL RbreakMOD RES (TC1=9e-4 TC2=5e-7)
.MODEL RdrainMOD RES (TC1=2.5e-2 TC2=7.8e-5)
.MODEL RSLCMOD RES (TC1=1e-3 TC2=3.5e-5)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.3e-5)
.MODEL RvtempMOD RES (TC1=-2.6e-3 TC2=1.3e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8 VOFF=-5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-8)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-1.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-2)
.ENDS
```



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV July 2002
template FDD10AN06A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl=2e-11,nl=1.06,rs=3.3e-3,trs1=2.4e-3,trs2=1.1e-6,cjo=1.25e-9,m=5.3e-1,tt=4.2e-8,xti=3.9)
dp..model dbreakmod = (rs=2.7e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod =  (cjo=4.7e-10,isl=10e-30,nl=10,m=0.44)
m..model mmedmod = (type=_n,vto=3.5,kp=5.5,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.25,kp=80,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.92,kp=0.03,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-8,voff=-5)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-5,voff=-8)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-2,voff=-1.5)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=-1.5,voff=-2)
c.ca n12 n8 = 7e-10
c.cb n15 n14 = 7e-10
c.cin n6 n8 = 1.8e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 67.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

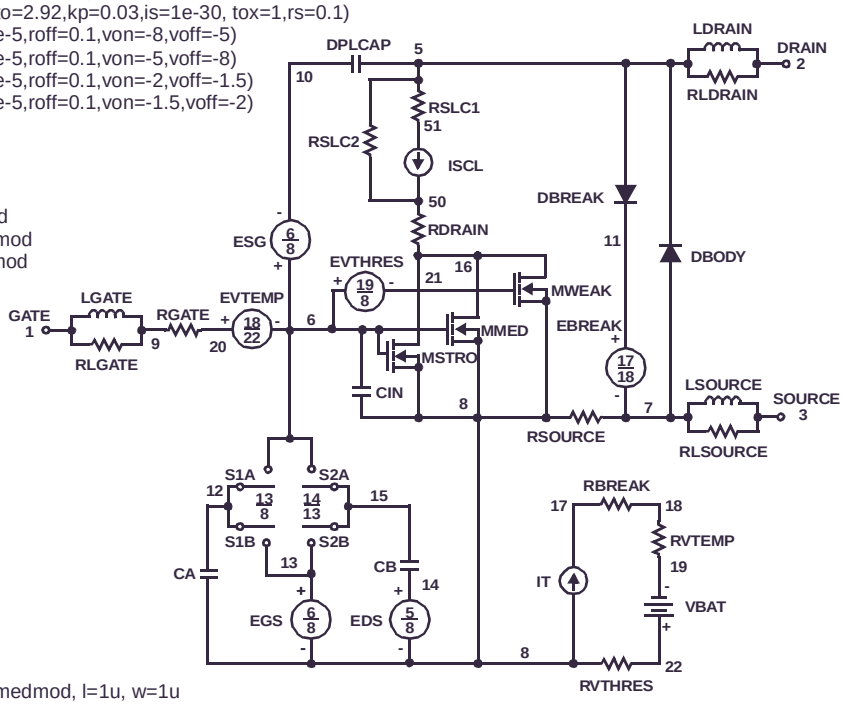
l.lgate n1 n9 = 3.2e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 1.2e-9

res.rlgate n1 n9 = 32
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 12

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=9e-4,tc2=5e-7
res.rdrain n50 n16  = 1.35e-3, tc1=2.5e-2,tc2=7.8e-5
res.rgate n9 n20 = 3.6
res.rslc1 n5 n51  = 1e-6, tc1=1e-3,tc2=3.5e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 6e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8  = 1, tc1=-5.3e-3,tc2=-1.3e-5
res.rvtemp n18 n19  = 1, tc1=-2.6e-3,tc2=1.3e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/250))** 7))
}
```



SPICE Thermal Model

REV 23 July 2002
FDD10AN06A0T

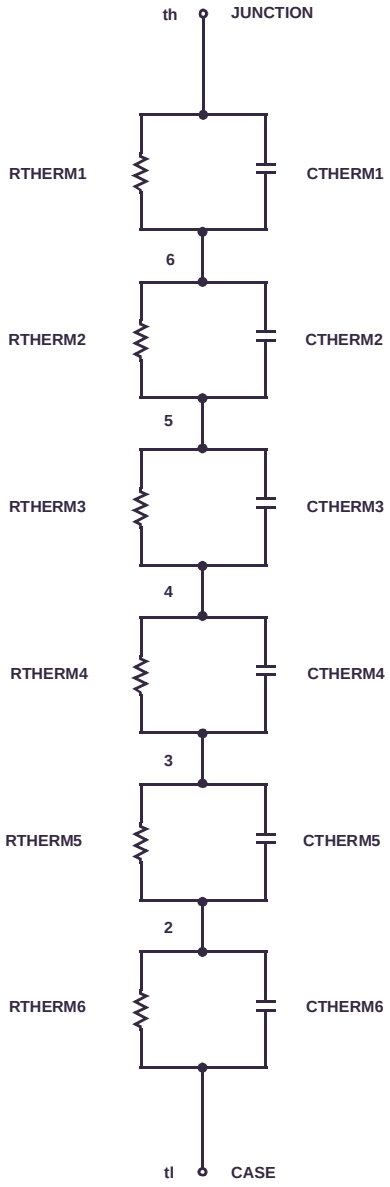
CTHERM1 TH 6 3.2e-3
CTHERM2 6 5 3.3e-3
CTHERM3 5 4 3.4e-3
CTHERM4 4 3 3.5e-3
CTHERM5 3 2 6.4e-3
CTHERM6 2 TL 1.9e-2

RTHERM1 TH 6 5.5e-4
RTHERM2 6 5 5.0e-3
RTHERM3 5 4 4.5e-2
RTHERM4 4 3 1.5e-1
RTHERM5 3 2 3.37e-1
RTHERM6 2 TL 3.5e-1

SABER Thermal Model

SABER thermal model FDD10AN06A0T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =3.2e-3
ctherm.ctherm2 6 5 =3.3e-3
ctherm.ctherm3 5 4 =3.4e-3
ctherm.ctherm4 4 3 =3.5e-3
ctherm.ctherm5 3 2 =6.4e-3
ctherm.ctherm6 2 tl =1.9e-2

rtherm.rtherm1 th 6 =5.5e-4
rtherm.rtherm2 6 5 =5.0e-3
rtherm.rtherm3 5 4 =4.5e-2
rtherm.rtherm4 4 3 =1.5e-1
rtherm.rtherm5 3 2 =3.37e-1
rtherm.rtherm6 2 tl =3.5e-1
}



FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP™*
BitSiC®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficentMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource^{SM}
Green Bridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Marking Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL ®*
The Power Franchise®
the power franchise®
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC®
TriFault Detect™
TRUECURRENT®*
μSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I61

ООО «НИОКРсистемс» - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование
- Работаем по 275 ФЗ

ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
ОГРН: 1167746717709