Intel StrataFlash® Memory (J3)

256-Mbit (x8/x16)

Datasheet

Product Features

- **Performance**
  - —110/115/120/150 ns Initial Access Speed
  - —125 ns Initial Access Speed (256 Mbit density only)
  - —25 ns Asynchronous Page mode Reads
  - —30 ns Asynchronous Page mode Reads (256Mbit density only)
  - —32-Byte Write Buffer
    - —6.8 µs per byte effective programming time
- **Software**
  - —Program and Erase suspend support
  - —Flash Data Integrator (FDI), Common Flash Interface (CFI) Compatible
- **Security**
  - —128-bit Protection Register
    - —64-bit Unique Device Identifier
    - —64-bit User Programmable OTP Cells
  - —Absolute Protection with V_{PEN} = GND
  - —Individual Block Locking
  - —Block Erase/Program Lockout during Power Transitions
- **Architecture**
  - —Multi-Level Cell Technology: High Density at Low Cost
  - —High-Density Symmetrical 128-Kbyte Blocks
    - —256 Mbit (256 Blocks) (0.18µm only)
    - —128 Mbit (128 Blocks)
    - —64 Mbit (64 Blocks)
    - —32 Mbit (32 Blocks)
- **Quality and Reliability**
  - —Operating Temperature: -40 °C to +85 °C
  - —100K Minimum Erase Cycles per Block
  - —0.18 µm ETOX™ VII Process (J3C)
  - —0.25 µm ETOX™ VI Process (J3A)
- **Packaging and Voltage**
  - —56-Lead TSOP Package
  - —64-Ball Intel® Easy BGA Package
  - —Lead-free packages available
  - —48-Ball Intel® VF BGA Package (32 and 64 Mbit) (x16 only)
  - —V_{CC} = 2.7 V to 3.6 V
  - —V_{CCQ} = 2.7 V to 3.6 V

Capitalizing on Intel's 0.25 and 0.18 micron, two-bit-per-cell technology, the Intel StrataFlash® Memory (J3) device provides 2X the bits in 1X the space, with new features for mainstream performance. Offered in 256-Mbit (32-Mbyte), 128-Mbit (16-Mbyte), 64-Mbit, and 32-Mbit densities, the J3 device brings reliable, two-bit-per-cell storage technology to the flash market segment. Benefits include more density in less space, high-speed interface, lowest cost-per-bit NOR device, support for code and data storage, and easy migration to future devices.

Using the same NOR-based ETOX™ technology as Intel's one-bit-per-cell products, the J3 device takes advantage of over one billion units of flash manufacturing experience since 1987. As a result, J3 components are ideal for code and data applications where high density and low cost are required. Examples include networking, telecommunications, digital set top boxes, audio recording, and digital imaging.

By applying FlashFile™ memory family pinouts, J3 memory components allow easy design migrations from existing Word-Wide FlashFile memory (28F160S3 and 28F320S3), and first generation Intel StrataFlash® memory (28F640J5 and 28F320J5) devices.

J3 memory components deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and the Scalable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Intel StrataFlash® memory devices. Manufactured on Intel® 0.18 micron ETOX™ VII (J3C) and 0.25 micron ETOX™ VI (J3A) process technology, the J3 memory device provides the highest levels of quality and reliability.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 290667-021
March 2005

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Revision History

Date of Revision	Version	Description
07/07/99	-001	Original Version
08/03/99	-002	A_0–A_2 indicated on block diagram
09/07/99	-003	Changed Minimum Block Erase time,I_{OL}, I_{OH}, Page Mode and Byte Mode currents. Modified RP# on *AC Waveform for Write Operations*
12/16/99	-004	Changed Block Erase time and t_{AVWH} Removed all references to 5 V I/O operation Corrected *Ordering Information*, Valid Combinations entries Changed Min program time to 211 µs Added DU to Lead Descriptions table Changed Chip Scale Package to Ball Grid Array Package Changed default read mode to page mode Removed erase queuing from Figure 10, *Block Erase Flowchart*
03/16/00	-005	Added Program Max time Added Erase Max time Added Max page mode read current Moved tables to correspond with sections Fixed typographical errors in ordering information and DC parameter table Removed V_{CCQ1} setting and changed $V_{CCQ2/3}$ to $V_{CCQ1/2}$ Added recommended resister value for STS pin Change operation temperature range Removed note that rp# could go to 14 V Removed V_{OL} of 0.45 V; Removed V_{OH} of 2.4 V Updated I_{CCR} Typ values Added Max lock-bit program and lock times Added note on max measurements
06/26/00	-006	Updated cover sheet statement of 700 million units to one billion Corrected Table 10 to show correct maximum program times Corrected error in Max block program time in section 6.7 Corrected typical erase time in section 6.7
2/15/01	-007	Updated cover page to reflect 100K minimum erase cycles Updated cover page to reflect 110 ns 32M read speed Removed Set Read Configuration command from Table 4 Updated Table 8 to reflect reserved bits are 1-7; not 2-7 Updated Table 16 bit 2 definition from R to PSS Changed V_{PENLK} Max voltage from 0.8 V to 2.0 V, Section 6.4, *DC Characteristics* Updated 32Mbit Read Parameters R1, R2 and R3 to reflect 110ns, Section 6.5, *AC Characteristics–Read-Only Operations* (1,2) Updated write parameter W13 (t_{WHRL}) from 90 ns to 500 ns, Section 6.6, *AC Characteristics–Write Operations* Updated Max. Program Suspend Latency W16 (t_{WHRH1}) from 30 to 75 µs, Section 6.7, *Block Erase, Program, and Lock-Bit Configuration Performance* (1,2,3)
04/13/01	-008	Revised Section 7.0, *Ordering Information*

Date of Revision	Version	Description
07/27/01	-009	Added Figure 4, *3 Volt Intel StrataFlash® Memory VF BGA Package (32 Mbit)* Added Figure 5, *3 Volt Intel StrataFlash® Memory VF BGA Mechanical Specifications* Updated Operating Temperature Range to Extended (Section 6.1 and Table 22) Reduced t_{EHQZ} to 35 ns. Reduced t_{WHEH} to 0 ns Added parameter values for –40 °C operation to Lock-Bit and Suspend Latency Updated V_{LKO} and V_{PENLK} to 2.2 V Removed Note #4, Section 6.4 and Section 6.6 Minor text edits
10/31/01	-010	Added notes under lead descriptions for VF BGA Package Removed 3.0 V - 3.6 V Vcc, and Vccq columns under AC Characteristics Removed byte mode read current row un DC characteristics Added ordering information for VF BGA Package Minor text edits
03/21/02	-011	Changed datasheet to reflect the best known methods Updated max value for Clear Block Lock-Bits time Minor text edits
12/12/02	-012	Added nomenclature for J3C (0.18 µm) devices.
01/24/03	-013	Added 115 ns access speed 64 Mb J3C device. Added 120 ns access speed 128 Mb J3C device. Added “TE” package designator for J3C TSOP package.
12/09/03	-014	Revised Asynchronous Page Read description. Revised Write-to-Buffer flow chart. Updated timing waveforms. Added 256-Mbit J3C pinout.
1/3/04	-015	Added 256Mbit device timings, device ID, and CFI information. Also corrected VLKO specification.
1/23/04	-016	Corrected memory block count from 257 to 255.
1/23/04	-016	Memory block count fix.
5/19/04	-018	Restructured the datasheet layout.
7/7/04	-019	Added lead-free part numbers and 8-word page information.
11/23/04	-020	Added Note to DC Voltage Characteristics table; “Speed Bin” to Read Operations table; Corrected format for AC Waveform for Reset Operation figure; Corrected “R” and “8W” headings in Enhanced Configuration Register table because they were transposed; Added 802 and 803 to ordering information and corrected 56-Lead TSOP combination number.
3/24/05	-021	Corrected ordering information.

1.0 Introduction

This document describes the Intel StrataFlash® Memory (J3) device. It includes a description of device features, operations, and specifications.

1.1 Nomenclature

AMIN:	AMIN = A0 for x8 AMIN = A1 for x16
AMAX:	32 Mbit AMAX = A21 64 Mbit AMAX = A22 128 Mbit AMAX = A23 256 Mbit AMAX = A24
Block:	A group of flash cells that share common erase circuitry and erase simultaneously
Clear:	Indicates a logic zero (0)
CUI:	Command User Interface
MLC:	Multi-Level Cell
OTP:	One Time Programmable
PLR:	Protection Lock Register
PR:	Protection Register
PRD	Protection Register Data
Program:	To write data to the flash array
RFU:	Reserved for Future Use
Set:	Indicates a logic one (1)
SR:	Status Register
SRD:	Status Register Data
VPEN:	Refers to a signal or package connection name
V_{PEN}:	Refers to timing or voltage levels
WSM:	Write State Machine
ECR:	Extended Configuration Register
XSR:	eXtended Status Register

1.2 Conventions

0x:	Hexadecimal prefix
0b:	Binary prefix
k (noun):	1,000
M (noun):	1,000,000
Nibble	4 bits
Byte:	8 bits
Word:	16 bits
Kword:	1,024 words
Kb:	1,024 bits
KB:	1,024 bytes
Mb:	1,048,576 bits
MB:	1,048,576 bytes
Brackets:	Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e., A[21:1], SR[4,1] and D[15:0]).

2.0 Functional Overview

The Intel StrataFlash® memory family contains high-density memories organized as 32 Mbytes or 16Mwords (256-Mbit, available on the 0.18µm lithography process only), 16 Mbytes or 8 Mwords (128-Mbit), 8 Mbytes or 4 Mwords (64-Mbit), and 4 Mbytes or 2 Mwords (32-Mbit). These devices can be accessed as 8- or 16-bit words. The 128-Mbit device is organized as one-hundred-twenty-eight 128-Kbyte (131,072 bytes) erase blocks. The 64-Mbit device is organized as sixty-four 128-Kbyte erase blocks while the 32-Mbit device contains thirty-two 128-Kbyte erase blocks. A 128-bit Protection Register has multiple uses, including unique flash device identification.

The device's optimized architecture and interface dramatically increases read performance by supporting page-mode reads. This read mode is ideal for non-clock memory systems.

A Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

Scalable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 128-Kbyte blocks typically within one second—independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block. Similarly, program suspend allows system software to suspend programming (byte/word program and write-to-buffer operations) to read data or execute code from any other block that is not being suspended.

Each device incorporates a Write Buffer of 32 bytes (16 words) to allow optimum programming performance. By using the Write Buffer, data is programmed in buffer increments. This feature can improve system program performance more than 20 times over non-Write Buffer writes.

Blocks are selectively and individually lockable in-system.Individual block locking uses block lock-bits to lock and unlock blocks. Block lock-bits gate block erase and program operations. Lock-bit configuration operations set and clear lock-bits (Set Block Lock-Bit and Clear Block Lock-Bits commands).

The Status Register indicates when the WSM's block erase, program, or lock-bit configuration operation is finished.

The STS (STATUS) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# signal. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is

suspended (and programming is inactive), program is suspended, or the device is in reset/power-down mode. Additionally, the configuration command allows the STS signal to be configured to pulse on completion of programming and/or block erases.

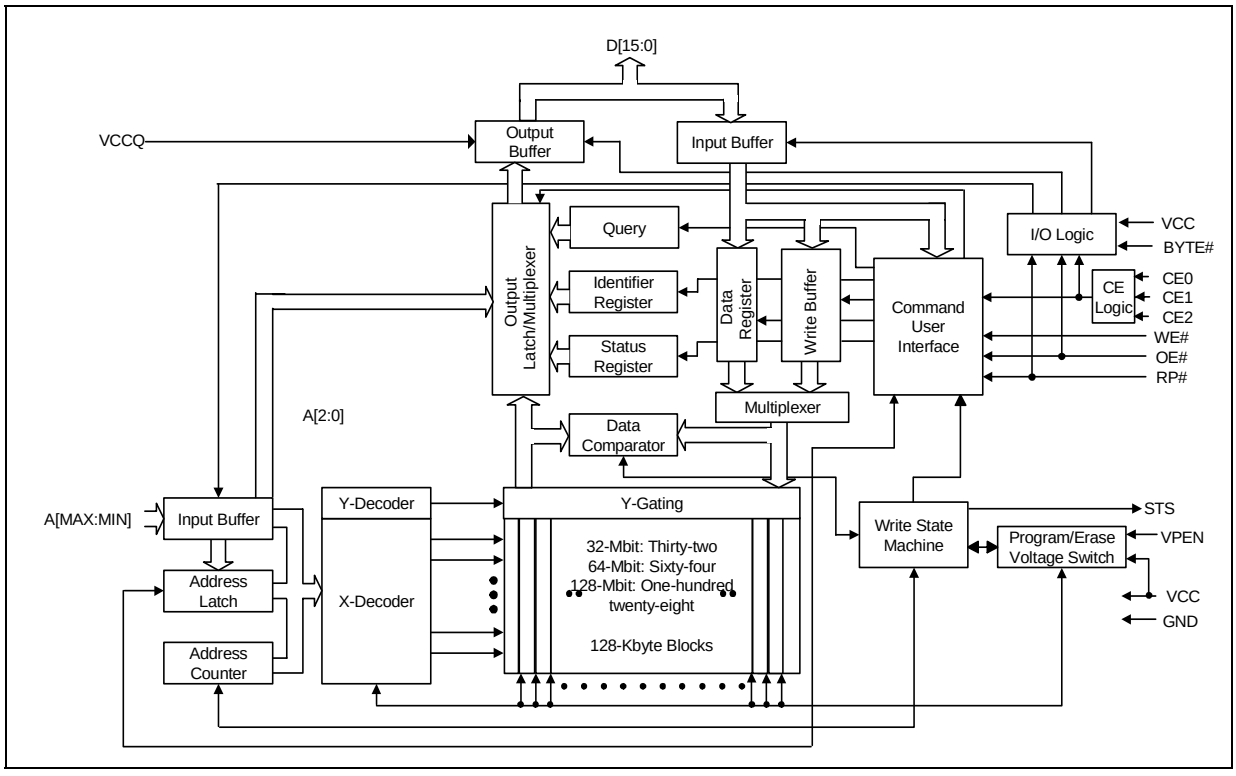
Three CE signals are used to enable and disable the device. A unique CE logic design (see Table 13, “Chip Enable Truth Table” on page 33) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# signal allows either x8 or x16 read/writes to the device. BYTE#-low selects 8-bit mode; address A0 selects between the low byte and high byte. BYTE#-high enables 16-bit operation; address A1 becomes the lowest order address and address A0 is not used (don’t care). A device block diagram is shown in Figure 4 on page 14.

When the device is disabled (see Table 13 on page 33), with CEx at V_{IH} and RP# at V_{IH}, the standby mode is enabled. When RP# is at V_{IL}, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# going high until data outputs are valid. Likewise, the device has a wake time (t_{PHWL}) from RP#-high until writes to the CUI are recognized. With RP# at V_{IL}, the WSM is reset and the Status Register is cleared.

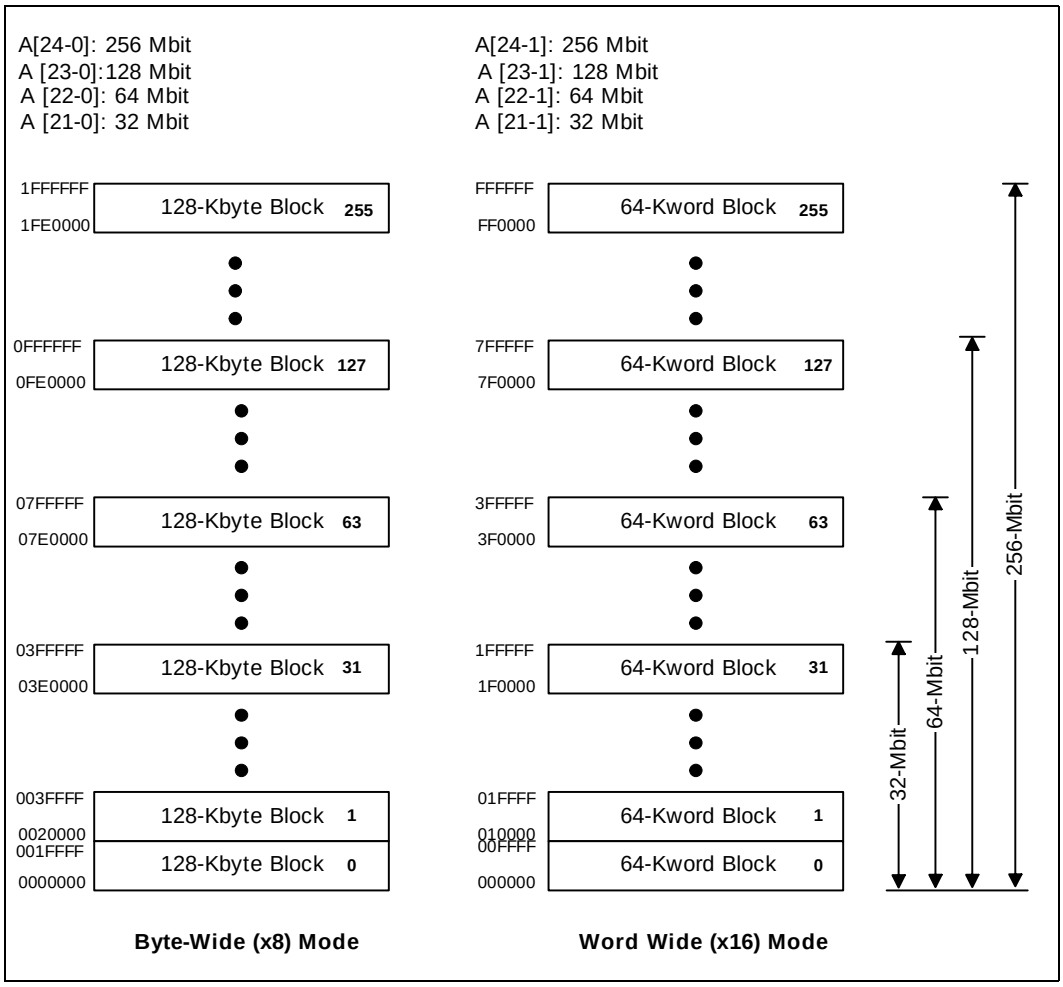
2.1 Block Diagram

Figure 1. 3 Volt Intel StrataFlash® Memory Block Diagram



2.2 Memory Map

Figure 2. Intel StrataFlash® Memory (J3) Memory Map



3.0 Package Information

3.1 56-Lead TSOP Package

Figure 3. 56-Lead TSOP Package Drawing and Specifications

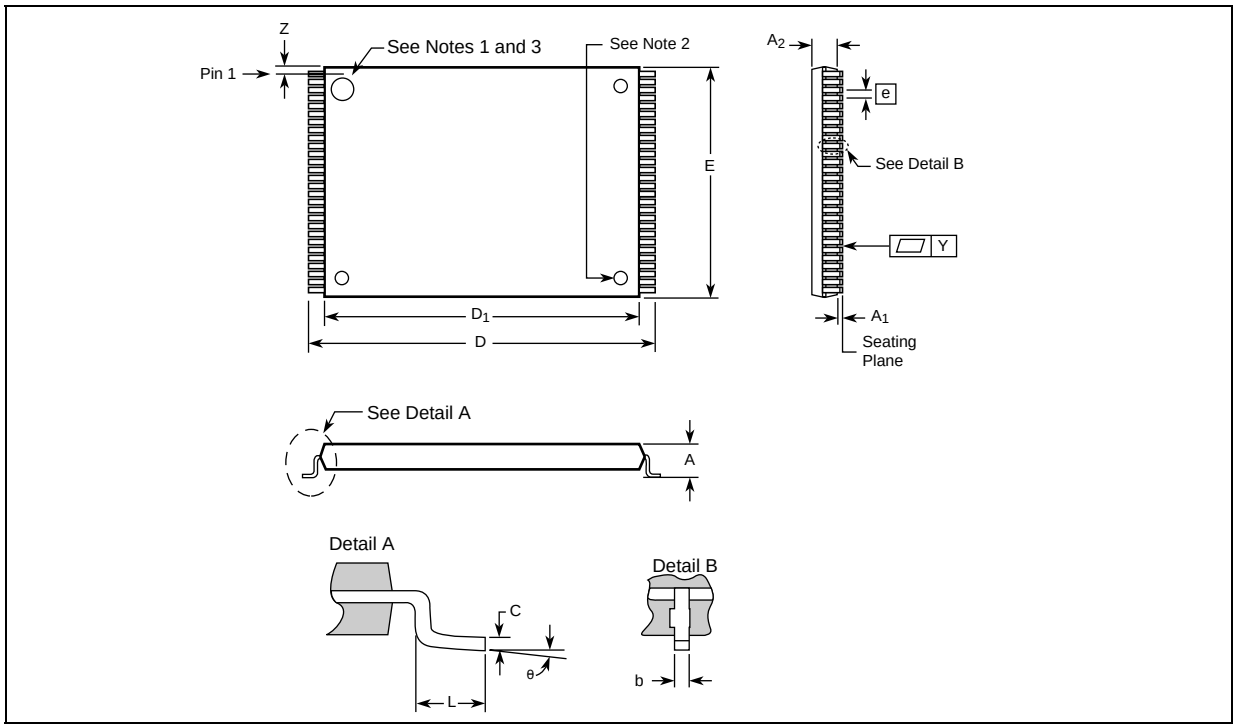


Table 1. 56-Lead TSOP Dimension Table

		Millimeters				Inches			
	Sym	Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A_1	0.050				0.002			
Package Body Thickness	A_2	0.965	0.995	1.025		0.038	0.039	0.040	
Lead Width	b	0.100	0.150	0.200		0.004	0.006	0.008	
Lead Thickness	c	0.100	0.150	0.200		0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	4
Package Body Width	E	13.800	14.000	14.200	4	0.543	0.551	0.559	4
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.00	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		56				56		
Lead Tip Angle	∅	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

3.2 Easy BGA (J3) Package

Figure 4. Intel StrataFlash® Memory (J3) Easy BGA Mechanical Specifications

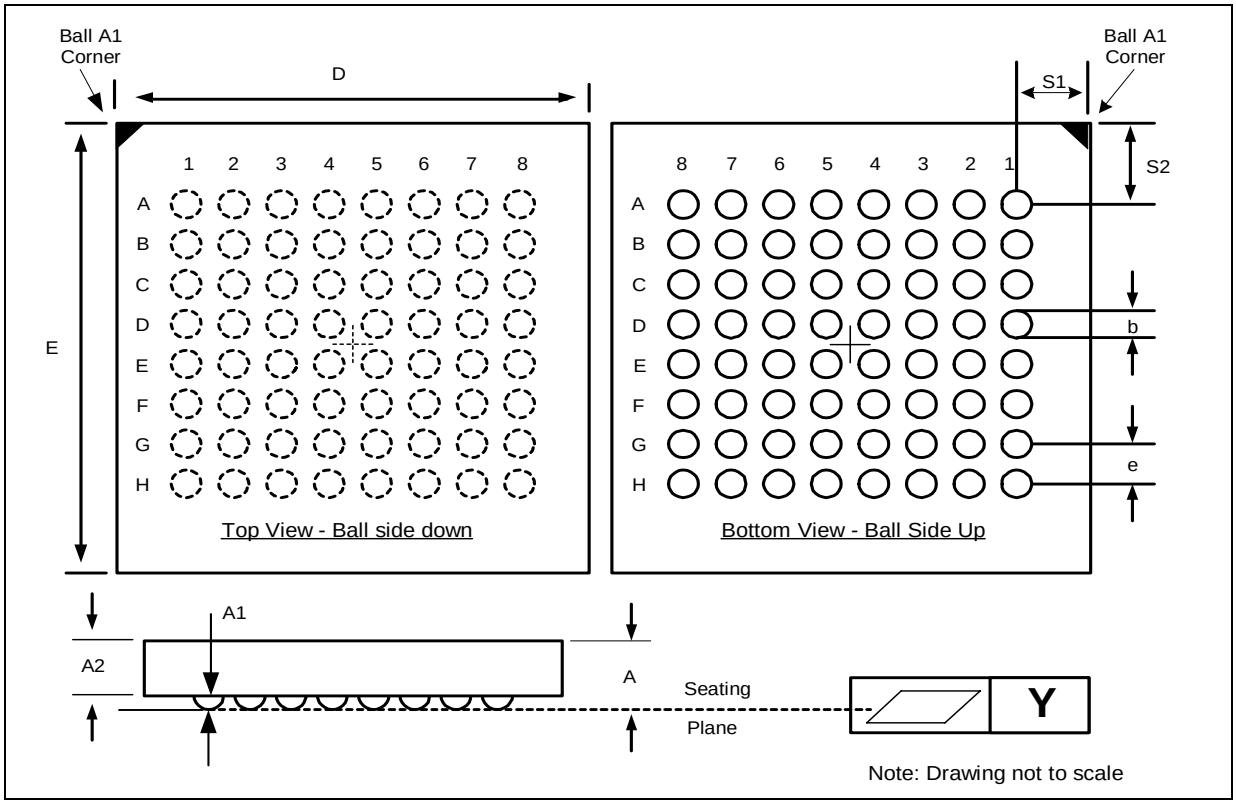


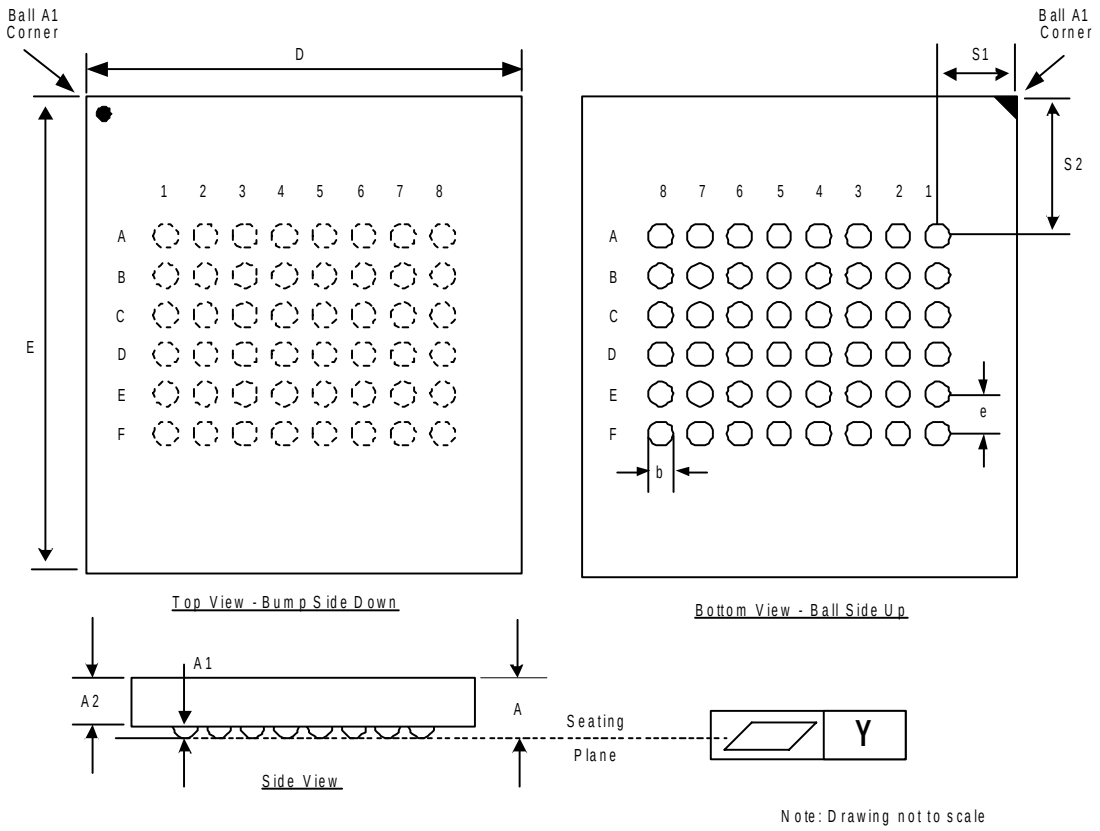
Table 2. Easy BGA Package Dimensions

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.250				0.0098		
Package Body Thickness	A2		0.780				0.0307	
Ball (Lead) Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209
Package Body Width (32 Mb, 64 Mb, 128 Mb, 256 Mb)	D	9.900	10.000	10.100	1	0.3898	0.3937	0.3976
Package Body Length (32 Mb, 64 Mb, 128 Mb)	E	12.900	13.000	13.100	1	0.5079	0.5118	0.5157
Package Body Length (256 Mb)	E	14.900	15.000	15.100	1	0.5866	0.5906	0.5945
Pitch	[e]		1.000				0.0394	
Ball (Lead) Count	N		64				64	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D (32/64/128/256 Mb)	S1	1.400	1.500	1.600	1	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E (32/64/128 Mb)	S2	2.900	3.000	3.100	1	0.1142	0.1181	0.1220
Corner to Ball A1 Distance Along E (256 Mb)	S2	3.900	4.000	4.100	1	0.1535	0.1575	0.1614

NOTES:
1. For Daisy Chain Evaluation Unit information refer to the Intel Flash Memory Packaging Technology Web page at; www.intel.com/design/packtech/index.htm
2. For Packaging Shipping Media information see www.intel.com/design/packtech/index.htm

3.3 VF-BGA (J3) Package

Figure 5. Intel StrataFlash® Memory (J3) VF BGA Mechanical Specifications



Dimensions Table

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.000				0.0394
Ball Height	A1	0.150				0.0059		
Package Body Thickness	A2		0.665				0.0262	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
	D	7.186	7.286	7.386	1	0.2829	0.2868	0.2908
Package Body Length	E	10.750	10.850	10.950	1	0.4232	0.4272	0.4311
Pitch	[e]		0.750				0.0295	
Ball (Lead) Count	N		48				48	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D	S1	0.918	1.018	1.118	1	0.0361	0.0401	0.0440
Corner to Ball A1 Distance Along E	S2	3.450	3.550	3.650	1	0.1358	0.1398	0.1437

Note: (1) Package dimensions are for reference only. These dimensions are estimates based on die size, and are subject to change.

NOTES:

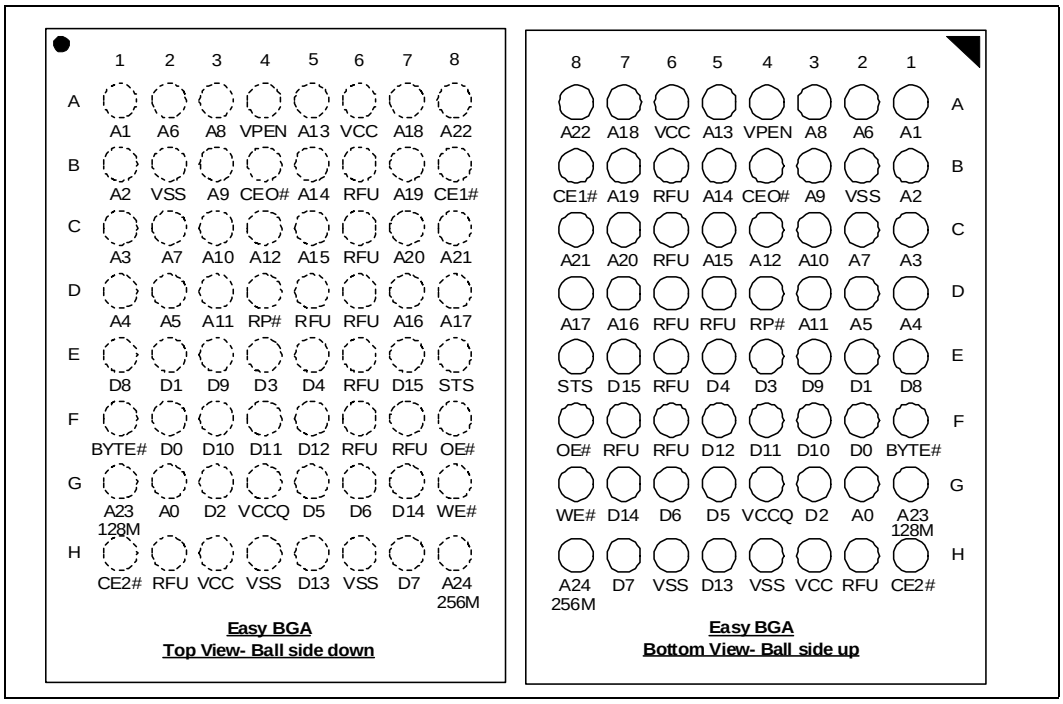
1. For Daisy Chain Evaluation Unit information refer to the Intel Flash Memory Packaging Technology Web page at; www.intel.com/design/packtech/index.htm
2. For Packaging Shipping Media information refer to the Intel Flash Memory Packaging Technology Web page at; www.intel.com/design/packtech/index.htm

4.0 Ballout and Signal Descriptions

Intel StrataFlash® memory is available in three package types. Each density of the J3C is supported on both 64-ball Easy BGA and 56-lead Thin Small Outline Package (TSOP) packages. A 48-ball VF BGA package is available on 32 and 64 Mbit devices. Figure 6, Figure 7, and Figure 8 show the pinouts.

4.1 Easy BGA Ballout (32/64/128/256 Mbit)

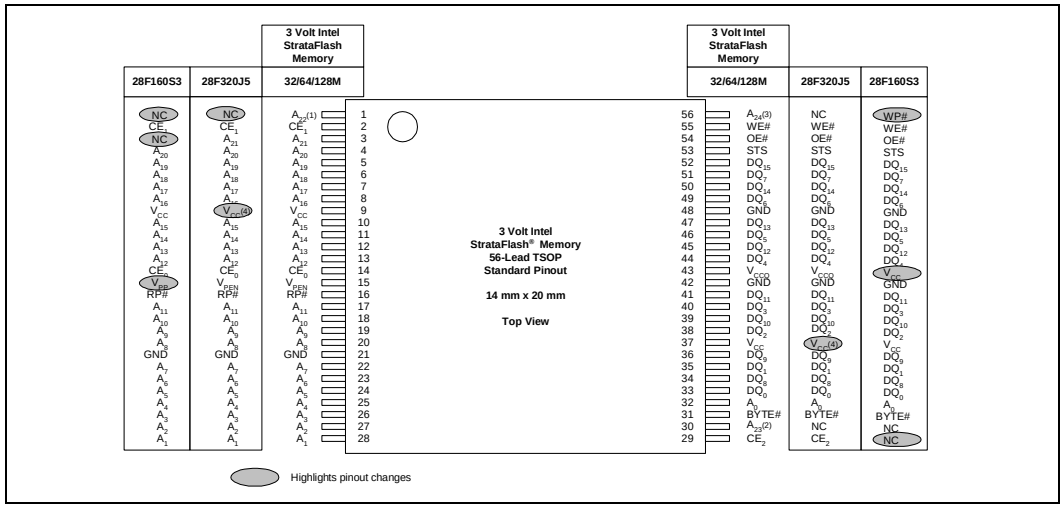
Figure 6. Intel StrataFlash® Memory Easy BGA Ballout (32/64/128/256 Mbit)



NOTES:
1. Address A22 is only valid on 64-Mbit densities and above, otherwise, it is a no connect (NC).
2. Address A23 is only valid on 128-Mbit densities and above, otherwise, it is a no connect (NC).
3. Address A24 is only valid on 256-Mbit densities and above, otherwise, it is a no connect (NC).

4.2 56-Lead TSOP (32/64/128/256 Mbit)

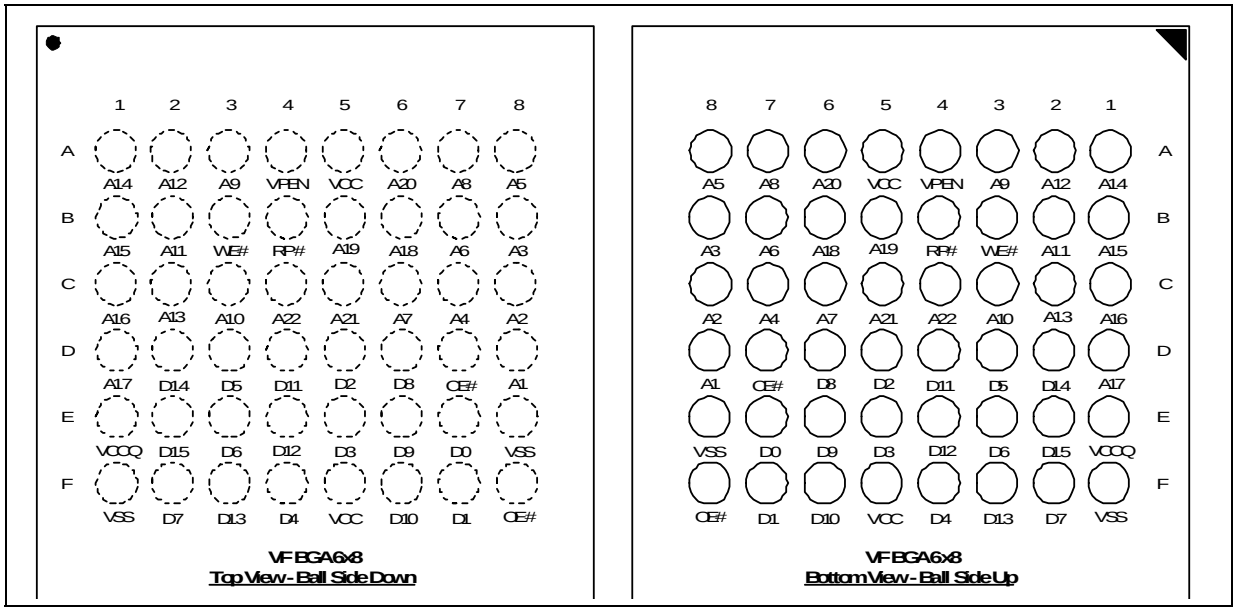
Figure 7. Intel StrataFlash® Memory 56-Lead TSOP (32/64/128/256 Mbit)



NOTES:
1. A22 exists on 64-, 128- and 256-Mbit densities. On 32-Mbit densities this signal is a no-connect (NC).
2. A23 exists on 128-Mbit densities. On 32- and 64-Mbit densities this signal is a no-connect (NC).
3. A24 exists on 256-Mbit densities. On 32-, 64- and 128-Mbit densities this signal is a no-connect (NC).
4. V_{CC} = 5 V ± 10% for the 28F640J5/28F320J5.

4.3 VF BGA Ballout (32 and 64 Mbit)

Figure 8. Intel StrataFlash® Memory VF BGA Ballout (32 and 64 Mbit)



NOTES:
1. CE# is equivalent to CE0, and CE1 and CE2 are internally grounded.
2. A22 exists on the 64 Mb density only. On the 32-Mbit density, this signal is a no-connect (NC).
3. STS not supported in this package.
4. x8 not supported in this package.

4.4 Signal Descriptions

Table 3 describes active signals used.

Table 3. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Name and Function
A0	Input	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[MAX:1]	Input	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle. 32-Mbit: A[21:0] 64-Mbit: A[22:0] 128-Mbit: A[23:0] 256-Mbit: A[24:0]
D[7:0]	Input/Output	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during write operations.
D[15:8]	Input/Output	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for Status Register reads. Data is internally latched during write operations in x16 mode. D[15-8] float in x8 mode
CE0, CE1, CE2	Input	**CHIP ENABLES:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 13 on page 33), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1, or CE2 that disables the device (see Table 13 on page 33).
RP#	Input	**RESET/ POWER-DOWN:** RP#-low resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	Input	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the CUI, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of WE#.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the STATUS signal, see the Configurations command. STS is to be tied to VCCQ with a pull-up resistor.
BYTE#	Input	**BYTE ENABLE:** BYTE#-low places the device in x8 mode; data is input or output on D[7:0], while D[15:8] is placed in High-Z. Address A0 selects between the high and low byte. BYTE#-high places the device in x16 mode, and turns off the A0 input buffer. Address A1 becomes the lowest-order address bit.
VPEN	Input	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
VCC	Power	**CORE POWER SUPPLY: Core (logic) source voltage. Writes to the flash array are inhibited when** $V_{CC} \le V_{LKO}$. Device operation at invalid Vcc voltages should not be attempted.
VCCQ	Power	**I/O POWER SUPPLY:** I/O Output-driver source voltage. This ball can be tied to V_{CC}.

Table 3. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Name and Function
GND	Supply	**GROUND:** Do not float any ground signals.
NC	—	**NO CONNECT:** Lead is not internally connected; it may be driven or floated.
RFU	—	**RESERVED** for **FUTURE USE:** Balls designated as RFU are reserved by Intel for future device functionality and enhancement**.**

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

This datasheet contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design. Absolute maximum ratings are shown in Table 4.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" **may cause permanent damage**. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Maximum Rating
Temperature under Bias Extended	–40 °C to +85 °C
Storage Temperature	–65 °C to +125 °C
Voltage On Any signal	–2.0 V to +5.0 V(1)
Output Short Circuit Current	100 mA(2)

NOTES:
1. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output signals and –0.2 V on V_{CC} and V_{PEN} signals. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output signals, V_{CC}, and V_{PEN} is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Table 5. Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A	Operating Temperature	–40	+85	°C	Ambient Temperature
V_{CC}	V_{CC1} Supply Voltage (2.7 V–3.6 V)	2.70	3.60	V	—
V_{CCQ}	V_{CCQ} Supply Voltage (2.7 V–3.6 V)	2.70	3.60	V	—

6.0 Electrical Specifications

6.1 DC Current Characteristics

Table 6. DC Current Characteristics (Sheet 1 of 2)

VCCQ			2.7 - 3.6V			Test Conditions	Notes
VCC			2.7 - 3.6V				
Symbol	Parameter		Typ	Max	Unit		
I_{LI}	Input and V_{PEN} Load Current			±1	µA	V_{CC} = V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or GND	1
I_{LO}	Output Leakage Current			±10	µA	V_{CC}= V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or GND	1
I_{CCS}	V_{CC} Standby Current		50	120	µA	CMOS Inputs, V_{CC} = V_{CC} Max, Device is disabled (see Table 13, “Chip Enable Truth Table” on page 33), RP# = V_{CCQ} ± 0.2 V	1,2,3
			0.71	2	mA	TTL Inputs, V_{CC} = V_{CC} Max, Device is disabled (see Table 13), RP# = V_{IH}	
I_{CCD}	V_{CC} Power-Down Current		50	120	µA	RP# = GND ± 0.2 V, I_{OUT} (STS) = 0 mA	
I_{CCR}	V_{CC} Page Mode Read Current	4-word Page	15	20	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 4 word page mode reads. Device is enabled (see Table 13) f = 5 MHz, I_{OUT} = 0 mA	1,3
			24	29	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 4 word page mode reads. Device is enabled (see Table 13) f = 33 MHz, I_{OUT} = 0 mA	
		8-word Page	10	15	mA	• CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. • Device is enabled (see Table 13) f = 5 MHz, I_{OUT} = 0 mA	
			30	54	mA	• CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. • Device is enabled (see Table 13) f = 33 MHz, I_{OUT} = 0 mA • Density: 128-, 64-, and 32- Mbit	
			26	46	mA	• CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. • Device is enabled (see Table 13) f = 33 MHz, I_{OUT} = 0 mA • Density: 256Mbit	
I_{CCW}	V_{CC} Program or Set Lock-Bit Current		35	60	mA	CMOS Inputs, V_{PEN} = V_{CC}	1,4
			40	70	mA	TTL Inputs, V_{PEN} = V_{CC}	

Table 6. DC Current Characteristics (Sheet 2 of 2)

VCCQ			2.7 - 3.6V			Test Conditions	Notes
VCC			2.7 - 3.6V				
Symbol	Parameter		Typ	Max	Unit		
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current		35	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$	1,4
			40	80	mA	TTL Inputs, $V_{PEN} = V_{CC}$	
I_{CCWS} I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current			10	mA	Device is enabled (see Table 13)	1,5

NOTES:
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
2. Includes STS.
3. CMOS inputs are either $V_{CC} \pm 0.2$ V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
4. Sampled, not 100% tested.
5. I_{CCWS} and I_{CCES} are specified with the device selected. If the device is read or written while in erase suspend mode, the device's current draw is I_{CCR} and I_{CCWS}

6.2 DC Voltage Characteristics

Table 7. DC Voltage Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions	Notes
V_{IL}	Input Low Voltage	–0.5	0.8	V		2, 6
V_{IH}	Input High Voltage	2.0	V_{CCQ} + 0.5	V		2,6
V_{OL}	Output Low Voltage		0.4	V	$V_{CCQ} = V_{CCQ}$ Min I_{OL} = 2 mA	1,2
			0.2	V	$V_{CCQ} = V_{CCQ}$ Min I_{OL} = 100 µA	
V_{OH}	Output High Voltage	0.85 × V_{CCQ}		V	$V_{CCQ} = V_{CCQ}$ Min I_{OH} = –2.5 mA	1,2
		V_{CCQ} – 0.2		V	$V_{CCQ} = V_{CCQ}$ Min I_{OH} = –100 µA	
V_{PENLK}	V_{PEN} Lockout during Program, Erase and Lock-Bit Operations		2.2	V		2,3,4,7

Table 7. DC Voltage Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions	Notes
V_{PENH}	V_{PEN} during Block Erase, Program, or Lock-Bit Operations	2.7	3.6	V		3,4
V_{LKO}	V_{CC} Lockout Voltage	2.0		V		5

NOTES:
1. Includes STS.
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when $V_{PEN} \leq V_{PENLK}$, and not guaranteed in the range between V_{PENLK} (max) and V_{PENH} (min), and above V_{PENH} (max).
4. Typically, V_{PEN} is connected to V_{CC} (2.7 V–3.6 V).
5. Block erases, programming, and lock-bit configurations are inhibited when $V_{CC} < V_{LKO}$, and not guaranteed in the range between V_{LKO} (min) and V_{CC} (min), and above V_{CC} (max).
6. Includes all operational modes of the device including standby and power-up sequences.
7. VCC operating condition for standby has to meet typical operationg coditons.

7.0 AC Characteristics

7.1 Read Operations

Table 8. Read Operations (Sheet 1 of 2)

Asynchronous Specifications (All units in ns unless otherwise noted)			V_{CC} = 2.7 V–3.6 V [3] V_{CCQ} = 2.7 V–3.6 V [3]											Notes
			Speed Bin	-110		-115		-120		-125		-150		
#	Sym	Parameter	Density	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
R1	t_{AVAV}	Read/Write Cycle Time	32 Mbit	110										1,2
			64 Mbit			115		120						1,2
			128 Mbit					120				150		1,2
			256 Mbit							125				1,2
R2	t_{AVQV}	Address to Output Delay	32 Mbit		110									1,2
			64 Mbit				115		120					1,2
			128 Mbit						120				150	1,2
			256 Mbit								125			1,2
R3	t_{ELQV}	CEx to Output Delay	32 Mbit		110									1,2
			64 Mbit				115		120					1,2
			128 Mbit						120				150	1,2
			256 Mbit								125			1,2
R4	t_{GLQV}	OE# to Non-Array Output Delay			50		50		50		50		50	1,2,4
R5	t_{PHQV}	RP# High to Output Delay	32 Mbit		150									1,2
			64 Mbit				180		180					1,2
			128 Mbit						210				210	1,2
			256 Mbit								210			
R6	t_{ELQX}	CEx to Output in Low Z		0		0		0		0		0		1,2,5
R7	t_{GLQX}	OE# to Output in Low Z		0		0		0		0		0		1,2,5
R8	t_{EHQZ}	CEx High to Output in High Z			35		35		35		35		35	1,2,5
R9	t_{GHQZ}	OE# High to Output in High Z			15		15		15		15		15	1,2,5
R10	t_{OH}	Output Hold from Address, CEx, or OE# Change, Whichever Occurs First		0		0		0		0		0		1,2,5
R11	t_{ELFL}/ t_{ELFH}	CEx Low to BYTE# High or Low			10		10		10		10		10	1,2,5

Table 8. Read Operations (Sheet 2 of 2)

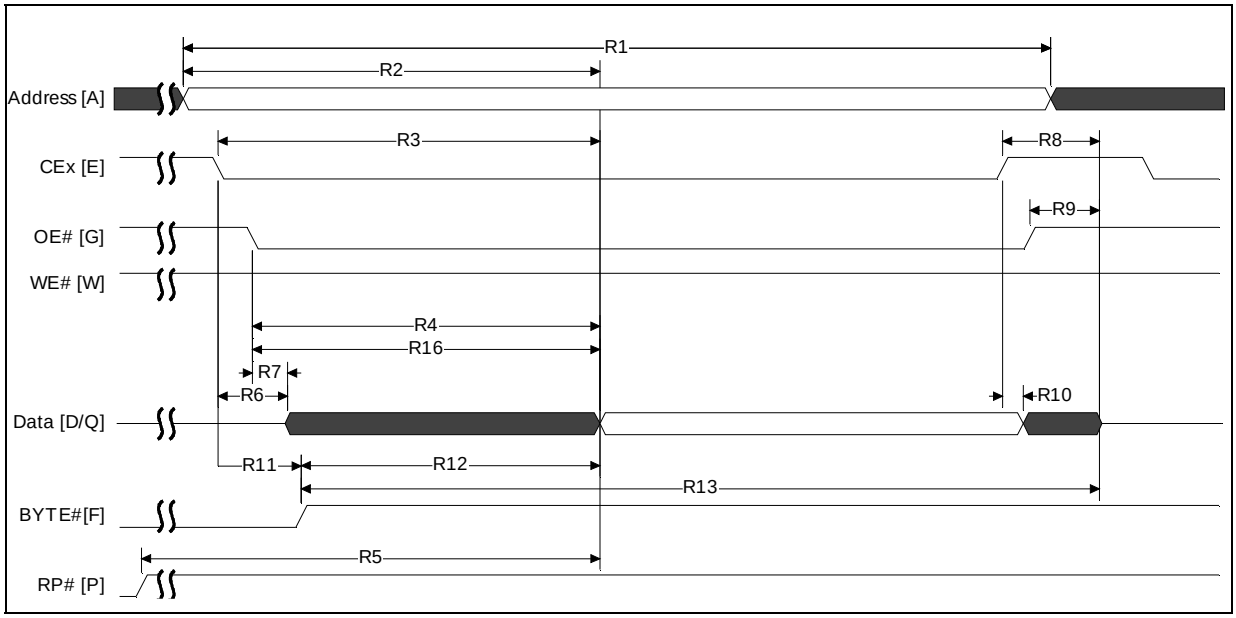
Asynchronous Specifications (All units in ns unless otherwise noted)			V_{CC} = 2.7 V–3.6 V (3) V_{CCQ} = 2.7 V–3.6 V (3)											Notes
			Speed Bin	-110		-115		-120		-125		-150		
#	Sym	Parameter	Density	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
R12	t_{FLQV}/ t_{FHQV}	BYTE# to Output Delay			1000		1000		1000		1000		1000	1,2
R13	t_{FLQZ}	BYTE# to Output in High Z			1000		1000		1000		1000		1000	1,2,5
R14	t_{EHEL}	CEx High to CEx Low		0		0		0		0		0		1,2,5
R15	t_{APA}	Page Address Access Time			25		25		25		30		25	5, 6
R16	t_{GLQV}	OE# to Array Output Delay			25		25		25		25		25	4

NOTES:

CE_X low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 13).

1. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the first edge of CE0, CE1, or CE2 that enables the device (see Table 13) without impact on t_{ELQV}.
3. See Figure 15, “Transient Input/Output Reference Waveform for VCCQ = 2.7 V–3.6 V” on page 29 and Figure 16, “Transient Equivalent Testing Load Circuit” on page 30 for testing characteristics.
4. When reading the flash array a faster t_{GLQV} (R16) applies. Non-array reads refer to Status Register reads, query reads, or device identifier reads.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R15 (t_{APA}) will equal R2 (t_{AVQV}).

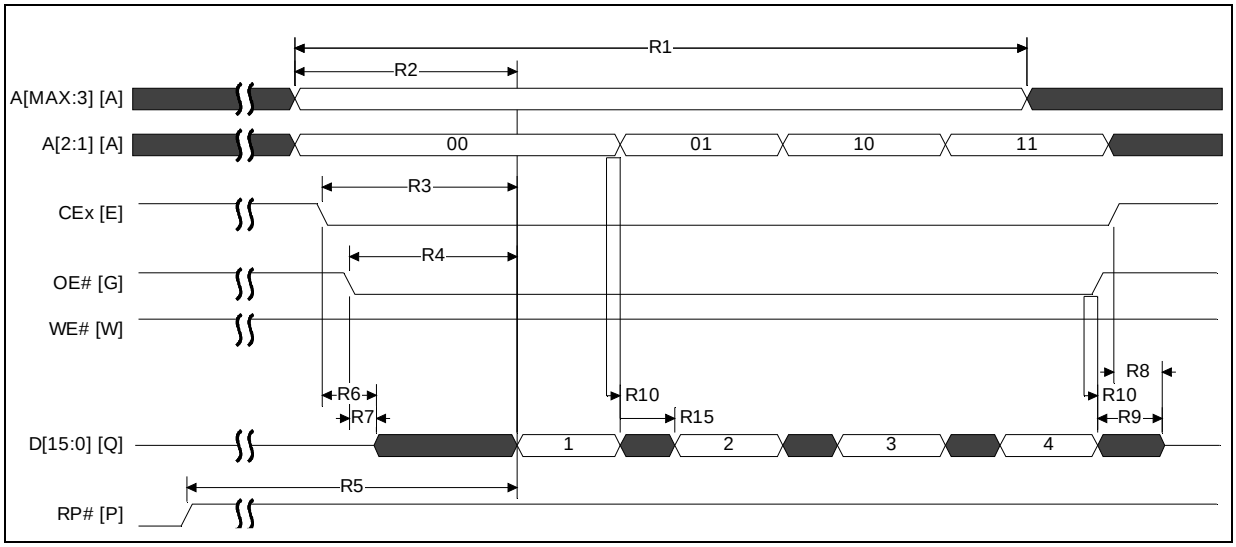
Figure 9. Single Word Asynchronous Read Waveform



0606_16

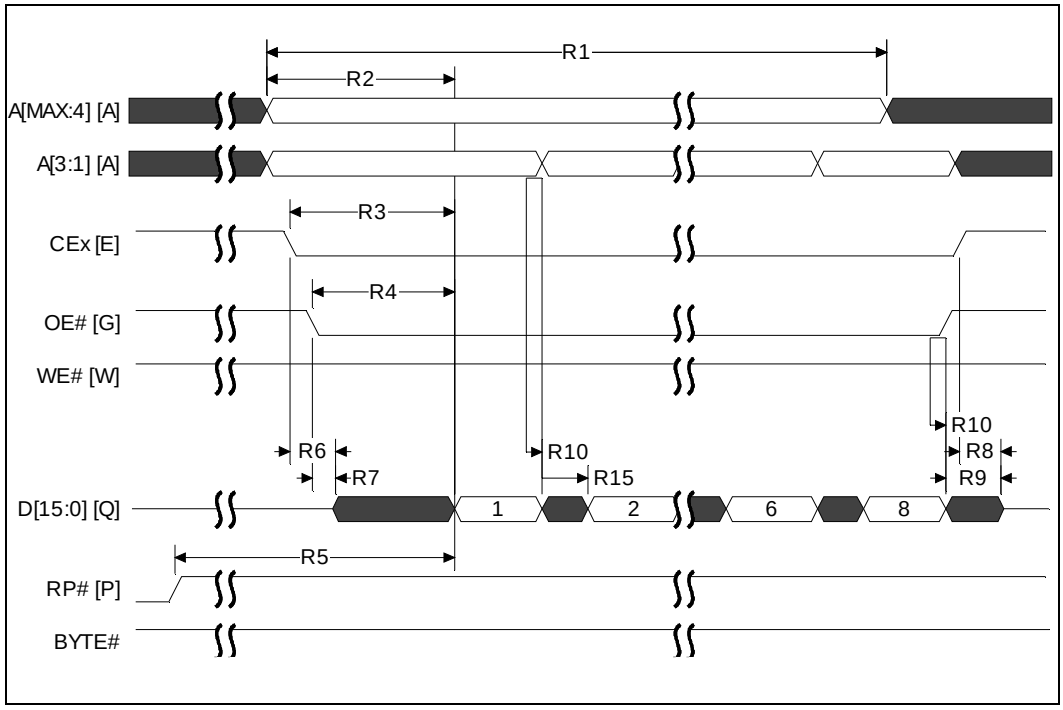
NOTES:
1. CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 13).
2. When reading the flash array a faster t_{GLQV} (R16) applies. For non-array reads, R4 applies (i.e.: Status Register reads, query reads, or device identifier reads).

Figure 10. 4-Word Page Mode Read Waveform



NOTE: CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 13).

Figure 11. 8-word Asynchronous Page Mode Read



NOTES:
1. CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 13).
2. In this diagram, BYTE# is asserted high.

7.2 Write Operations

Table 9. Write Operations

Versions			Valid for All Speeds		Unit	Notes
#	Symbol	Parameter	Min	Max		
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE_X) Going Low	1		µs	1,2,3
W2	t_{ELWL} (t_{WLEL})	CE_X (WE#) Low to WE# (CE_X) Going Low	0		ns	1,2,4
W3	t_{WP}	Write Pulse Width	70		ns	1,2,4
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE_X) Going High	50		ns	1,2,5
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE_X) Going High	55		ns	1,2,5
W6	t_{WHEH} (t_{EHWH})	CE_X (WE#) Hold from WE# (CE_X) High	0		ns	1,2,
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE_X) High	0		ns	1,2,
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE_X) High	0		ns	1,2,
W9	t_{WPH}	Write Pulse Width High	30		ns	1,2,6
W11	t_{VPWH} (t_{VPEH})	V_{PEN} Setup to WE# (CE_X) Going High	0		ns	1,2,3
W12	t_{WHGL} (t_{EHGL})	Write Recovery before Read	35		ns	1,2,7
W13	t_{WHRL} (t_{EHRL})	WE# (CE_X) High to STS Going Low		500	ns	1,2,8
W15	t_{QVVL}	V_{PEN} Hold from Valid SRD, STS Going High	0		ns	1,2,3,8,9

NOTES:

CE_X low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 13).

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to *AC Characteristics–Read-Only Operations*.
2. A write operation can be initiated and terminated with either CE_X or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from CE_X or WE# going low (whichever goes low last) to CE_X or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Refer to Table 14 for valid A_{IN} and D_{IN} for block erase, program, or lock-bit configuration.
6. Write pulse width high (t_{WPH}) is defined from CE_X or WE# going high (whichever goes high first) to CE_X or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
7. For array access, t_{AVQV} is required in addition to t_{WHGL} for any accesses after a write.
8. STS timings are based on STS configured in its RY/BY# default mode.
9. V_{PEN} should be held at V_{PENH} until determination of block erase, program, or lock-bit configuration success (SR[1,3,4:5] = 0).

7.3 Block Erase, Program, and Lock-Bit Configuration Performance

Table 10. Configuration Performance

#	Sym	Parameter	Typ	Max[8]	Unit	Notes
W16		Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)	218	654	µs	1,2,3,4,5,6,7
W16	t_{WHQV3} t_{EHQV3}	Byte Program Time (Using Word/Byte Program Command)	210	630	µs	1,2,3,4
		Block Program Time (Using Write to Buffer Command)	0.8	2.4	sec	1,2,3,4
W16	t_{WHQV4} t_{EHQV4}	Block Erase Time	1.0	5.0	sec	1,2,3,4
W16	t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	64	75/85	µs	1,2,3,4,9
W16	t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	0.5	0.70/1.4	sec	1,2,3,4,10
W16	t_{WHRH1} t_{EHRH1}	Program Suspend Latency Time to Read	25	75/90	µs	1,2,3,9
W16	t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read	26	35/40	µs	1,2,3,9

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical).
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical).
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles (except as noted).
9. Max values are expressed at -25 °C/-40 °C.
10. Max values are expressed at 25 °C/-40 °C.

Figure 12. Asynchronous Write Waveform

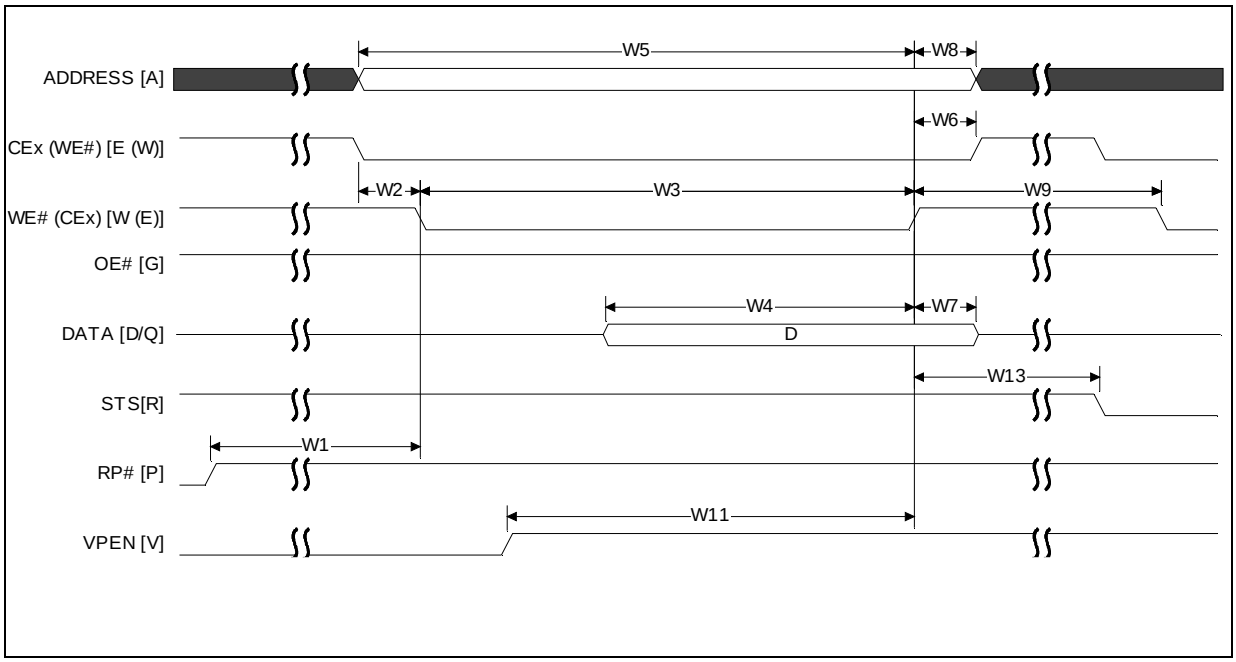
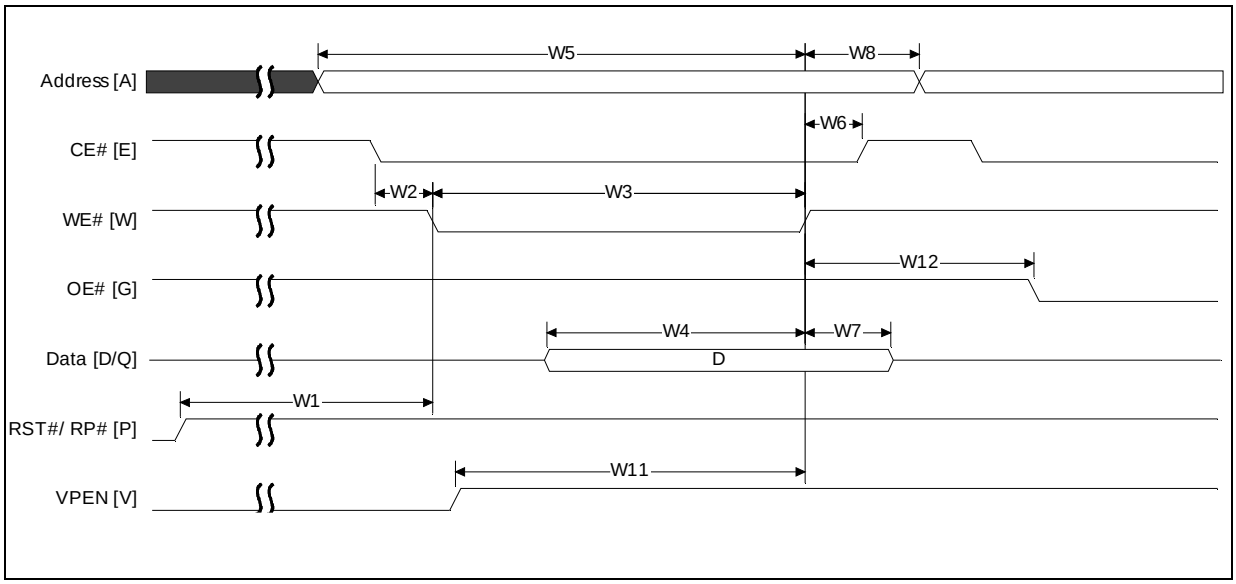
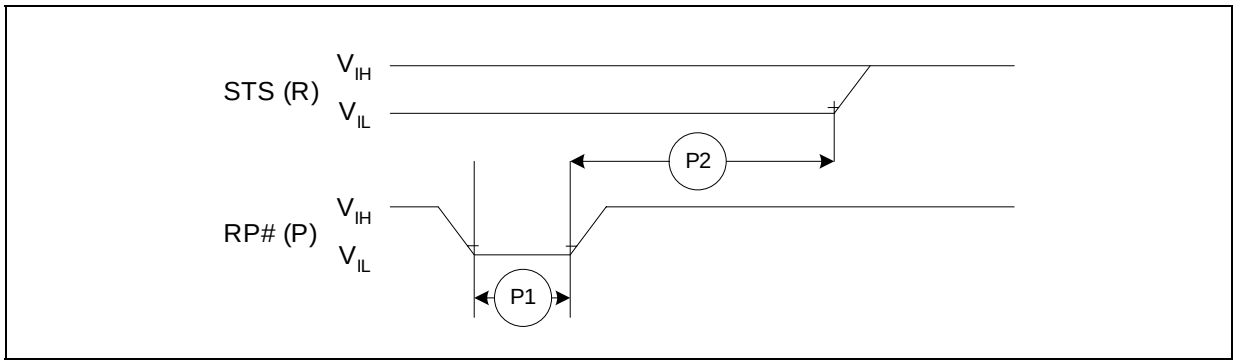


Figure 13. Asynchronous Write to Read Waveform



7.4 Reset Operation

Figure 14. AC Waveform for Reset Operation



NOTE: STS is shown in its default mode (RY/BY#).

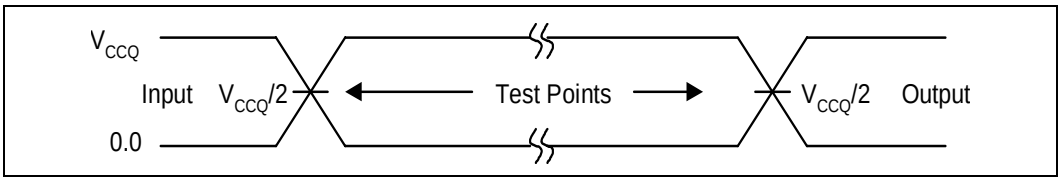
Table 11. Reset Specifications

#	Sym	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)	35		µs	1,2
P2	t_{PHRH}	RP# High to Reset during Block Erase, Program, or Lock-Bit Configuration		100	ns	1,3

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, program, or lock-bit configuration operation is not executing then the minimum required RP# Pulse Low Time is 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of STS (in RY/BY# mode) or RP# going high until outputs are valid.

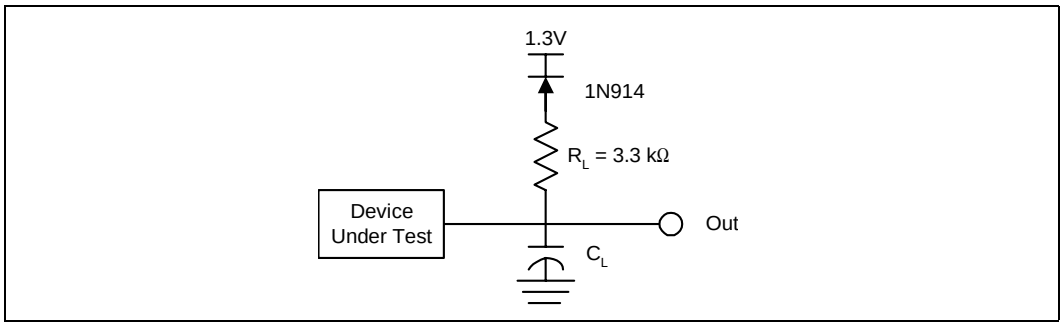
7.5 AC Test Conditions

Figure 15. Transient Input/Output Reference Waveform for V_{CCQ} = 2.7 V–3.6 V



NOTE: AC test inputs are driven at V_{CCQ} for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$ V (50% of V_{CCQ}). Input rise and fall times (10% to 90%) < 5 ns.

Figure 16. Transient Equivalent Testing Load Circuit



NOTE: C_L Includes Jig Capacitance.

Test Configuration	C_L (pF)
$V_{CCQ} = V_{CC}$ = 2.7 V–3.6 V	30

7.6 Capacitance

T_A = +25 °C, f = 1 MHz

Symbol	Parameter[1]	Type	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

NOTES:
1. Sampled, not 100% tested.

8.0 Power and Reset Specifications

This section provides an overview of system level considerations for the Intel StrataFlash® memory family device. This section provides a brief description of power-up, power-down, decoupling and reset design considerations.

8.1 Power-Up/Down Characteristics

In order to prevent any condition that may result in a spurious write or erase operation, it is recommended to power-up and power-down VCC and VCCQ together. It is also recommended to power-up VPEN with or slightly after VCC. Conversely, VPEN must power down with or slightly before VCC.

8.2 Power Supply Decoupling

When the device is enabled, many internal conditions change. Circuits are energized, charge pumps are switched on, and internal voltage nodes are ramped. All of this internal activities produce transient signals. The magnitude of the transient signals depends on the device and system loading. To minimize the effect of these transient signals, a 0.1 µF ceramic capacitor is required across each VCC/VSS and VCCQ signal. Capacitors should be placed as close as possible to device connections.

Additionally, for every eight flash devices, a 4.7 µF electrolytic capacitor should be placed between VCC and VSS at the power supply connection. This 4.7 µF capacitor should help overcome voltage slumps caused by PCB (printed circuit board) trace inductance.

8.3 Reset Characteristics

By holding the flash device in reset during power-up and power-down transitions, invalid bus conditions may be masked. The flash device enters reset mode when RP# is driven low. In reset, internal flash circuitry is disabled and outputs are placed in a high-impedance state. After return from reset, a certain amount of time is required before the flash device is able to perform normal operations. After return from reset, the flash device defaults to asynchronous page mode. If RP# is driven low during a program or erase operation, the program or erase operation will be aborted and the memory contents at the aborted block or address are no longer valid. See Figure 14, “AC Waveform for Reset Operation” on page 29 for detailed information regarding reset timings.

9.0 Bus Operations

This section provides an overview of device bus operations. The on-chip Write State Machine (WSM) manages all erase and program algorithms. The system CPU provides control of all in-system read, write, and erase operations of the device via the system bus.

Device commands are written to the CUI to control all of the flash memory device's operations. The CUI does not occupy an addressable memory location; it's the mechanism through which the flash device is controlled.

9.1 Bus Operations Overview

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Table 12. Bus Operations

Mode	RP#	CE[2:0][1]	OE#[2]	WE#[2]	Address	VPEN	Data[3]	STS (default mode)	Notes
Read Array	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}	High Z[7]	4,5,6
Output Disable	V_{IH}	Enabled	V_{IH}	V_{IH}	X	X	High Z	X	
Standby	V_{IH}	Disabled	X	X	X	X	High Z	X	
Reset/Power-Down Mode	V_{IL}	X	X	X	X	X	High Z	High Z[7]	
Read Identifier Codes	V_{IH}	Enabled	V_{IL}	V_{IH}	See Table 17	X	Note 8	High Z[7]	
Read Query	V_{IH}	Enabled	V_{IL}	V_{IH}	See Table 10.3	X	Note 9	High Z[7]	
Read Status (WSM off)	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}		
Read Status (WSM on)	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D7 = D_{OUT} D[15:8] = High Z D[6:0] = High Z		
Write	V_{IH}	Enabled	V_{IH}	V_{IL}	X	V_{PENH}	D_{IN}	X	6,10,11

NOTES:
1. See Table 13 on page 33 for valid CE configurations.
2. OE# and WE# should never be enabled simultaneously.
3. D refers to D[7:0] if BYTE# is low and D[15:0] if BYTE# is high.
4. Refer to *DC Characteristics*. When $V_{PEN} \le V_{PENLK}$, memory contents can be read, but not altered.
5. X can be V_{IL} or V_{IH} for control and address signals, and V_{PENLK} or V_{PENH} for V_{PEN}. See *DC Characteristics* for V_{PENLK} and V_{PENH} voltages.
6. In default mode, STS is V_{OL} when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is V_{OH} when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset/power-down mode.
7. High Z will be V_{OH} with an external pull-up resistor.
8. See Section 10.2, "Read Identifier Codes" on page 39 for read identifier code data.
9. See Section 10.3, "Read Query/CFI" on page 41 for read query data.
10. Command writes involving block erase, program, or lock-bit configuration are reliably executed when $V_{PEN} = V_{PENH}$ and V_{CC} is within specification.

Table 13. Chip Enable Truth Table

CE2	CE1	CE0	DEVICE
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

NOTE: For single-chip applications, CE2 and CE1 can be connected to V_{IL}.

9.1.1 Bus Read Operation

To perform a bus read operation, CEx (refer to Table 13 on page 33) and OE# must be asserted. CEx is the device-select control; when active, it enables the flash memory device. OE# is the data-output control; when active, the addressed flash memory data is driven onto the I/O bus. For all read states, WE# and RP# must be de-asserted. See Section 7.1, “Read Operations” on page 22. Refer to Section 10.0, “Read Operations” on page 37 for details on reading from the flash array, and refer to Section 14.0, “Special Modes” on page 50 for details regarding all other available read states.

9.1.2 Bus Write Operation

Writing commands to the Command User Interface enables various modes of operation, including the reading of array data, CFI data, identifier codes, inspection and clearing of the Status Register, and, when $V_{PEN} = V_{PENH}$, block erasure, program, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and block within the device to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when the device is enabled and WE# is active. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CE0, CE1, or CE2 that disables the device (see Table 13 on page 33). Standard microprocessor write timings are used.

9.1.3 Output Disable

With CEx asserted, and OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output signals D[15:0] are placed in a high-impedance state.

9.1.4 Standby

CE0, CE1, and CE2 can disable the device (see Table 13 on page 33) and place it in standby mode. This manipulation of CEx substantially reduces device power consumption. D[15:0] outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, program, or lock-bit configuration, the WSM continues functioning, and consuming active power until the operation completes.

9.1.5 Reset/Power-Down

RP# at V_{IL} initiates the reset/power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off numerous internal circuits. RP# must be held low for a minimum of t_{PLPH}. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and Status Register is set to 0x80.

During block erase, program, or lock-bit configuration modes, RP#-low will abort the operation. In default mode, STS transitions low and remains low for a maximum time of $t_{PLPH} + t_{PHRH}$ until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a program or partially altered after an erase or lock-bit configuration. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, program, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Intel StrataFlash® memory family devices allow proper initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

9.2 Device Commands

When the V_{PEN} voltage ≤ V_{PENLK}, only read operations from the Status Register, CFI, identifier codes, or blocks are enabled. Placing V_{PENH} on V_{PEN} additionally enables block erase, program, and lock-bit configuration operations. Device operations are selected by writing specific commands into the CUI. Table 14, "Command Bus-Cycle Definitions" on page 35 defines these commands.

Table 14. Command Bus-Cycle Definitions (Sheet 1 of 2)

Command	Scalable or Basic Command Set[2]	Bus Cycles Req'd.	First Bus Cycle			Second Bus Cycle			Notes
			Oper[3]	Addr[4]	Data[5,6]	Oper[3]	Addr[4]	Data[5,6]	
Read Array	SCS/BCS	1	Write	X	0xFF				1
Read Identifier Codes	SCS/BCS	≥ 2	Write	X	0X90	Read	IA	ID	1,7
Read Query	SCS	≥ 2	Write	X	0x98	Read	QA	QD	1
Read Status Register	SCS/BCS	2	Write	X	0x70	Read	X	SRD	1,8
Clear Status Register	SCS/BCS	1	Write	X	0x50				1
Write to Buffer	SCS/BCS	> 2	Write	BA	0xE8	Write	BA	N	1,9, 10, 11
Word/Byte Program	SCS/BCS	2	Write	X	0x40 or 0x10	Write	PA	PD	1,12,13
Block Erase	SCS/BCS	2	Write	BA	0x20	Write	BA	0xD0	1,11,12
Block Erase, Program Suspend	SCS/BCS	1	Write	X	0xB0				1,12,14
Block Erase, Program Resume	SCS/BCS	1	Write	X	0xD0				1,12
Configuration	SCS	2	Write	X	0xB8	Write	X	CC	1
Set Block Lock-Bit	SCS	2	Write	X	0x60	Write	BA	0x01	1

Table 14. Command Bus-Cycle Definitions (Sheet 2 of 2)

Command	Scalable or Basic Command Set[2]	Bus Cycles Req'd.	First Bus Cycle			Second Bus Cycle			Notes
			Oper[3]	Addr[4]	Data[5,6]	Oper[3]	Addr[4]	Data[5,6]	
Clear Block Lock-Bits	SCS	2	Write	X	0x60	Write	X	0xD0	1,15
Protection Program		2	Write	X	0xC0	Write	PA	PD	1

NOTES:

1. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.
2. The Basic Command Set (BCS) is the same as the 28F008SA Command Set or Intel Standard Command Set. The Scalable Command Set (SCS) is also referred to as the Intel Extended Command Set.
3. Bus operations are defined in Table 12.
4. X = Any valid address within the device.
   BA = Address within the block.
   IA = Identifier Code Address: see Table 17.
   QA = Query database Address.
   PA = Address of memory location to be programmed.
   RCD = Data to be written to the read configuration register. This data is presented to the device on A[16:1]; all other address inputs are ignored.
5. ID = Data read from Identifier Codes.
   QD = Data read from Query database.
   SRD = Data read from Status Register. See Table 18 for a description of the Status Register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.
   CC = Configuration Code.
6. The upper byte of the data bus (D[15:8]) during command writes is a "Don't Care" in x16 operation.
7. Following the Read Identifier Codes command, read operations access manufacturer, device and block lock codes. See Section 10.2 for read identifier code data.
8. If the WSM is running, only D7 is valid; D[15:8] and D[6:0] float, which places them in a high-impedance state.
9. After the Write to Buffer command is issued check the XSR to make sure a buffer is available for writing.
10. The number of bytes/words to be written to the Write Buffer = N + 1, where N = byte/word count argument. Count ranges on this device for byte mode are N = 00H to N = 1FH and for word mode are N = 0x00 to N = 0x0F. The third and consecutive bus cycles, as determined by N, are for writing data into the Write Buffer. The Confirm command (0xD0) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. See Figure 18, "Write to Buffer Flowchart" on page 59 for additional information
11. The write to buffer or erase operation does not begin until a Confirm command (0xD0) is issued.
12. Attempts to issue a block erase or program to a locked block.
13. Either 0x40 or 0x10 are recognized by the WSM as the byte/word program setup.
14. Program suspends can be issued after either the Write-to-Buffer or Word/Byte-Program operation is initiated.
15. The clear block lock-bits operation simultaneously clears all block lock-bits.

10.0 Read Operations

The device supports four types of read modes: Read Array, Read Identifier, Read Status, and CFI query. Upon power-up or return from reset, the device defaults to read array mode. To change the device's read mode, the appropriate read-mode command must be written to the device. (See Section 9.2, "Device Commands" on page 35.) See Section 14.0, "Special Modes" on page 50 for details regarding read status, read ID, and CFI query modes.

Upon initial device power-up or after exit from reset/power-down mode, the device automatically resets to read array mode. Otherwise, write the appropriate read mode command (Read Array, Read Query, Read Identifier Codes, or Read Status Register) to the CUI. Six control signals dictate the data flow in and out of the component: CE0, CE1, CE2, OE#, WE#, and RP#. The device must be enabled (see Table 13, "Chip Enable Truth Table" on page 33), and OE# must be driven active to obtain data at the outputs. CE0, CE1, and CE2 are the device selection controls and, when enabled (see Table 13), select the memory device. OE# is the data output (D[15:0]) control and, when active, drives the selected memory data onto the I/O bus. WE# must be at V_{IH}.

10.1 Read Array

Upon initial device power-up and after exit from reset/power-down mode, the device defaults to read array mode. The device defaults to four-word asynchronous read page mode. The Read Array command also causes the device to enter read array mode. The device remains enabled for reads until another command is written. If the internal WSM has started a block erase, program, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase or Program Suspend command. The Read Array command functions independently of the V_{PEN} voltage.

10.1.1 Asynchronous Page Mode Read

There are two Asynchronous Page mode configurations that are available depending on the user's system design requirements:

- Four-Word Page mode: This is the default mode on power-up or reset. Array data can be sensed up to four words (8 Bytes) at a time.
- Eight-Word Page mode: Array data can be sensed up to eight words (16 Bytes) at a time. This mode must be enabled on power-up or reset by using the command sequence found in Table 14, "Command Bus-Cycle Definitions" on page 35. Address bits A[3:1] determine which word is output during a read operation, and A[3:0] determine which byte is output for a x8 bus width.

After the initial access delay, the first word out of the page buffer corresponds to the initial address. In Four-Word Page mode, address bits A[2:1] determine which word is output from the page buffer for a x16 bus width, and A[2:0] determine which byte is output from the page buffer for a x8 bus width. Subsequent reads from the device come from the page buffer. These reads are output on D[15:0] for a x16 bus width and D[7:0] for a x8 bus width after a minimum delay as long as A[2:0] (Four-Word Page mode) or A[3:0] (Eight-Word Page mode) are the only address bits that change.

Data can be read from the page buffer multiple times, and in any order. In Four-Word Page Mode, if address bits A[MAX:3] (A[MAX:4] for Eight-Word Page Mode) change at any time, or if CE# is toggled, the device will sense and load new data into the page buffer. Asynchronous Page Mode is the default read mode on power-up or reset.

To perform a page mode read after any other operation, the Read Array command must be issued to read from the flash array. Asynchronous page mode reads are permitted in all blocks and are used to access register information. During register access, only one word is loaded into the page buffer.

10.1.2 Enhanced Configuration Register (ECR)

The Enhanced Configuration Register (ECR) is a volatile storage register that when addressed to by the Set Enhanced Configuration Register command, and can select between Four-Word Page mode and Eight-Word Page mode. The ECR is volatile; all bits will be reset to default values when RP# is deasserted or power is removed from the device. To modify ECR settings, use the Set Enhanced Configuration Register command. The Set Enhanced Configuration Register command is written along with the configuration register value, which is placed on the lower 16 bits of the address bus A[15:0]. This is followed by a second write that confirms the operation and again presents the enhanced configuration register data on the address bus. After executing this command, the device returns to Read Array mode. The ECR is shown in Table 15, “Enhanced Configuration Register” on page 38.

Note: For forward compatibility reasons, if the 8-word Asynchronous Page mode is to be used on J3C, a Clear Status Register command must be issued after issuing the Set Enhanced Configuration Register command. See Table 16, “J3C Asynchronous 8-Word Page Mode Command Bus-Cycle Definition” on page 38 for further details.

Table 15. Enhanced Configuration Register

Res.		Reserved													
R	R	8W	R	R	R	R	R	R	R	R	R	R	R	R	R
ECR .15	ECR .14	ECR .13	ECR .12	ECR .11	ECR .10	ECR .9	ECR .8	ECR .7	ECR .6	ECR .5	ECR .4	ECR .3	ECR .2	ECR .1	ECR .0

BITS	DESCRIPTION	NOTES
ECR[15:14]	Reserved	Reserved for Future Use. Set to 0 until further notice.
ECR[13]	• “1” = 8Word Page mode • “0” = 4Word Page mode	
ECR[12:0]	Reserved	Reserved for Future Use. Set to 0 until further notice.

NOTE: Any reserved bits should be set to 0.

Table 16. J3C Asynchronous 8-Word Page Mode Command Bus-Cycle Definition

Command	Bus Cycles Req'd.	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
		Oper	Addr(1)	Data	Oper	Addr(1)	Data	Oper	Addr(1)	Data
Set Enhanced Configuration Register (Set ECR)	3	Write	ECD	0x60	Write	ECD	0x04	Write	X	0x50

NOTE: X = Any valid address within the device. ECD = Enhanced Configuration Register Data.

10.2 Read Identifier Codes

The Read identifier codes operation outputs the manufacturer code, device-code, and the block lock configuration codes for each block (See Section 9.2, “Device Commands” on page 35 for details on issuing the Read Device Identifier command). Page-mode reads are not supported in this read mode. To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PEN} voltage. This command is valid only when the WSM is off or the device is suspended. Following the Read Identifier Codes command, the following information can be read.

Table 17. Read Identifier Codes

Code		Address[1]	Data
Manufacture Code		00000	(00) 89
Device Code	32-Mbit	00001	(00) 16
	64-Mbit	00001	(00) 17
	128-Mbit	00001	(00) 18
	256-Mbit	00001	(00) 1D
Block Lock Configuration		X0002[2]	
• Block Is Unlocked			D0 = 0
• Block Is Locked			D0 = 1
• Reserved for Future Use			D[7:1]

NOTES:
1. A0 is not used in either x8 or x16 modes when obtaining the identifier codes. The lowest order address line is A1. Data is always presented on the low byte in x16 mode (upper byte contains 00h).
2. X selects the specific block’s lock configuration code.
3. D[7:1] are invalid and should be ignored.

10.2.1 Read Status Register

The Status Register may be read to determine when a block erase, program, or lock-bit configuration is complete and whether the operation completed successfully. It may be read only after the specified time W12 (see Table 9, “Write Operations” on page 26). After writing this command, all subsequent read operations output data from the Status Register until another valid command is written. Page-mode reads are not supported in this read mode. The Status Register contents are latched on the falling edge of OE# or the first edge of CE0, CE1, or CE2 that enables the device (see Table 13, “Chip Enable Truth Table” on page 33). OE# must toggle to V_{IH} or the device must be disabled before further reads to update the Status Register latch. The Read Status Register command functions independently of the V_{PEN} voltage.

During a program, block erase, set lock-bit, or clear lock-bit command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O signals D[6:0] and D[15:8] are placed in a high-impedance state. When the operation completes or suspends (check SR.7), all contents of the Status Register are valid when read.

Table 18. Status Register Definitions

WSMS	ESS	ECLBS	PSLBS	VPENS	PSS	DPS	R
bit 7	bit 6	bit 5	bit 4	bit 3	bit2	bit 1	bit 0
High Z When Busy?	Status Register Bits				Notes		
No	SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy				Check STS or SR.7 to determine block erase, program, or lock-bit configuration completion. SR[6:0] are not driven while SR.7 = “0.”		
Yes	SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed						
Yes	SR.5 = ERASE AND CLEAR LOCK-BITSSTATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits				If both SR.5 and SR.4 are “1”s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.		
Yes	SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Program Error / Error in Setting Lock-Bit 0 = Successful Program/Set Block Lock Bit						
Yes	SR.3 = PROGRAMMING VOLTAGE STATUS 1 = Low Programming Voltage Detected, Operation Aborted 0 = Programming Voltage OK				SR.3 does not provide a continuous programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Program, Set Block Lock-Bit, or Clear Block Lock-Bits command sequences.		
Yes	SR.2 = PROGRAM SUSPEND STATUS 1 = Program suspended 0 = Program in progress/completed						
Yes	SR.1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit Detected, Operation Abort 0 = Unlock				SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bits only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set. Read the block lock configuration codes using the Read Identifier Codes command to determine block lock-bit status.		
Yes	SR0 = RESERVED FOR FUTURE ENHANCEMENTS				SR0 is reserved for future use and should be masked when polling the Status Register.		

Table 19. Extended Status Register Definitions

WBS	Reserved	
bit 7	Bits 6 -- 0	
High Z When Busy?	Status Register Bits	Notes
No	XSR.7 = WRITE BUFFER STATUS 1 = Write buffer available 0 = Write buffer not available	After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.
Yes	XSR.6–XSR0 = RESERVED FOR FUTURE ENHANCEMENTS	SR[6:0] are reserved for future use and should be masked when polling the Status Register.

10.3 Read Query/CFI

The query register contains an assortment of flash product information such as block size, density, allowable command sets, electrical specifications and other product information. The data contained in this register conforms to the Common Flash Interface (CFI) protocol. To obtain any information from the query register, execute the Read Query Register command. See Section 9.2, “Device Commands” on page 35 for details on issuing the CFI Query command. Refer to Appendix A, “Query Structure Overview” on page 53 for a detailed explanation of the CFI register. Information contained in this register can only be accessed by executing a single-word read.

11.0 Programming Operations

The device supports two different programming methods: word programming, and write-buffer programming. Successful programming requires the addressed block to be unlocked. An attempt to program a locked block will result in the operation aborting, and SR.1 and SR.4 being set, indicating a programming error. The following sections describe device programming in detail.

11.1 Byte/Word Program

Byte/Word program is executed by a two-cycle command sequence. Byte/Word program setup (standard 0x40 or alternate 0x10) is written followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the program and program verify algorithms internally. After the program sequence is written, the device automatically outputs SRD when read (see Figure 20, “Byte/Word Program Flowchart” on page 61). The CPU can detect the completion of the program event by analyzing the STS signal or SR.7.

When program is complete, SR.4 should be checked. If a program error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for “1”s that do not successfully program to “0”s. The CUI remains in Read Status Register mode until it receives another command.

Reliable byte/word programming can only occur when V_{CC} and V_{PEN} are valid. If a byte/word program is attempted while $V_{PEN} \leq V_{PENLK}$, SR.4 and SR.3 will be set. Successful byte/word programs require that the corresponding block lock-bit be cleared. If a byte/word program is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set.

11.2 Write to Buffer

To program the flash device, a Write to Buffer command sequence is initiated. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the flash device. First, the Write to Buffer Setup command is issued along with the Block Address (see Figure 18, “Write to Buffer Flowchart” on page 59). At this point, the eXtended Status Register (XSR, see Table 19) information is loaded and XSR.7 reverts to “buffer available” status. If XSR.7 = 0, the write buffer is not available. To retry, continue monitoring XSR.7 by issuing the Write to Buffer setup command with the Block Address until XSR.7 = 1. When XSR.7 transitions to a “1,” the buffer is ready for loading.

Next, a word/byte count is given to the part with the Block Address. On the next write, a device start address is given along with the write buffer data. Subsequent writes provide additional device addresses and data, depending on the count. All subsequent addresses must lie within the start address plus the count.

Internally, this device programs many flash cells in parallel. Because of this parallel programming, maximum programming performance and lower power are obtained by aligning the start address at the beginning of a write buffer boundary (i.e., A[4:0] of the start address = 0).

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM (Write State Machine) to begin copying the buffer data to the flash array. If a command other than Write Confirm is written to the device, an “Invalid Command/Sequence” error will be generated and SR.5 and SR.4 will be set. For additional buffer writes, issue another Write to Buffer Setup command and check XSR.7.

If an error occurs while writing, the device will stop writing, and SR.4 will be set to indicate a program failure. The internal WSM verify only detects errors for “1”s that do not successfully program to “0”s. If a program error is detected, the Status Register should be cleared. Any time SR.4 and/or SR.5 is set (e.g., a media failure occurs during a program or an erase), the device will not accept any more Write to Buffer commands. Additionally, if the user attempts to program past an erase block boundary with a Write to Buffer command, the device will abort the write to buffer operation. This will generate an “Invalid Command/Sequence” error and SR.5 and SR.4 will be set.

Reliable buffered writes can only occur when $V_{PEN} = V_{PENH}$. If a buffered write is attempted while $V_{PEN} \leq V_{PENLK}$, SR.4 and SR.3 will be set. Buffered write attempts with invalid V_{CC} and V_{PEN} voltages produce spurious results and should not be attempted. Finally, successful programming requires that the corresponding block lock-bit be reset. If a buffered write is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set.

11.3 Program Suspend

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the programming process starts (either by initiating a write to buffer or byte/word program operation), writing the Program Suspend command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output SRD when read after the Program Suspend command is written. Polling SR.7 can determine when the programming operation has been suspended. When SR.7 = 1, SR.2 should also be set, indicating that the device is in the program suspend mode. STS in level RY/BY# mode will also transition to V_{OH}. Specification t_{WHRH1} defines the program suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while programming is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Program Resume. After a Program Resume command is written, the WSM will continue the programming process. SR.2 and SR.7 will automatically clear and STS in RY/BY# mode will return to V_{OL}. After the Program Resume command is written, the device automatically outputs SRD when read. V_{PEN} must remain at V_{PENH} and V_{CC} must remain at valid V_{CC} levels (the same V_{PEN} and V_{CC} levels used for programming) while in program suspend mode. Refer to Figure 21, “Program Suspend/Resume Flowchart” on page 62.

11.4 Program Resume

To resume (i.e., continue) a program suspend operation, execute the Program Resume command. The Resume command can be written to any device address. When a program operation is nested within an erase suspend operation and the Program Suspend command is issued, the device will suspend the program operation. When the Resume command is issued, the device will resume and complete the program operation. Once the nested program operation is completed, an additional Resume command is required to complete the block erase operation. The device supports a maximum suspend/resume of two nested routines. See Figure 21, “Program Suspend/Resume Flowchart” on page 62).

12.0 Erase Operations

Flash erasing is performed on a block basis; therefore, only one block can be erased at a time. Once a block is erased, all bits within that block will read as a logic level one. To determine the status of a block erase, poll the Status Register and analyze the bits. This following section describes block erase operations in detail.

12.1 Block Erase

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires an appropriate address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs SRD when read (see Figure 22, “Block Erase Flowchart” on page 63). The CPU can detect block erase completion by analyzing the output of the STS signal or SR.7. Toggle OE#, CE0, CE1, or CE2 to update the Status Register.

When the block erase is complete, SR.5 should be checked. If a block erase error is detected, the Status Register should be cleared before system software attempts corrective actions. The CUI remains in Read Status Register mode until a new command is issued.

This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both SR.4 and SR.5 being set. Also, reliable block erasure can only occur when V_{CC} is valid and $V_{PEN} = V_{PENH}$. If block erase is attempted while $V_{PEN} \leq V_{PENLK}$, SR.3 and SR.5 will be set. Successful block erase requires that the corresponding block lock-bit be cleared. If block erase is attempted when the corresponding block lock-bit is set, SR.1 and SR.5 will be set.

12.2 Block Erase Suspend

The Block Erase Suspend command allows block-erase interruption to read or program data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs SRD when read after the Block Erase Suspend command is written. Polling SR.7 then SR.6 can determine when the block erase operation has been suspended (both will be set). In default mode, STS will also transition to V_{OH}. Specification t_{WHRH} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A program command sequence can also be issued during erase suspend to program data in other blocks. During a program operation with block erase suspended, SR.7 will return to “0” and STS output (in default mode) will transition to V_{OL}. However, SR.6 will remain “1” to indicate block erase suspend status. Using the Program Suspend command, a program operation can also be suspended. Resuming a suspended programming operation by issuing the Program Resume command allows continuing of the suspended programming operation. To resume the suspended erase, the user must wait for the programming operation to complete before issuing the Block Erase Resume command.

The only other valid commands while block erase is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. SR.6 and SR.7 will automatically clear and STS (in default mode) will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs SRD when read (see Figure 23, “Block Erase Suspend/Resume Flowchart” on page 64). V_{PEN} must remain at V_{PENH} (the same V_{PEN} level used for block erase) while block erase is suspended. Block erase cannot resume until program operations initiated during block erase suspend have completed.

12.3 Erase Resume

To resume (i.e., continue) an erase suspend operation, execute the Erase Resume command. The Resume command can be written to any device address. When a program operation is nested within an erase suspend operation and the Program Suspend command is issued, the device will suspend the program operation. When the Resume command is issued, the device will resume the program operations first. Once the nested program operation is completed, an additional Resume command is required to complete the block erase operation. The device supports a maximum suspend/resume of two nested routines. See Figure 22, “Block Erase Flowchart” on page 63.

13.0 Security Modes

This device offers both hardware and software security features. Block lock operations, PRs, and VPEN allow the user to implement various levels of data protection. The following section describes security features in detail.

Other security features are available that are not described in this datasheet. Please contact your local Intel Field Representative for more information.

13.1 Set Block Lock-Bit

A flexible block locking scheme is enabled via block lock-bits. The block lock-bits gate program and erase operations. Individual block lock-bits can be set using the Set Block Lock-Bit command. This command is invalid while the WSM is running or the device is suspended.

Set block lock-bit commands are executed by a two-cycle sequence. The set block setup along with appropriate block address is followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs Status Register data when read (see Figure 24 on page 65). The CPU can detect the completion of the set lock-bit event by analyzing the STS signal output or SR.7.

When the set lock-bit operation is complete, SR.4 should be checked. If an error is detected, the Status Register should be cleared. The CUI will remain in Read Status Register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in SR.4 and SR.5 being set. Also, reliable operations occur only when V_{CC} and V_{PEN} are valid. With $V_{PEN} \leq V_{PENLK}$, lock-bit contents are protected against alteration.

13.2 Clear Block Lock-Bits

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. Block lock-bits can be cleared using only the Clear Block Lock-Bits command. This command is invalid while the WSM is running or the device is suspended.

Clear block lock-bits command is executed by a two-cycle sequence. A clear block lock-bits setup is first written. The device automatically outputs Status Register data when read (see Figure 25 on page 66). The CPU can detect completion of the clear block lock-bits event by analyzing the STS signal output or SR.7.

When the operation is complete, SR.5 should be checked. If a clear block lock-bit error is detected, the Status Register should be cleared. The CUI will remain in Read Status Register mode until another command is issued.

This two-step sequence of setup followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in SR.4 and SR.5 being set. Also, a reliable clear block lock-bits operation can only occur when V_{CC} and V_{PEN} are valid. If a clear block lock-bits operation is attempted while $V_{PEN} \leq V_{PENLK}$, SR.3 and SR.5 will be set.

If a clear block lock-bits operation is aborted due to V_{PEN} or V_{CC} transitioning out of valid range, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

13.3 Protection Register Program

The Intel StrataFlash® memory (J3) includes a 128-bit Protection Register (PR) that can be used to increase the security of a system design. For example, the number contained in the PR can be used to "mate" the flash component with other system components such as the CPU or ASIC, preventing device substitution.

The 128-bits of the PR are divided into two 64-bit segments. One of the segments is programmed at the Intel factory with a unique 64-bit number, which is unalterable. The other segment is left blank for customer designers to program as desired. Once the customer segment is programmed, it can be locked to prevent further programming.

13.3.1 Reading the Protection Register

The Protection Register is read in the identification read mode. The device is switched to this mode by issuing the Read Identifier command (0x90). Once in this mode, read cycles from addresses shown in Table 8 or Table 21 retrieve the specified information. To return to read array mode, write the Read Array command (0xFF).

13.3.2 Programming the Protection Register

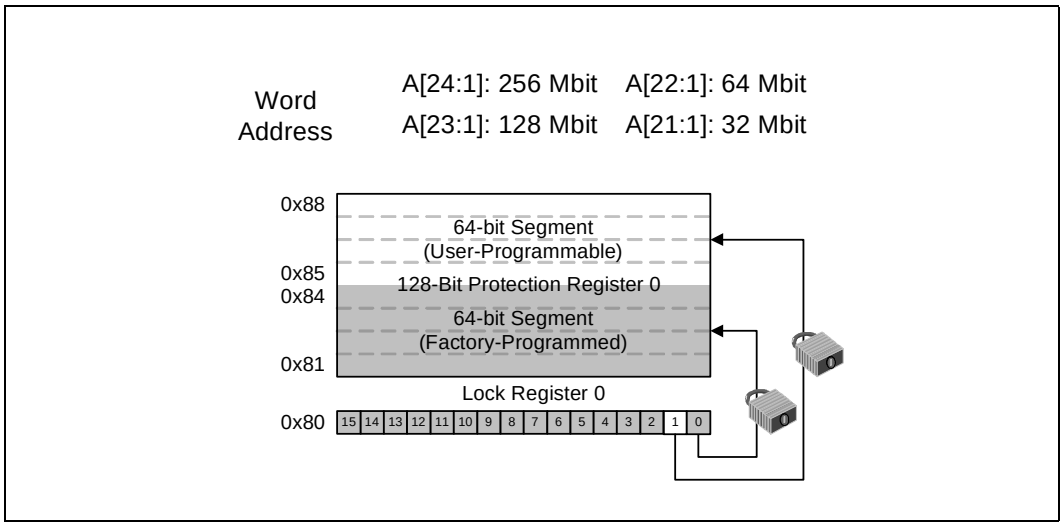
Protection Register bits are programmed using the two-cycle Protection Program command. The 64-bit number is programmed 16 bits at a time for word-wide configuration and eight bits at a time for byte-wide configuration. First write the Protection Program Setup command, 0xC0. The next write to the device will latch in address and data and program the specified location. The allowable addresses are shown in Table 8 or Table 21. See Figure 26, "Protection Register Programming Flowchart" on page 67

Any attempt to address Protection Program commands outside the defined PR address space will result in a Status Register error (SR.4 will be set). Attempting to program a locked PR segment will result in a Status Register error (SR.4 and SR.1 will be set).

13.3.3 Locking the Protection Register

The user-programmable segment of the Protection Register is lockable by programming Bit 1 of the PLR to 0. Bit 0 of this location is programmed to 0 at the Intel factory to protect the unique device number. Bit 1 is set using the Protection Program command to program "0xFFFD" to the PLR. After these bits have been programmed, no further changes can be made to the values stored in the Protection Register. Protection Program commands to a locked section will result in a Status Register error (SR.4 and SR.1 will be set). PR lockout state is not reversible.

Figure 17. Protection Register Memory Map



NOTE: A0 is not used in x16 mode when accessing the Protection Register map (See Table 8 for x16 addressing). For x8 mode A0 is used (See Table 21 for x8 addressing).

Table 20. Word-Wide Protection Register Addressing

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Table 21. Byte-Wide Protection Register Addressing (Sheet 1 of 2)

Byte	Use	A8	A7	A6	A5	A4	A3	A2	A1	A0
LOCK	Both	1	0	0	0	0	0	0	0	0
LOCK	Both	1	0	0	0	0	0	0	0	1
0	Factory	1	0	0	0	0	0	0	1	0
1	Factory	1	0	0	0	0	0	0	1	1
2	Factory	1	0	0	0	0	0	1	0	0
3	Factory	1	0	0	0	0	0	1	0	1
4	Factory	1	0	0	0	0	0	1	1	0
5	Factory	1	0	0	0	0	0	1	1	1

Table 21. Byte-Wide Protection Register Addressing (Sheet 2 of 2)

6	Factory	1	0	0	0	0	1	0	0	0
7	Factory	1	0	0	0	0	1	0	0	1
8	User	1	0	0	0	0	1	0	1	0
9	User	1	0	0	0	0	1	0	1	1
A	User	1	0	0	0	0	1	1	0	0
B	User	1	0	0	0	0	1	1	0	1
C	User	1	0	0	0	0	1	1	1	0
D	User	1	0	0	0	0	1	1	1	1
E	User	1	0	0	0	1	0	0	0	0
F	User	1	0	0	0	1	0	0	0	1

NOTE: All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e.g., A[MAX:9] = 0.

13.4 Array Protection

The V_{PEN} signal is a hardware mechanism to prohibit array alteration. When the V_{PEN} voltage is below the V_{PENLK} voltage, array contents cannot be altered. To ensure a proper erase or program operation, V_{PEN} must be set to a valid voltage level. To determine the status of an erase or program operation, poll the Status Register and analyze the bits.

14.0 Special Modes

This section describes how to read the status, ID, and CFI registers. This section also details how to configure the STS signal.

14.1 Set Read Configuration Register Command

This command is no longer supported on J3A or J3C. The J3A device will ignore this command, while the J3C device will **result in an invalid command sequence (SR.4 and SR.5 =1).**

14.2 Status (STS)

The Status (STS) signal can be configured to different states using the Configuration command. Once the STS signal has been configured, it remains in that configuration until another configuration command is issued or RP# is asserted low. Initially, the STS signal defaults to RY/BY# operation where RY/BY# low indicates that the WSM is busy. RY/BY# high indicates that the state machine is ready for a new operation or suspended. Table 22, “STS Configuration Coding Definitions” on page 50 displays the possible STS configurations.

To reconfigure the Status (STS) signal to other modes, the Configuration command is given followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described below. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Program Complete interrupt pulse. Supplying the 0x00 configuration code with the Configuration command resets the STS signal to the default RY/BY# level mode. The possible configurations and their usage are described in Table 22, “STS Configuration Coding Definitions” on page 50. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status. An invalid configuration code will result in both SR.4 and SR.5 being set. When configured in one of the pulse modes, the STS signal pulses low with a typical pulse width of 250 ns.

Table 22. STS Configuration Coding Definitions

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Pulse on Program Complete (1)	Pulse on Erase Complete (1)

D[1:0] = STS Configuration Codes	Notes
00 = default, level mode; device ready indication	Used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's WSM is busy.
01 = pulse on Erase Complete	Used to generate a system interrupt pulse when any flash device in an array has completed a block erase. Helpful for reformatting blocks after file system free space reclamation or “cleanup.”

Table 22. STS Configuration Coding Definitions

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Pulse on Program Complete (1)	Pulse on Erase Complete (1)

D[1:0] = STS Configuration Codes	Notes
10 = pulse on Program Complete	Used to generate a system interrupt pulse when any flash device in an array has completed a program operation. Provides highest performance for servicing continuous buffer write operations.
11 = pulse on Erase or Program Complete	Used to generate system interrupts to trigger servicing of flash arrays when either erase or program operations are completed, when a common interrupt service routine is desired.

NOTES:
1. When configured in one of the pulse modes, STS pulses low with a typical pulse width of 250 ns.
2. An invalid configuration code will result in both SR.4 and SR.5 being set.

Appendix A Common Flash Interface

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. It allows flash vendors to standardize their existing interfaces for long-term compatibility.

This appendix defines the data structure or "database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query command is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

A.1 Query Structure Output

The Query "database" allows system software to gain information for controlling the flash component. This section describes the device's CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (D[7:0]) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two bytes of the Query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII "Q" in the low byte (D[7:0]) and 0x00 (00h) in the high byte (D[15:8]).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 23. Summary of Query Structure Output as a Function of Device and Mode

Device Type/ Mode	Query start location in maximum device bus width addresses	Query data with maximum device bus width addressing			Query data with byte addressing		
		Hex Offset	Hex Code	ASCII Value	Hex Offset	Hex Code	ASCII Value
x16 device x16 mode	10h	10: 11: 12:	0051 0052 0059	“Q” “R” “Y”	20: 21: 22:	51 00 52	“Q” “Null” “R”
x16 device x8 mode	N/A(1)	N/A(1)			20: 21: 22:	51 51 52	“Q” “Q” “R”

NOTE:
1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing, where these lower addresses are not toggled by the system, is "Not Applicable" for x8-configured devices.

Table 24. Example of Query Structure Output of a x16- and x8-Capable Device

Word Addressing			Byte Addressing		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_{15}–A_0	D15–D_0		A_7–A_0	D_7–D_0	
0010h	0051	“Q”	20h	51	“Q”
0011h	0052	“R”	21h	51	“Q”
0012h	0059	“Y”	22h	52	“R”
0013h	P_ID_{LO}	PrVendor	23h	52	“R”
0014h	P_ID_{HI}	ID #	24h	59	“Y”
0015h	P_{LO}	PrVendor	25h	59	“Y”
0016h	P_{HI}	TblAdr	26h	P_ID_{LO}	PrVendor
0017h	A_ID_{LO}	AltVendor	27h	P_ID_{LO}	ID #
0018h	A_ID_{HI}	ID #	28h	P_ID_{HI}	ID #
...	...	...	...	...	...

A.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or “database.” The structure sub-sections and address locations are summarized below. See *AP-646 Common Flash Interface (CFI) and Command Sets* (order number 292204) for a full description of CFI commands.

The following sections describe the Query structure sub-sections in detail.

Table 25. Query Structure

Offset	Sub-Section Name	Description	Notes
00h		Manufacturer Code	1
01h		Device Code	1
(BA+2)h[2]	Block Status Register	Block-Specific Information	1,2
04-0Fh	Reserved	*Reserved for Vendor-Specific Information*	1
10h	CFI Query Identification String	*Reserved for Vendor-Specific Information*	1
1Bh	System Interface Information	Command Set ID and Vendor Data Offset	1
27h	Device Geometry Definition	Flash Device Layout	1
P[3]	Primary Intel-Specific Extended Query Table	Vendor-Defined Additional Information Specific to the Primary Vendor Algorithm	1,3

NOTES:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block Address beginning location (i.e., 02000h is block 2's beginning location when the block size is 128 Kbyte).
3. Offset 15 defines "P" which points to the *Primary Intel-Specific Extended Query* Table.

A.3 Block Status Register

The block status register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Table 26. Block Status Register

Offset	Length	Description	Address	Value
(BA+2)h[1]	1	Block Lock Status Register	BA+2:	--00 or --01
		BSR.0 Block Lock Status 0 = Unlocked 1 = Locked	BA+2:	(bit 0): 0 or 1
		BSR 1–7: *Reserved for Future Use*	BA+2:	(bit 1–7): 0

NOTE:
1. BA = The beginning location of a Block Address (i.e., 008000h is block 1's (64-KB block) beginning location in word mode).

A.4 CFI Query Identification String

The CFI Query Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 27. CFI Identification (Sheet 1 of 2)

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string "QRY"	10 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--01 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--31 --00	
17h	2	Alternate vendor command set and control interface ID code.	17:	--00	

Table 27. CFI Identification (Sheet 2 of 2)

Offset	Length	Description	Add.	Hex Code	Value
		0000h means no second vendor-specified algorithm exists	18:	--00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

A.5 System Interface Information

The following device information can optimize system interface software.

Table 28. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--27	2.7 V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--36	3.6 V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--00	0.0 V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--00	0.0 V
1Fh	1	“n” such that typical single word program time-out = 2^n µs	1F:	--08	256 µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µs	20:	--08	256 µs
21h	1	“n” such that typical block erase time-out = 2^n ms	21:	--0A	1 s
22h	1	“n” such that typical full chip erase time-out = 2^n ms	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--04	2 ms
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--04	2 ms
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--04	16 s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

A.6 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 29. Device Geometry Definition (Sheet 1 of 2)

Offset	Length	Description	Code See Table Below		
27h	1	“n” such that device size = 2^n in number of bytes	27:		
28h	2	Flash device interface: x8 async x16 async x8/x16 async 28:00,29:00 28:01,29:00 28:02,29:00	28: 29:	--02 --00	x8/ x16
2Ah	2	“n” such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--05 --00	32

Table 29. Device Geometry Definition (Sheet 2 of 2)

Offset	Length	Description	Code See Table Below		
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in “bulk” 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2C:	--01	1
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:		

Device Geometry Definition

Address	32 Mbit	64 Mbit	128 Mbit	256Mbit
27:	--16	--17	--18	--19
28:	--02	--02	--02	--02
29:	--00	--00	--00	-00
2A:	--05	--05	--05	-05
2B:	--00	--00	--00	-00
2C:	--01	--01	--01	-01
2D:	--1F	--3F	--7F	-FF
2E:	--00	--00	--00	--00
2F:	--00	--00	--00	--00
30:	--02	--02	--02	--02

A.7 Primary-Vendor Specific Extended Query Table

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 30. Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	31:	--50	“P”
(P+1)h		Unique ASCII string “PRI”	32:	--52	“R”
(P+2)h			33:	--49	“I”
(P+3)h	1	Major version number, ASCII	34:	--31	“1”
(P+4)h	1	Minor version number, ASCII	35:	--31	“1”

Table 30. Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support (1=yes, 0=no) *bits 9–31 are reserved; undefined bits are "0." If bit 31 is "1" then another 31 bit field of optional features follows at the end of the bit-30 field.*	36: 37: 38: 39:	--0A --00 --00 --00	
		bit 0 Chip erase supported	bit 0 = 0		No
		bit 1 Suspend erase supported	bit 1 = 1		Yes
		bit 2 Suspend program supported	bit 2 = 1		Yes
		bit 3 Legacy lock/unlock supported	bit 3 = 1[1]		Yes[1]
		bit 4 Queued erase supported	bit 4 = 0		No
		bit 5 Instant Individual block locking supported	bit 5 = 0		No
		bit 6 Protection bits supported	bit 6 = 1		Yes
		bit 7 Page-mode read supported	bit 7 = 1		Yes
		bit 8 Synchronous read supported	bit 8 = 0		No
(P+9)h	1	Supported functions after suspend: read Array, Status, Query Other supported operations are: *bits 1–7 reserved; undefined bits are "0"*	3A:	--01	
		bit 0 Program supported after erase suspend	bit 0 = 1		Yes
(P+A)h (P+B)h	2	Block status register mask *bits 2–15 are Reserved; undefined bits are "0"*	3B: 3C:	--01 --00	
		bit 0 Block Lock-Bit Status register active	bit 0 = 1		Yes
		bit 1 Block Lock-Down Bit Status active	bit 1 = 0		No
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage bits 0–3 BCD value in 100 mV bits 4–7 BCD value in volts	3D:	--33	3.3 V
(P+D)h	1	V_{PP} optimum program/erase supply voltage bits 0–3 BCD value in 100 mV bits 4–7 HEX value in volts	3E:	--00	0.0 V

NOTE:
1. Future devices may not support the described "Legacy Lock/Unlock" function. Thus bit 3 would have a value of "0."

Table 31. Protection Register Information

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available	3F:	--01	01
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection Register bytes. Some are pre-programmed with device-unique serial numbers. Others are user-programmable. Bits 0-15 point to the Protection Register lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0-7 = Lock/bytes JEDEC-plane physical low address bits 8-15 = Lock/bytes JEDEC-plane physical high address bits 16-23 = "n" such that 2^n = factory pre-programmed bytes bits 24-31 = "n" such that 2^n = user-programmable bytes	40: 41: 42: 43:	--80 --00 --03 --03	80h 00h 8bytes 8bytes

NOTE:
1. The variable P is a pointer which is defined at CFI offset 15h.

Table 32. Burst Read Information

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	44:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	45:	--00	0
(P+15)h		*Reserved for future use*	46:		

NOTE:
1. The variable P is a pointer which is defined at CFI offset 15h.

Appendix B Flow Charts

Figure 18. Write to Buffer Flowchart

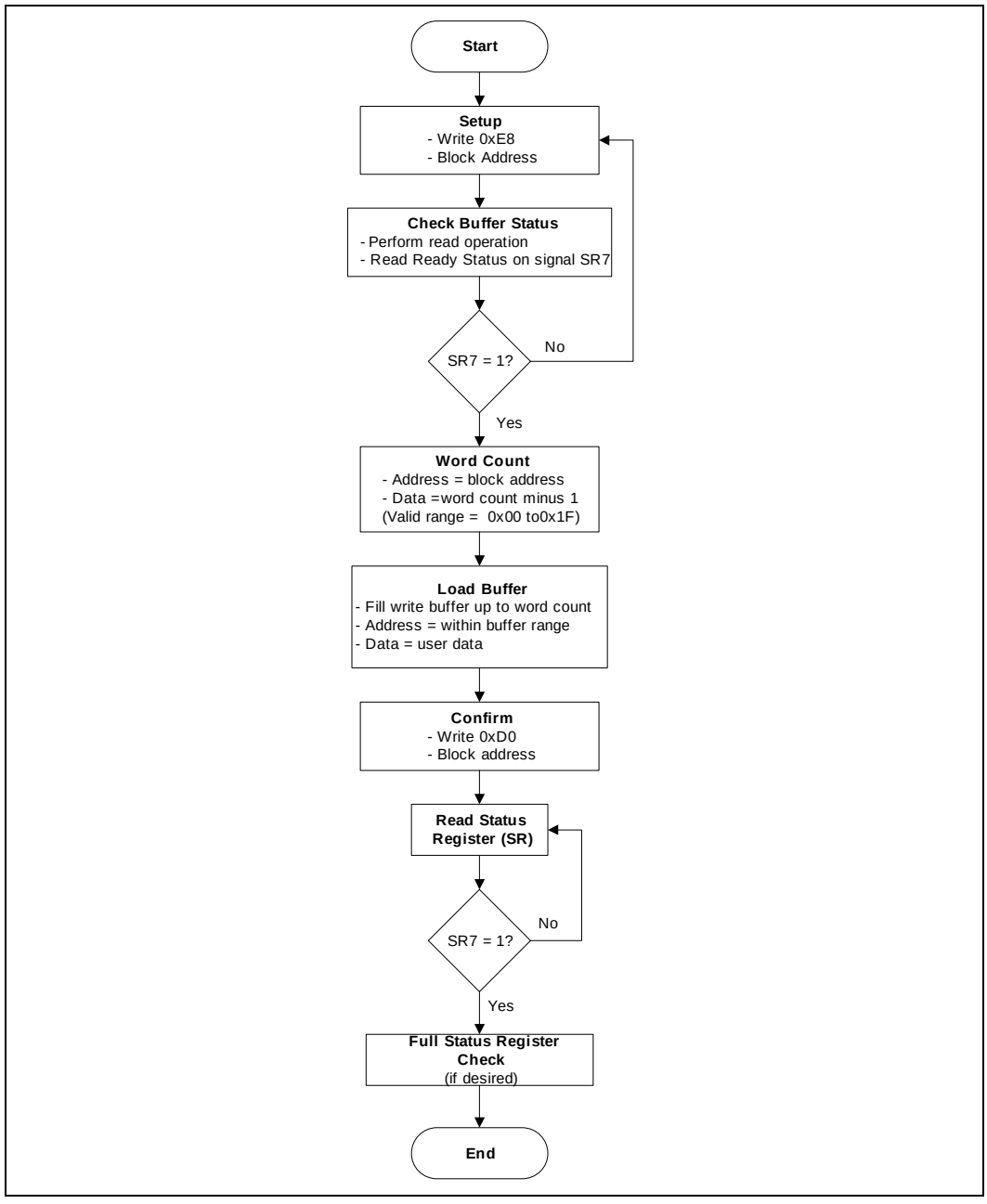


Figure 19. Status Register Flowchart

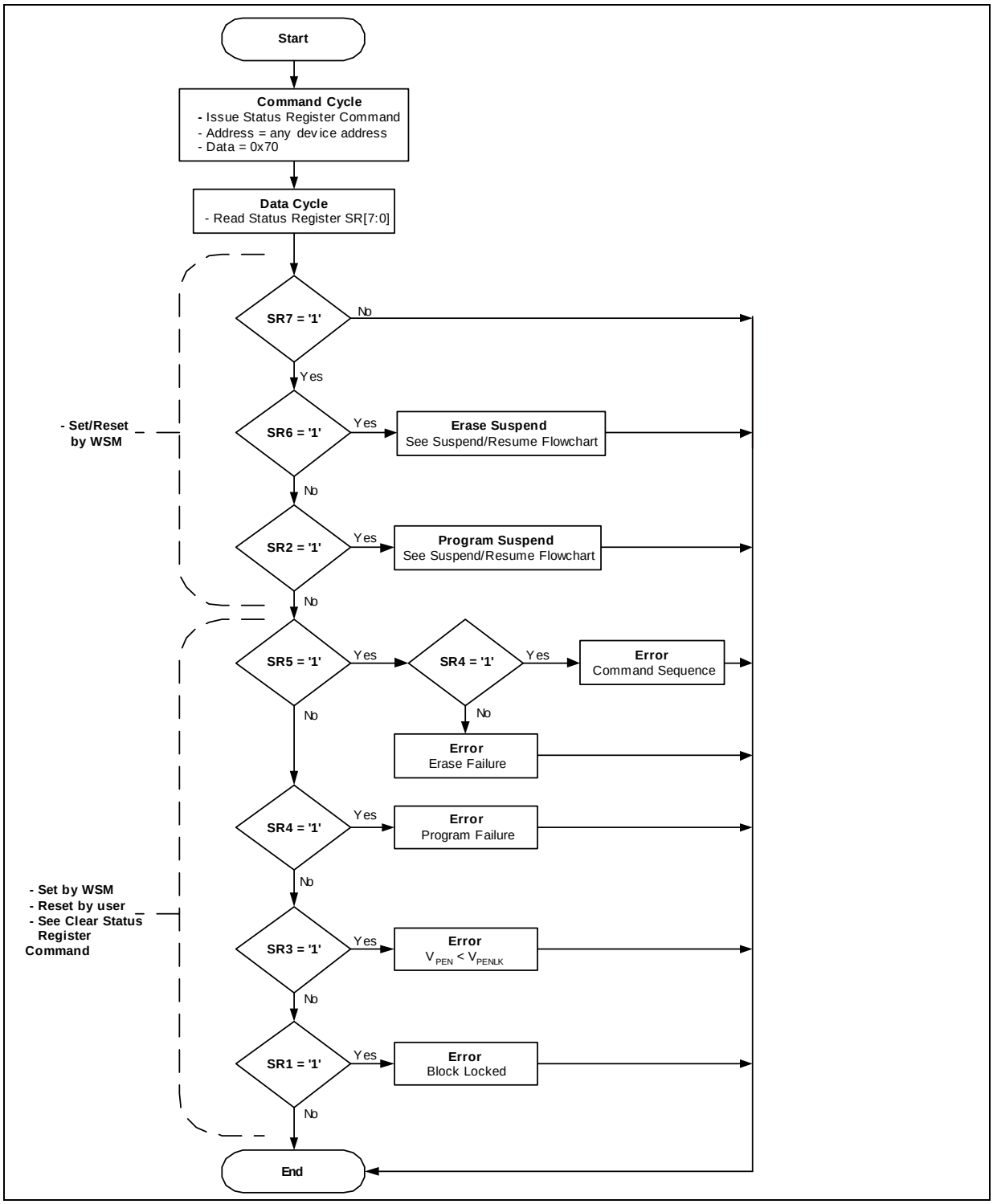
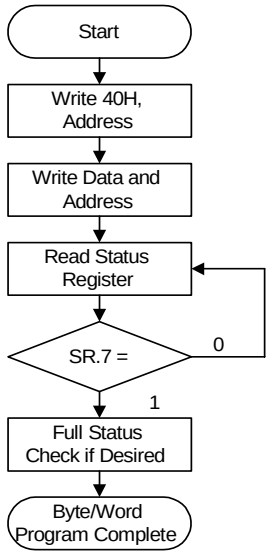


Figure 20. Byte/Word Program Flowchart



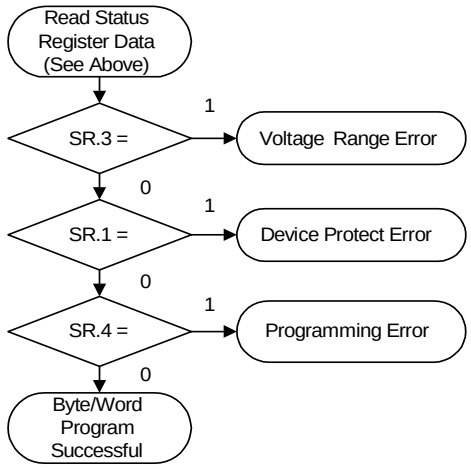
Bus Operation	Command	Comments
Write	Setup Byte/ Word Program	Data = 40H Addr = Location to Be Programmed
Write	Byte/Word Program	Data = Data to Be Programmed Addr = Location to Be Programmed
Read (Note 1)		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

1. Toggling OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR full status check can be done after each program operation, or after a sequence of programming operations.

Write FFH after the last program operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



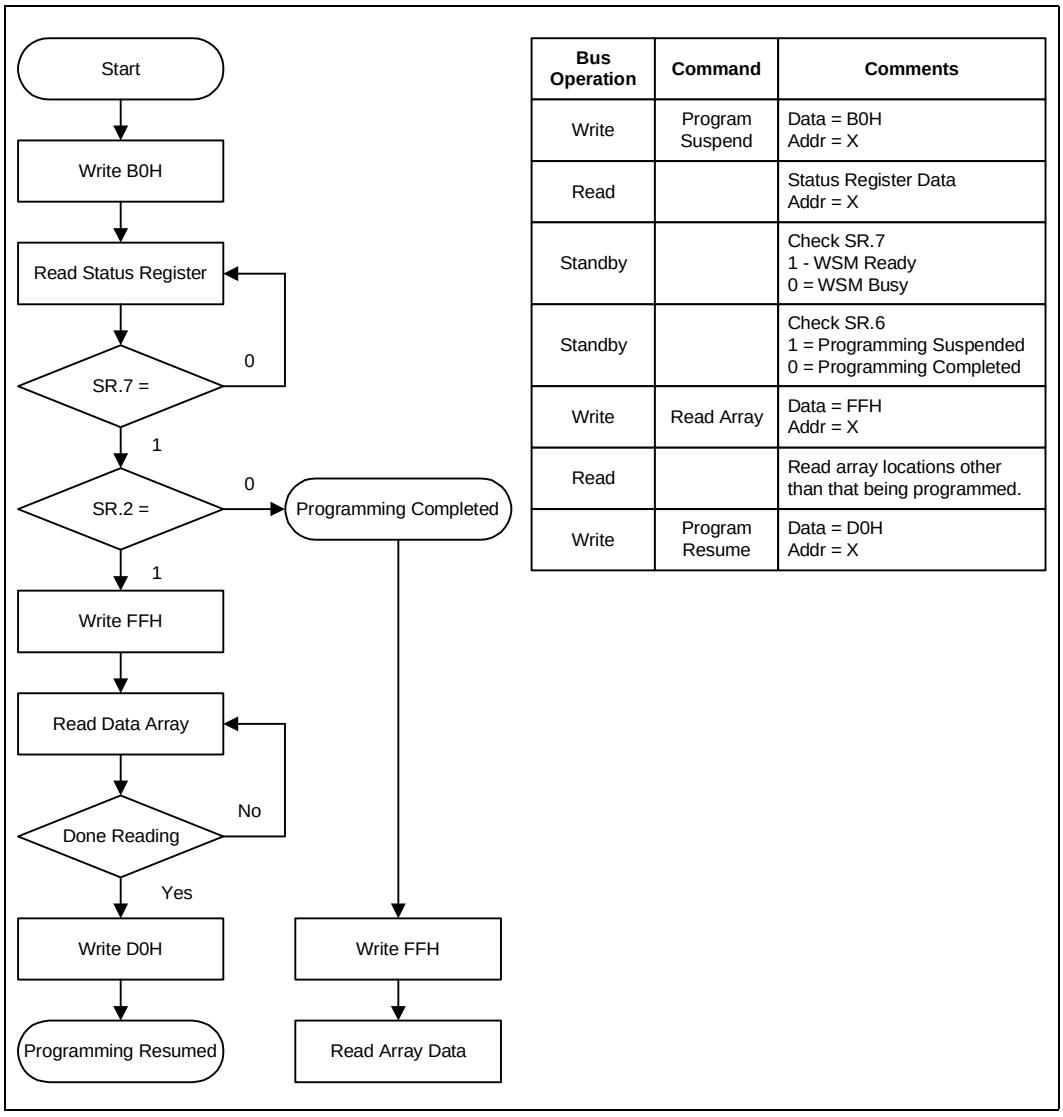
Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming to Voltage Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit Is Set Only required for systems implemeting lock-bit configuration.
Standby		Check SR.4 1 = Programming Error

Toggling OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 21. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 - WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Programming Suspended 0 = Programming Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being programmed.
Write	Program Resume	Data = D0H Addr = X

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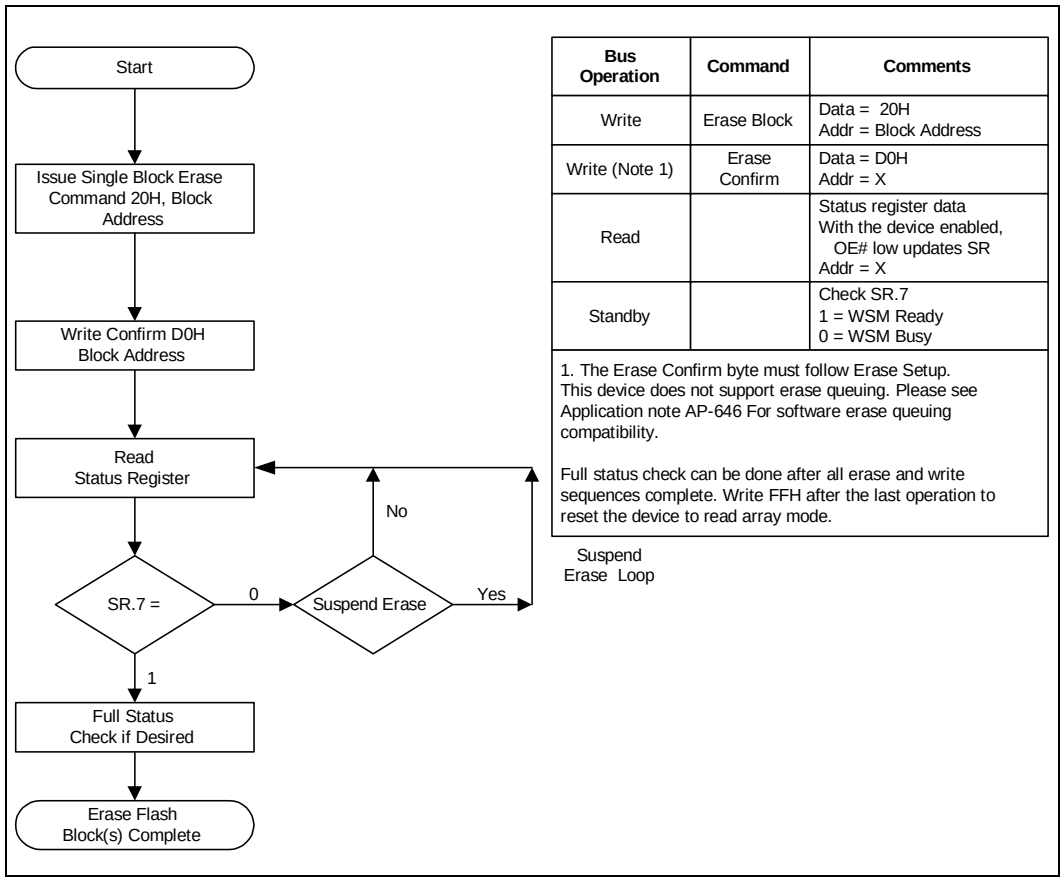
Figure 22. Block Erase Flowchart

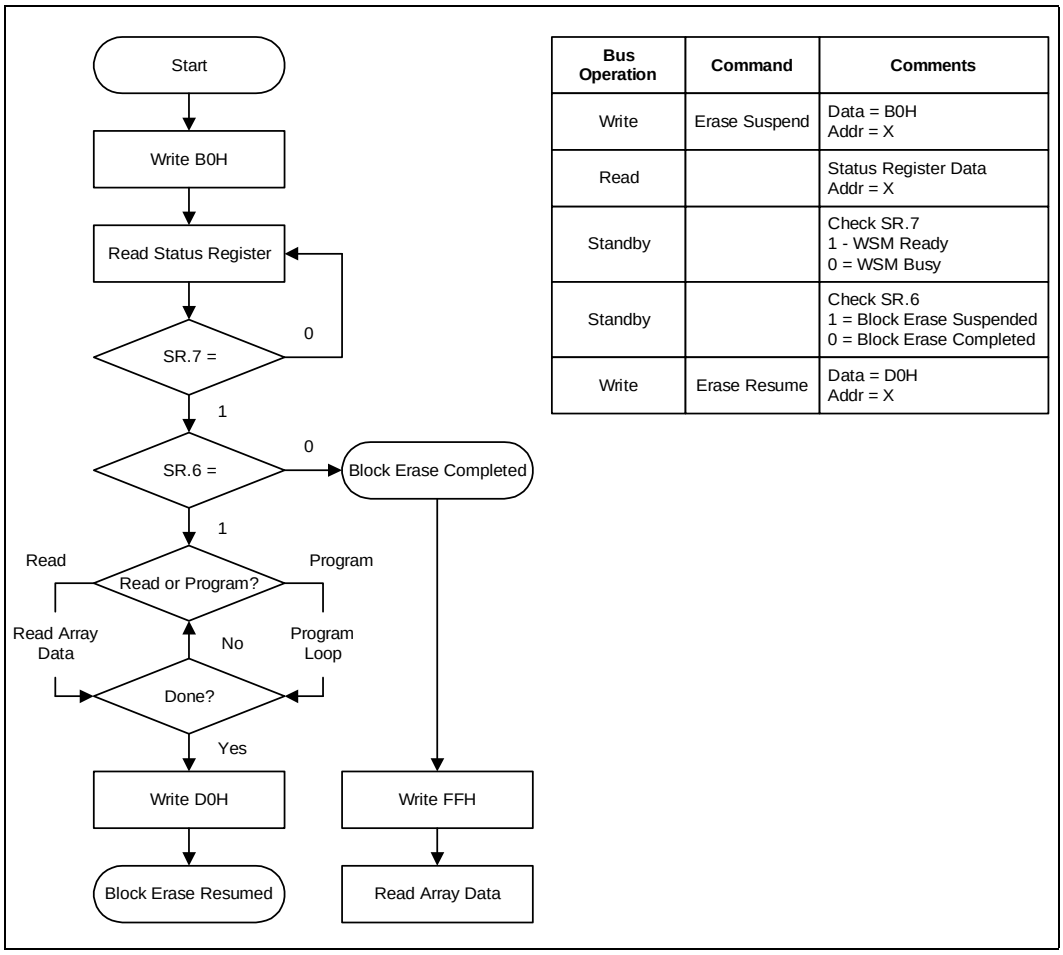


Bus Operation	Command	Comments
Write	Erase Block	Data = 20H Addr = Block Address
Write (Note 1)	Erase Confirm	Data = D0H Addr = X
Read		Status register data With the device enabled, OE# low updates SR Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

1. The Erase Confirm byte must follow Erase Setup. This device does not support erase queuing. Please see Application note AP-646 For software erase queuing compatibility.

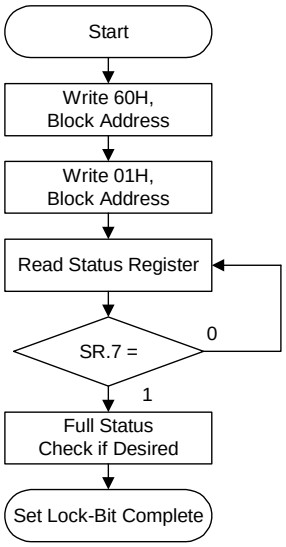
Full status check can be done after all erase and write sequences complete. Write FFH after the last operation to reset the device to read array mode.

Figure 23. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 - WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Figure 24. Set Block Lock-Bit Flowchart



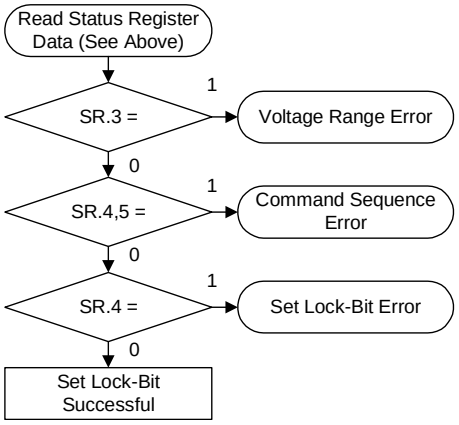
Bus Operation	Command	Comments
Write	Set Block Lock-Bit Setup	Data = 60H Addr =Block Address
Write	Set Block Lock-Bit Confirm	Data = 01H Addr = Block Address
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent lock-bit operations.

Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.

Write FFH after the last lock-bit set operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

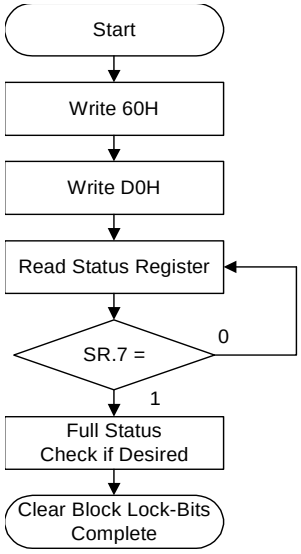


Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error

SR.5, SR.4 and SR.3 are only cleared by the Clear Status Register command, in cases where multiple lock-bits are set before full status is checked.

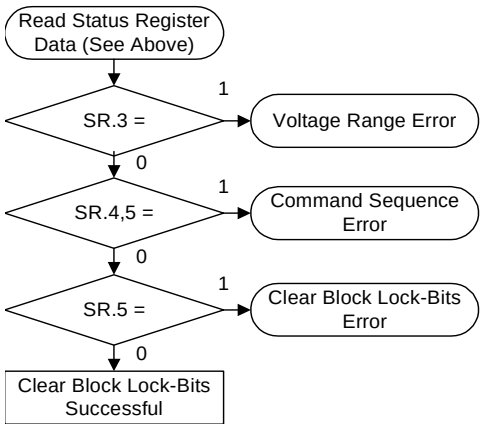
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 25. Clear Lock-Bit Flowchart



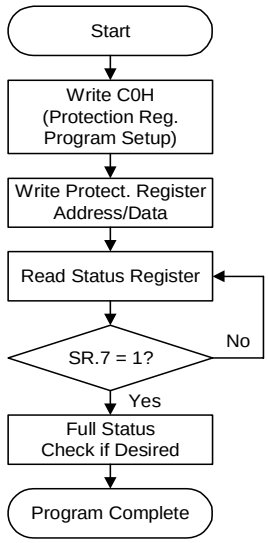
Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block or Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the clear lock-bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, and SR.3 are only cleared by the Clear Status Register command. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 26. Protection Register Programming Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data = C0H
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

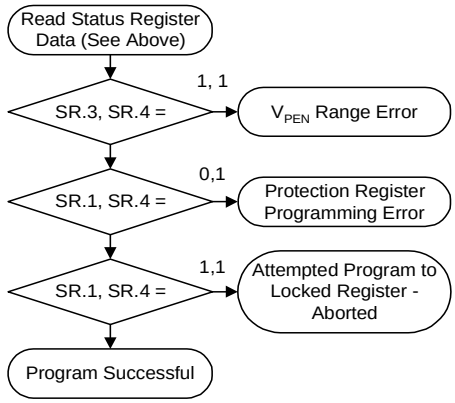
Protection Program operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error.

Repeat for subsequent programming operations.

SR Full Status Check can be done after each program or after a sequence of program operations.

Write FFH after the last program operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		SR.1 SR.3 SR.4 0 1 1 V_{PEN} Low
Standby		0 0 1 Prot. Reg. Prog. Error
Standby		1 0 1 Register Locked: Aborted

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases of multiple protection register program operations before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

Appendix C Design Considerations

C.1 Three-Line Output Control

The device will often be used in large memory arrays. Intel provides five control inputs (CE0, CE1, CE2, OE#, and RP#) to accommodate multiple memory connections. This control provides for:

a. Lowest possible memory power dissipation.

b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable the device (see Table 13) while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while de-selected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

C.2 STS and Block Erase, Program, and Lock-Bit Configuration Polling

STS is an open drain output that should be connected to VCCQ by a pull-up resistor to provide a hardware method of detecting block erase, program, and lock-bit configuration completion. It is recommended that a 2.5k resister be used between STS# and VCCQ. In default mode, it transitions low after block erase, program, or lock-bit configuration commands and returns to High Z when the WSM has finished executing the internal algorithm. For alternate configurations of the STS signal, see the Configuration command.

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also High Z when the device is in block erase suspend (with programming inactive), program suspend, or in reset/power-down mode.

C.3 Input Signal Transitions—Reducing Overshoots and Undershoots When Using Buffers or Transceivers

As faster, high-drive devices such as transceivers or buffers drive input signals to flash memory devices, overshoots and undershoots can sometimes cause input signals to exceed flash memory specifications. (See "DC Voltage Characteristics" on page 20.) Many buffer/transceiver vendors now carry bus-interface devices with internal output-damping resistors or reduced-drive outputs. Internal output-damping resistors diminish the nominal output drive currents, while still leaving sufficient drive capability for most applications. These internal output-damping resistors help reduce unnecessary overshoots and undershoots. Transceivers or buffers with balanced- or light-drive outputs also reduce overshoots and undershoots by diminishing output-drive currents. When considering a buffer/transceiver interface design to flash, devices with internal output-damping resistors or reduced-drive outputs should be used to minimize overshoots and undershoots. For additional information, please refer to AP-647, *5 Volt Intel StrataFlash® Memory Design Guide* (Order Number: 292205).

C.4 V_{CC}, V_{PEN}, RP# Transitions

Block erase, program, and lock-bit configuration are not guaranteed if V_{PEN} or V_{CC} falls outside of the specified operating ranges, or RP# ≠ V_{IH}. If RP# transitions to V_{IL} during block erase, program, or lock-bit configuration, STS (in default mode) will remain low for a maximum time of $t_{PLPH} + t_{PHRH}$ until the reset operation is complete. Then, the operation will abort and the device will enter reset/power-down mode. The aborted operation may leave data partially corrupted after programming, or partially altered after an erase or lock-bit configuration. Therefore, block erase and lock-bit configuration commands must be repeated after normal operation is restored. Device power-off or RP# = V_{IL} clears the Status Register.

The CUI latches commands issued by system software and is not altered by V_{PEN}, CE_0, CE_1, or CE_2 transitions, or WSM actions. Its state is read array mode upon power-up, after exit from reset/ power-down mode, or after V_{CC} transitions below V_{LKO}. V_{CC} must be kept at or above V_{PEN} during V_{CC} transitions.

After block erase, program, or lock-bit configuration, even after V_{PEN} transitions down to V_{PENLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired. V_{PEN} must be kept at or below V_{CC} during V_{PEN} transitions.

C.5 Power Dissipation

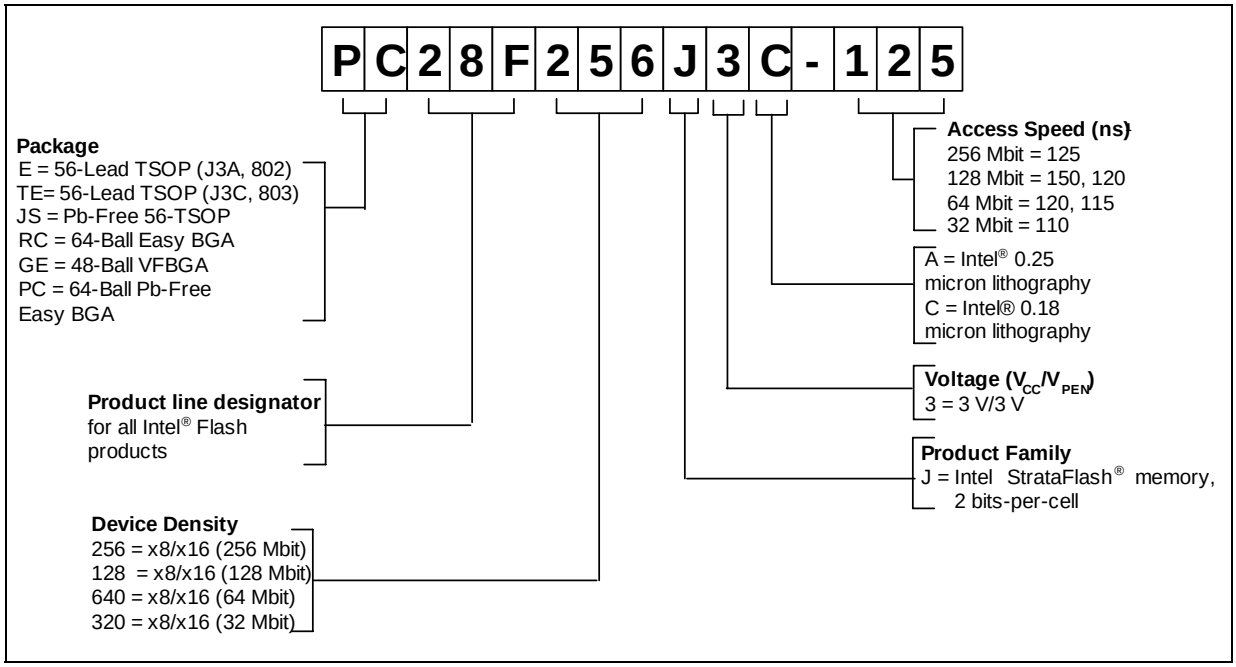
When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

Appendix D Additional Information

Order Number	Document/Tool
298130	*Intel® StrataFlash™ Memory (J3); 28F256J3, 28F128J3, 28F640J3, 28F320J3 Specification Update*
298136	*Intel® Persistent Storage Manager (IPSM) User's Guide* Software Manual
297833	*Intel® Flash Data Integrator (FDI) User's Guide* Software Manual
290737	*Intel StrataFlash® Synchronous Memory (K3/K18); 28F640K3, 28F640K18, 28F128K3, 28F128K18, 28F256K3, 28F256K18*
292280	*AP-732 3 Volt Intel StrataFlash® Memory J3 to K3/K18 Migration Guide*
292237	*AP-689 Using Intel® Persistent Storage Manager*
290606	*5 Volt Intel® StrataFlash™ MemoryI28F320J5 and 28F640J5* datasheet
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
253418	*Intel® Wireless Communications and Computing Package User's Guide*

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.

Appendix E Ordering Information



NOTE:
1. Speeds are for either the standard asynchronous read access times or for the first access of a page-mode read sequence.

VALID COMBINATIONS

56-Lead TSOP	64-Ball Easy BGA	48-Ball VF BGA
E28F320J3A-110	RC28F320J3A-110	GE28F320J3A-110
E28F640J3A-120	RC28F640J3A-120	GE28F320J3C-110
E28F128J3A-150	RC28F128J3A-150	GE28F640J3C-115
TE28F320J3C-110	RC28F320J3C-110	GE28F640J3C-120
TE28F640J3C-115	RC28F640J3C-115	
TE28F640J3C-120	RC28F640J3C-120	
TE28F128J3C-120	RC28F128J3C-120	
TE28F128J3C-150	RC28F128J3C-150	
TE28F256J3C-125	RC28F256J3C-125	
56-Lead Pb-Free TSOP	**64-Ball Pb-Free Easy BGA**	
JS28F256J3C125	PC28F256J3C125	
JS28F128J3C120	PC28F128J3C120	
JS28F640J3C115	PC28F640J3C115	
JS28F320J3C110	PC28F320J3C110	

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