FAIRCHILD SEMICONDUCTOR™

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74ABT899
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The ABT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction.

The ABT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

Features

- Latchable transceiver with output sink of 64 mA
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the 543 and 280
- May be used in system applications in place of the 657 and 373 (no need to change T/$\overline{\text{R}}$ to check parity)
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

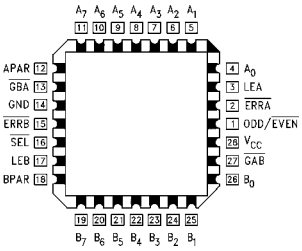
Ordering Code:

Order Number	Package Number	Package Description
74ABT899CSC	M28B	28-Lead Small Outline Integrated Circuit (SOIC), MS-013, 0.300" Wide Body
74ABT899CMSA	MSA28	28-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT899CQC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450" Square

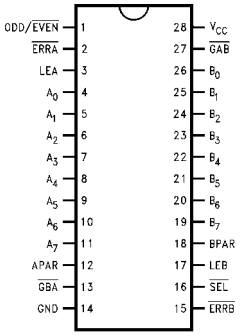
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignment for PLCC



Pin Assignment for SOIC and SSOP



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Pin Descriptions

Pin Names	Descriptions
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs/Outputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The ABT899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

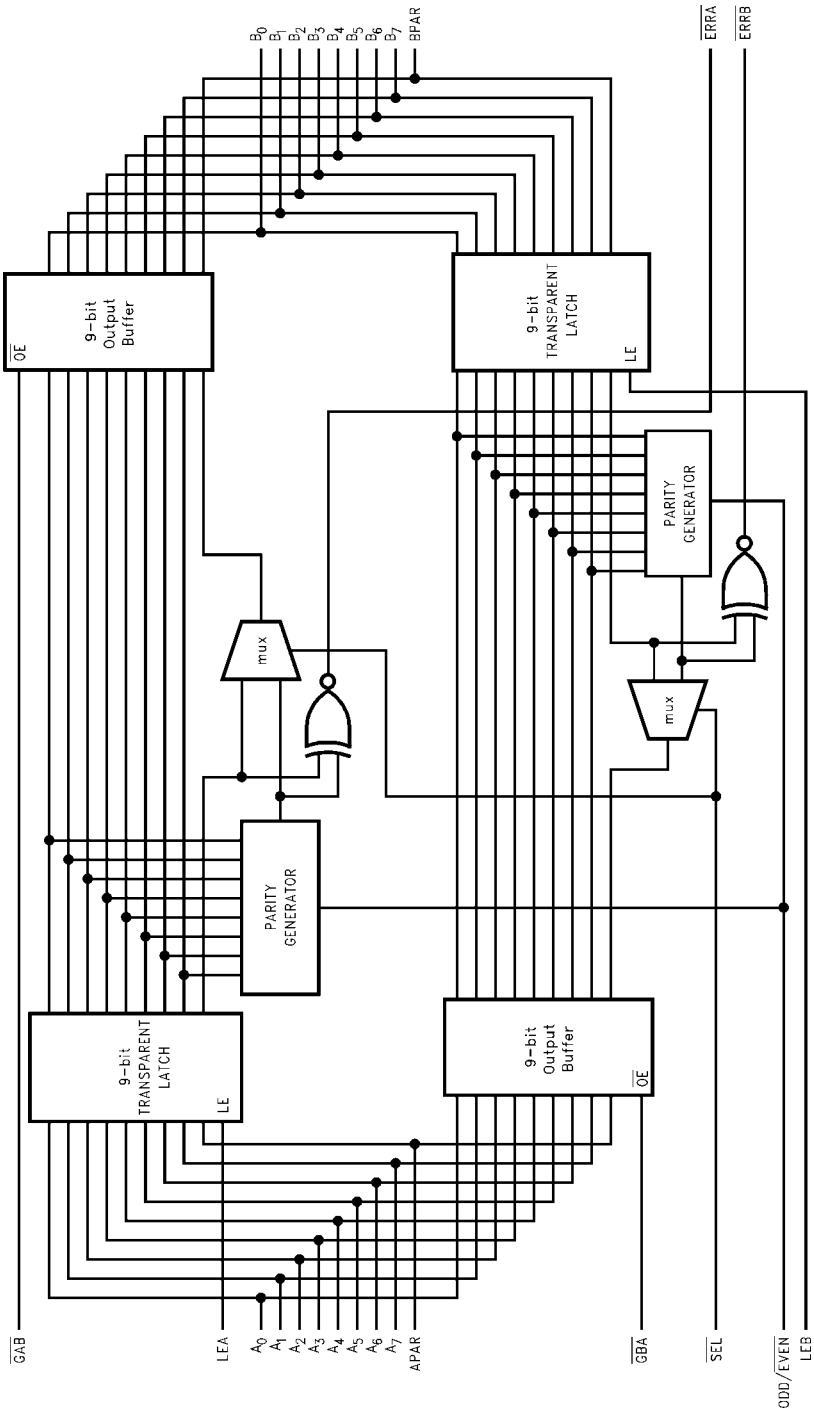
Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are 3-STATE.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: O/$\overline{\text{E}}$ = ODD/$\overline{\text{EVEN}}$

Functional Block Diagram



Absolute Maximum Ratings (Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5 2.0			V	Min	I_{OH} = −3 mA, (A_n, B_n, APAR, BPAR) I_{OH} = −32 mA, (A_n, B_n, APAR, BPAR)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n, APAR, BPAR)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 4) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n, APAR, BPAR)
I_{IL}	Input LOW Current			−5	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 4) V_{IN} = 0.0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			50	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{GAB}$ and $\overline{GBA}$ = 2.0V
$I_{IL} + I_{OZL}$	Output Leakage Current			−50	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{GAB}$ and $\overline{GBA}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n, APAR, BPAR)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n, APAR, BPAR)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n, APAR, BPAR); All Others GND
I_{CCH}	Power Supply Current			250	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			34	mA	Max	All Outputs LOW, ERRA/B = HIGH (Note 5)
I_{CCZ}	Power Supply Current			250	µA	Max	Outputs 3-STATE All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}: No Load (Note 4)			0.4	mA/MHz	Max	Outputs Open $\overline{GAB}$ or $\overline{GBA}$ = GND, LE = HIGH Non-I/O = GND or V_{CC} One bit toggling, 50% duty cycle

Note 4: Guaranteed, but not tested.

Note 5: Add 3.75 mA for each $\overline{ERR}$ LOW.

DC Electrical Characteristics

(PLCC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.8	1.1	V	5.0	T_A = 25°C (Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.3	–0.8		V	5.0	T_A = 25°C (Note 6)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 8)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.2	1.8		V	5.0	T_A = 25°C (Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		0.8	0.5	V	5.0	T_A = 25°C (Note 7)

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 8: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and PLCC Package)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.0	4.8	1.5	4.8	ns
t_{PHL}	A_n, to B_n	1.5	3.5	4.8	1.5	4.8	
t_{PLH}	Propagation Delay	2.5	5.9	9.2	2.5	9.2	ns
t_{PHL}	A_n, B_n to BPAR, APAR	2.5	5.8	9.2	2.5	9.2	
t_{PLH}	Propagation Delay	2.5	5.4	8.5	2.5	8.5	ns
t_{PHL}	A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	2.5	5.4	8.5	2.5	8.5	
t_{PLH}	Propagation Delay	1.5	3.7	6.0	1.5	6.0	ns
t_{PHL}	APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	1.5	3.7	6.0	1.5	6.0	
t_{PLH}	Propagation Delay	2.0	4.4	6.9	2.0	6.9	ns
t_{PHL}	ODD/EVEN to APAR, BPAR	2.0	4.4	6.9	2.0	6.9	
t_{PLH}	Propagation Delay	1.8	4.0	6.0	1.8	6.0	ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	1.8	4.0	6.0	1.8	6.0	
t_{PLH}	Propagation Delay	1.5	3.8	6.0	1.5	6.0	ns
t_{PHL}	SEL to APAR, BPAR	1.5	3.8	6.0	1.5	6.0	
t_{PLH}	Propagation Delay	1.5	3.2	4.6	1.5	4.6	ns
t_{PHL}	LEA, LEB to B_n, A_n	1.5	3.2	4.6	1.5	4.6	
t_{PLH}	Propagation Delay	2.5	5.9	8.8	2.5	8.8	
t_{PHL}	LEA, LEB to BPAR, APAR Generate Mode	2.5	5.7	8.8	2.5	8.8	ns
t_{PLH}	Propagation Delay	1.5	3.6	5.1	1.5	5.1	ns
t_{PHL}	LEA, LEB to BPAR, APAR, Feed Thru Mode	1.5	3.6	5.1	1.5	5.1	
t_{PLH}	Propagation Delay	1.6	5.4	8.4	1.6	8.4	ns
t_{PHL}	LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	1.6	5.4	8.4	1.6	8.4	
t_{PZH}	Output Enable Time	1.5	3.6	6.0	1.5	6.0	ns
t_{PZL}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.5	3.4	6.0	1.5	6.0	
t_{PHZ}	Output Disable Time	1.0	4.0	6.0	1.0	6.0	ns
t_{PLZ}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.0	3.3	6.0	1.0	6.0	
$t_{PLH}t_{PHL}$	Propagation Delay	1.5	3.3	5.4	1.5	5.4	ns
	APAR to BPAR, BPAR to APAR	1.5	3.8	5.4	1.5	5.4	

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.0	5.3	1.5	5.3	ns
t_{PHL}	A_n, to B_n	1.5	3.5	5.3	1.5	5.3	
t_{PLH}	Propagation Delay	2.5	5.9	9.9	2.5	9.9	ns
t_{PHL}	A_n, B_n to BPAR, APAR	2.5	5.8	9.9	2.5	9.9	
t_{PLH}	Propagation Delay	2.5	5.4	9.4	2.5	9.4	ns
t_{PHL}	A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	2.5	5.4	9.4	2.5	9.4	
t_{PLH}	Propagation Delay	1.5	3.7	6.5	1.5	6.5	ns
t_{PHL}	APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	1.5	3.7	6.5	1.5	6.5	
t_{PLH}	Propagation Delay	2.0	4.4	7.4	2.0	7.4	ns
t_{PHL}	ODD/EVEN to APAR, BPAR	2.0	4.4	7.4	2.0	7.4	
t_{PLH}	Propagation Delay	1.8	4.0	6.5	1.8	6.5	ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	1.8	4.0	6.5	1.8	6.5	
t_{PLH}	Propagation Delay	1.5	3.8	6.5	1.5	6.5	ns
t_{PHL}	SEL to APAR, BPAR	1.5	3.8	6.5	1.5	6.5	
t_{PLH}	Propagation Delay	1.5	3.2	5.1	1.5	5.1	ns
t_{PHL}	LEA, LEB to B_n, A_n	1.5	3.2	5.1	1.5	5.1	
t_{PLH}	Propagation Delay	2.5	5.9	9.2	2.5	9.2	
t_{PHL}	LEA, LEB to BPAR, APAR Generate Mode	2.5	5.7	9.2	2.5	9.2	ns
t_{PLH}	Propagation Delay	1.5	3.6	5.6	1.5	5.6	ns
t_{PHL}	LEA, LEB to BPAR, APAR, Feed Thru Mode	1.5	3.6	5.6	1.5	5.6	
t_{PLH}	Propagation Delay	1.6	5.4	8.9	1.6	8.9	ns
t_{PHL}	LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	1.6	5.4	8.9	1.6	8.9	
t_{PZH}	Output Enable Time	1.5	3.6	6.5	1.5	6.5	ns
t_{PZL}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.5	3.4	6.5	1.5	6.5	
t_{PHZ}	Output Disable Time	1.0	4.0	6.5	1.0	6.5	ns
t_{PLZ}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.0	3.3	6.5	1.0	6.5	
t_{PLH}	Propagation Delay	1.5	3.3	5.9	1.5	5.9	ns
t_{PHL}	APAR to BPAR, BPAR to APAR	1.5	3.8	5.9	1.5	5.9	

AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW A_n,	1.5		1.5		ns
$t_S(L)$	APAR to LEA or B_n, BPAR to LEB	1.5		1.5		
$t_H(H)$	Hold Time, HIGH or LOW A_n,	1.0		1.0		ns
$t_H(L)$	APAR to LEA or B_n, BPAR to LEB	1.0		1.0		
$t_W(H)$	Pulse Width, HIGH LEA or LEB	3.0		3.0		ns

Extended AC Electrical Characteristics

(SOIC and PLCC Package)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, 9 Outputs Switching (Note 9)			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 10)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 9 Outputs Switching (Note 11)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		6.2	2.0	7.2	2.5	9.5	ns
t_{PHL}	A_n to B_n	1.5		6.2	2.0	7.2	2.5	9.5	
t_{PLH}	Propagation Delay	1.5		6.8	2.0	8.0	2.5	10.0	ns
t_{PHL}	APAR to BPAR	1.5		6.8	2.0	8.0	2.0	10.0	
t_{PLH}	Propagation Delay	2.5		10.0	3.0	12.5	3.5	13.5	ns
t_{PHL}	A_n, B_n to BPAR, APAR	2.5		10.0	3.0	12.5	3.5	13.5	
t_{PLH}	Propagation Delay		(Note 13)		3.0	12.0		(Note 13)	ns
t_{PHL}	A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$				3.0	12.0			
t_{PLH}	Propagation Delay		(Note 13)		2.0	9.0		(Note 13)	ns
t_{PHL}	APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$				2.0	9.0			
t_{PLH}	Propagation Delay		(Note 13)		2.5	9.9		(Note 13)	ns
t_{PHL}	ODD/EVEN to APAR, BPAR				2.5	9.9			
t_{PLH}	Propagation Delay		(Note 13)		2.0	8.8		(Note 13)	ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$				2.0	8.8			
t_{PLH}	Propagation Delay		(Note 13)		2.0	9.5		(Note 13)	ns
t_{PHL}	SEL to APAR, BPAR				2.0	9.5			
t_{PLH}	Propagation Delay	1.5		5.7	2.0	7.9	2.5	10.0	ns
t_{PHL}	LEA, LEB to B_n, A_n	1.5		5.7	2.0	7.9	2.5	10.0	
t_{PLH}	Propagation Delay	1.5		9.5	2.0	12.0	2.5	13.0	ns
t_{PHL}	LEA, LEB to BPAR, APAR	1.5		9.5	2.0	12.0	2.5	13.0	
t_{PLH}	Propagation Delay		(Note 13)		2.0	11.5		(Note 13)	ns
t_{PHL}	LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$				2.0	11.5			
t_{PZH}	Output enable time	1.5		7.0	2.0	8.5	2.5	10.5	
t_{PZL}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.5		7.0	2.0	8.5	2.5	10.5	ns
t_{PHZ}	Output disable time	1.0		6.5					
t_{PLZ}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.0		6.5	(Note 12)		(Note 12)		ns

Note 9: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 10: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load

Note 12: The 3-STATE delay time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 13: Not applicable for multiple output switching.

Extended AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, 9 Outputs Switching (Note 14)			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 15)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 9 Outputs Switching (Note 16)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		6.7	2.0	7.7	2.5	10.1	ns
t_{PHL}	A_n to B_n	1.5		6.7	2.0	7.7	2.5	10.1	
t_{PLH}	Propagation Delay	1.5		7.3	2.0	8.5	2.5	10.6	ns
t_{PHL}	APAR to BPAR	1.5		7.3	2.0	8.5	2.0	10.6	
t_{PLH}	Propagation Delay	2.5		10.7	3.0	13.2	3.5	14.3	ns
t_{PHL}	A_n, B_n to BPAR, APAR	2.5		10.7	3.0	13.2	3.5	14.3	
t_{PLH}	Propagation Delay		(Note 18)		3.0	12.9	(Note 18)		ns
t_{PHL}	A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$				3.0	12.9			
t_{PLH}	Propagation Delay		(Note 18)		2.0	9.5	(Note 18)		ns
t_{PHL}	APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$				2.0	9.5			
t_{PLH}	Propagation Delay		(Note 18)		2.5	10.4	(Note 18)		ns
t_{PHL}	ODD/EVEN to APAR, BPAR				2.5	10.4			
t_{PLH}	Propagation Delay		(Note 18)		2.0	9.3	(Note 18)		ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$				2.0	9.3			
t_{PLH}	Propagation Delay		(Note 18)		2.0	10.0	(Note 18)		ns
t_{PHL}	SEL to APAR, BPAR				2.0	10.0			
t_{PLH}	Propagation Delay	1.5		6.2	2.0	8.4	2.5	10.6	ns
t_{PHL}	LEA, LEB to B_n, A_n	1.5		6.2	2.0	8.4	2.5	10.6	
t_{PLH}	Propagation Delay	1.5		10.0	2.0	12.5	2.5	13.6	ns
t_{PHL}	LEA, LEB to BPAR, APAR	1.5		10.0	2.0	12.5	2.5	13.6	
t_{PLH}	Propagation Delay		(Note 18)		2.0	12.0	(Note 18)		ns
t_{PHL}	LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$				2.0	12.0			
t_{PZH}	Output enable time	1.5		7.5	2.0	9.0	2.5	11.1	
t_{PZL}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.5		7.5	2.0	9.0	2.5	11.1	ns
t_{PHZ}	Output disable time	1.0		7.0					
t_{PLZ}	$\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.0		7.0	(Note 17)		(Note 17)		ns

Note 14: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 15: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 16: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load

Note 17: The 3-STATE delay time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 18: Not applicable for multiple output switching.

Skew

(PLCC package) (Note 2)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 9 Outputs Switching (Note 19)	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 9 Outputs Switching (Note 20)	Units
		Max	Max	
t_{OSHL} (Note 21)	Pin to Pin Skew HL Transitions	1.0	2.0	ns
t_{OSLH} (Note 21)	Pin to Pin Skew LH Transitions	1.1	2.1	ns
t_{PS} (Note 22)	Duty Cycle LH–HL Skew	2.0	3.5	ns
t_{OST} (Note 21)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns
t_{PV} (Note 23)	Device to Device Skew LH/HL Transitions	3.0	4.0	ns

Note 19: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 20: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 21: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested. Skew applies to propagation delays individually; i.e., A_n to B_n separate from LEA to A_n.

Note 22: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

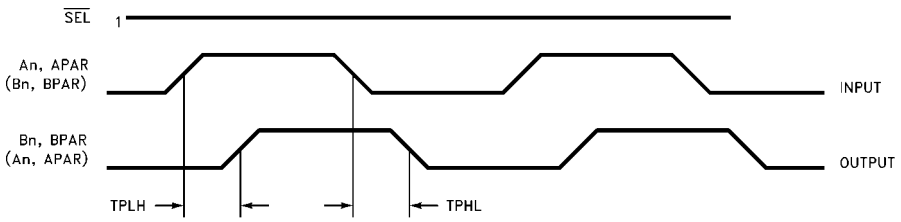
Note 23: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Pin Capacitance	5.0	pF	$V_{CC} = 0V$
$C_{I/O}$ (Note 24)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$

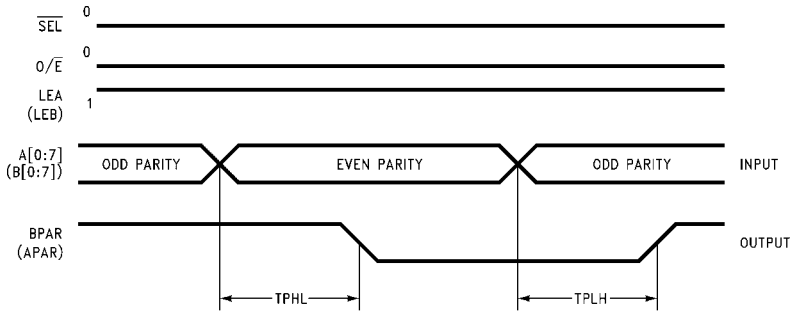
Note 24: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Path



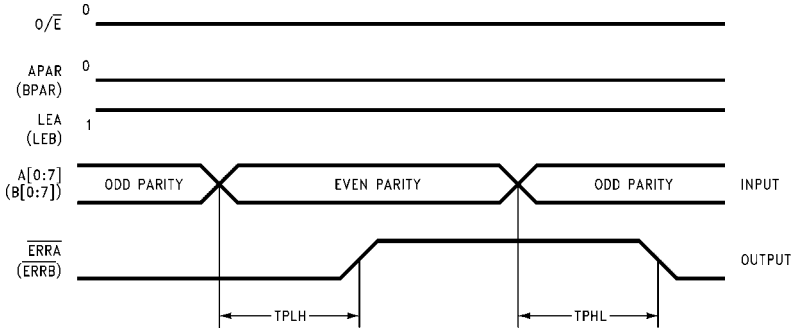
A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

FIGURE 1.



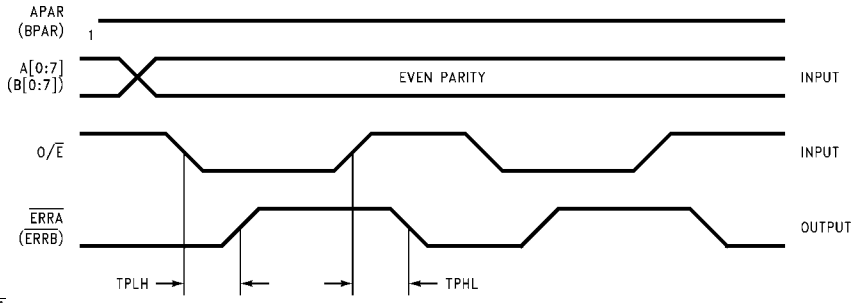
A_n → BPAR
(B_n → APAR)

FIGURE 2.



A_n → $\overline{ERRA}$
(B_n → $\overline{ERRB}$)

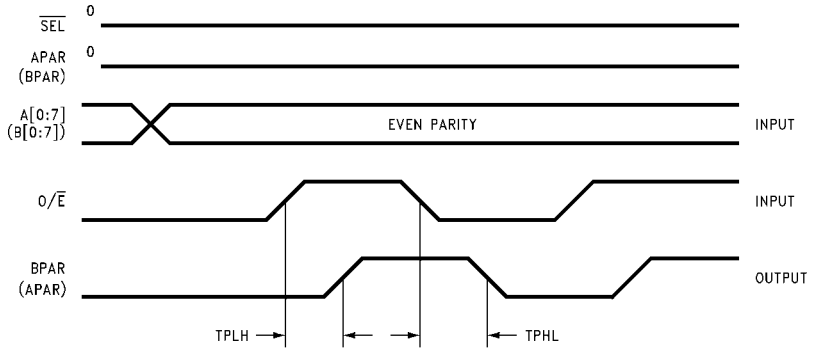
FIGURE 3.



O/$\overline{E}$ → $\overline{ERRA}$
O/$\overline{E}$ → $\overline{ERRB}$

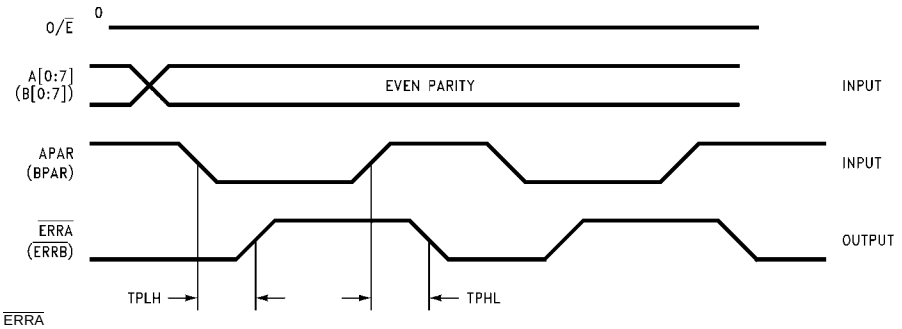
FIGURE 4.

AC Path (Continued)



O/E → BPAR
(O/E → APAR)

FIGURE 5.



APAR → ERRA
(BPAR → ERRB)

FIGURE 6.

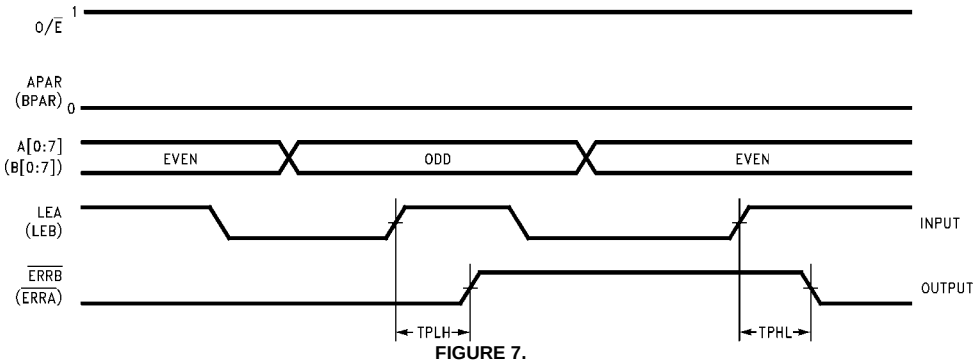
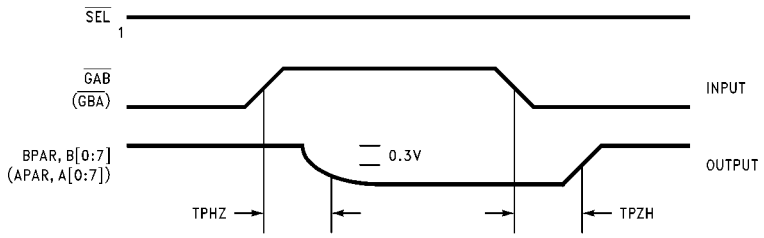


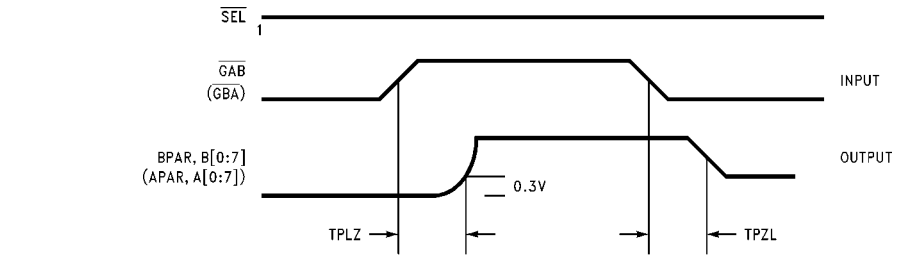
FIGURE 7.



ZH, HZ

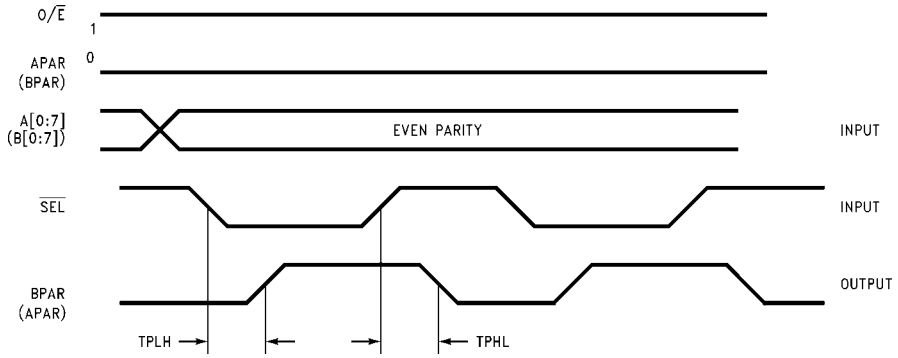
FIGURE 8.

AC Path (Continued)



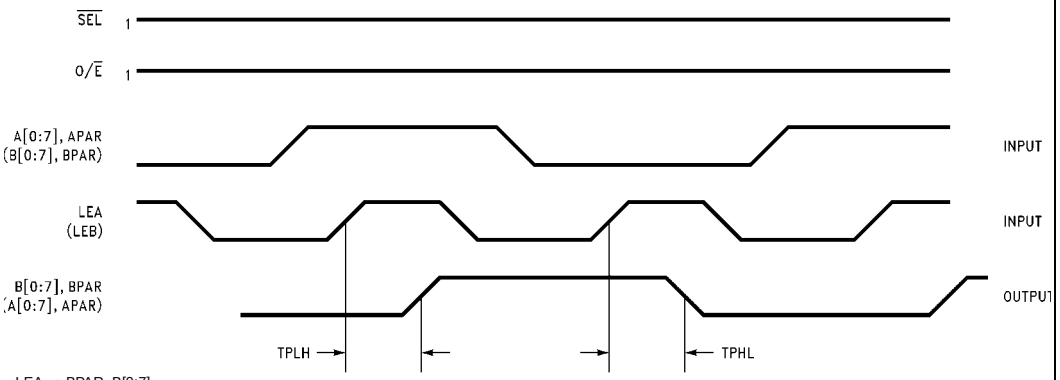
ZL, LZ

FIGURE 9.



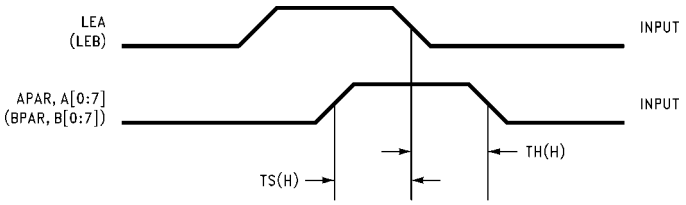
SEL → BPAR
(SEL → APAR)

FIGURE 10.



LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

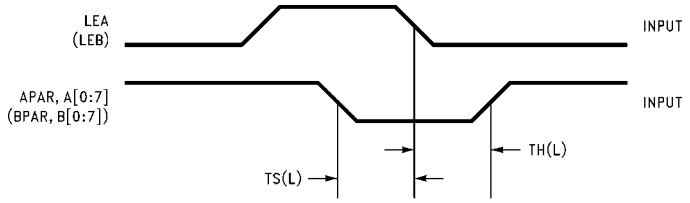
FIGURE 11.



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

FIGURE 12.

AC Path (Continued)



TS(L), TH(L)

LEA → APAR, A[0:7]

(LEB → BPAR, B[0:7])

FIGURE 13.

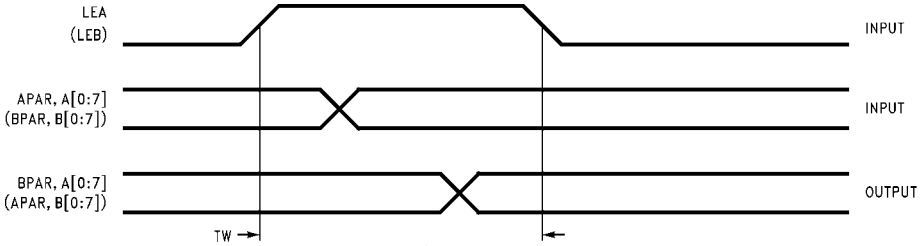
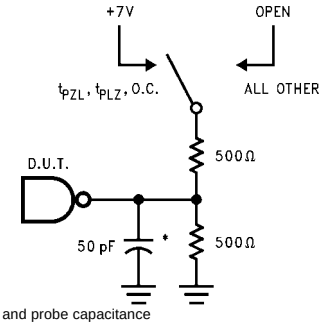


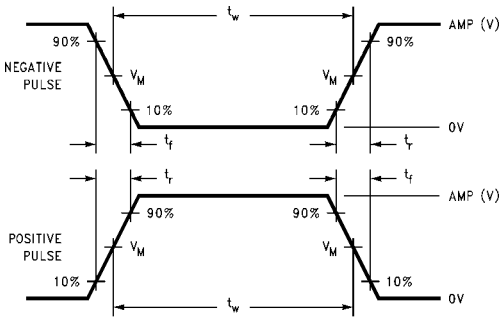
FIGURE 14.

AC Loading



*Includes jig and probe capacitance

FIGURE 15. Standard AC Test Load



$V_M = 1.5V$

FIGURE 16.

Input Pulse Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 17. Test Input Signal Requirements

AC Waveforms

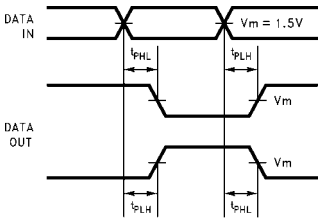


FIGURE 18. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

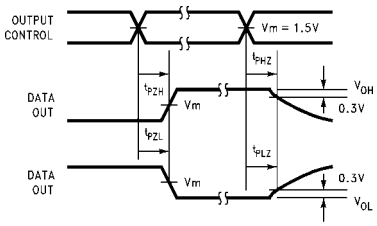


FIGURE 20. 3-STATE Output HIGH and LOW Enable and Disable Times

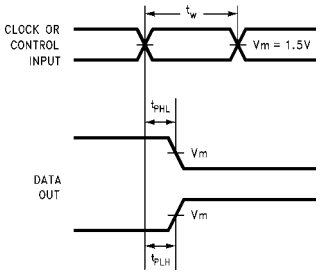


FIGURE 19. Propagation Delay, Pulse Width Waveforms

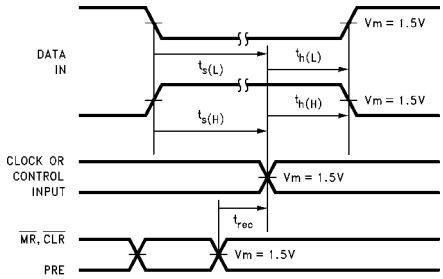
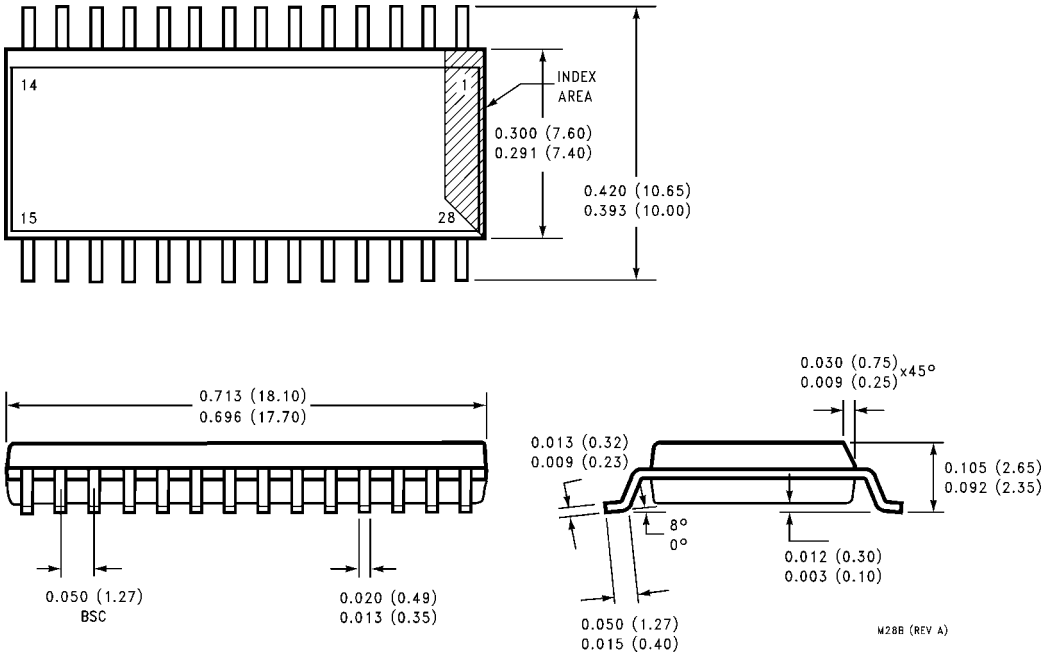
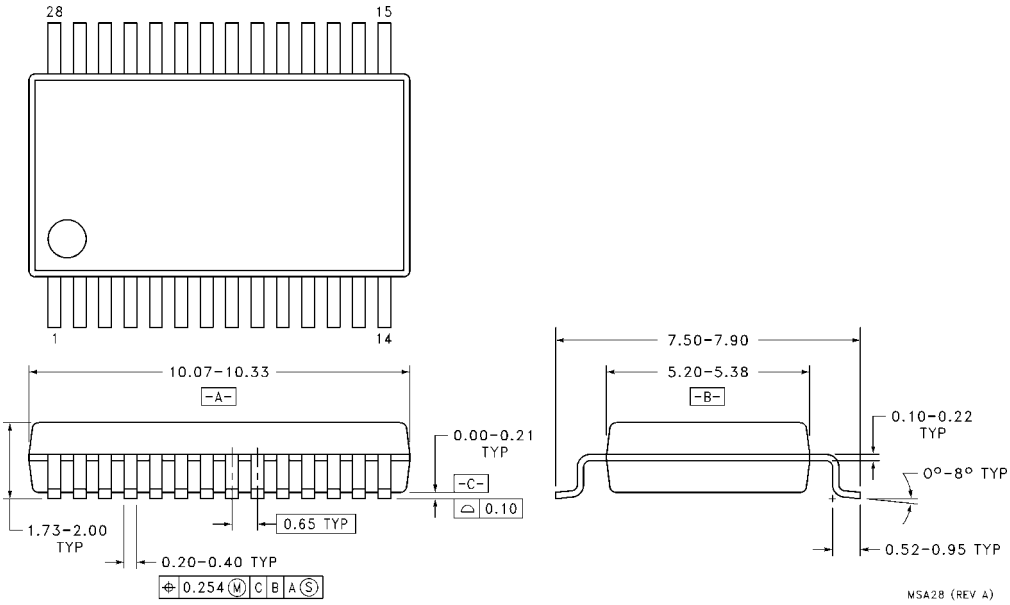


FIGURE 21. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

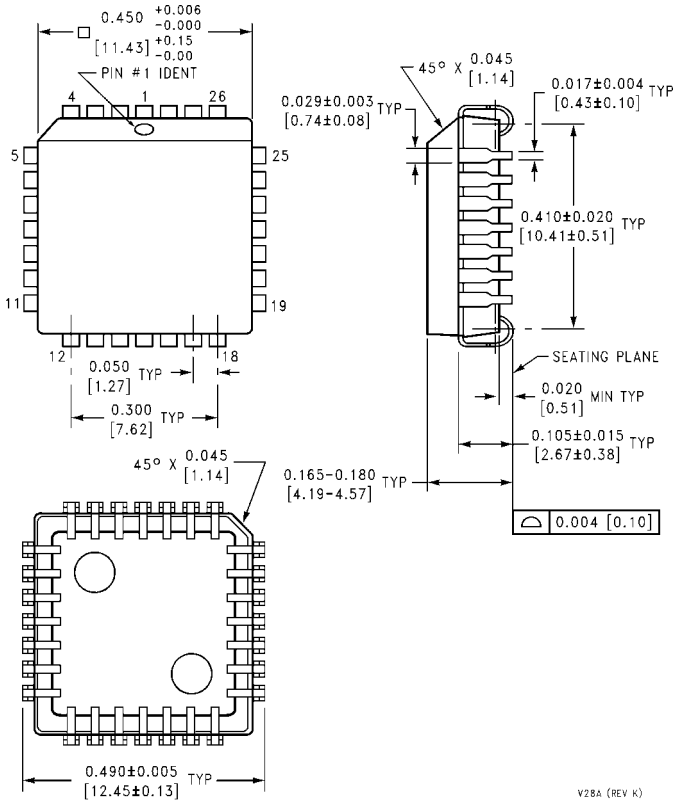


28-Lead Small Outline Integrated Circuit (SOIC), MS-013, 0.300" Wide Body
Package Number M28B



28-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA28

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450" Square
Package Number V28A

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