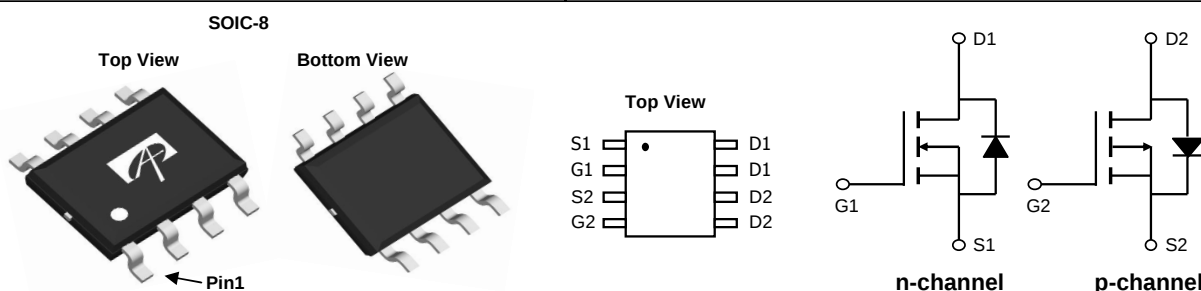


General Description

The AO4622 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

Product Summary

N-Channel	P-Channel
V_{DS} (V) = 20V	-20V
I_D = 7.3A ($V_{GS}=4.5V$)	-5A ($V_{GS}=-4.5V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 23m Ω ($V_{GS}=10V$)	< 53m Ω ($V_{GS} = -4.5V$)
< 30m Ω ($V_{GS}=4.5V$)	< 87m Ω ($V_{GS} = -2.5V$)
< 84m Ω ($V_{GS}=2.5V$)	
100% UIS Tested	100% UIS Tested
100% Rg Tested	100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 16	± 12	V
Continuous Drain Current ^A	I_D	7.3	-5	A
Current ^A	I_D	6.2	-4.2	A
Pulsed Drain Current ^B	I_{DM}	35	-25	A
Power Dissipation	P_D	2	2	W
Power Dissipation	P_D	1.44	1.44	W
Avalanche Current ^B	I_{AR}	13	13	A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	25	25	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	40	$^\circ\text{C/W}$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =16V, V _{GS} =0V T _J =55°C			1 5	uA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±16V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.6	1.25	2	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	35			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7.3A T _J =125°C		19 28	23 33.6	mΩ
		V _{GS} =4.5V, I _D =6.4A		24	30	mΩ
		V _{GS} =2.5V, I _D =2A		67	84	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =7.3A		17		S
V _{SD}	Diode Forward Voltage	I _S =1A		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz		900	1100	pF
C _{oss}	Output Capacitance			162		pF
C _{rss}	Reverse Transfer Capacitance			105		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.9	1.35	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =10V, I _D =6.5A		15	18	nC
Q _{g(4.5V)}	Total Gate Charge			7.2	9	nC
Q _{gs}	Gate Source Charge			1.8		nC
Q _{gd}	Gate Drain Charge			2.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =10V, R _L =1.4Ω, R _{GEN} =3Ω		4.5		ns
t _r	Turn-On Rise Time			9.2		ns
t _{D(off)}	Turn-Off DelayTime			18.7		ns
t _f	Turn-Off Fall Time			3.3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =7.3A, dI/dt=100A/μs		18		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =7.3A, dI/dt=100A/μs		9.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

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N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

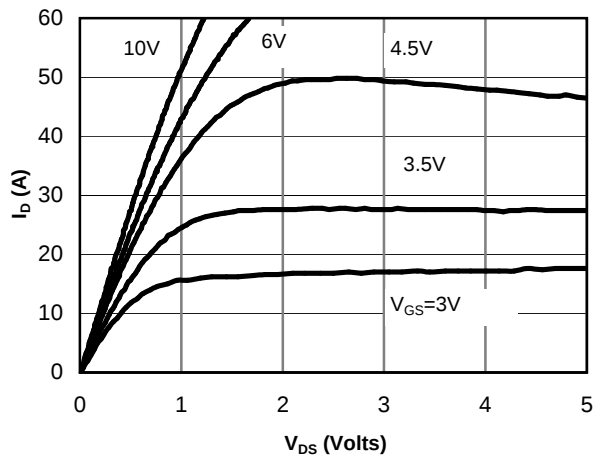


Figure 1: On-Region Characteristics

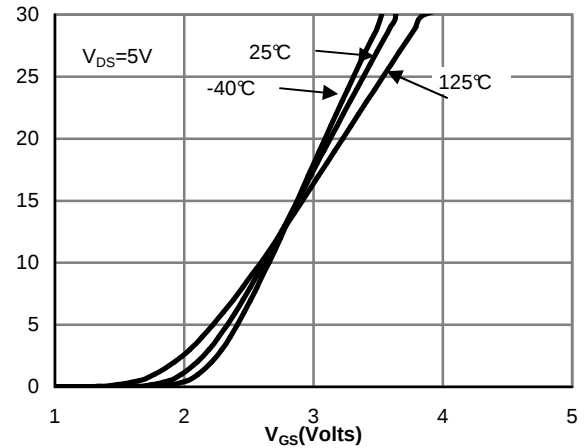


Figure 2: Transfer Characteristics

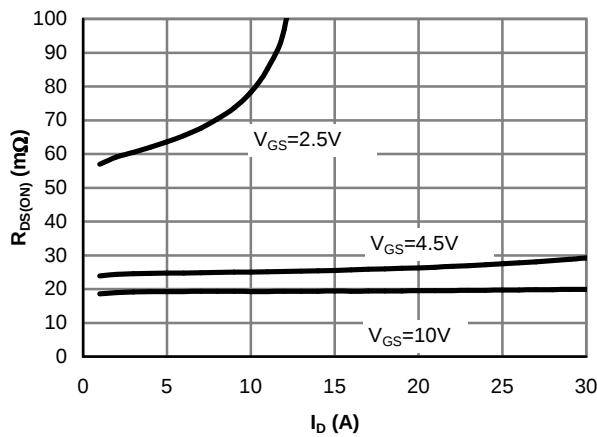


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

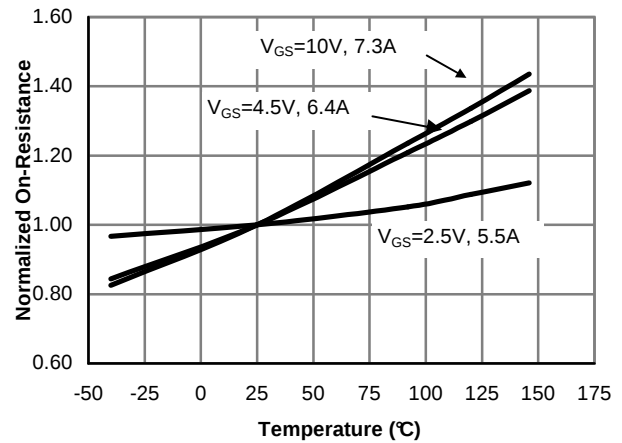


Figure 4: On-Resistance vs. Junction Temperature

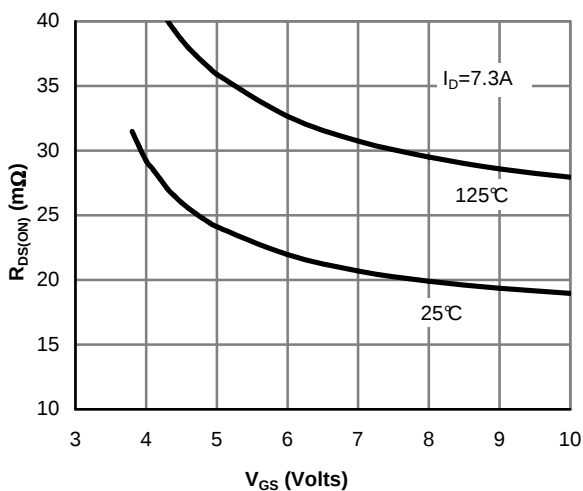


Figure 5: On-Resistance vs. Gate-Source Voltage

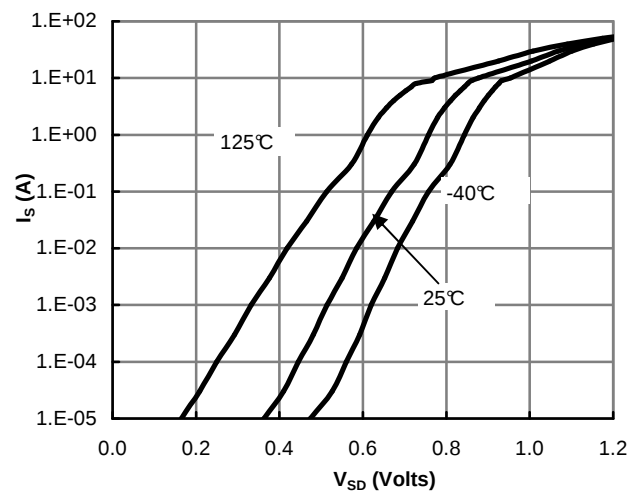
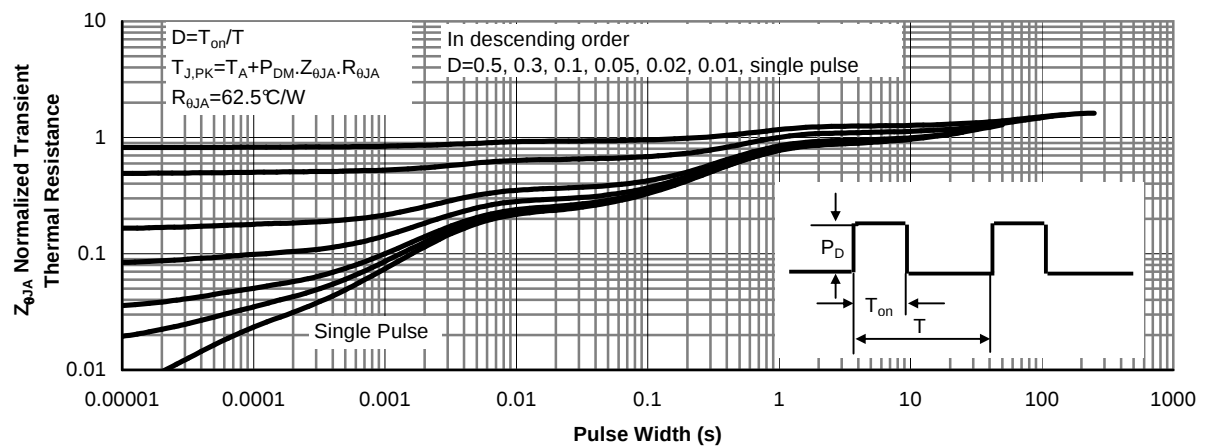
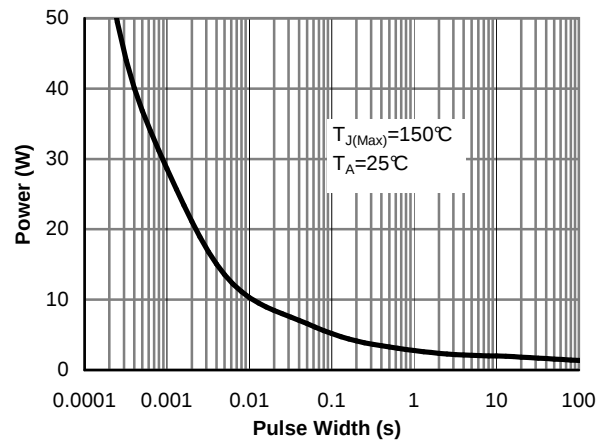
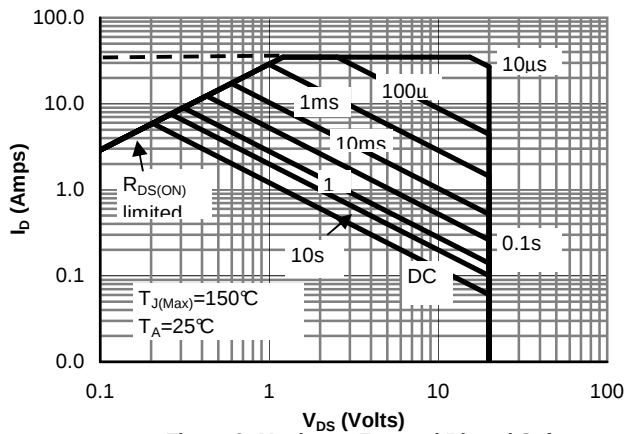
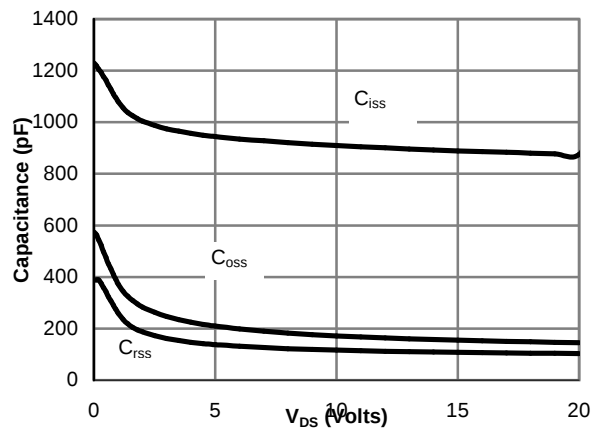
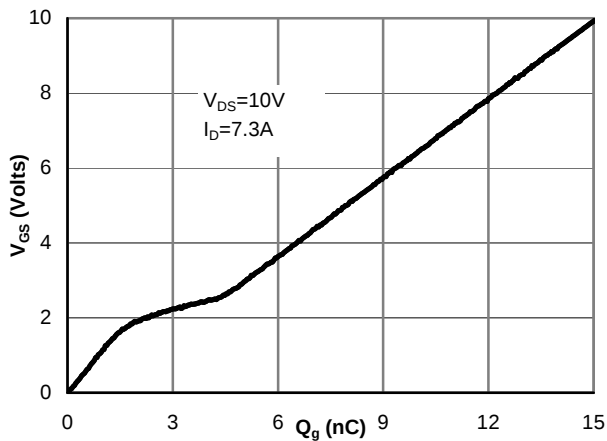
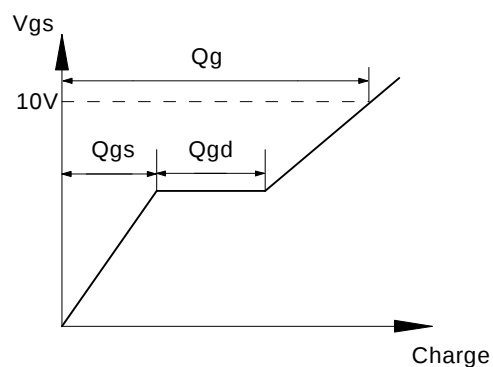
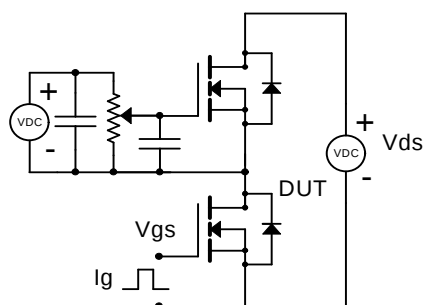


Figure 6: Body-Diode Characteristics

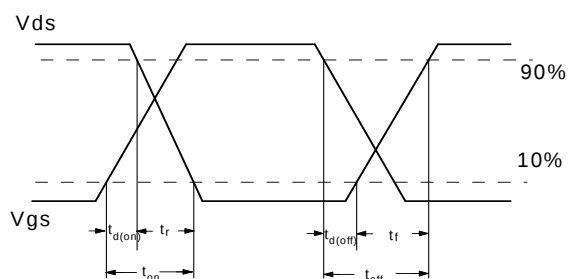
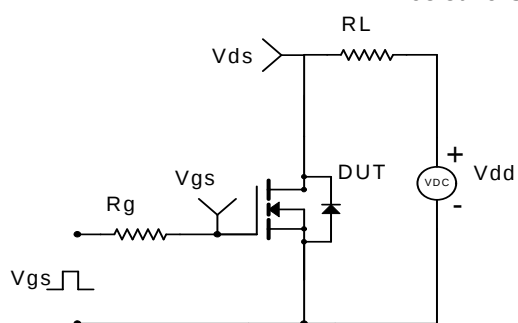
N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



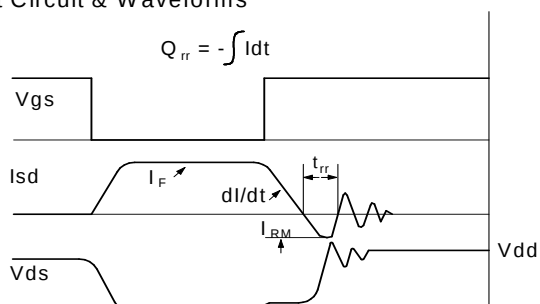
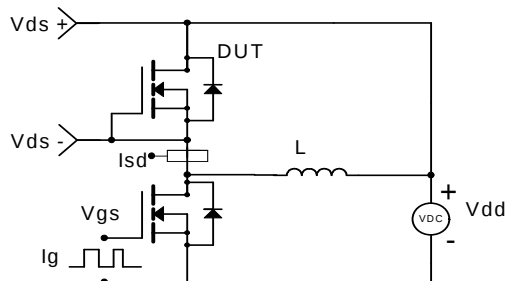
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-16V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-0.9	-0.5	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-5A T _J =125°C		44 59	53 71	mΩ
		V _{GS} =-2.5V, I _D =-4.2A		67	87	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		800	960	pF
C _{oss}	Output Capacitance			131		pF
C _{rss}	Reverse Transfer Capacitance			103		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		6.7	10	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4.5A		15.5		nC
Q _g (4.5V)	Total Gate Charge (4.5V)			7.4		nC
Q _{gs}	Gate Source Charge			1.3		nC
Q _{gd}	Gate Drain Charge			2.9		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =2Ω, R _{GEN} =3Ω		4.4		ns
t _r	Turn-On Rise Time			7.6		ns
t _{D(off)}	Turn-Off DelayTime			44		ns
t _f	Turn-Off Fall Time			13.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5A, dI/dt=100A/μs		20		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5A, dI/dt=100A/μs		9		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

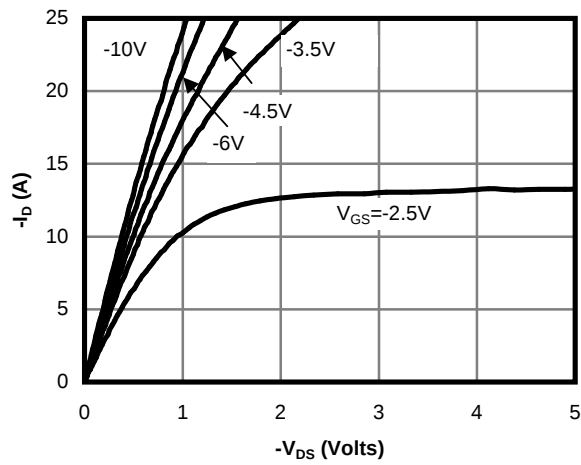


Fig 1: On-Region Characteristics

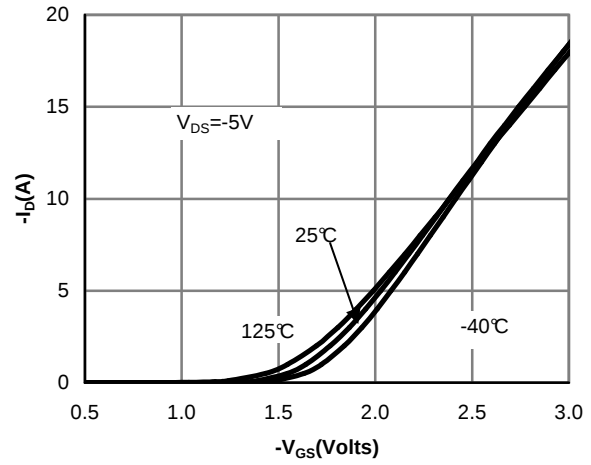


Figure 2: Transfer Characteristics

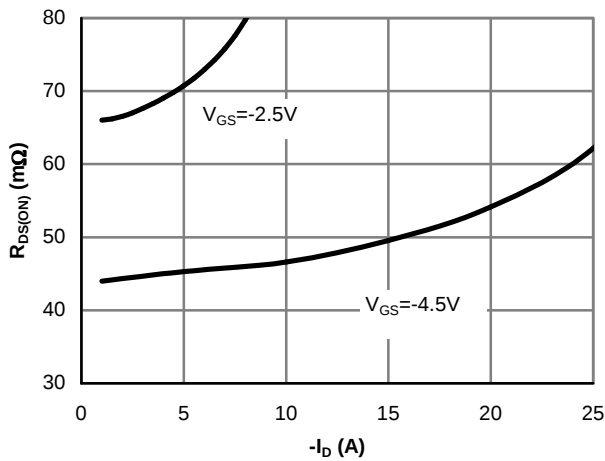


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

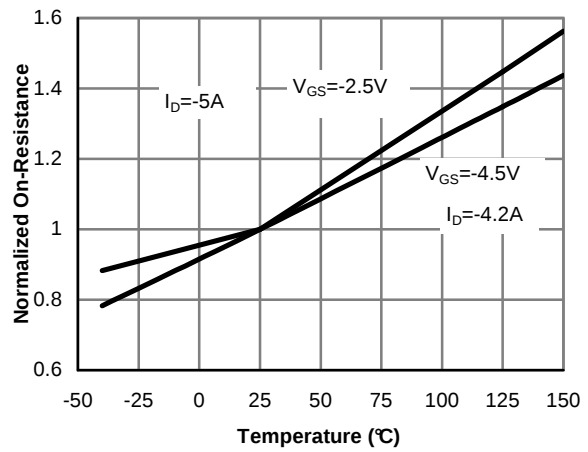


Figure 4: On-Resistance vs. Junction Temperature

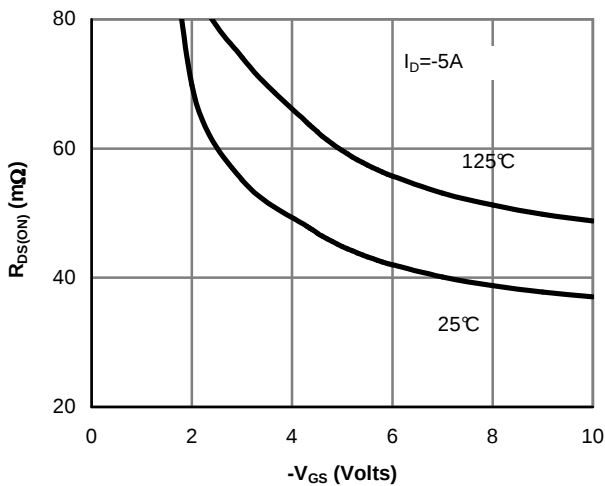


Figure 5: On-Resistance vs. Gate-Source Voltage

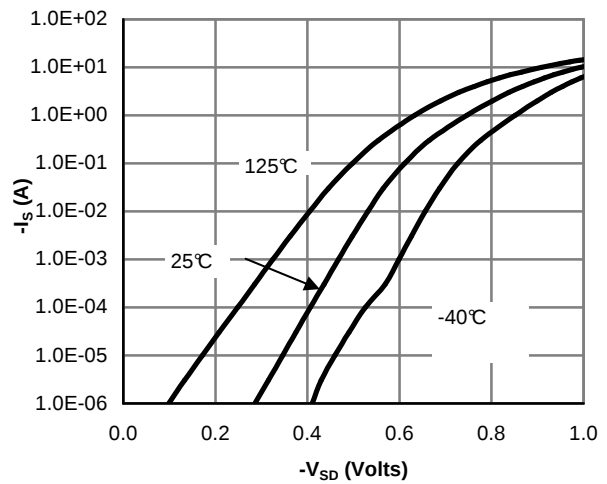


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

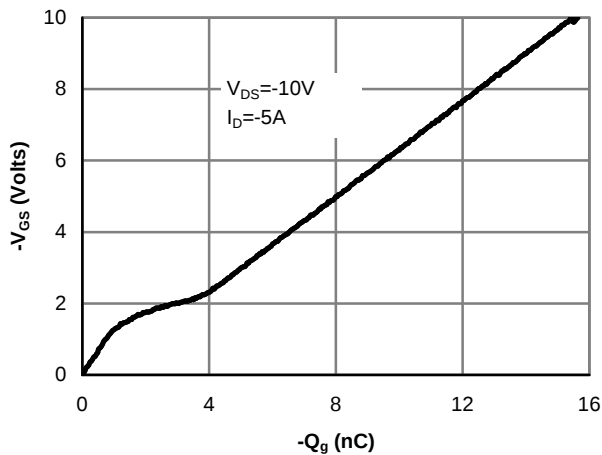


Figure 7: Gate-Charge Characteristics

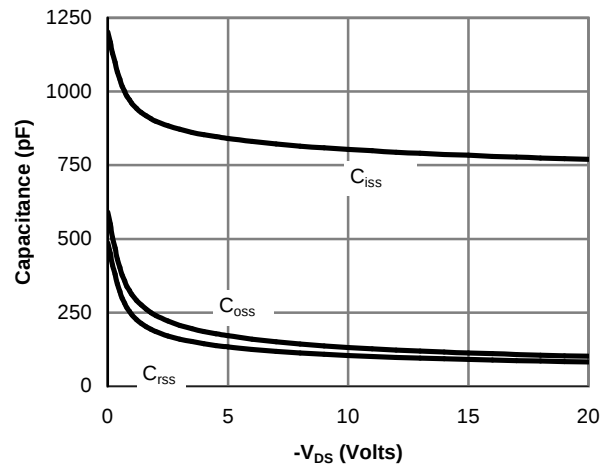


Figure 8: Capacitance Characteristics

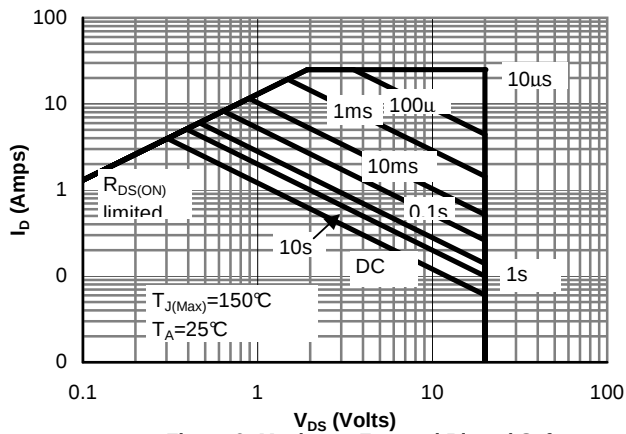


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

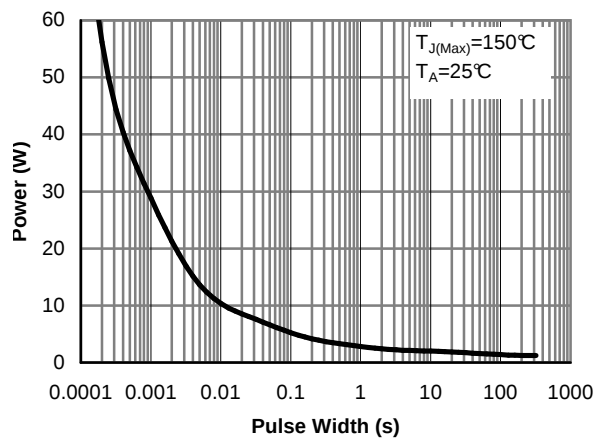


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

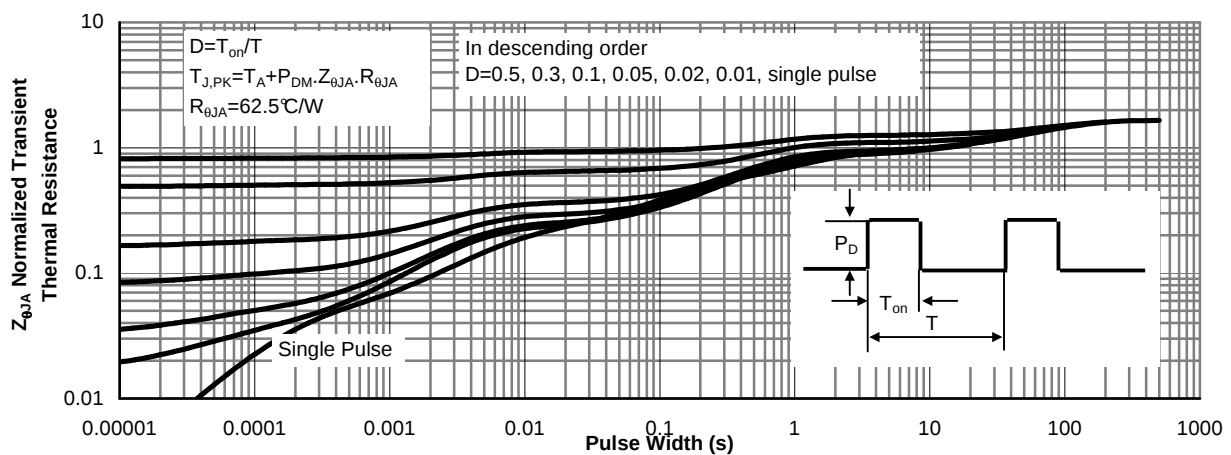
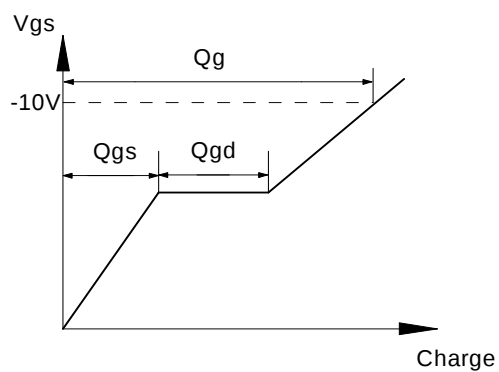
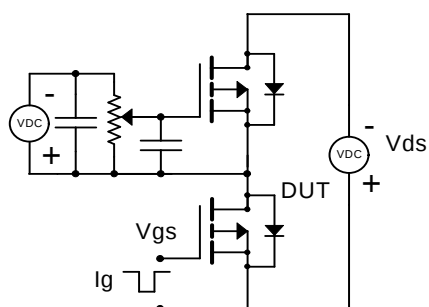
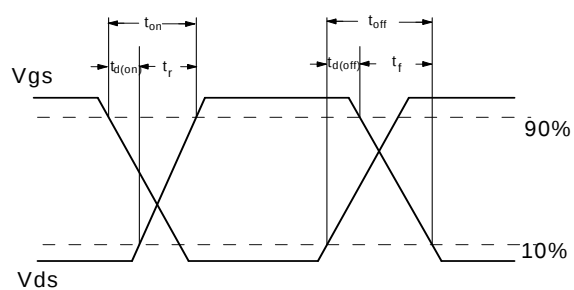
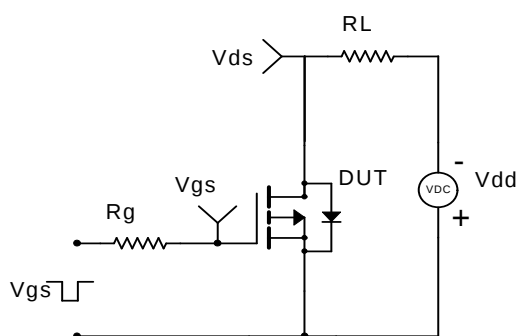


Figure 11: Normalized Maximum Transient Thermal Impedance

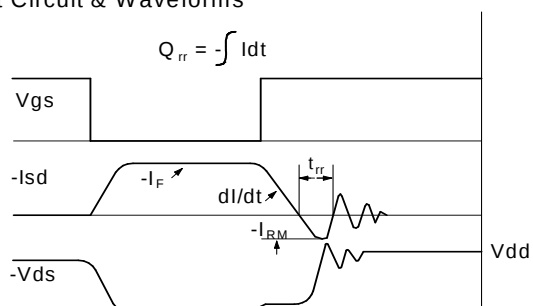
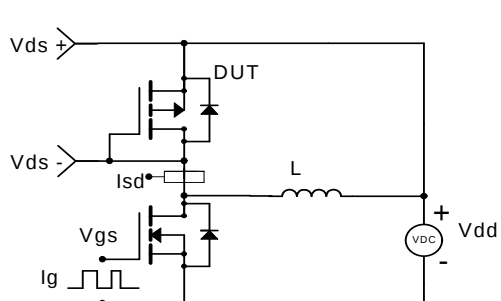
Gate Charge Test Circuit & Waveform



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