ACT8505
Radiation Hardened
64-Channel Analog Multiplexer Module
With MUX Output Monitor Function

AEROFLEX
CIRCUIT TECHNOLOGY
www.aeroflex.com

Features

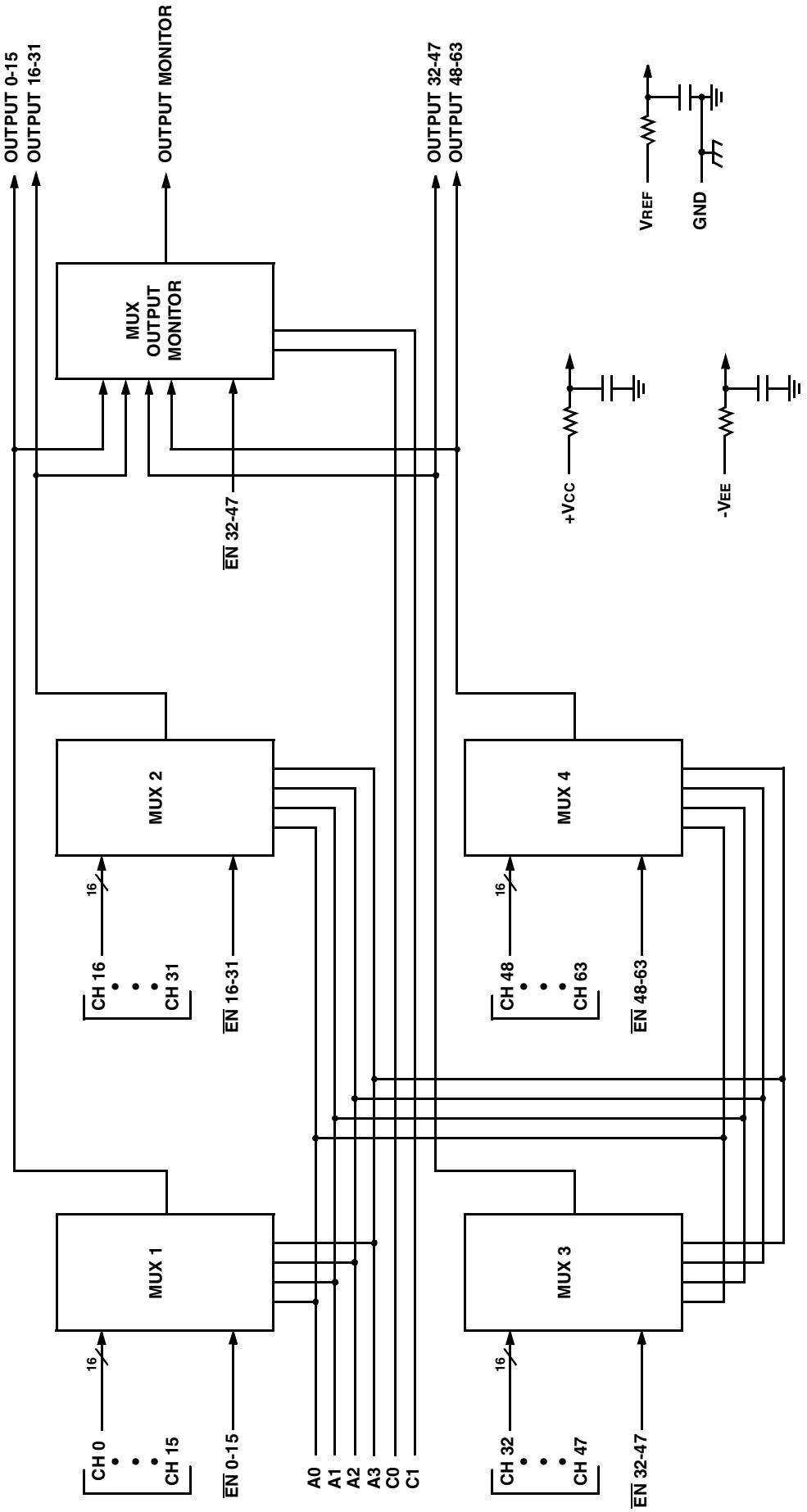
- **Radiation Environment**
  - **Radiation 300K(Si) Total Dose**
  - **No Latch-Up or SEE to 120MeV/cm^2/mg**
- **Full Military Temperature Range**
- **Low Power Consumption < 75mW, typical 50mW**
- **64 Channels Provided by Four (4) HS-1840RH Multiplexers**
- **Address Bus (A_{0-3}), and Four Enable lines afford flexible organization**
- **Output Monitoring of HS-1840RH outputs to a Fifth HS1840RH. Controlled with C_0, C_1 Address Lines.**
- **Fast Access Time 1500ns**
- **±35V Input Over Voltage Protection (Power On or Off)**
- **Break-Before-Make Switching**
- **High Analog Input Impedance (Power On or Off)**
- **Dielectrically Isolated Device Islands**
- **No Latch-Up**
- **Same *Form / Fit / Function* as ACT8504 but no input Transorbs**
- **Packaging – Hermetic Ceramic Quad Flat Pack**
  - **96 Leads, 1.32"Sq x .20"Ht Quad Flat Pack**
  - **Typical Weight 15 grams**
- **DESC SMD Pending**

AEROFLEX LABS INC. ISO 9001 CERTIFIED

General Description

Aeroflex's ACT8505 is a radiation hardened, multi-chip 64 channel multiplexer MCM (multi-chip module) for use in space applications.

The ACT8505 has been specifically designed to meet exposure to radiation environments. The multiplexer is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (QFP) and is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the ACT8505 is ideal for demanding military and space applications.



ACT8505 64 Channel Analog MUX Block Diagram

Organization and Application

The ACT8505 consists of four 16 channel muxes arranged as shown in the Block Diagram. The muxes channels 0-63 are controlled by address lines A_0 - A_3. The mux output monitor is controlled by address lines C_0, C_1.

The ACT8505 design is inherently Radiation Hard due to the HS1840RH Multiplexers as well as Microsemi Corp. Transient Suppressors (Reference Microsemi MicroNotes Series 050 - page 14).

NOTE: It is recommended that all "NC or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.

Absolute Maximum Ratings 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-55 to +150	°C
Supply Voltage +V_{CC} (Pin 44) -V_{EE} (Pin 46) V_{REF} (Pin 48)	 +20 -20 +20	 V V V
Digital Input Overvoltage V_{EN} (Pins 5, 6, 91, 92), V_A (Pins 93, 95, 1, 3), VC (Pins 2, 4)	 < V_R +4 > GND -4	 V V
Analog Input Over Voltage V_S	 ±18	 V

Notes:

1/ All measurements are made with respect to ground.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
+V_{CC}	+15V Power Supply Voltage	+15.0	V
-V_{EE}	-15V Power Supply Voltage	-15.0	V
V_{REF}	Reference Voltage	+5.00	V
V_{AL}	Logic Low Level	+0.8	V
V_{AH}	Logic High Level	+4.0	V

DC Electrical Performance Characteristics 1/

(Tc = -55°C to +125°C, +V_{EE} = +15V, -V_{EE} = -15V, V_{REF} = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Supply Current	I+	$V_{EN(0-63)}$ = $V_{A(0-3)A}$ = $V_{A(0-1)C}$ = 0	.25	2.5	mA
	I-	$V_{EN(0-63)}$ = $V_{A(0-3)A}$ = $V_{A(0-1)C}$ = 0	-2.5	-.25	mA
	+I_{SBY}	$V_{EN(0-63)}$ = 4V, $V_{A(0-3)A}$ = $V_{A(0-1)C}$ = 0 6/	0.25	2.5	mA
	-I_{SBY}	$V_{EN(0-63)}$ = 4V, $V_{A(0-3)A}$ = $V_{A(0-1)C}$ = 0 6/	-2.5	0.25	mA
Address Input Current	$I_{AL(0-3)A}$	V_A = 0V 1/	-4	4	µA
	$I_{AH(0-3)A}$	V_A = 5V 1/	-4	4	µA
	$I_{AL(0-1)C}$	V_A = 0V 1/	-1	1	µA
	$I_{AH(0-1)C}$	V_A = 5V 1/	-1	1	µA
Enable Input Current	$I_{ENL(0-15)}$	$V_{EN(0-15)}$ = 0V	-1	1	µA
	$I_{ENH(0-15)}$	$V_{EN(0-15)}$ = 5V	-1	1	µA
	$I_{ENL(16-31)}$	$V_{EN(16-31)}$ = 0V	-1	1	µA
	$I_{ENH(16-31)}$	$V_{EN(16-31)}$ = 5V	-1	1	µA
	$I_{ENL(32-47),(MUXMON)}$	$V_{EN(32-47)}$, $V_{EN(MUXMON)}$ = 0V	-2	2	µA
	$I_{ENH(32-47),(MUXMON)}$	$V_{EN(32-47)}$, $V_{EN(MUXMON)}$ = 5V	-2	2	µA
	$I_{ENL(48-63)}$	$V_{EN(48-63)}$ = 0V	-1	1	µA
	$I_{ENH(48-63)}$	$V_{EN(48-63)}$ = 5V	-1	1	µA

DC Electrical Performance Characteristics 1/ (con't)

(Tc = -55°C to +125°C, +VEE = +15V, -VEE = -15V, VREF = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Positive Input Leakage Current CH0-CH63	+ISOFFOUTPUT(ALL)	VIN = +10V, VEN = 4V, output and all unused MUX inputs under test = -10V 2/, 3/	-100	+100	nA
	+ISOFFCURRENT(ALL)		-100	+100	nA
Negative Input Leakage Current CH0-CH63	-ISOFFOUTPUT(ALL)	VIN = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 2/, 3/	-100	+100	nA
	-ISOFFCURRENT(ALL)		-100	+100	nA
Output Leakage Current OUTPUTS (pins 3,13, 23 & 33) Mux Monitor (pin 69)	+IDOFFOUTPUT(ALL)	VOUT = +10V, VEN = 4V, output and all unused MUX inputs under test = -10V 3/, 4/	-100	+100	nA
	+IDOFFCURRENT(ALL)		-100	+100	nA
Output Leakage Current OUTPUTS (pins 3,13, 23 & 33) Mux Monitor (pin 69)	-IDOFFOUTPUT(ALL)	VOUT = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 3/, 4/	-100	+100	nA
	-IDOFFCURRENT(ALL)		-100	+100	nA
Switch ON Resistance OUTPUTS (pins 25, 26, 68 & 70)	$R_{DS(ON)(0\text{-}63)_A}$	VIN = +15V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/	500	3000	Ω
	$R_{DS(ON)(0\text{-}63)_B}$	VIN = +5V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/	500	3000	Ω
	$R_{DS(ON)(0\text{-}63)_C}$	VIN = -5V, VEN = 0.8V, IOUT = +1mA 2/, 3/, 5/	500	3000	Ω
Switch ON Resistance Mux Monitor Only (pin 69) 6/	$R_{DS(ON)(MuxMon)}$	-	500	3000	Ω

Notes:

1/ Measure inputs sequentially. Ground all unused inputs of the MUX under test. VA is the applied input voltage to the MUXes' address lines A(0-5).

2/ VIN is the applied input voltage to the MUXes' input channel CH0-CH63.

3/ VEN is the applied input voltage to the MUXes' enable line En(0-15), En(16-31), En(32-47) and En(48-63).

4/ VOUT is the applied input voltage to the MUXes' output line OUTPUT(1-15), OUTPUT(16-31), OUTPUT(32-47) and OUTPUT(48-63).

5/ Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.

6/ If not tested, shall be guaranteed to the specified limits.

Switching Characteristics

(Tc = -55°C to +125°C, VDD = +15V, VEE = -15V, VR = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Switching Test MUX (For Mux Output Monitor, See Note 6/)	t_{ONA}	RL = 10KΩ, CL = 50pF	10	1500	ns
	t_{OFFA}	RL = 10KΩ, CL = 50pF	10	2000	ns
	t_{ONEN}	RL = 1KΩ, CL = 50pF	10	1500	ns
	t_{OFFEN}	RL = 1KΩ, CL = 50pF	10	1000	ns

Truth Table (CH0 – CH15)

A3	A2	A1	A0	EN(0-15)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT (0-15)

Truth Table (CH16 – CH31)

A3	A2	A1	A0	EN(16-31)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between CH16-31 and OUTPUT (16-31)

Truth Table (CH32 – CH47)

A3	A2	A1	A0	EN(32-47)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH32
L	L	L	H	L	CH33
L	L	H	L	L	CH34
L	L	H	H	L	CH35
L	H	L	L	L	CH36
L	H	L	H	L	CH37
L	H	H	L	L	CH38
L	H	H	H	L	CH39
H	L	L	L	L	CH40
H	L	L	H	L	CH41
H	L	H	L	L	CH42
H	L	H	H	L	CH43
H	H	L	L	L	CH44
H	H	L	H	L	CH45
H	H	H	L	L	CH46
H	H	H	H	L	CH47

1/ Between CH32-47 and OUTPUT (32-47)

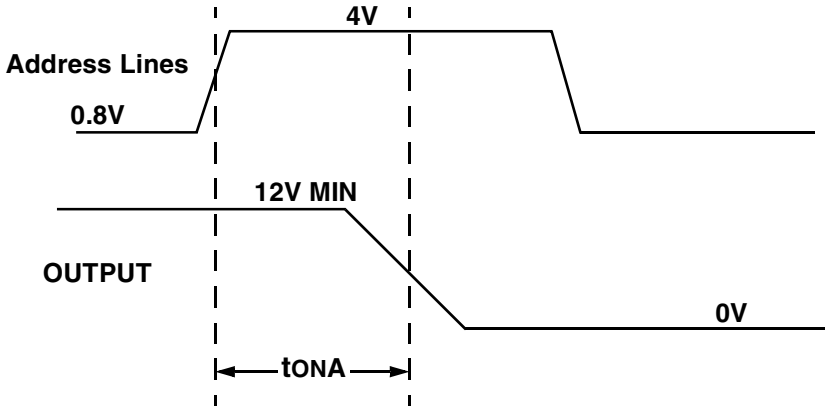
Truth Table (CH48 – CH63)

A3	A2	A1	A0	EN(47-63)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH48
L	L	L	H	L	CH49
L	L	H	L	L	CH50
L	L	H	H	L	CH51
L	H	L	L	L	CH52
L	H	L	H	L	CH53
L	H	H	L	L	CH54
L	H	H	H	L	CH55
H	L	L	L	L	CH56
H	L	L	H	L	CH57
H	L	H	L	L	CH58
H	L	H	H	L	CH59
H	H	L	L	L	CH60
H	H	L	H	L	CH61
H	H	H	L	L	CH62
H	H	H	H	L	CH63

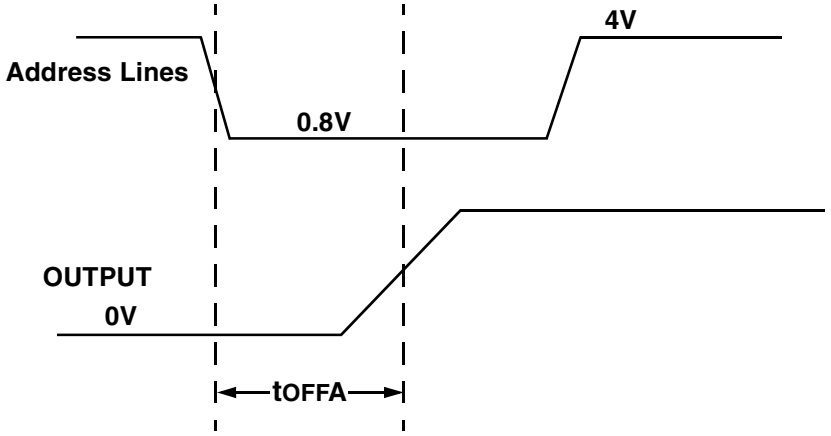
1/ Between CH48-63 and OUTPUT (48-63)

Truth Table (Mux Output Monitor)

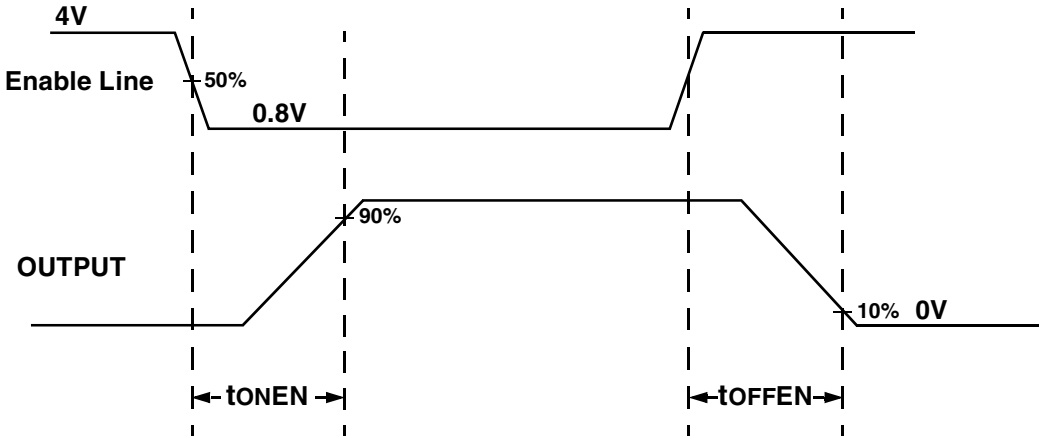
C1	C0	EN(32-47)	"ON" CHANNEL
X	X	H	NONE
L	L	L	Output Channels 0-15
L	H	L	Output Channels 16-31
H	L	L	Output Channels 32-47
H	H	L	Output Channels 48-63



Definition of t_{ONA}



Definition of t_{OFFA}



Definition of t_{ONEN} and t_{OFFEN}

Lead Numbers & Functions

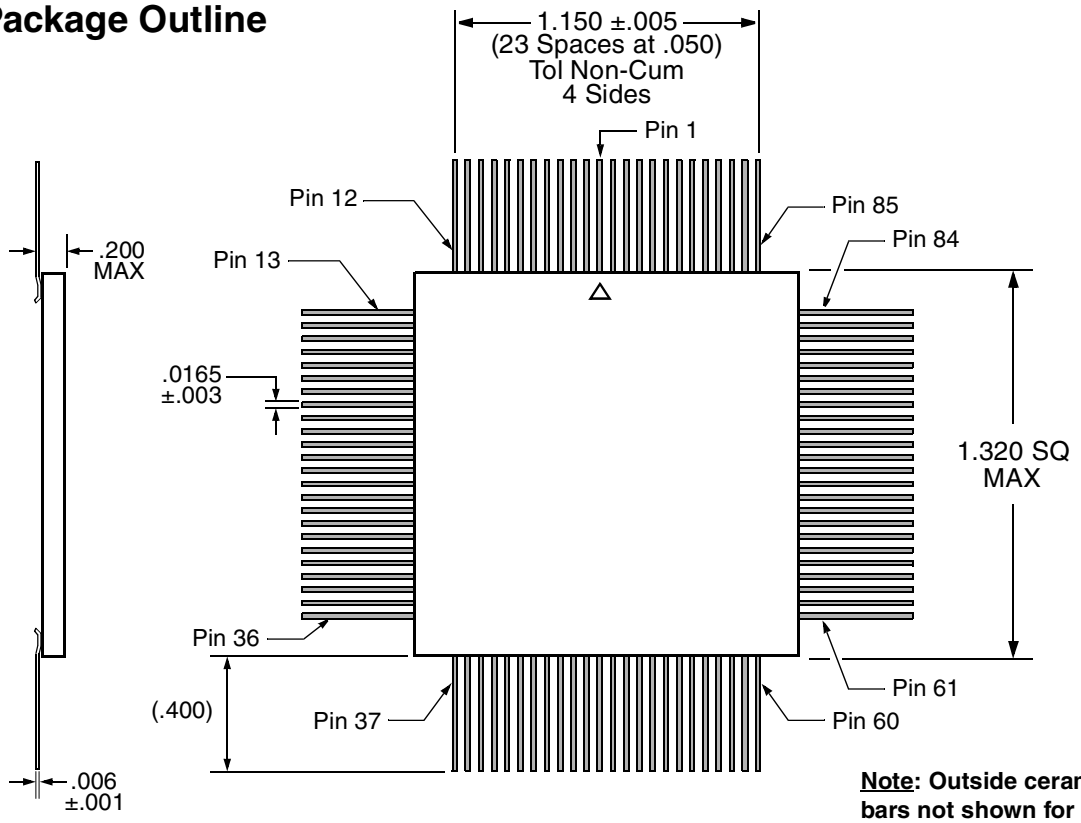
ACT8505 – 96 Leads Ceramic QUAD Flat Pack					
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
1	A_2	33	CH11	65	CH49
2	C_0	34	CH27	66	CH48
3	A_3	35	CH12	67	NC
4	C_1	36	CH28	68	Output V(48-63)
5	$\overline{EN}$ 0-15	37	CH13	69	Mux Output Monitor
6	$\overline{EN}$ 16-31	38	CH29	70	Output V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	$+V_{CC}$	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	$-V_{EE}$	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	V_{REF}	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	CASE GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	Output V(0-15)	57	CH57	89	GND
26	Output V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ 48-63
28	CH24	60	CH54	92	$\overline{EN}$ 32-47
29	CH9	61	CH53	93	A_0
30	CH25	62	CH52	94	NC
31	CH10	63	CH51	95	A_1
32	CH26	64	CH50	96	NC

NOTE: It is recommended that all "NC or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.

Ordering Information

Model Number	Screening	DESC SMD #	Package
ACT8505-S	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883 IAW MIL-PRF-38534 Class K	Pending	QUAD Flat Pack
ACT8505	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883 IAW MIL-PRF-38534 Class H		
ACT8505-7	Commercial Flow, +25°C testing only	NA	
ACT8505-T	Commercial Flow, -55°C to +125°C testing only		
ACT8505-I	Commercial Flow, -40°C to +85°C testing only		
ACT8505-C	Commercial Flow, -0°C to +70°C testing only		

Flat Package Outline



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details

Specifications subject to change without notice

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