High Performance ISM Band ASK/FSK/GFSK Transmitter IC

ADF7011

FEATURES

Single Chip Low Power UHF Transmitter
Frequency Band
  433 MHz to 435 MHz
  868 MHz to 870 MHz
On-Chip VCO and Fractional-N PLL
2.3 V to 3.6 V Supply Voltage
Programmable Output Power
  –16 dBm to +12 dBm, 0.3 dB Steps
Data Rates up to 76.8 kbps
Low Current Consumption
  29 mA at +10 dBm at 433.92 MHz
Power-Down Mode (<1 μA)
24-Lead TSSOP Package Hooks to External VCO for
  < 1.4 GHz Operation

APPLICATIONS

Low Cost Wireless Data Transfer
Wireless Metering
Remote Control/Security Systems
Keyless Entry

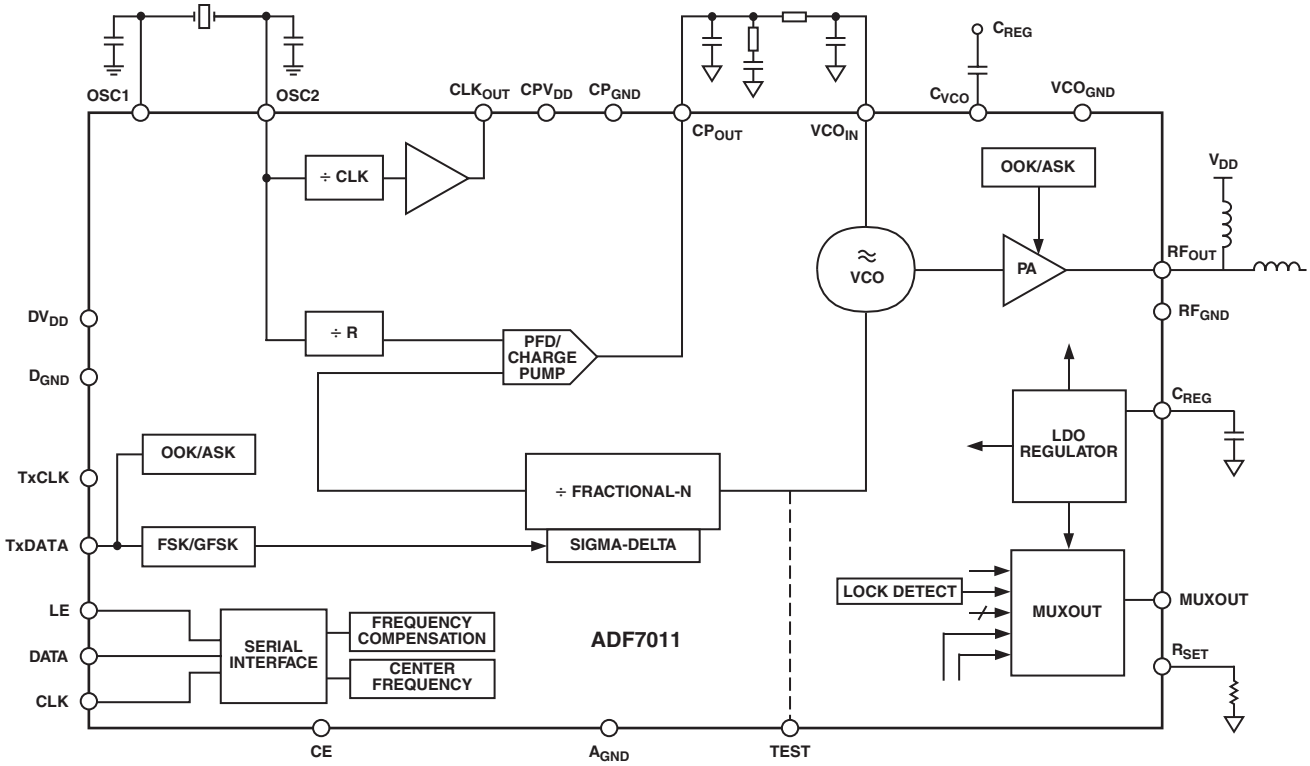
GENERAL DESCRIPTION

The ADF7011 is a low power OOK/ASK/FSK/GFSK UHF transmitter designed for use in ISM band systems. It contains and integrated VCO and Σ-Δ fractional-N PLL. The output power, channel spacing, and output frequency are programmable with four 24-bit registers. The fractional-N PLL enables the user to select any channel frequency within the European 433 MHz and 868 MHz bands, allowing the use of the ADF7011 in frequency hopping systems. The fractional-N also allows the transmitter to operate in the less congested sub-bands of the 868 MHz to 870 MHz SRD band.

It is possible to choose from the four different modulation schemes: Binary or Gaussian Frequency Shift Keying (FSK/GFSK), Amplitude Shift Keying (ASK), or On/Off Keying (OOK). The device also features a crystal compensation register that can provide ±1 ppm resolution in the output frequency. Indirect temperature compensation of the crystal can be accomplished inexpensively using this register.

Control of the four on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.3 V to 3.6 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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ADF7011–SPECIFICATIONS[1]

(V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C, FPFD = 4 MHz @ 433 MHz, FPFD = 22.1184/5.)

Parameter	Min	Typ	Max	Unit
RF CHARACTERISTICS				
Output Frequency Ranges				
Lower SRD Band	433		435	MHz
Upper SRD Band	868		870	MHz
Phase Frequency Detector Frequency	3.4		20	MHz
TRANSMISSION PARAMETERS				
Transmit Rate[2]				
FSK	0.3		76.8	kbits/s
ASK	0.3		9.6	kbits/s
GFSK	0.3		76.8	kbits/s
Frequency Shift Keying				
FSK Separation[3]	1		110	kHz using 3.625 MHz PFD
	4.88		620	kHz using 20 MHz PFD
Gaussian Filter βt		0.5		
Amplitude Shift Keying Depth			28	dB
On/Off Keying			40	dB
Output Power (No Filtering)[4]				
868 MHz			3	dBm
433 MHz			10	dBm
Output Power Variation				
Max Power Setting	9	12		dBm V_{DD} = 3.6 V
Max Power Setting		11		dBm V_{DD} = 3.0 V
Max Power Setting		9.5		dBm V_{DD} = 2.3 V
Programmable Step Size				
–16 dBm to +12 dBm		0.3125		dB
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.7 \times V_{DD}$			V
V_{INL}, Input Low Voltage			$0.2 \times V_{DD}$	V
I_{INH}/I_{INL}, Input Current			±1	µA
C_{IN}, Input Capacitance			10	pF
Control Clock Input			50	MHz
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	$DV_{DD} - 0.4$			V, I_{OH} = 500 µA
V_{OL}, Output Low Voltage			0.4	V, I_{OL} = 500 µA
CLK_{OUT} Rise/Fall Time		16		ns F_{CLK} = 4.8 MHz into 10 pF
CLK_{OUT} Mark: Space Ratio		50:50		
POWER SUPPLIES				
Voltage Supply				
DV_{DD}	2.3		3.6	V
Transmit Current Consumption				
433 MHz				
0 dBm (1 mW)		17		mA
10 dBm (10 mW)		29		mA
868 MHz				
0 dBm (1 mW)		19		mA
3 dBm (2 mW)		20.5		mA
10 dBm (10 mW)		34		mA
Crystal Oscillator Block Current Consumption		190		µA
Regulator Current Consumption		280		µA
Power-Down Mode				
Low Power Sleep Mode		0.2	1	µA

Parameter	Min	Typ	Max	Unit
PHASE-LOCKED LOOP				
VCO Gain 433 MHz/868 MHz		40/80		MHz/V @ 868 MHz
Phase Noise (In-Band)[5] 433 MHz		–81		dBc/Hz @ 5 kHz offset
Phase Noise (Out-of-Band)[6]		–90		dBc/Hz @ 1 MHz offset
Phase Noise (In-Band)[7] 868 MHz		–83		dBc/Hz @ 5 kHz offset
Phase Noise (Out-of-Band)[8]		–95		dBc/Hz @ 1 MHz offset
				100 kHz loop BW
Spurious[9, 10]				
47–74, 87.5–118, 174–230, 470–862 MHz			–54	dBm
9 kHz – 1 GHz			–36	dBm
Above 1 GHz			–30	dBm. Assumes external harmonic filter.
Harmonics[10]				
Second Harmonic, 433 MHz/868 MHz		–23/–28	–20/–23	dBc
Third Harmonic, 433 MHz/868 MHz		–25/–29	–22/–25	dBc
Other Harmonics, 433 MHz/868 MHz		–26/–40	–23/–35	dBc
REFERENCE INPUT				
Crystal Reference				
433 MHz	1.7		22.1184	MHz
868 MHz	3.4		22.1184	MHz
External Oscillator				
Frequency	3.4		40	MHz
Input Level, High Voltage	0.7 V_{DD}			V
Input Level, Low Voltage			0.2 V_{DD}	V
FREQUENCY COMPENSATION				
Pull In Range of Register	1		100	ppm
PA CHARACTERISTICS				
RF Output Impedance				
868 MHz		16 – j33		Ω, Z_{REF} = 50 Ω
433 MHz		25 – j2.6		Ω, Z_{REF} = 50 Ω
TIMING INFORMATION				
Chip Enabled to Regulator Ready[10]		50	200	µs
Crystal Oscillator to CLK_{OUT} OK				
4 MHz Crystal		1.8		ms
22.1184 MHz Crystal		2.2		ms
TEMPERATURE RANGE – T_A	–40		+85	°C

NOTES

[1] Operating temperature range is as follows: –40°C to +85°C.

[2] Datarates should be limited to adhere to edge of band requirements in accordance with ETSI 300-220

[3] Frequency Deviation = (PFD Frequency × Mod Deviation)/2^{12}.
GFSK Frequency Deviation = (PFD Frequency × $2^{m)}/2^{12}$ where m = Mod Control.

[4] The output power is limited by the spurious requirements of ETSI at +55°C. The addition of an output filter (see Applications section) will allow increased output levels to >10 dBm at both 433 MHz and 868 MHz

[5] V_{DD} = 3 V, PFD = 4 MHz, PA = 10 dBm

[6] V_{DD} = 3 V, Loop Filter BW = 100 kHz

[7] V_{DD} = 3 V, PFD = 4.42368 MHz, PA = 3 dBm

[8] V_{DD} = 3 V, Loop Filter BW = 100 kHz

[9] These spurious levels are based on a maximum output power of +3 dBm for 868 MHz and +10 dBm for 433 MHz. It assumes a PFD frequency of <5 MHz. Recommended PFD frequencies are 4.42368 MHz (22.1184/5) for 868 MHz, and 4 MHz for 433 MHz operation. Compliance for higher output powers will require an external filter. See Applications section.

[10] Not production tested. Based on characterization.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 3 V ± 10%; VGND = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulsewidth

Guaranteed by design but not production tested.
Specifications subject to change without notice.

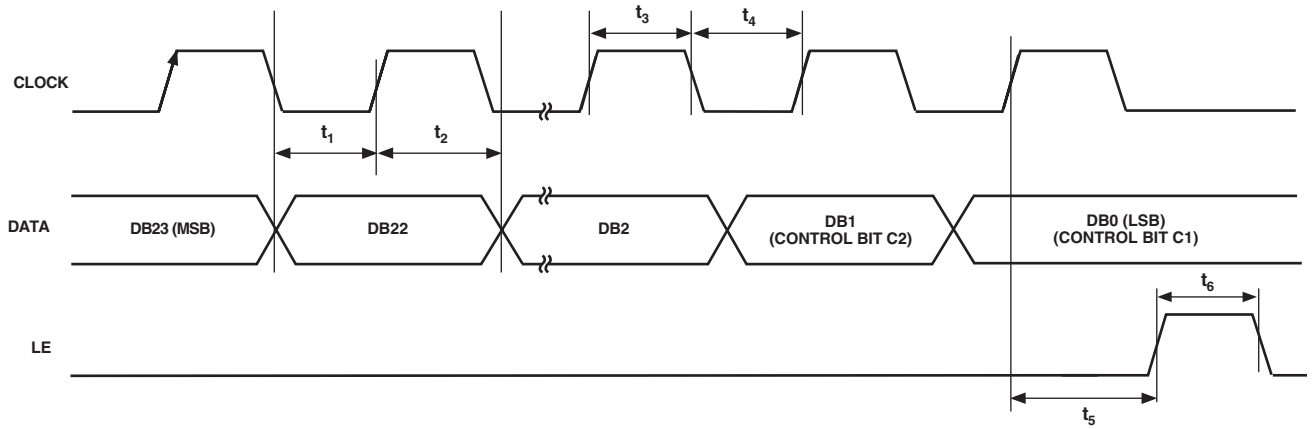


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND[3] . . . . . –0.3 V to + 7 V
CPV_{DD} to GND . . . . . –0.3 V to + 7 V
Digital I/O Voltage to GND . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +125°C
Maximum Junction Temperature . . . . . 125°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) . . . . . 235°C
  Infrared (15 sec) . . . . . 240°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] This device is a high performance RF integrated circuit with an ESD rating of <1 kV and is ESD sensitive. Proper precautions should be taken for handling and assembly.
[3] GND = VCOGND = CPGND = RFGND = DGND = AGND = 0 V.

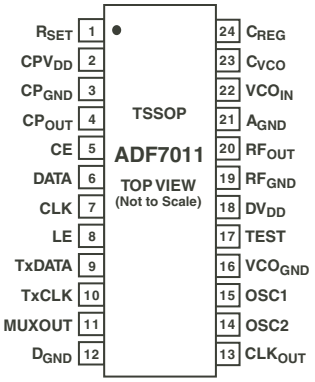
ORDERING GUIDE

Model	Temperature Range	Package Option
ADF7011BRU	–40°C to +85°C	RU-24 (TSSOP)
ADF7011BRU-REEL	–40°C to +85°C	RU-24 (TSSOP)
ADF7011BRU-REEL7	–40°C to +85°C	RU-24 (TSSOP)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF7011 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

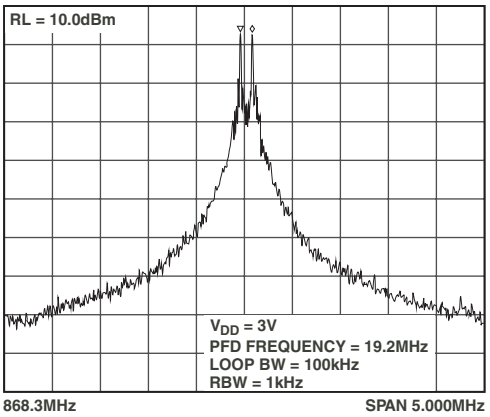


PIN FUNCTION DESCRIPTIONS

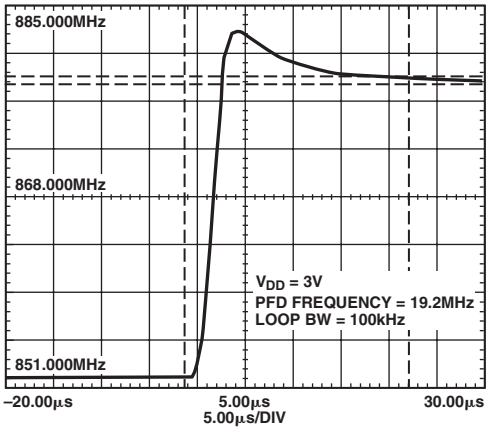
Pin No.	Mnemonic	Function
1	R_{SET}	External Resistor to Set Change Pump Current and Some Internal Bias Currents. Use 4.7 kΩ as default: $I_{CP\ MAX} = \frac{9.5}{R_{SET}}$ So, with R_{SET} = 4.7 kΩ, $I_{CP\ MAX}$ = 2.02 mA.
2	CPV_{DD}	Charge Pump Supply. This should be biased at the same level as RF_{OUT} and DV_{DD}. The pin should be decoupled with a 0.1 µF capacitor as close to the pin as possible.
3	CP_{GND}	Charge Pump Ground.
4	CP_{OUT}	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
5	CE	Chip Enable. A logic low applied to this pin powers down the part. This must be high for the part to function. This is the only way to power down the regulator circuit.
6	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This is a high impedance CMOS input.
7	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
8	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
9	TxDATA	Digital data to be transmitted is input on this pin.
10	TxCLK	GFSK Only. This clock output is used to synchronize microcontroller data to the TxDATA pin of the ADF7011. The clock is provided at the same frequency as the data rate.
11	MUXOUT	This multiplexer output allows either the digital lock detect (most common), the scaled RF, or the scaled reference frequency to be accessed externally. Used commonly for system debug. See the Function Register Map.
12	D_{GND}	Ground Pin for the RF Digital Circuitry.
13	CLK_{OUT}	The Divided Down Crystal Reference with 50:50 Mark-Space Ratio. May be used to drive the clock input of a microcontroller. To reduce spurious components in the output spectrum, the sharp edges can be reduced with a series RC. For 4.8 MHz output clock, a series 50 Ω into 10 pF will reduce spurs to < –50 dBc. Defaults on power-up to divide by 16.
14	OSC2	Oscillator Pin. If a single-ended reference (such as a TCXO) is used, it should be applied to this pin. When using an external signal generator, a 51 Ω resistor should be tied from this pin to ground. The $\overline{XOE}$ bit in the R register should set high when using an external reference.

PIN FUNCTION DESCRIPTIONS (continued)

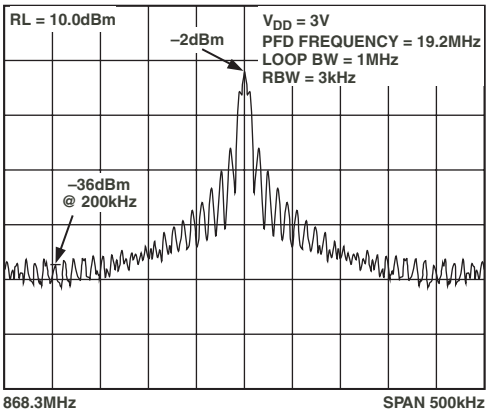
Pin No.	Mnemonic	Function
15	OSC1	Oscillator Pin. For use with crystal reference only. This is three-stated when an external reference oscillator is used.
16	VCO_{GND}	Voltage Controlled Oscillator Ground.
17	TEST	Input to the RF Fractional-N Divider. This pin allows the user to connect an external VCO to the part. Disabling the internal VCO activates this pin. If the internal VCO is used, this pin should be grounded.
18	DV_{DD}	Positive Supply for the Digital Circuitry. This must be between 2.3 V and 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
19	RF_{GND}	Ground for Output Stage of Transmitter.
20	RF_{OUT}	The modulated signal is available at this pin. Output power levels are from –16 dBm to +12 dBm. The output should be impedance matched to the desired load using suitable components. See the RF Output Stage section.
21	A_{GND}	Ground Pin for the RF Analog Circuitry.
22	VCO_{IN}	The tuning voltage on this pin determines the output frequency of the Voltage Controlled Oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
23	C_{VCO}	A 0.22 µF capacitor should be added to reduce noise on VCO bias lines. Tied to the C_{REG} pin.
24	C_{REG}	A 2.2 µF capacitor should be added at C_{REG}, tied to GND, to reduce regulator noise and improve stability. A reduced capacitor will improve regulator power-on time but may cause higher spurious components.



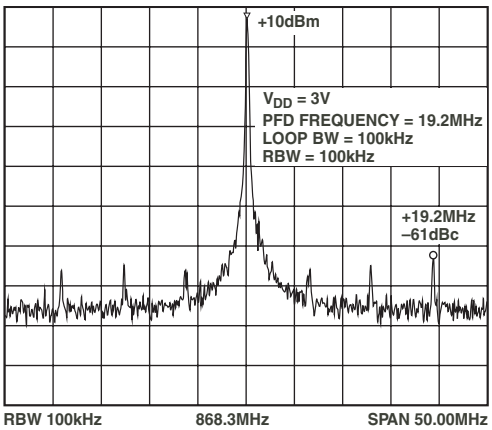
TPC 1. FSK Modulated Signal, $F_{DEVIATION}$ = 58 kHz, Data Rate = 19.2 kbps, 10 dBm



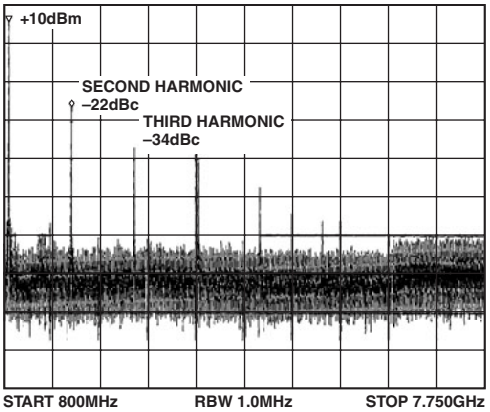
TPC 4. PLL Settling Time, 852 MHz to 878 MHz, 23 µs (±400 kHz)



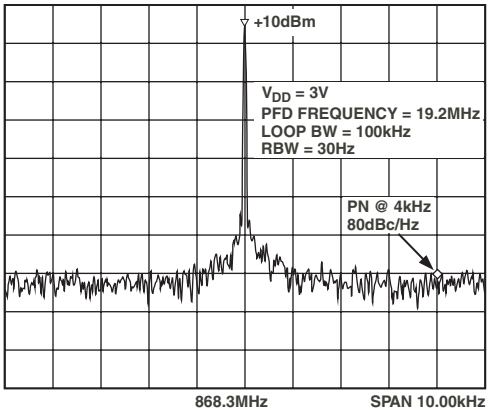
TPC 2. OOK Modulated Signal, Data Rate = 4.8 kbps, 4 dBm



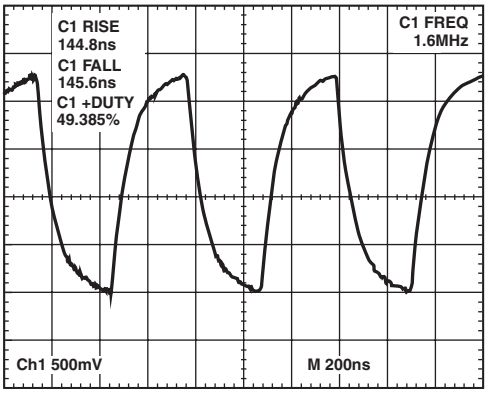
TPC 5. PFD Spurious/Fractional Spurious Components



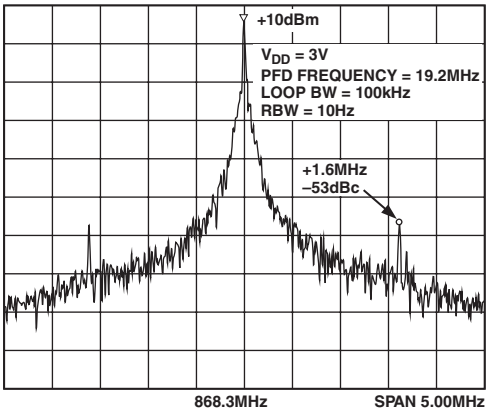
TPC 3. Harmonic Levels at 10 dBm Output Power. See Figure 15.



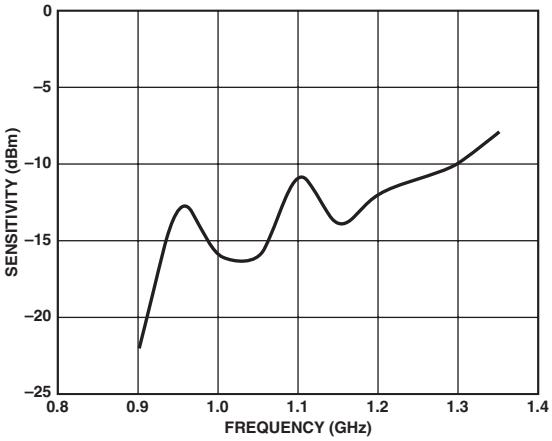
TPC 6. In-Band Phase Noise



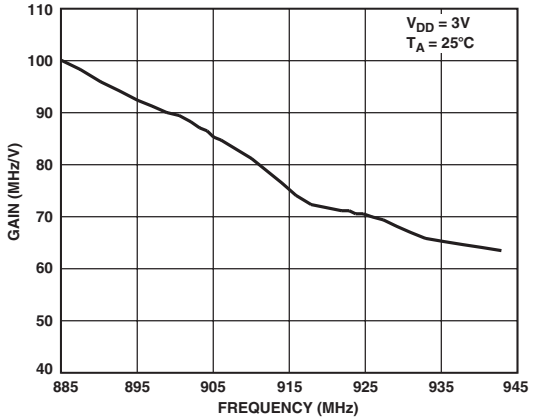
TPC 7. 1.6 MHz $CLOCK_{OUT}$ Waveform



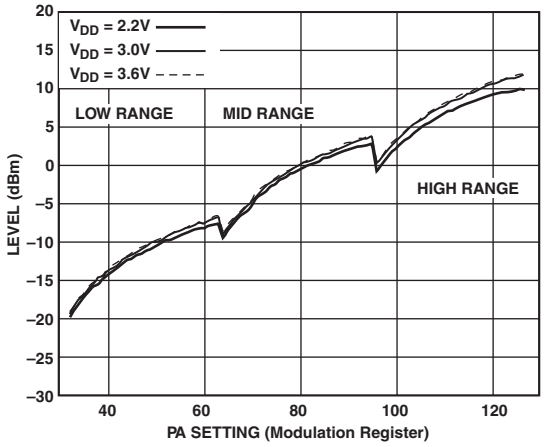
TPC 8. Spurious Signal Generated by $CLOCK_{OUT}$



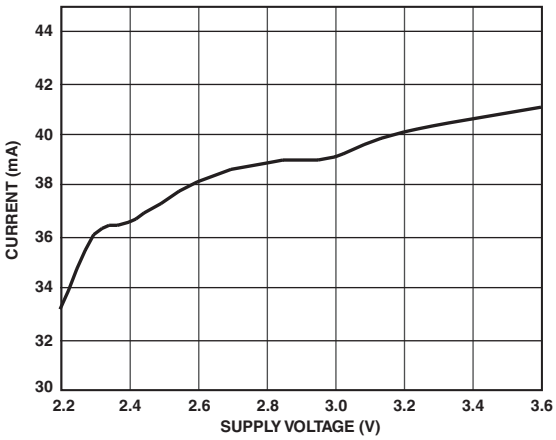
TPC 9. N-Divider Input Sensitivity



TPC 10. Typical VCO Gain



TPC 11. PA Output Programmability, T_A = 25°C



TPC 12. I_{DD} vs. V_{DD} @ 10 dBm

REGISTER MAPS

RF R REGISTER

RESERVED		CLK_{OUT}				$\overline{XOE}$	4-BIT R-VALUE				11-BIT FREQUENCY ERROR CORRECTION											CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R2	R1	CL4	CL3	CL2	CL1	X1	R4	R3	R2	R1	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

RF N REGISTER

LD PRECISION	VCO BAND	8-BIT INTEGER-N								12-BIT FRACTIONAL-N												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LDP	V1	N8	N7	N6	N5	N4	N3	N2	N1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

MODULATION REGISTER

PRE-SCALER	INDEX COUNTER		GFSK MOD CONTROL			MODULATION DEVIATION							POWER AMPLIFIER							MODULATION SCHEME		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	IC2	IC1	MC3	MC2	MC1	D7	D6	D5	D4	D3	D2	D1	P7	P6	P5	P4	P3	P2	P1	S2	S1	C2 (1)	C1 (0)

FUNCTION REGISTER

TEST MODES									MUXOUT				VCO DISABLE	FAST LOCK		CHARGE PUMP		DATA INVERT	CLK_{OUT} ENABLE	PA ENABLE	PLL ENABLE	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T9	T8	T7	T6	T5	T4	T3	T2	T1	M4	M3	M2	M1	VP1	CP4	CP3	CP2	CP1	I1	PD3	PD2	PD1	C2 (1)	C1 (1)

RF R Register

RESERVED		CLK_{OUT}				$\overline{XOE}$	4-BIT R-VALUE				11-BIT FREQUENCY ERROR CORRECTION											CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R2	R1	CL4	CL3	CL2	CL1	X1	R4	R3	R2	R1	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

X1	$\overline{XOE}$
0	XTAL OSCILLATOR ON
1	XTAL OSCILLATOR OFF

F11	.....	F3	F2	F1	F-COUNTER OFFSET
0	.....	1	1	1	+1023
0	.....	1	1	0	+1022
0	.....	.	.	.	.
0	.....	0	0	1	+1
0	.....	0	0	0	+0
1	.....	1	1	1	−1
1	.....	1	1	0	−2
	.....	.	.	.	.
1	.....	0	0	1	−1023
1	.....	0	0	0	−1024

e.g., F-COUNTER OFFSET = −1, FRACTIONAL OFFSET = $-1/2^{15}$

CL4	CL3	CL2	CL1	CLK_{OUT} DIVIDE RATIO
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

R4	R3	R2	R1	RF R COUNTER DIVIDE RATIO
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

RF N Register

LD PRECISION	VCO BAND	8-BIT INTEGER-N								12-BIT FRACTIONAL-N												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LDP	V1	N8	N7	N6	N5	N4	N3	N2	N1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

e.g., SETTING F = 0 IN FSK MODE TURNS ON THE Σ-Δ WHILE THE PLL IS AN INTEGER VALUE

M12	M11	M10	.....	M3	M2	M1	MODULUS DIVIDE RATIO
0	0	0	.....	1	0	0	4
0	0	0	.....	1	0	1	5
0	0	0	.....	1	1	0	6
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

e.g., MODULUS DIVIDE RATIO = 2048 –> FRACTION 1/2

N8	N7	N6	N5	N4	N3	N2	N1	N COUNTER DIVIDE RATIO
0	0	0	1	1	1	1	1	31
0	0	1	0	0	0	0	0	32
0	0	1	0	0	0	0	1	33
0	0	1	0	0	0	1	0	34
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

V1	VCO BAND (MHz)
0	866–870
1	433–435

THE N VALUE CHOSEN IS A MINIMUM OF $P^2 + 3P + 3$. FOR PRESCALER = 8/9, THIS MEANS A MINIMUM N DIVIDE OF 91.

LDP	LOCK DETECT PRECISION
0	3 CYCLES < 15ns
1	5 CYCLES < 15ns

Modulation Register

PRE-SCALER	INDEX COUNTER		GFSK MOD CONTROL			MODULATION DEVIATION							POWER AMPLIFIER							MODULATION SCHEME		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	IC2	IC1	MC3	MC2	MC1	D7	D6	D5	D4	D3	D2	D1	P7	P6	P5	P4	P3	P2	P1	S2	S1	C2 (1)	C1 (0)

S2	S1	MODULATION SCHEME
0	0	FSK
0	1	GFSK
1	0	ASK
1	1	OOK

P1	RF PRESCALER
0	4/5
1	8/9

IF AMPLITUDE SHIFT KEYING SELECTED, TxDATA = 0

D7	D6	.	D2	D1	
0	0	.	X	X	PA OFF
0	1	.	0	0	−16.0dBm
0	1	.	0	1	−16+1×(10/32)
.	.	.	.	.	.
0	1	.	1	1	−16+31×(10/32)
1	0	.	0	0	−6dBm
1	0	.	0	1	−6+1×(10/32)
.	.	.	.	.	.
1	0	.	1	1	−6+1×(10/32)
1	1	.	0	0	2dBm
1	1	.	0	1	2+1×(10/32)
1	1	.	.	.	.
1	1	.	1	1	12dBm

POWER AMPLIFIER OUTPUT LEVEL

P7	P6	.	P2	P1	
0	0	.	X	X	PA OFF
0	1	.	0	0	−16.0dBm
0	1	.	0	1	−16+1×(10/32)
.	.	.	.	.	.
0	1	.	1	1	−16+31×(10/32)
1	0	.	0	0	−6dBm
1	0	.	0	1	−6+1×(10/32)
.	.	.	.	.	.
1	0	.	1	1	−6+1×(10/32)
1	1	.	0	0	2dBm
1	1	.	0	1	2+1×(10/32)
1	1	.	.	.	.
1	1	.	1	1	12dBm

IF FREQUENCY SHIFT KEYING SELECTED

D7. . . .	D3	D2	D1	F DEVIATION
0	0	0	0	PLL MODE
0	0	0	1	$1 \times F_{STEP}$
0	0	1	0	$2 \times F_{STEP}$
0	0	1	1	$3 \times F_{STEP}$
.	.	.	.	.....
1	1	1	1	$127 \times F_{STEP}$

$F_{STEP} = F_{PFD}/2^{12}$

IF GAUSSIAN FREQUENCY SHIFT KEYING SELECTED

IC2	IC1	INDEX COUNTER
0	0	16
0	1	32
1	0	64
1	1	128

D7	D3	D2	D1	DIVIDER FACTOR
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.....
1	1	1	1	127

MC3	MC2	MC1	GFSK MOD CONTROL
0	0	0	0
0	0	1	1
.	.	.	.
1	1	1	7

Function Register

TEST MODES									MUXOUT				VCO DISABLE	FAST LOCK		CHARGE PUMP		DATA INVERT	CLK_{OUT} ENABLE	PA ENABLE	PLL ENABLE	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T9	T8	T7	T6	T5	T4	T3	T2	T1	M4	M3	M2	M1	VP1	CP4	CP3	C2	C1	I1	PD3	PD2	PD1	C2 (1)	C1 (1)

VP1	VCO DISABLE
0	VCO ON
1	VCO OFF

I1	DATA INVERT
0	DATA
1	DATA

CP4	CP FLOCK DOWN
0	BLEED OFF
1	BLEED ON

PD1	PLL ENABLE
0	PLL OFF
1	PLL ON

CP3	CP FLOCK UP
0	BLEED OFF
1	BLEED ON

PD2	PA ENABLE
0	PA OFF
1	PA ON

CP2	CP1	I_{CP} (mA)		
	R_{SET}	2.7kΩ	4.7kΩ	10kΩ
0	0	0.50	0.29	0.14
0	1	1.50	0.87	0.41
1	0	2.51	1.44	0.68
1	1	3.51	2.02	0.95

PD3	CLK_{OUT} ENABLE
0	CLK_{OUT} OFF
1	CLK_{OUT} ON

M4	M3	M2	M1	MUXOUT
0	0	0	0	LOGIC LOW
0	0	0	1	LOGIC HIGH
0	0	1	0	THREE-STATE
0	0	1	1	REGULATOR READY (DEFAULT)
0	1	0	0	DIGITAL LOCK DETECT
0	1	0	1	ANALOG LOCK DETECT
0	1	1	0	R DIVIDER / 2 OUTPUT
0	1	1	1	N DIVIDER / 2 OUTPUT
1	0	0	0	RF R DIVIDER OUTPUT
1	0	0	1	RF N DIVIDER OUTPUT
1	0	1	0	DATA RATE
1	0	1	1	LOGIC LOW
1	1	0	0	LOGIC LOW
1	1	0	1	LOGIC LOW
1	1	1	0	NORMAL TEST MODES
1	1	1	1	Σ-Δ TEST MODES

Default Values for Registers

R REGISTER

RESERVED		CLK_{OUT}				$\overline{XOE}$	4-BIT R-VALUE				11-BIT FREQUENCY ERROR CORRECTION											CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	C2 (0)	C1 (0)

N REGISTER

LD PRECISION	VCO BAND	8-BIT INTEGER-N								12-BIT FRACTIONAL-N												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	C2 (0)	C1 (1)

MODULATION REGISTER

PRE-SCALER	INDEX COUNTER		GFSK MOD CONTROL			MODULATION DEVIATION							POWER AMPLIFIER							MODULATION SCHEME		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	C2 (1)	C1 (0)

FUNCTION REGISTER

TEST MODES									MUXOUT				VCO DISABLE	FAST LOCK		CHARGE PUMP		DATA INVERT	CLK_{OUT} ENABLE	PA ENABLE	PLL ENABLE	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0	C2 (1)	C1 (1)

CIRCUIT DESCRIPTION

Reference Input Section

The on-board crystal oscillator circuitry (Figure 2), allows the use of an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting $\overline{XOE}$ low. It is enabled by default on power-up and is disabled by bringing CE low. Two parallel resonant capacitors are required for oscillation at the correct frequency; the value of these is dependant on the crystal specification. Errors in the crystal can be corrected using the error correction register within the R register. A single-ended reference (TCXO, CXO) may be used. The CMOS levels should be applied to OSC2, with $\overline{XOE}$ set high.

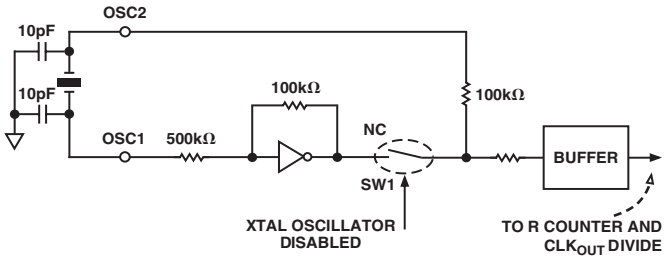


Figure 2. Oscillator Circuit on the ADF7011

CLK_{OUT} Divider and Buffer

The CLK_{OUT} circuit takes the reference clock signal from the oscillator section above and supplies a divided down 50:50 mark-space signal to the CLK_{OUT} pin. An even divide from 2 to 30 is available. This divide is set by the four MSBs in the R register. On power-up, the CLK_{OUT} defaults to divide by 16.

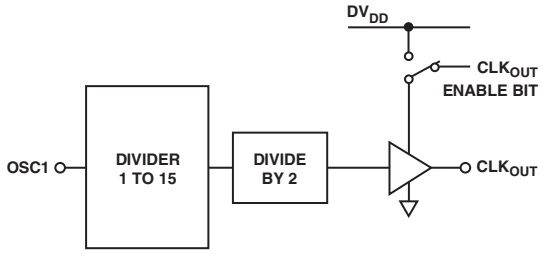


Figure 3. CLK_{OUT} Stage

The output buffer to CLK_{OUT} is enabled by setting Bit DB4 in the function register high. On power-up, this bit is set high. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at F_{CLK}.

R Counter

The 4-bit R Counter divides the reference input frequency by an integer from 1 to 15. The divided down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in the R register. Maximizing the PFD frequency reduces the N value. Having a higher PFD will result in a higher level of spurious components. A PFD of close to 4 MHz is recommended. This reduces the noise multiplied at a rate of 20 log(N) to the output, as well as reduces occurrences of spurious components. The R register defaults to R = 1 on power-up.

Prescaler, Phase Frequency Detector (PFD), and Charge Pump

The dual-modulus prescaler ($P/P + 1$) divides the RF signal from the VCO to a lower frequency that is manageable by the CMOS counters.

The PFD takes inputs from the R Counter and the N Counter ($N = Int + Fraction$) and produces an output proportional to the phase and frequency difference between them. Figure 4 is a simplified schematic.

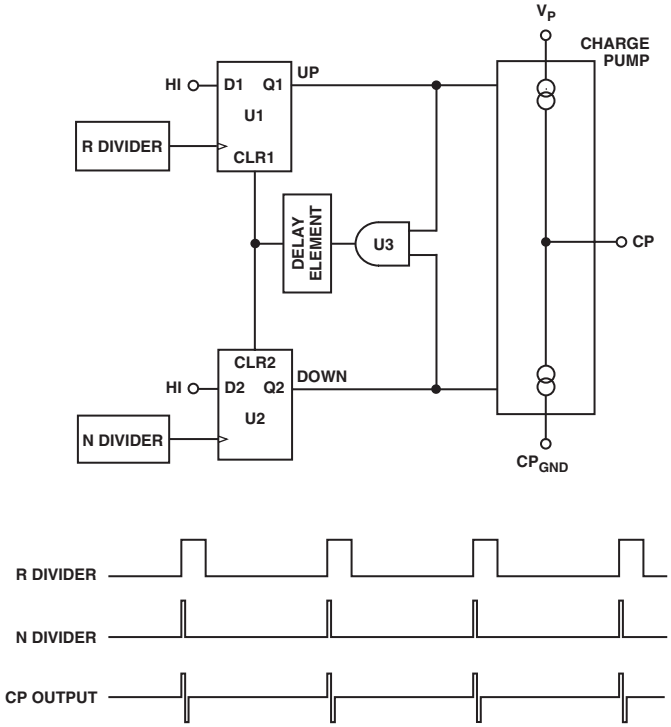


Figure 4. PFD Stage

The PFD includes a delay element that sets the width of the antibacklash pulse. The typical value for this in the ADF7011 is 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

MUXOUT and Lock Detect

The MUXOUT pin allows the user to access various internal points in the ADF7011. The state of MUXOUT is controlled by Bits M1 to M4 in the function register.

Regulator Ready

This is the default setting on MUXOUT after the transmitter has been powered up. The power-up time of the regulator is typically 50 µs. Since the serial interface is powered from the regulator, it is necessary for the regulator to be at its nominal voltage before the ADF7011 can be programmed. The status of the regulator can be monitored at MUXOUT. Once the Regulator Ready signal on MUXOUT is high, programming of the ADF7011 may begin.

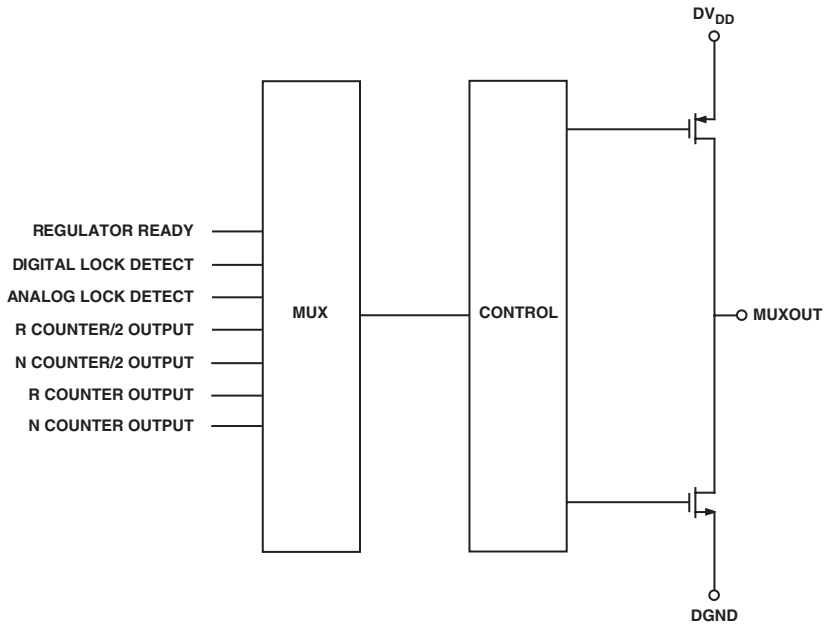


Figure 5. MUXOUT Stage

Digital Lock Detect
Digital lock detect is active high. The lock detect circuit is contained at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until 25 ns phase error is detected at the PFD. Since no external components are needed for digital lock detect, it is more widely used than analog lock detect.

Analog Lock Detect
This N-channel open-drain lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output will be high with narrow low-going pulses.

Voltage Regulator
The ADF7011 requires a stable voltage source for the VCO and modulation blocks. The on-board regulator provides 2.2 V using a band gap reference. A 2.2 µF capacitor from C_{REG} to ground is used to improve stability of the regulator over a supply ranging from 2.3 V to 3.6 V. The regulator consumes less than 400 µA and can only be powered down using the chip enable (CE) pin. Bringing CE low disables the regulator and also erases all values held in the registers. The serial interface operates off the regulator supply; therefore, to write to the part, the user must have CE high. Regulator status can be monitored using the Regulator Ready signal from MUXOUT.

Loop Filter
The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 6.

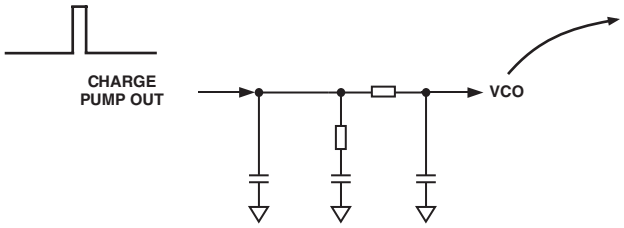


Figure 6. Typical Loop Filter Configuration—Third Order Integrator

In FSK, the loop should be designed so that the loop bandwidth (LBW) is approximately five times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies but may cause insufficient spurious attenuation.

For ASK systems, the wider the loop BW the better. The sudden large transition between two power levels will result in VCO pulling and can cause a wider output spectrum than is desired. By widening the loop BW to >10 times the data rate, the amount of the VCO pulling is reduced since the loop will quickly settle back to the correct frequency. The wider LBW may restrict the output power and data rate of ASK based systems, compared with FSK based systems.

Narrow-loop bandwidths may result in the loop taking long periods of time to attain lock. Careful design of the loop filter is critical in obtaining accurate FSK/GFSK modulation.

For GFSK, it is recommended that an LBW of 2.0 to 2.5 times the data rate be used to ensure sufficient samples are taken of the input data while filtering system noise.

Voltage Controlled Oscillator (VCO)

An on-chip VCO is included on the transmitter. The VCO converts the control voltage generated by the loop filter into an output frequency that is sent to the antenna via the power amplifier (PA). The VCO has a typical gain of 80 MHz/V and operates from 866 MHz to 870 MHz. The PD1 bit in the function register is the active high bit that turns on the VCO. A frequency divided by 2 is included to allow operation in the lower 450 MHz band. To enable operation in the lower band, the V1 bit in the N Register should be set to 1.

The VCO needs an external 220 nF between the VCO and the regulator to reduce internal noise.

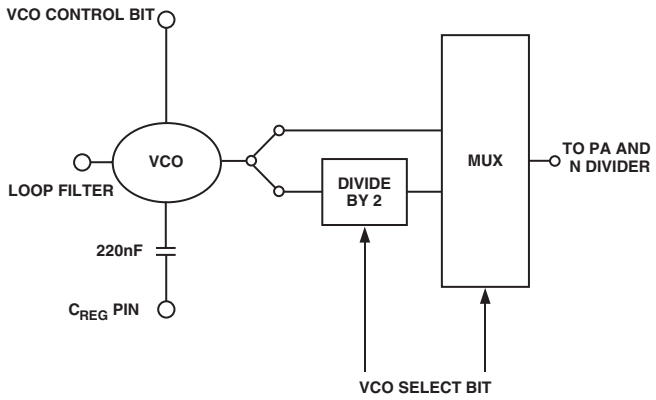


Figure 7. Voltage Controlled Oscillator

RF Output Stage

The RF output stage consists of a DAC with a number of current sources to adjust the output power level. To set up the power level

- FSK GFSK: The output power is set using the modulation Register by entering a 7-bit number into Bits P1–P7. The two MSBs set the range of the output stage, while the five LSBs set the output power in the selected range.
- ASK: The output power as set up for FSK is the output power for a TxDATA of 1. The output power for a zero data bit is set up the same way but using Bits D1–D7.

The output stage is powered down by setting Bit PD2 in the function register to zero.

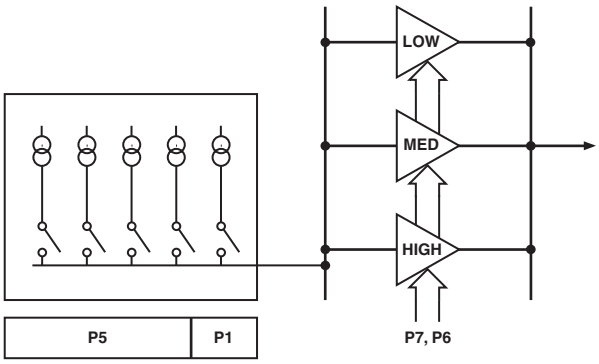


Figure 8. Output Stage

Serial Interface

The serial interface allows the user to program the four 24-bit registers using a 3-wire interface (CLK, Data, and Load Enable).

The serial interface consists of a level shifter, a 24-bit shift register, and four latches. Signals should be CMOS compatible. The serial interface is powered by the regulator, and therefore is inactive when CE is low.

Table I. C2, C1 Truth Table

C2	C1	Data Latch
0	0	R Register
0	1	N Register
1	0	Modulation Register
1	1	Function Register

Data is clocked into the shift register, MSB first, on the rising edge of each clock (CLK). Data is transferred to one of four latches on the rising edge of LE. The destination latch is determined by the value of the two control bits (C2 and C1). These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 1.

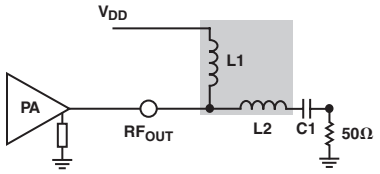


Figure 9. Output Stage Matching

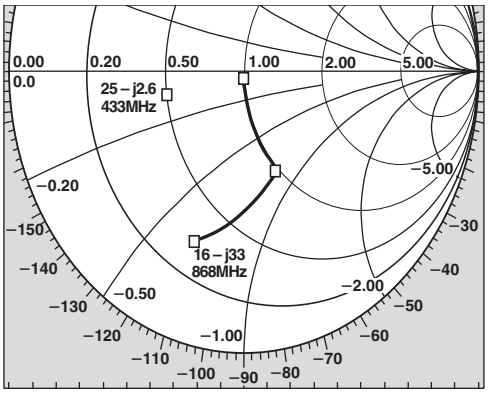


Figure 10. Output Impedance on Smith Chart

Fractional-N

N Counter and Error Correction

The ADF7011 consists of a 15-bit Σ-Δ fractional-N divider. The N Counter divides the output frequency to the output stage back to the PFD frequency. It consists of a prescaler, integer, and fractional part.

The prescaler can be 4/5 or 8/9. A prescaler setting of 8/9 is recommended for 868 MHz operation. A prescaler setting of 4/5 is recommended for 433 MHz operation.

The output frequency of the PLL is

$$PFD\ Frequency \times \left[Int + \frac{(8 \times Fractional) + Error}{2^{15}} \right]$$

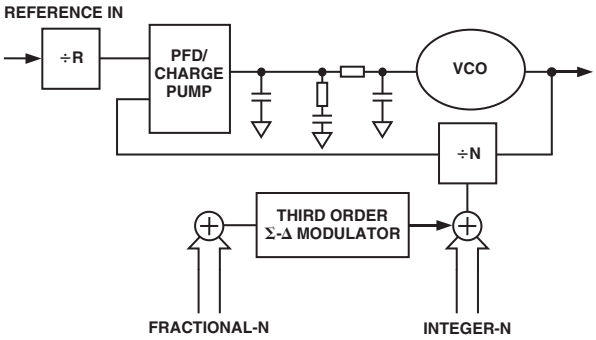


Figure 11. Fractional-N PLL

Fractional-N Registers

The fractional part is made up of a 15-bit divide, made up of a 12-bit N value in the N register summed with a 10-bit value (plus sign bit) in the R register that is used for error correction, as shown in Figure 12.

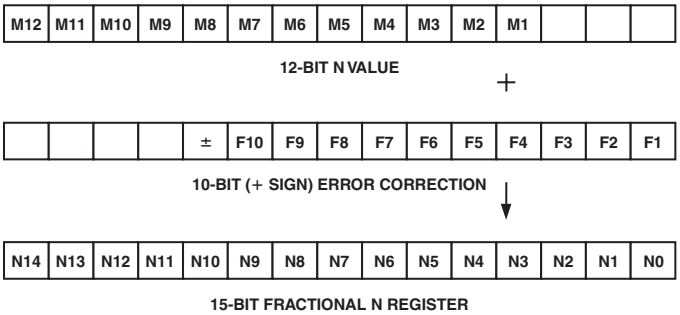


Figure 12. Fractional Components

The resolution of each register is the smallest amount that the output frequency can be changed by changing the LSB of the register.

Changing the Output Frequency

The fractional part of the N register changes the output frequency by

$$\frac{PFD\ Frequency \times Fractional\ Register\ Value}{2^{12}}$$

The frequency error correction contained in the R register changes the output frequency by

$$\frac{PFD\ Frequency \times Error\ Correction\ Register\ Value}{2^{15}}$$

By default, this will be set to 0. The user can calibrate the system and set this by writing a twos complement number to Bits F1–F11 in the R register. This can be used to compensate for initial error, temperature drift, and aging effects in the crystal reference.

Integer-N Register

The integer part of the N Counter contains the prescaler and A and B Counters. It is eight bits wide and offers a divide of $P^2 + 3P + 3$ to 255.

The combination of the integer (255) and the fractional (31767/31768) gives a maximum N Divider of 256. The minimum usable PFD is

$$\frac{Maximum\ Required\ Output\ Frequency}{(255+1)}$$

For use in the European 868 MHz to 870 MHz band, there is a restriction to using a minimum PFD of 3.4 MHz to allow the user to have a center frequency of 870 MHz.

PFD Frequency

The PFD frequency is the number of times a comparison is made between the reference frequency and the feedback signal from the output.

The higher the PFD frequency, the more often a comparison is made at the PFD. This means that the frequency lock time will be reduced when jumping from one frequency to another by increasing the PFD. Having a PFD of > 5 MHz will reduce the available output power due to EN300-220 spurious regulations.

MODULATION SCHEMES

Frequency Shift Keying (FSK)

Frequency shift keying is implemented by setting the N value for the center frequency and then toggling this with the TxDATA line. The deviation from the center frequency is set using Bits D1–D7 in the modulation register. The deviation from the center frequency in Hz is

$$FSK_{DEVIATION}(Hz) = \frac{PFD\ Frequency \times Modulation\ Number}{2^{12}}$$

The modulation number is a number from 1 to 127 (Bits D1–D7 in modulation register). FSK is selected by setting Bits S1 and S2 to zero in the modulation register.

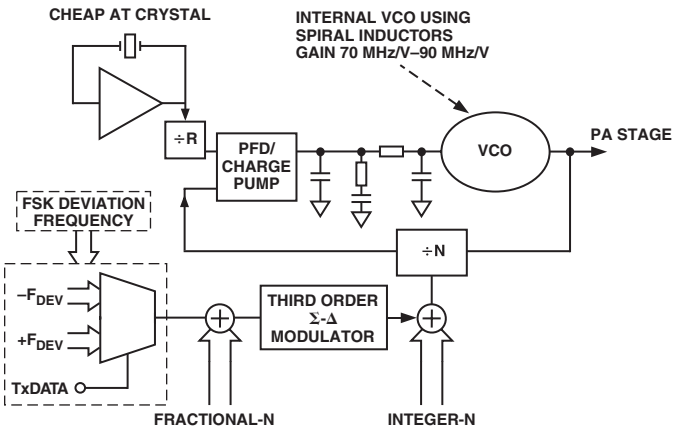


Figure 13. FSK Implementation

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the TxDATA. A TxCLK output line is provided from the ADF7011 for synchronization of TxDATA from the microcontroller. The TxCLK line may be connected to the clock input of an external shift register that clocks data to the transmitter at exact data rate.

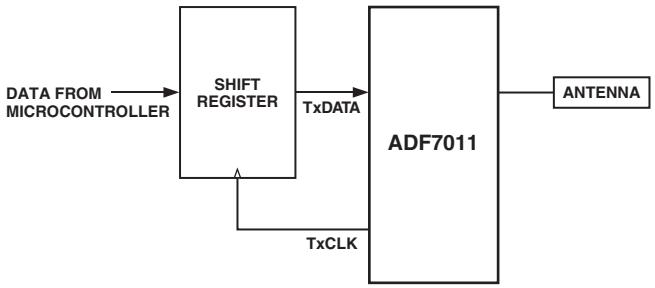


Figure 14. TxCLK Pin Synchronizing Data for GFSK

Setting Up the ADF7011 for GFSK

To set up the frequency deviation, set the PFD and the mod control Bits MC1 to MC3.

$$GFSK_{DEVIATION}(Hz) = \frac{PFD\ Frequency \times 2^{m}}{2^{12}}$$

where *m* is mod control (Bits MC1 to MC3 in the modulation register).

To set up the GFSK data rate

$$Data\ Rate\ (bits/s) = \frac{PFD\ Frequency}{Divider\ Factor \times Index\ Counter}$$

Amplitude Shift Keying (ASK)

Amplitude shift keying is implemented by switching the output stage between two discrete power levels. This is implemented by toggling the DAC, which controls the output level between two 7-bit values set up in the modulation register. A zero TxDATA bit sends Bits D1–D7 to the DAC. A high TxDATA bit sends Bits P1–P7 to the DAC. A maximum modulation depth of 30 dB is possible. ASK is selected by setting Bit S2 = 1 and Bit S1 = 0.

On-Off Keying (OOK)

On-off keying is implemented by switching the output stage to a certain power level for a high TxDATA bit and switching the output stage off for a zero. Due to feedthrough effects, a maximum modulation depth of 33 dB is specified. For OOK, the transmitted power for a high input is programmed using Bits P1–P7 in the modulation register. OOK is selected by setting Bits S1 and S2 to 1 in the modulation register.

CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

The fractional-N PLL allows the selection of any channel within 868 MHz to 870 MHz to a resolution of <l00 Hz, as well as facilitating frequency hopping systems.

Careful selection of the RF transmit channels must be made to achieve best spurious performance. The architecture of fractional-N results in some level of the nearest integer channel moving through the loop to the RF output. These “beat-note” spurs are not attenuated by the loop if the desired RF channel and the nearest integer channel are separated by a frequency of less than the loop BW.

The occurrence of beat-note spurs is rare, as the integer frequencies are at multiples of the reference, which is typically >4 MHz.

The beat-note spurs can be significantly reduced in amplitude by avoiding very small or very large values in the fractional register. By having a channel 1 MHz away from an integer frequency, a 100 kHz loop filter will reduce the level to < –45 dBc. When using an external VCO, the Fast Lock (bleed) function will reduce the spurs to < –60 dBc for the same conditions above.

APPLICATION EXAMPLES

Application Example 1

Operating Frequency	433.92 MHz
Output Power	+10 dBm
Current Consumption	<30 mA
Modulation	ASK/FSK

This system should be set up as shown Figure 15. The spurious levels using a crystal frequency of 4 MHz are sufficiently low so as not to require any band-pass filtering of the output. However, 2 dB of attenuation will be required at 541.50 MHz in order to comply with ES-300-220. This can be achieved easily with the harmonic filter. The harmonic filter can be designed at the output of the matching network with 50 Ω impedance, or it may be integrated into the matching network. The ADF7011 will allow multichannel operation in the 433 MHz band. If FSK modulation is used, the BW should be about five times the data rate. In the case of ASK modulation, a minimum data rate of 1 MHz should be used to minimize the occupied spectrum. The free design tool, ADIsimPLL, should be downloaded from www.analog.com/pll to ascertain the values of the filter components.

Application Example 2

Operating Frequency	868.3 MHz
Output Power	+3 dBm
Current Consumption	<25 mA
Modulation	ASK/FSK

In order to meet the ETSI requirement EN300-220, the maximum output power without using a filter is +3 dBm. This is because the spurious levels scale with output power. Utilizing a PFD frequency of 4.42 MHz will reduce the level of the reference spurs, and place the first spur in a –36 dBm bin, 4.4 MHz below the carrier. ADIsimPLL should be used to design the loop filter, aiming for a loop bandwidth of five times the data rate for FSK. ASK modulation requires a loop BW > 1 MHz to minimize spectral occupancy.

Application Example 3

Operating Frequency	868.3 MHz
Output Power	+10 dBm
Current Consumption	<40 mA
Modulation	ASK/FSK

In order to meet the ETSI requirements at +10 dBm output power, it is necessary to add an inexpensive GigaFILT from Murata at the output. This will reduce the prescaler and reference spurious levels to –54 dBm, and also reduce the harmonic levels to within the –30 dBm level. Given that the insertion loss is 2 dB, it is necessary to use the maximum +12 dBm power from the ADF7011 to achieve an antenna port level of +10 dBm. The filter layout is important to ensure that there is margin in the output spectrum; filter data sheet guidelines should be adhered to.

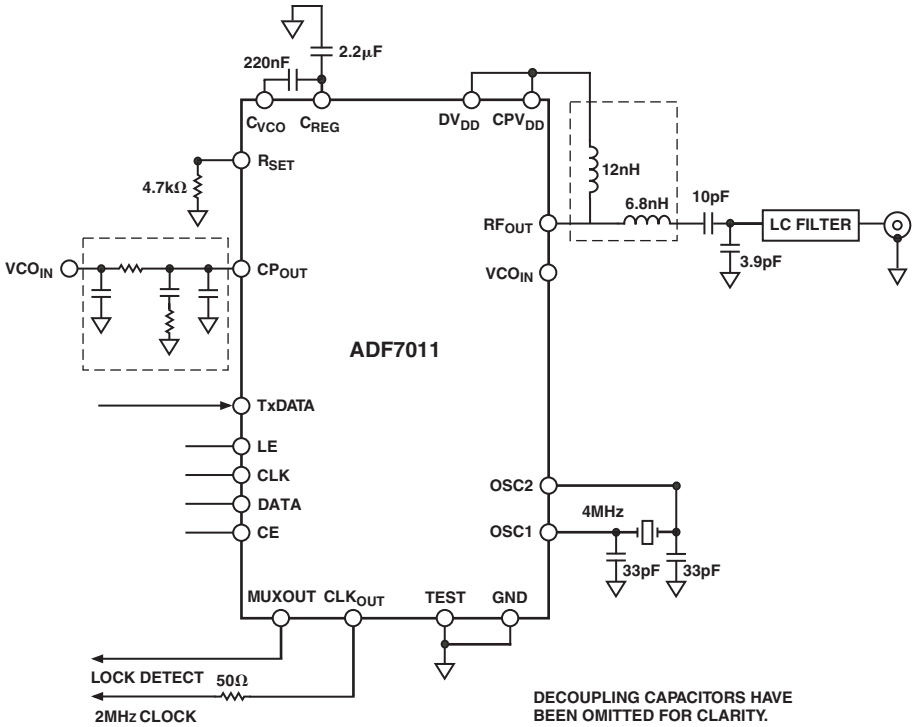


Figure 15. Application Diagram—433 MHz Operation with +10 dBm Output Power

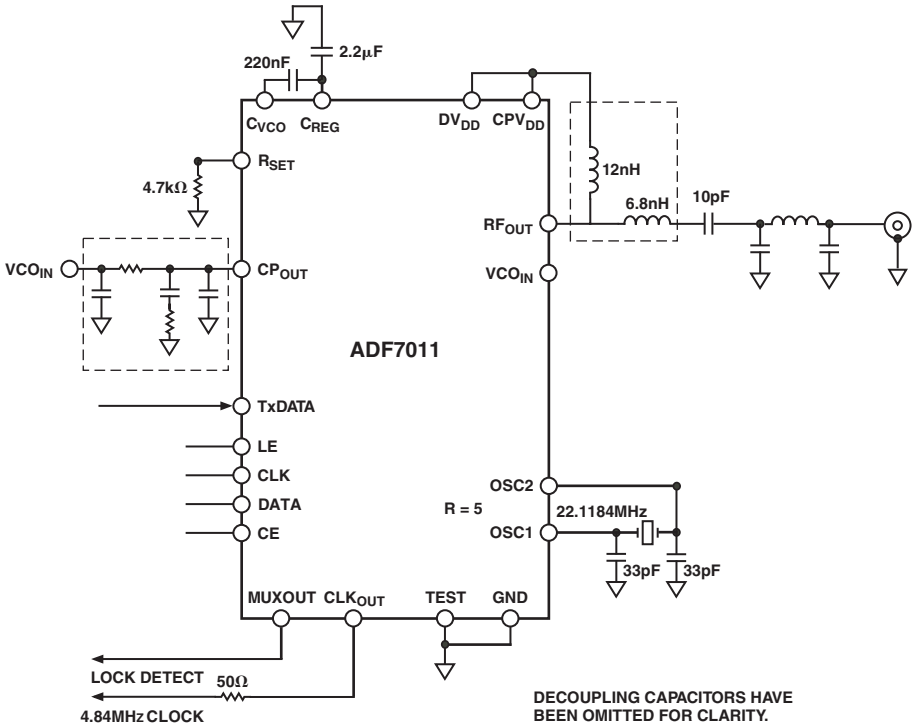


Figure 16. Application Diagram—868 MHz Operation with +3 dBm Output Power

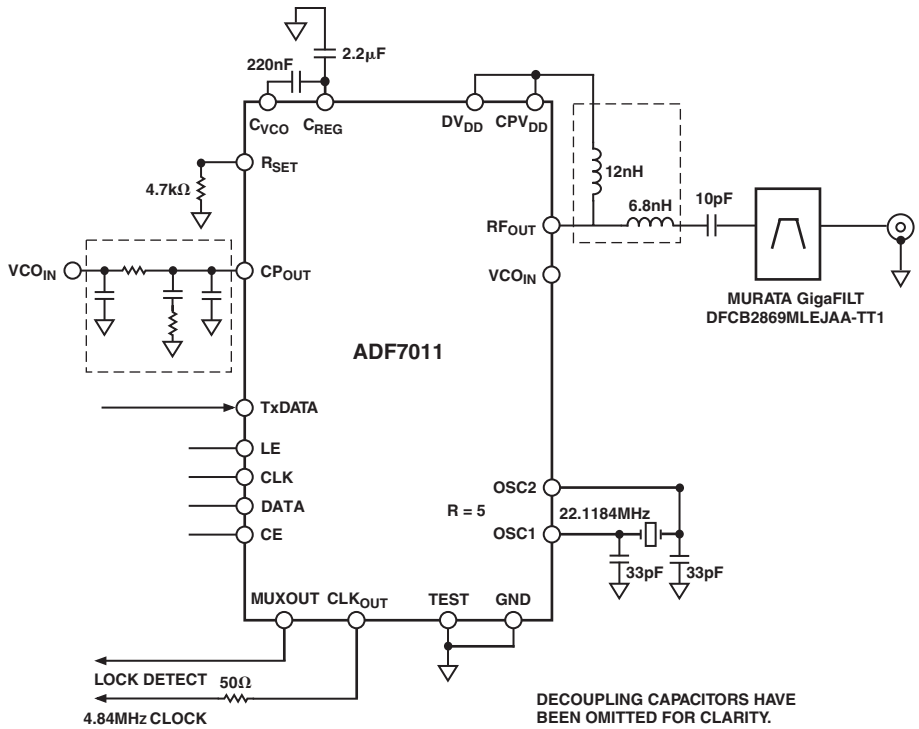
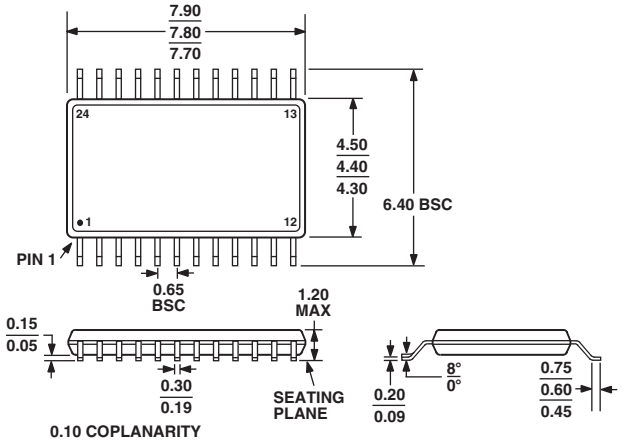


Figure 17. Application Diagram—868 MHz Operation with +10 dBm Output Power

OUTLINE DIMENSIONS

24-Lead Thin Shrink Small Outline Package [TSSOP] (RU-24)

Dimensions shown in millimeters



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