AUTOMOTIVE GRADE

CS8161

12V, 5V Low Dropout Dual Regulator with ENABLE

Description

The CS8161 is a 12V/5V dual output linear regulator. The 12V ± 5% output sources 400mA and the 5V ±2.0% output sources 200mA.

The on board ENABLE function controls the regulator's two outputs. When the ENABLE pin is low, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 200nA of quiescent current.

The primary output, V_{OUT_1} is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

The CS8161 is packaged in a 5 lead TO–220 with copper tab. The copper tab can be connected to a heat sink if necessary. It is also available in a 16 lead SO wide package.

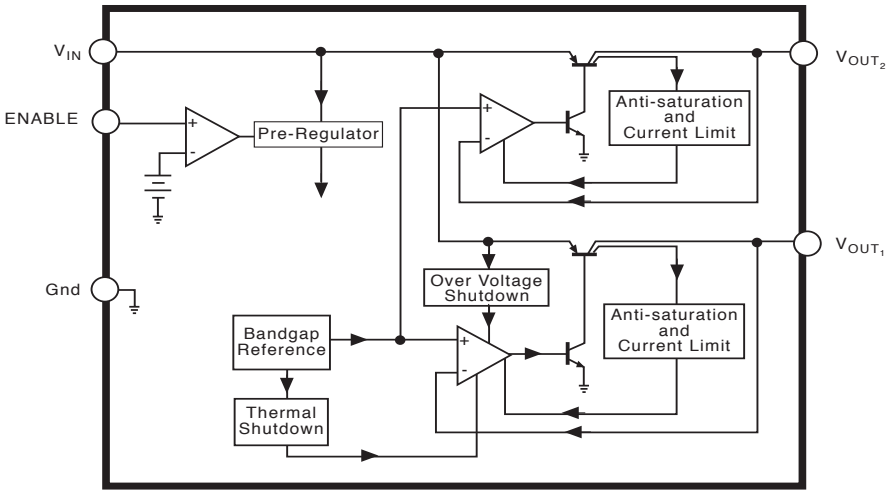
Absolute Maximum Ratings

Input Voltage
- Operating Range .....–15V to 26V
- Overvoltage Protection.....74V

Internal Power Dissipation .....Internally Limited
Junction Temperature Range.....–40°C +150°C
Storage Temperature Range.....–65°C to +150°C
Lead Temperature Soldering
- Wave Solder (through hole styles only).....10 sec. max, 260°C peak
- Reflow (SMD styles only).....60 sec. max above 183°C, 230°C peak

ESD (Human Body Model) 2kV

Block Diagram

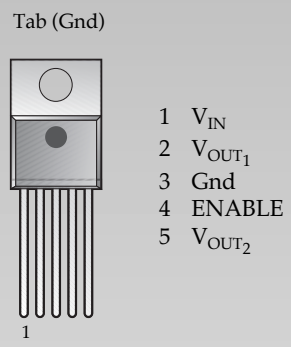


Features

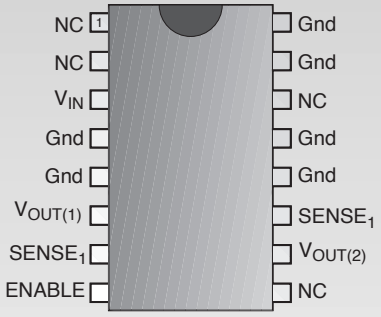
- **Two regulated outputs**
  - **12V ±5.0%; 400mA**
  - **5V ±2.0%; 200mA**
- **Very low SLEEP mode current drain 200nA**
- **Fault Protection**
  - **Reverse Battery (-15V)**
  - **74V Load Dump**
  - **-100V Reverse Transient**
  - **Short Circuit**
  - **Thermal Shutdown**

Package Options

TO-220 5 Lead



16 Lead SO Wide
(internally fused leads)



Cherry Semiconductor

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Electrical Characteristics for V_{OUT}: 6V ≤ V_{IN} ≤ 26V, I_{OUT_1} = 5mA, I_{OUT_2} = 5mA, -40°C ≤ T_J ≤ +150°C, -40°C ≤ T_A ≤ +125°C; unless otherwise specified.

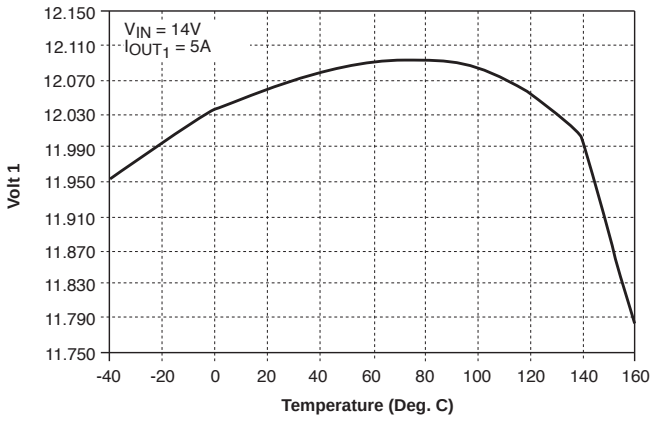
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Primary Output Stage(V_{OUT_1})					
Output Voltage, V_{OUT_1}	13V≤V_{IN}≤26V, I_{OUT_1}≤400mA	11.4	12.0	12.6	V
Dropout Voltage	I_{OUT_1}=400mA		0.35	0.6	V
Line Regulation	13V≤V_{IN}≤20V,5mA≤ I_{OUT}<400mA			80	mV
Load Regulation	5mA≤ I_{OUT_1}≤400mA, V_{IN}=14V			80	mV
Quiescent Current	I_{OUT_1} =100mA, No Load on V_{OUT_2} I_{OUT_1} =400mA, No Load on V_{OUT_2}		8 50	12 75	mA mA
Ripple Rejection	f=120Hz, I_{OUT}=300µA, V_{IN}=15.0V_{DC}, 2V_{RMS}	42			dB
Current Limit		0.40		1.0	A
Reverse Polarity Input Voltage, DC	V_{OUT_1} ≥-0.6V, 10Ω Load		-30	-18	V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, t=100ms, V_{OUT}≥-6V, 10Ω Load		-80	-50	V
Over-voltage Shutdown		28	34	45	V
Short Circuit Current				700	mA
■ Secondary Output (V_{OUT_2})					
Output Voltage, (V_{OUT_2})	6V≤V_{IN}≤26V, I_{OUT_2}≤200mA	4.90		5.10	V
Dropout Voltage	I_{OUT_2} ≤200mA		0.35	0.60	V
Line Regulation	6V≤V_{IN}≤26V, 1mA≤I_{OUT}≤200mA			50	mV
Load Regulation	1mA≤I_{OUT_2}≤200mA, 9V_{IN}=14V			50	mV
Quiescent Current	I_{OUT_2} =50mA I_{OUT_2} =200mA		5 20	10 35	mA mA
Ripple Rejection	f=120Hz; I_{OUT}=10mA, V_{IN}=15V, 2V_{RMS}	42			dB
Current Limit		200		600	mA
Short Circuit Current				400	mA
■ ENABLE Function (ENABLE)					
Input ENABLE Threshold	V_{OUT_1} Off V_{OUT_1} On	 2.00	1.30 1.30	0.80	V V
Input ENABLE Current	V_{ENABLE}=5.5V V_{ENABLE}<0.8V	80 -10		500 10	µA µA
■ Other Features					
Sleep Mode	V_{ENABLE}<0.4V		0.2	50	µA
Thermal Shutdown		150		210	°C
Quiescent Current in Dropout	I_{OUT_1}=100mA, I_{OUT_2}=50mA			60	mA

Package Pin Description

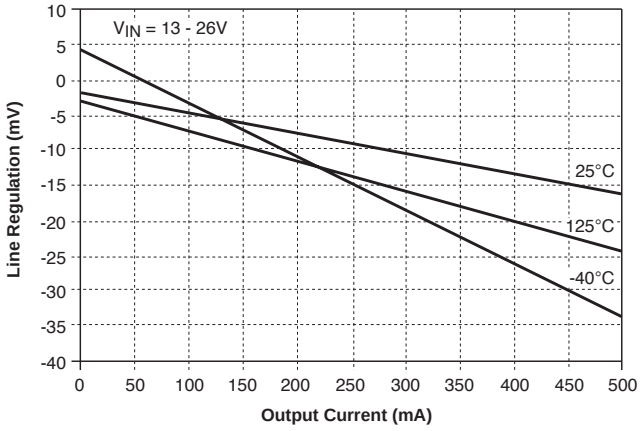
PACKAGE PIN #		PIN SYMBOL	FUNCTION
5 L TO-220	16L SO Wide		
1	3	V_{IN}	Supply voltage, usually direct from battery.
2	6	V_{OUT_1}	Regulated output 12V, 400mA (typ)
3	4,5,12,13,15,16	Gnd	Ground connection.
4	8	ENABLE	CMOS compatible input pin; switches outputs on and off. When ENABLE is high V_{OUT_1} and V_{OUT_2} are active.
5	10	V_{OUT_2}	Output 5V, 200mA (typ).
N/A	7	$Sense_1$	Kelvin connection that allows remote sensing of V_{OUT_1} for improved regulation. If remote sensing is not required, connect to V_{OUT_1}.
N/A	11	$Sense_2$	Kelvin connection that allows remote sensing of V_{OUT_2} for improved regulation. If remote sensing is not required, connect to V_{OUT_2}.
N/A	1,2,9,14	NC	No Connection

Typical Performance Characteristics

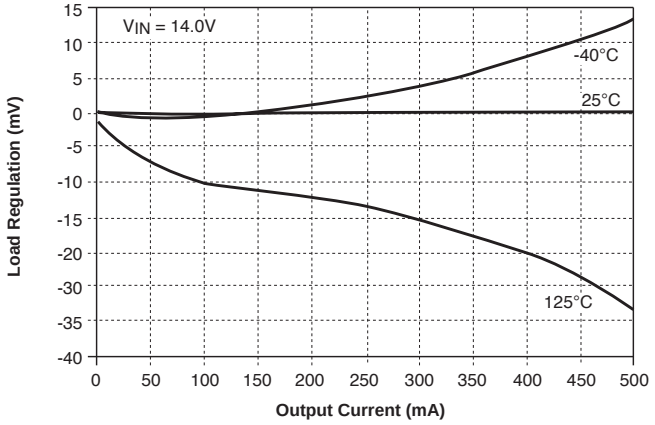
Output Voltage vs. Temperature for V_{OUT_1}



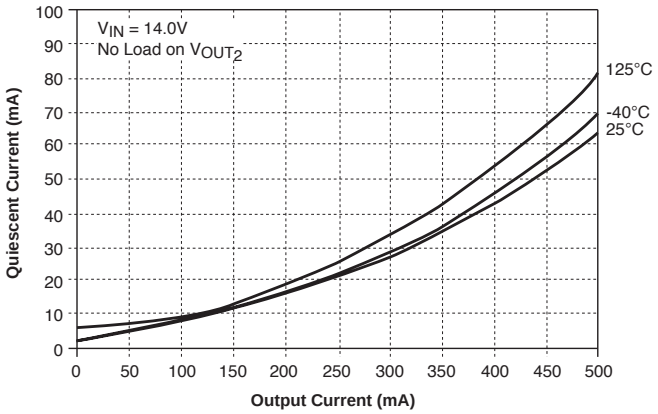
Line Regulation vs. Output Current for V_{OUT_1}



Load Regulation vs. Output Current for V_{OUT_1}

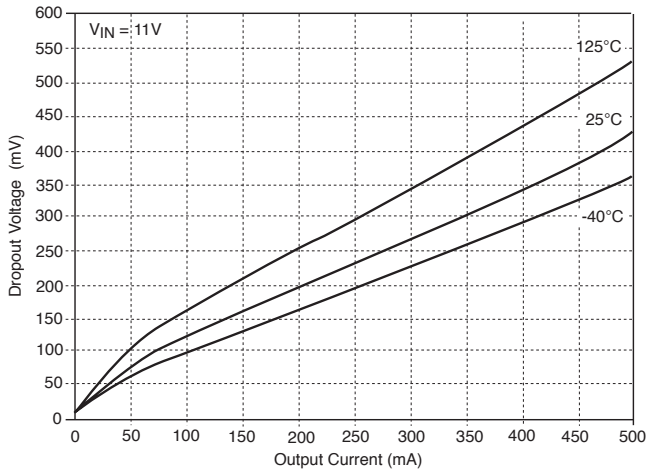


Quiescent Current vs. Output Current for V_{OUT_1}

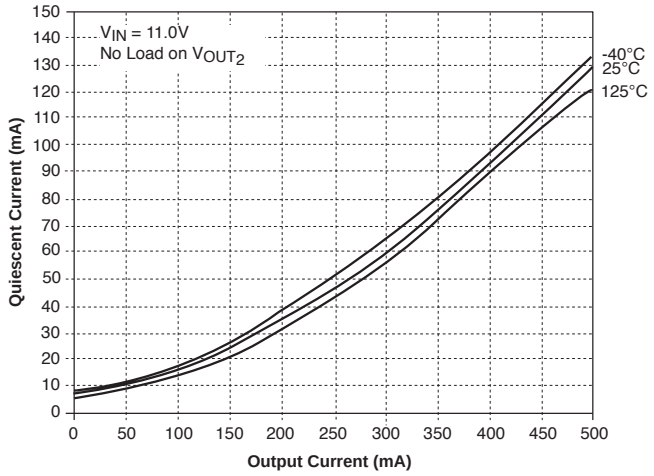


Typical Performance Characteristics: continued

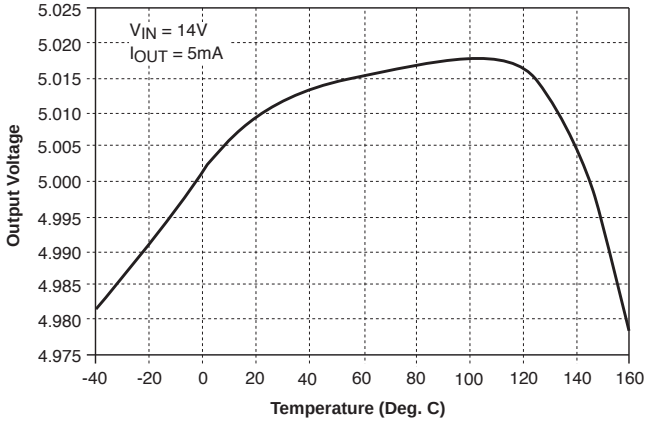
Dropout Voltage vs. Output Voltage for V_{OUT_1}



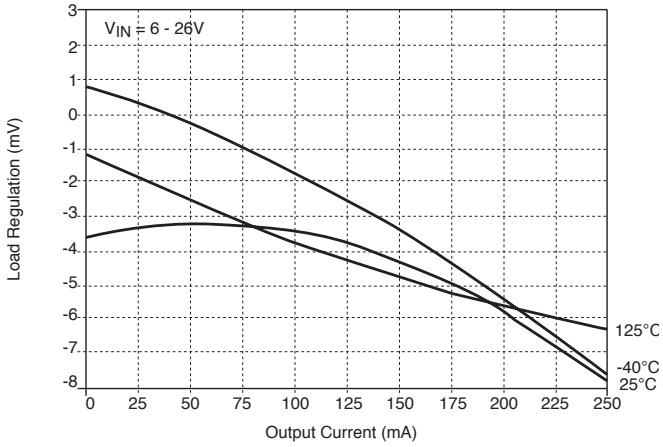
Quiescent Current vs Output Current @ Dropout for V_{OUT_1}



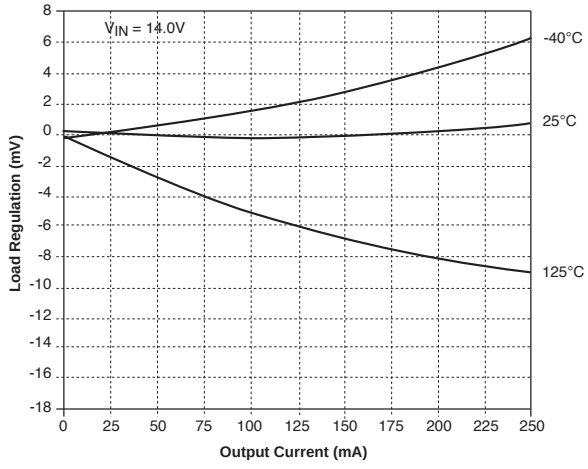
Output Voltage vs. Temperature for V_{OUT_2}



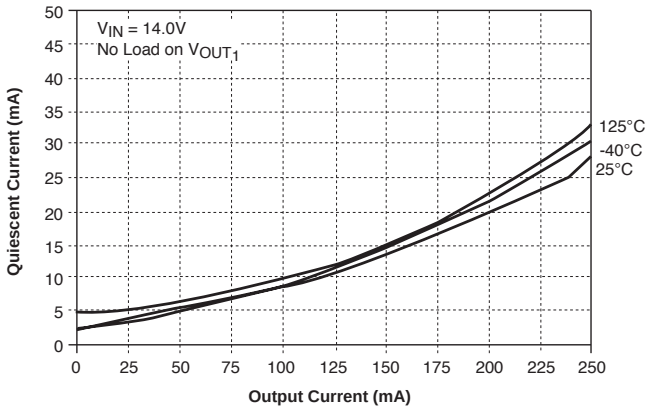
Line Regulation vs Output Current for V_{OUT_2}



Load Regulation vs Output Current for V_{OUT_2}

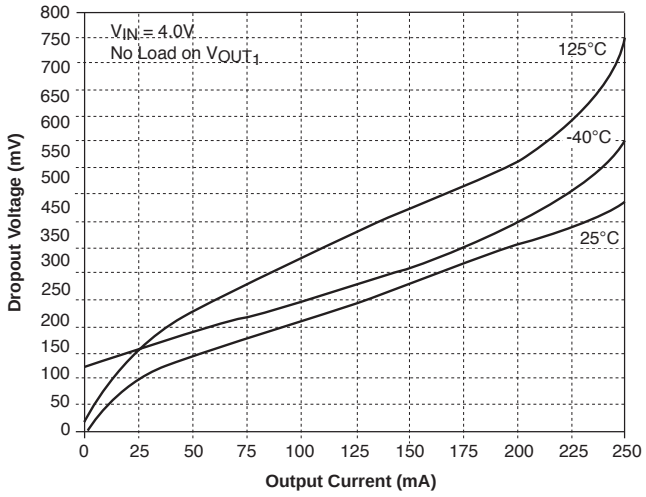


Quiescent Current vs Output Current for V_{OUT_2}

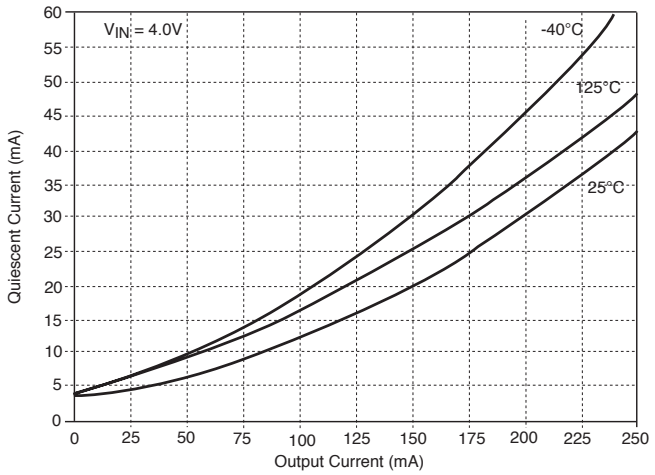


Typical Performance Characteristics: continued

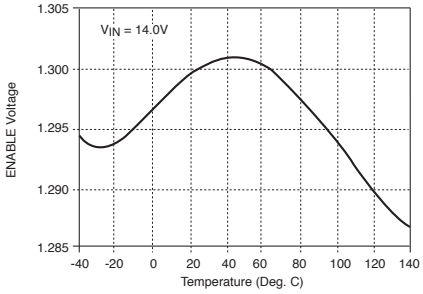
Dropout Voltage vs. Output Current for V_{OUT_2}



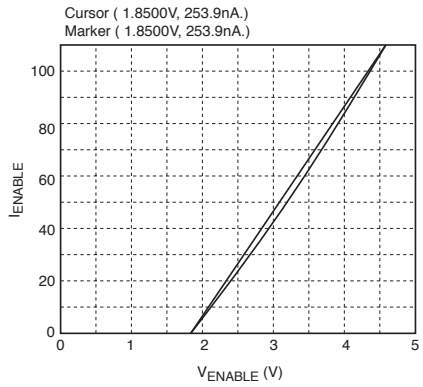
Quiescent Current vs. Output Current @ Dropout for V_{OUT_2}



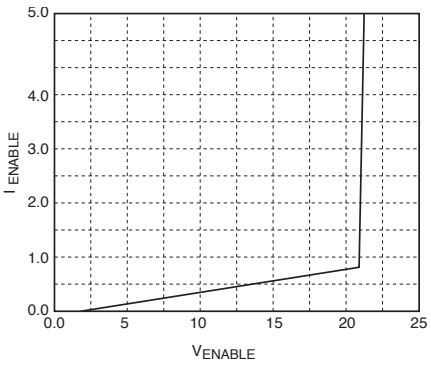
Enable Threshold Voltage vs. Temperature



ENABLE Current vs. ENABLE Voltage



12mA ENABLE Current vs. ENABLE Voltage



Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

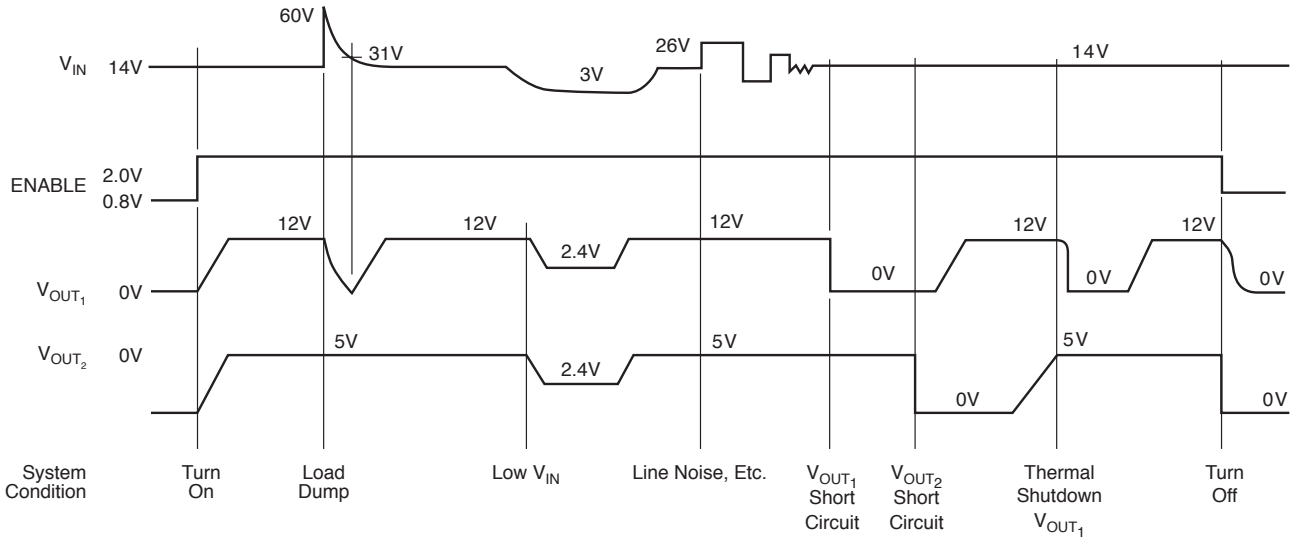
Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. i.e., the regulator ground lead current.

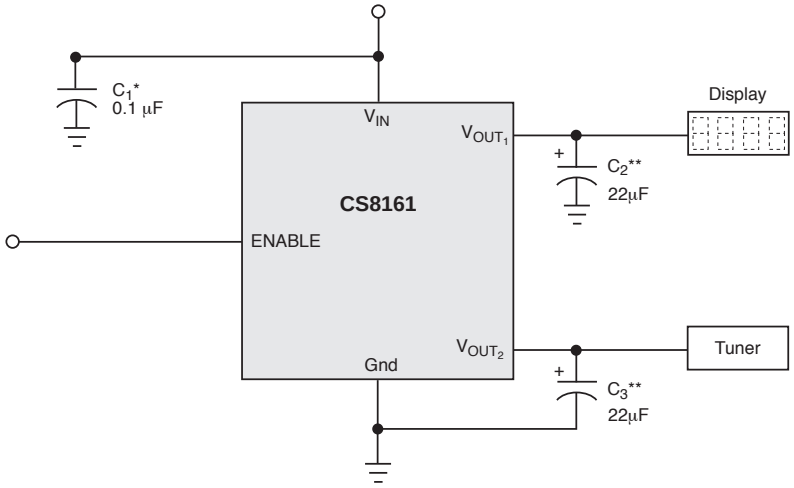
Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_{OUT}: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Typical Circuit Waveform



Application Diagram



NOTES:
* C1 required if regulator is located far from power supply filter.
** C2, C3 required for stability, value may be increased. Capacitor must operate at minimum temperature expected.

Application Notes

Since both outputs are controlled by the same ENABLE, the CS8161 is ideal for applications where a sleep mode is required. Using the CS8161, a section of circuitry such as a display and nonessential 5V circuits can be shut down under microprocessor control to conserve energy.

The example in the Applications Diagram shows an automotive radio application where the display is powered by the 12V on V_{OUT_1} and the Tuner IC is powered by the 5V on V_{OUT_2}. Neither output is required unless both the ignition and the Radio On/Off switch are on.

Stability Considerations

The output compensation capacitor (Application diagram C_2 and C_3) helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The values for the output capacitors C_2 and C_3 shown in the Applications Circuit should work for most applications, however it is not necessarily the best solution.

To determine an acceptable value for C_2 and C_3 for a particular application, start with tantalum capacitors of the recommended value on each output and work towards less expensive alternative parts for each output in turn.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor C_2 will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor C_2 is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of +/-20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above. Once the value for C2 is determined, repeat the steps to determine the appropriate value for C3.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 1) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT_1(max)} + \{V_{IN(max)} - V_{OUT_2(min)}\}I_{OUT_2(max)} + V_{IN(max)}IQ \quad (1)$$

Where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT_1(min)}$ is the minimum output voltage from V_{OUT_1},

$V_{OUT_2(min)}$ is the minimum output voltage from V_{OUT_2},

$I_{OUT_1(max)}$ is the maximum output current, for the application

$I_{OUT_2(max)}$ is the maximum output current, for the application

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R\Theta_{JA}$ can be calculated:

$$R\Theta_{JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R\Theta_{JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R\Theta_{JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

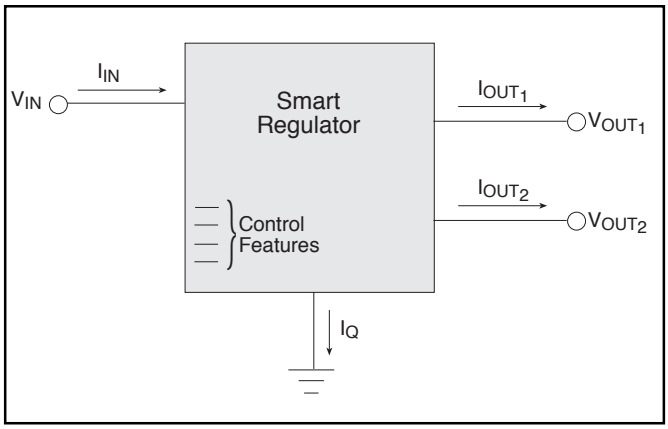


Figure 1: Dual output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R\Theta_{JA}$.

$$R\Theta_{JA} = R\Theta_{JC} + R\Theta_{CS} + R\Theta_{SA} \quad (3)$$

where

$R\Theta_{JC}$ = the junction–to–case thermal resistance,
$R\Theta_{CS}$ = the case–to–heatsink thermal resistance, and
$R\Theta_{SA}$ = the heatsink–to–ambient thermal resistance.

$R\Theta_{JC}$ appears in the package section of the data sheet. Like $R\Theta_{JA}$, it too is a function of package type. $R\Theta_{CS}$ and $R\Theta_{SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Package Specification

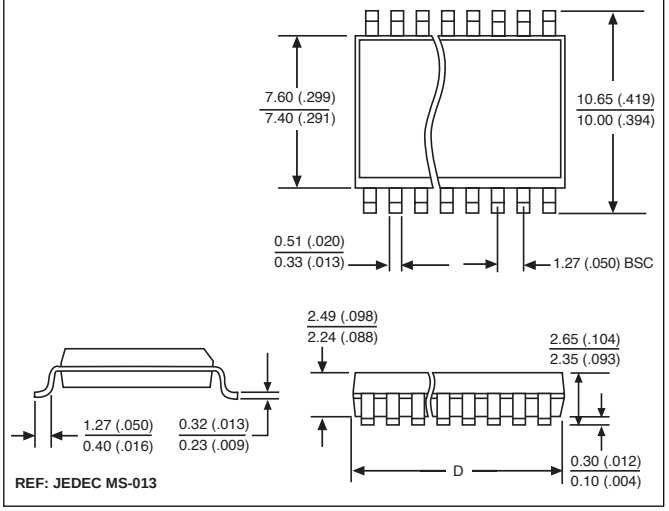
PACKAGE DIMENSIONS IN mm(INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L SO Wide *(internally fused leads)*	10.50	10.10	.413	.398

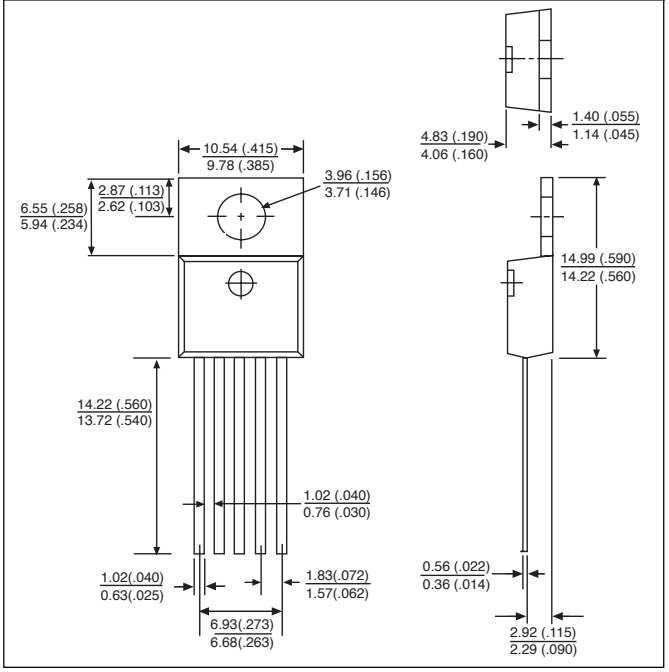
PACKAGE THERMAL DATA

Thermal Data		5L TO-220	16L SO Wide	
$R\Theta_{JC}$	typ	2.0	18	°C/W
$R\Theta_{JA}$	typ	50	75	°C/W

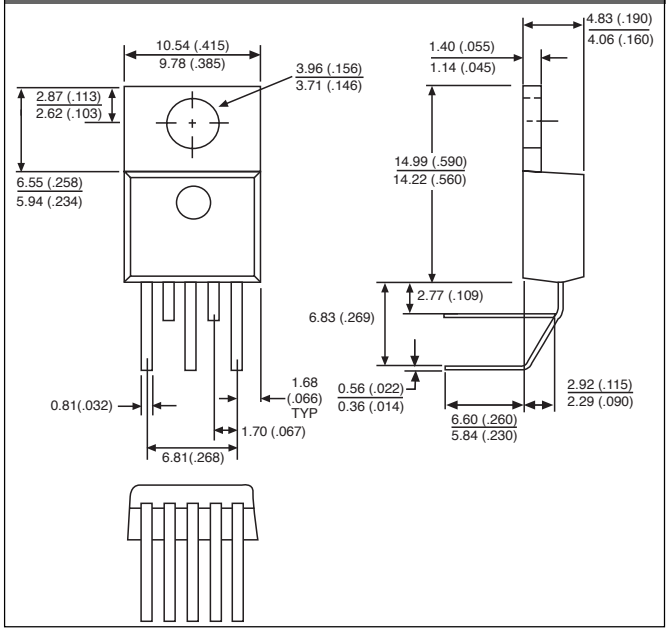
Surface Mount Wide Body (DW); 300 mil wide



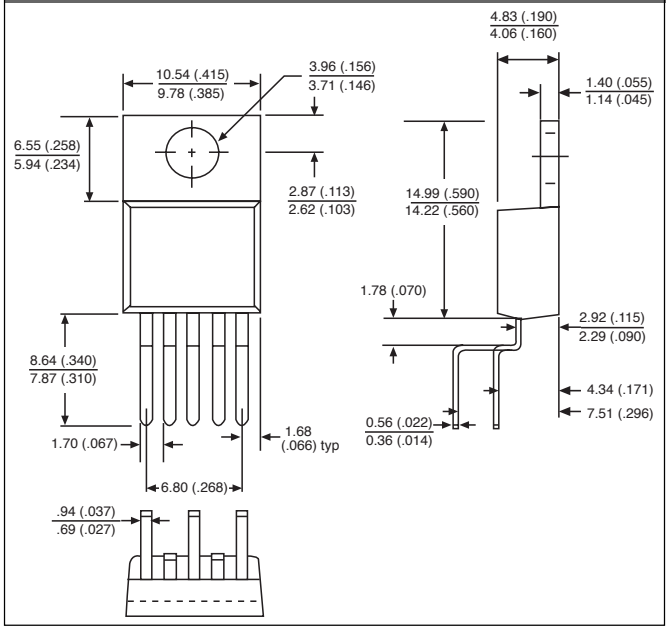
5 Lead TO-220 (T) Straight



5 Lead TO-220 (THA) Horizontal



5 Lead TO-220 (TVA) Vertical



Ordering Information

Part Number	Description
CS8161YT5	5L TO-220 Straight
CS8161YTVA5	5L TO-220 Vertical
CS8161YTHA5	5L TO-220 Horizontal
CS8161YDWF16	16L SO Wide
CS8161YDWFR16	16L SO Wide *(tape & reel)*

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