Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES

Pretrimmed to ±1.0% (AD532K)
No external components required
Guaranteed ±1.0% maximum 4-quadrant error (AD532K)
Differential Inputs for $(X_1 - X_2)(Y_1 - Y_2)/10$ V transfer function
Monolithic construction, low cost

APPLICATIONS

Multiplication, division, squaring, square rooting
Algebraic computation
Power measurements
Instrumentation applications
Available in chip form

FUNCTIONAL BLOCK DIAGRAM

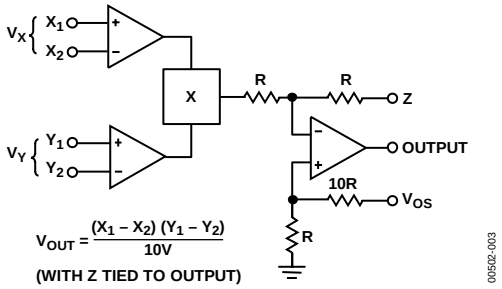

Figure 1.

GENERAL DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10 V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks.

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1 - X_2)(Y_1 - Y_2)/10$ V, divides in two quadrants with a 10 V $Z/(X_1 - X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10\text{ V } Z}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as XY/10 V, $(X^2 - Y^2)/10$ V, $\pm X^2/10$ V, and 10 V $Z/(X_1 - X_2)$, are easily attained and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75 dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at 25°C, and are rated for operation from 0°C to 70°C. The AD532S has a maximum multiplying error of ±1% of full scale at 25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of −55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can, TO-116 ceramic DIP or LCC packages. The J, K, and S grade chips are also available.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable because standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

Rev. D
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IMPORTANT LINKS for the AD532*

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PARAMETRIC SELECTION TABLES

Find Similar Products By Operating Parameters

DOCUMENTATION

AN-213: Low Cost, Two-Chip, Voltage -Controlled Amplifier and Video Switch

Space Qualified Parts List

EVALUATION KITS & SYMBOLS & FOOTPRINTS

Symbols and Footprints

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Quality and Reliability
Lead(Pb)-Free Data

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Flexibility of Operation ... 1
Guaranteed Performance Over Temperature ... 1
Advantages of On-The-Chip Trimming of The Monolithic AD532 ... 1
Revision History ... 2
Specifications ... 3
Thermal Resistance ... 5
Chip Dimensions And Bonding Diagram ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 8
Functional Description ... 10
AD532 Performance Characteristics ... 11
Nonlinearity ... 11
AC Feedthrough ... 11
Common-Mode Rejection ... 11
Dynamic Characteristics ... 11
Power Supply Considerations ... 11
Noise Characteristics ... 11
Applications ... 12
Replacing Other IC Multipliers ... 12
Square Root ... 13
Difference of Squares ... 13
Outline Dimensions ... 14
Ordering Guide ... 15

REVISION HISTORY

2/11—Rev. C to Rev. D

Updated Format ... Universal
Added Pin Configuration and Function Descriptions Section ... 6
Added Typical Performance Characteristics Section ... 8
Changes to Figure 11 ... 8
Changes to Figure 12 and Figure 13 ... 9
Changes to Ordering Guide ... 15

SPECIFICATIONS

At 25°C, V_S = ±15 V, R ≥ 2 kΩ V_{OS} grounded, unless otherwise noted.

Table 1.

Model	Conditions	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Unit
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error	−10 V ≤ X, Y ≤ +10 V		±1.5	±2.0		±0.7	±1.0		±0.5	±1.0	%
T_A = Minimum to Maximum			±2.5			±1.5				±4.0	%
Total Error vs. Temperature			±0.04			±0.03			±0.01	±0.04	%/°C
Supply Rejection	±15 V ±10%		±0.05			±0.05			±0.05		%/%
Nonlinearity, X	X = 20 V p-p, Y = 10 V		± 0.8			±0.5			±0.5		%
Nonlinearity, Y	Y = 20 V p-p, X = 10 V		±0.3			±0.2			±0.2		%
Feedthrough, X	Y nulled, X = 20 V p-p 50 Hz		50	200		30	100		30	100	mV
Feedthrough, Y (X Nulled, Y = 20 V p-p 50 Hz)			30	150		25	80		25	80	mV
Feedthrough vs. Temperature			2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply			±0.25			±0.25			±0.25		mV/%
DYNAMICS											
Small Signal BW	V_{OUT} = 0.1 rms		1			1			1		MHz
1% Amplitude Error			75			75			75		kHz
Slew Rate	V_{OUT} 20 p-p		45			45			45		V/µs
Settling Time	to 2%, ΔV_{OUT} = 20 V		1			1			1		µs
NOISE											
Wideband Noise			0.6			0.6			0.6		mV (rms)
f = 5 Hz to 10 kHz											
f = 5 Hz to 5 MHz			3.0			3.0			3.0		mV (rms)
OUTPUT											
Voltage Swing		±10	±13		±10	±13		±10	±13		V
Impedance	f ≤ 1 kHz		1			1			1		Ω
Offset Voltage			±40				±30			±30	mV
Offset Voltage vs. Temperature			0.7			0.7				2.0	mV/°C
Offset Voltage vs. Supply			±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y, and Z)											
Signal Voltage Range	Differential or CM operating differential		±10			±10			±10		V
CMRR		40			50			50			dB
Input Bias Current											
X, Y Inputs			3			1.5	4		1.5	4	µA
X, Y Inputs T_{MIN} to T_{MAX}			10			8			8	±15	µA
Z Input			±10			±5	±15		±5		µA
Z Input T_{MIN} to T_{MAX}			±30			±25			±25		µA
Offset Current			±0.3			±0.1			±0.1		µA
Differential Resistance			10			10			10		MΩ
DIVIDER PERFORMANCE											
Transfer Function	$X_I > X_2$		10 V Z/(X_1 – X_2)			10 V Z/(X_1 – X_2)			10 V Z/(X_1 – X_2)		
Total Error											
	V_X = −10 V, −10 V ≤ V_Z ≤ +10 V		±2			±1			±1		%
	V_X = −1 V, −10 V ≤ V_Z ≤ +10 V		±4			±3			±3		%

Model	Conditions	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Unit
SQUARE PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10V}$			$\frac{(X_1 - X_2)^2}{10V}$			$\frac{(X_1 - X_2)^2}{10V}$		
Total Error			±0.8			±0.4			±0.4		%
SQUARE ROOTER PERFORMANCE											
Transfer Function			$-\sqrt{10\ V\ Z}$			$-\sqrt{10\ V\ Z}$			$-\sqrt{10\ V\ Z}$		
Total Error	$0\ V \le V_Z \le 10\ V$		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS											
Supply Voltage											
Rated Performance			±15			±15			±15		V
Operating		±10		±18	±10		±18	±10		±22	V
Supply Current											
Quiescent			4	6		4	6		4	6	mA

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 2. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
H-10A	150	25	°C/W
E-20A	85	22	°C/W
D-14	85	22	°C/W

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.

Dimensions are shown in inches and (mm).

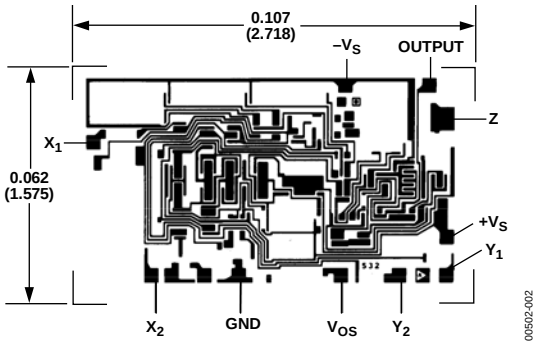

Figure 2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

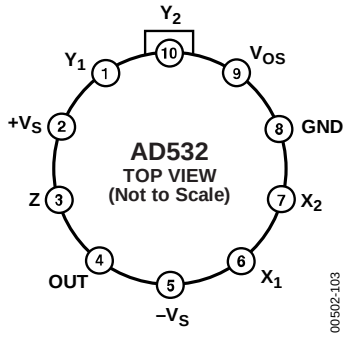

Figure 3. 10-Lead Header Pin Configuration (H-10)

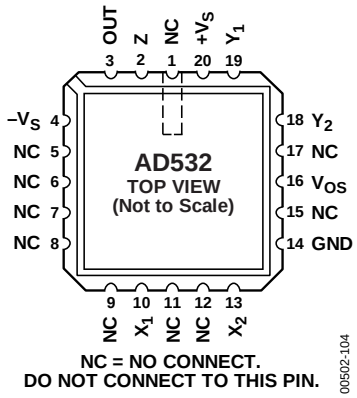

Figure 4. 20-Lead Leadless Chip Carrier Pin Configuration (E-20A)

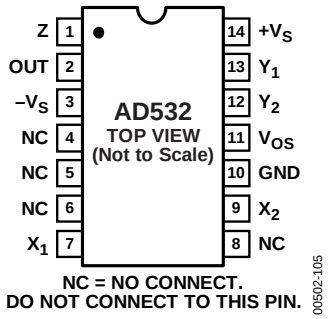

Figure 5. 14-Lead Side Braize DIP (D-14)

Table 3. 10 Lead Header Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y_1	Y Multiplicand Input 1
2	$+V_S$	Positive Supply Voltage
3	Z	Dual Purpose Input
4	OUT	Product Output
5	$–V_S$	Negative Supply Voltage
6	X_1	X Multiplicand Input 1
7	X_2	X Multiplicand Input 2
8	GND	Common
9	V_{OS}	Output Offset Adjust
10	Y_2	Y Multiplicand Input 2

Table 4. 20 Lead Leadless Chip Carrier Pin Function Descriptions

Pin No.	Mnemonic	Description
2	Z	Dual Purpose Input
3	OUT	Product Output
4	$-V_S$	Negative Supply Voltage
1, 5, 6, 7, 8, 9, 11, 12, 15, 17	NC	No Connection
10	X_1	X Multiplicand Input 1
13	X_2	X Multiplicand Input 2
14	GND	Common
16	V_{OS}	Output Offset Adjust
18	Y_2	Y Multiplicand Input 2
19	Y_1	Y Multiplicand Input 1
20	$+V_S$	Positive Supply Voltage

Table 5. 14 Lead Side Braize DIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Z	Dual Purpose Input
2	OUT	Product Output
3	$-V_S$	Negative Supply Voltage
4, 5, 6	NC	No Connection
7	X_1	X Multiplicand Input 1
9	X_2	X Multiplicand Input 2
10	GND	Common
11	V_{OS}	Output Offset Adjust
12	Y_2	Y Multiplicand Input 2
13	Y_1	Y Multiplicand Input 1
14	$+V_S$	Positive Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

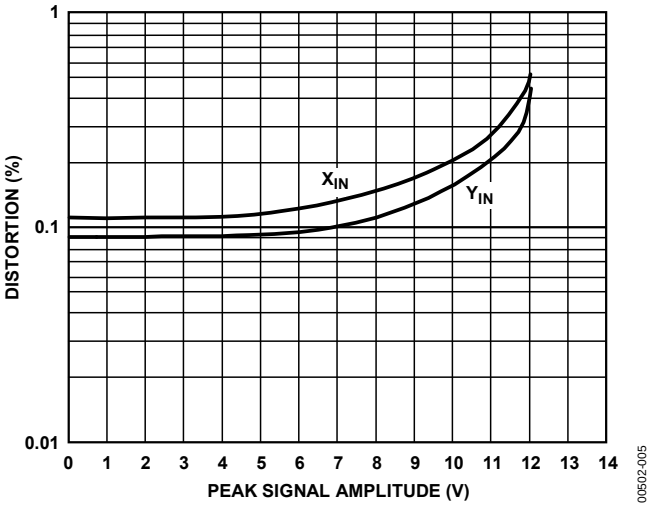

Figure 6. Distortion vs. Peak Signal Amplitude

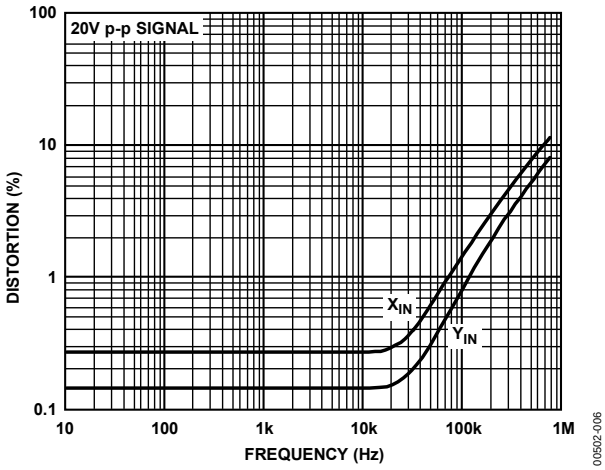

Figure 7. Distortion vs. Frequency

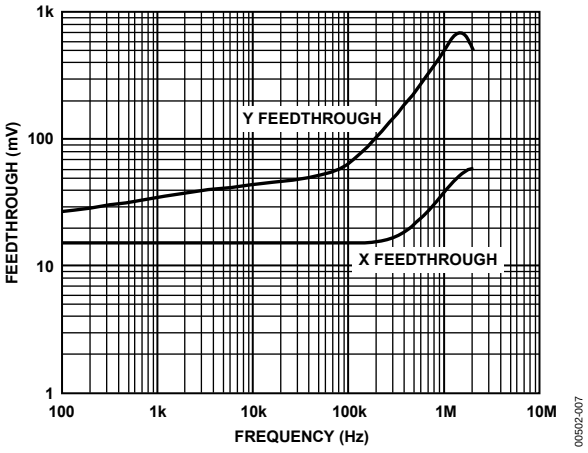

Figure 8. Feedthrough vs. Frequency

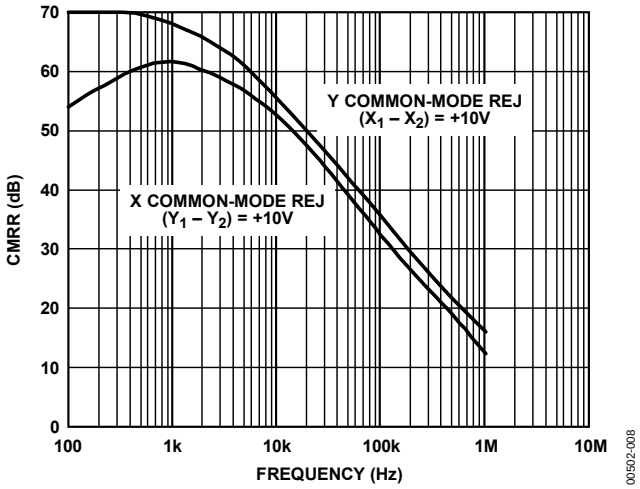

Figure 9. CMRR vs. Frequency

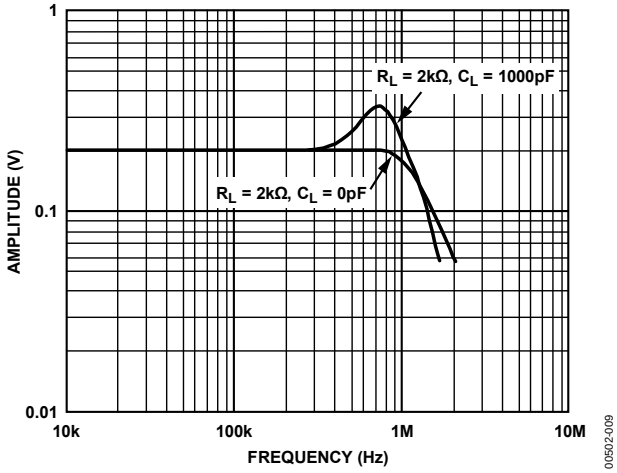

Figure 10. Frequency Response, Multiplying

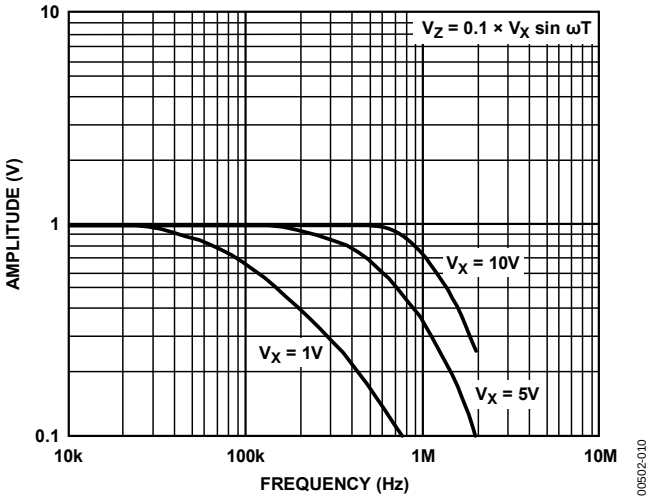

Figure 11. Frequency Response, Dividing

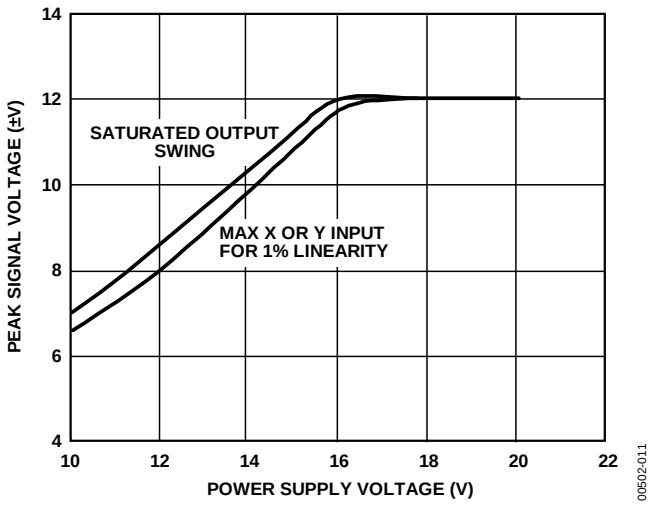

Figure 12. Signal Swing vs. Supply

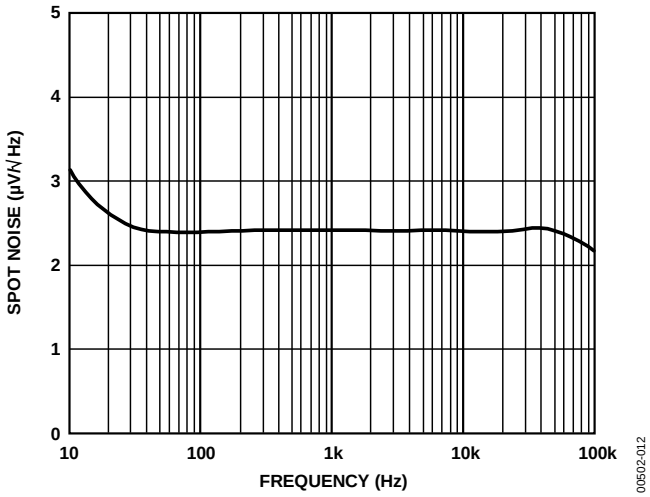

Figure 13. Spot Noise vs. Frequency

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1and the complete schematic in Figure 14. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. In the divide mode, it is used as an input terminal.

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common-mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{OS} in critical applications. Otherwise, the V_{OS} pin should be grounded.

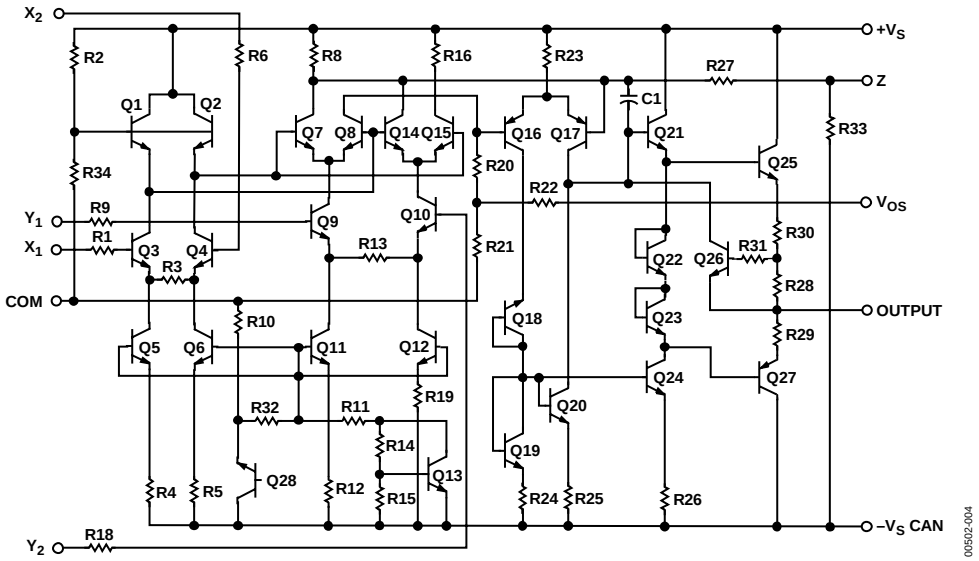

Figure 14. Schematic Diagram

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at 25°C with the rated power supply. The value specified is in percent of full scale and includes X_{IN} and Y_{IN} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common-mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components because they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 17. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Therefore, as the denominator is reduced, output offset, bandwidth, and other multiplier cell errors are adversely affected. The divide error and drift are then $\varepsilon_m \times 10\ V/X_1 - X_2)$ where ε_m represents multiplier full-scale error and drift, and $(X_1 - X_2)$ is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figure 6 and Figure 7 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10 V dc. In Figure 7, the sine wave amplitude is 20 V (p-p).

AC FEEDTHROUGH

AC feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 8. It is measured for the condition $V_X = 0$, $V_Y = 20$ V (p-p) and $V_Y = 0$, $V_X = 20$ V (p-p) over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

COMMON-MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common-mode rejection for both inputs as a function of frequency is shown in Figure 9. It is measured with $X_1 = X_2 = 20$ V (p-p), $(Y_1 - Y_2) = 10$ V dc and $Y_1 = Y_2 = 20$ V (p-p), $(X_1 - X_2) = 10$ V dc.

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3 dB bandwidth of 1 MHz and rolls off at 6 dB/octave, thereafter. Response through all inputs is essentially the same as shown in Figure 10. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 11.

Stable operation is maintained with capacitive loads to 1000 pF in all modes, except the square root for which 50 pF is a safe upper limit. Higher capacitive loads can be driven if a 100 Ω resistor is connected in series with the output for isolation.

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15 V dc supplies, it may be operated at any supply voltage from ±10 V to ±18 V for the J and K versions, and ±10 V to ±22 V for the S version. The input and output signals must be reduced proportionately to prevent saturation; however, with supply voltages below ±15 V, as shown in Figure 12. Because power supply sensitivity is not dependent on external null networks as in other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 13.

APPLICATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin-film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Therefore, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. The V_{OS} terminal should always be grounded when unused.

Multiplication

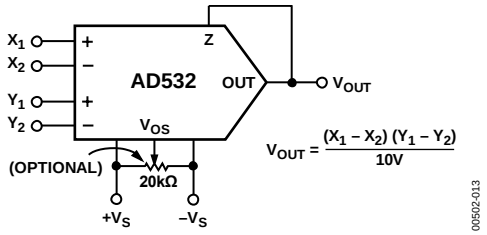

Figure 15. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 15. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

Squaring

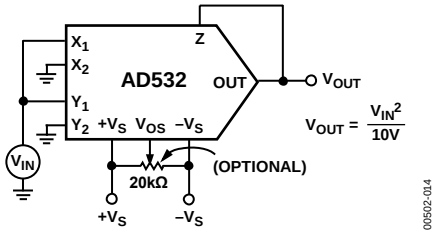

Figure 16. Squarer Connection

The squaring circuit in Figure 16 is a simple variation of the multiplier. The differential input capability of the AD532, however, can be used to obtain a positive or negative output response to the input, a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

Division

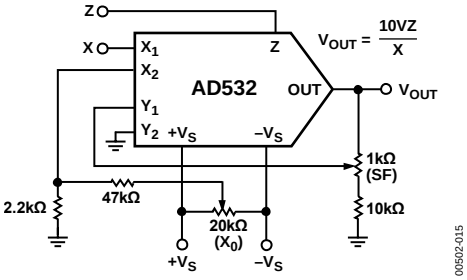

Figure 17. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 17. It should be noted, however, that the output error is given approximately by 10 V $\varepsilon_m/(X_1 - X_2)$, where ε_m is the total error specification for the multiply mode; and bandwidth by $f_m \times (X_1 - X_2)/10$ V, where fm is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus, for single-ended negative inputs (0 V to −10 V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0 V to +10 V), connect the input to X_2 and the offset null to X1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table 6.

For practical reasons, the useful range in denominator input is approximately 500 mV ≤ $|(X_1 - X_2)|$ ≤ 10 V. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and $(X_1 - X_2)$ at full scale.

Table 6. Adjustment Procedure (Divider or Square Rooter)

	Divider			Square Rooter	
	With:		Adjust for:	With:	Adjust: for:
Adjust	X	Z	V_{OUT}	Z	V_{OUT}
Scale Factor	−10 V	+10 V	−10 V	+10 V	−10 V
X_0 (Offset)	−1 V	+0.1 V	−1 V	+0.1 V	−1 V

Repeat if required.

SQUARE ROOT

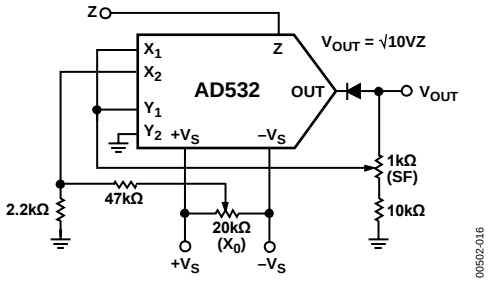

Figure 18. Square Rooter Connection

The connections for square root mode are shown in Figure 18. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{IN} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{IN} = +0.1 V dc, adjusting V_{OS} to obtain −1.0 V dc in the output, $V_{OUT} = -\sqrt{10\text{ V Z}}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table 6.

DIFFERENCE OF SQUARES

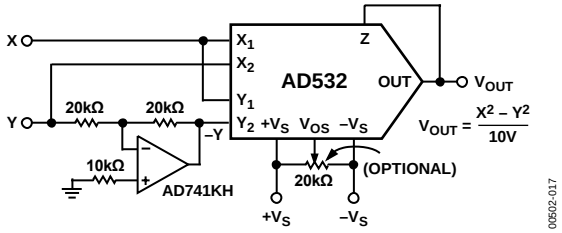

Figure 19. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X_2 - Y_2/10$ V. As shown in Figure 19, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{IN}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

OUTLINE DIMENSIONS

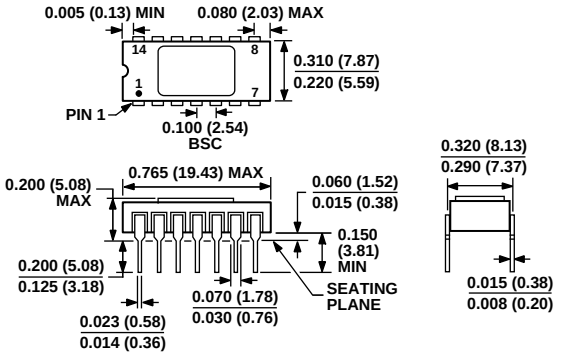

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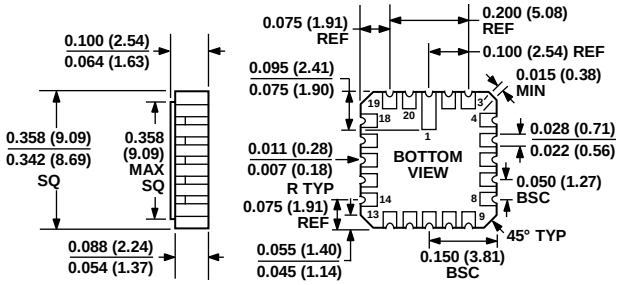
Figure 20. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-14)
Dimensions shown in inches and (millimeters)



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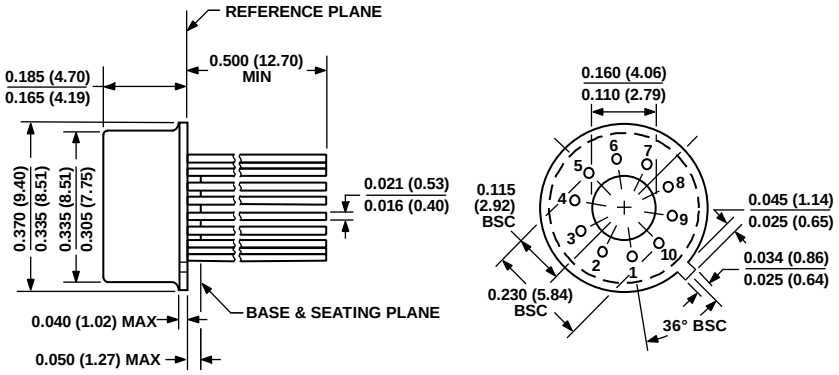
022106-A

Figure 21. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20-1)
Dimensions shown in inches and (millimeters)



DIMENSIONS PER JEDEC STANDARDS MO-006-AF
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022306-A

Figure 22. 10-Pin Metal Header Package [TO-100] (H-10)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD532JCHIPS	0°C to 70°C	Chip	
AD532JD	0°C to 70°C	14-Lead SBDIP	D-14
AD532JDZ	0°C to 70°C	14-Lead SBDIP	D-14
AD532JH	0°C to 70°C	10-Pin Metal Header Package [TO-100]	H-10
AD532JHZ	0°C to 70°C	10-Pin Metal Header Package [TO-100]	H-10
AD532KD	0°C to 70°C	14-Lead SBDIP	D-14
AD532KDZ	0°C to 70°C	14-Lead SBDIP	D-14
AD532KH	0°C to 70°C	10-Pin Metal Header Package [TO-100]	H-10
AD532KHZ	0°C to 70°C	10-Pin Metal Header Package [TO-100]	H-10
AD532SCHIPS	−55°C to +125°C	Chip	
AD532SD	−55°C to +125°C	14-Lead SBDIP	D-14
AD532SD/883B	−55°C to +125°C	14-Lead SBDIP	D-14
AD532SE/883B	−55°C to +125°C	20-Terminal LCC	E-20-1
AD532SH	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD532SH/883B	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10

[1] Z = RoHS Compliant Part.

NOTES

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