# CS8161

# 12 V, 5.0 V Low Dropout Dual Regulator with ENABLE

The CS8161 is a 12 V/5.0 V dual output linear regulator. The 12 V ±5.0% output sources 400 mA and the 5.0 V ±2.0% output sources 200 mA.

The on board ENABLE function controls the regulator's two outputs. When the ENABLE pin is low, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 200 nA of quiescent current.

The primary output, $V_{OUT1}$ is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

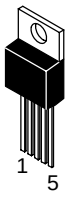
The CS8161 is packaged in a 5 lead TO−220 with copper tab. The copper tab can be connected to a heat sink if necessary.

### Features

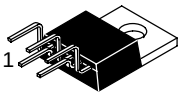
- Two Regulated Outputs
  - 12 V ±5.0%; 400 mA
  - 5.0 V ±2.0%; 200 mA
- Very Low SLEEP Mode Current Drain 200 nA
- Fault Protection
  - Reverse Battery (−15 V)
  - 74 V Load Dump
  - −100 V Reverse Transient
  - Short Circuit
  - Thermal Shutdown
- Pb−Free Packages are Available*

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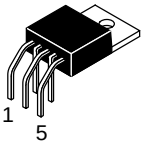
**http://onsemi.com**




**TO−220**
**FIVE LEAD**
**T SUFFIX**
**CASE 314D**

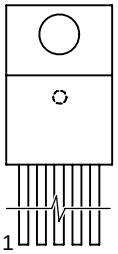



**TO−220**
**FIVE LEAD**
**TVA SUFFIX**
**CASE 314K**




**TO−220**
**FIVE LEAD**
**THA SUFFIX**
**CASE 314A**

### PIN CONNECTIONS




Tab = GND

Pin 1. $V_{IN}$
2. $V_{OUT1}$
3. GND
4. ENABLE
5. $V_{OUT2}$

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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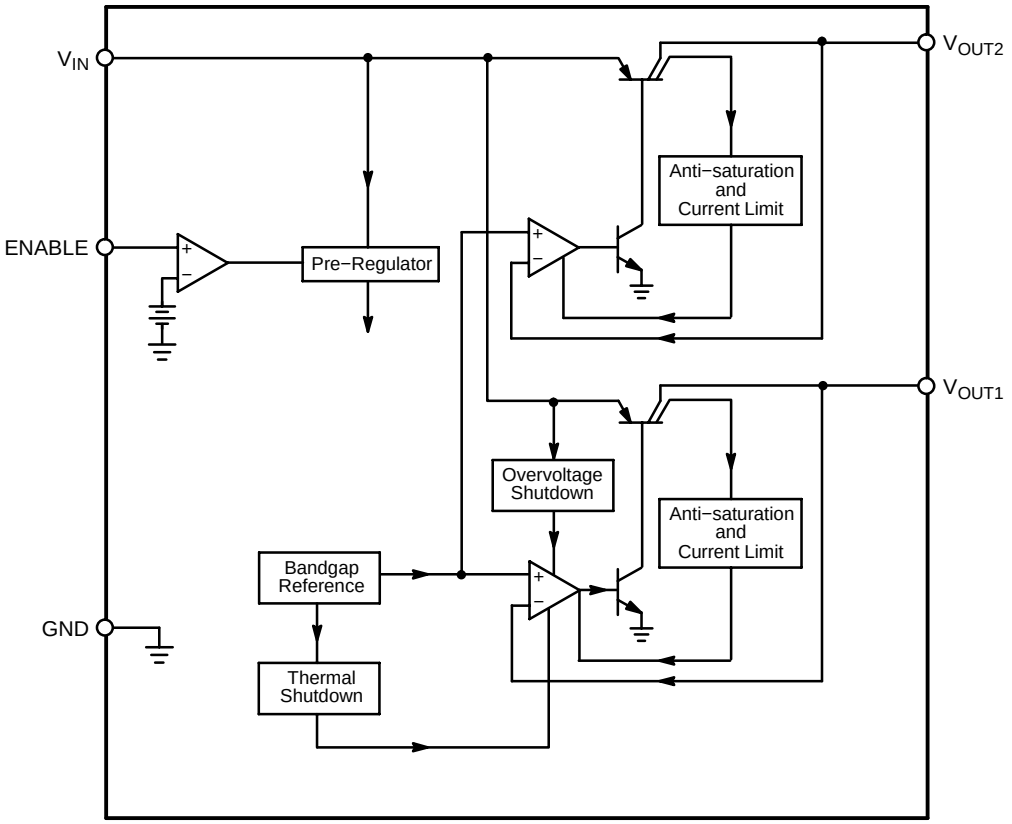



**Figure 1. Block Diagram**

## ABSOLUTE MAXIMUM RATINGS

| Rating | | Value | Unit |
|---|---|---|---|
| Input Voltage: | Operating Range<br>Overvoltage Protection | −15 to 26<br>74 | V<br>V |
| Internal Power Dissipation | | Internally Limited | − |
| Junction Temperature Range | | −40 to +150 | °C |
| Storage Temperature Range | | −65 to +150 | °C |
| Lead Temperature Soldering | Wave Solder (through hole styles only) (Note 1)<br>Reflow (SMD styles only) (Note 2) | 260 peak<br>230 peak | °C<br>°C |
| ESD (Human Body Model) | | 2.0 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 second maximum.
2. 60 second maximum above 183°C

**ELECTRICAL CHARACTERISTICS for $V_{OUT}$:** (6.0 V ≤ $V_{IN}$ ≤ 26 V; $I_{OUT1}$ = 5.0 mA; $I_{OUT2}$ = 5.0 mA; −40°C ≤ $T_J$ ≤ +150°C; −40°C ≤ $T_A$ ≤ +125°C; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **PRIMARY OUTPUT STAGE ($V_{OUT1}$)** | | | | | |
| Output Voltage, $V_{OUT1}$ | 13 V ≤ $V_{IN}$ ≤ 26 V, $I_{OUT1}$ ≤ 400 mA | 11.4 | 12.0 | 12.6 | V |
| Dropout Voltage | $I_{OUT1}$ = 400 mA | – | 0.35 | 0.6 | V |
| Line Regulation | 13 V ≤ $V_{IN}$ ≤ 20 V, 5.0 mA ≤ $I_{OUT}$ < 400 mA | – | – | 80 | mV |
| Load Regulation | 5.0 mA ≤ $I_{OUT1}$ ≤ 400 mA, $V_{IN}$ = 14 V | – | – | 80 | mV |
| Quiescent Current | $I_{OUT1}$ ≤ 100 mA, No Load on $V_{OUT2}$<br>$I_{OUT1}$ ≤ 400 mA, No Load on $V_{OUT2}$ | –<br>– | 8.0<br>50 | 12<br>75 | mA<br>mA |
| Ripple Rejection | f = 120 Hz, $I_{OUT}$ = 300 μA, $V_{IN}$ = 15.0 $V_{DC}$, 2.0 $V_{RMS}$ | 42 | – | – | dB |
| Current Limit | – | 0.40 | – | 1.0 | A |
| Reverse Polarity Input Voltage, DC | $V_{OUT1}$ ≥ −0.6 V, 10 Ω Load | – | −30 | −18 | V |
| Reverse Polarity Input Voltage, Transient | 1.0% Duty Cycle, t = 100 ms, $V_{OUT}$ ≥ −6.0 V, 10 Ω Load | – | −80 | −50 | V |
| Overvoltage Shutdown | – | 28 | 34 | 45 | V |
| Short Circuit Current | – | – | – | 700 | mA |
| **SECONDARY OUTPUT ($V_{OUT2}$)** | | | | | |
| Output Voltage, ($V_{OUT2}$) | 6.0 V ≤ $V_{IN}$ ≤ 26 V, $I_{OUT2}$ ≤ 200 mA | 4.90 | – | 5.10 | V |
| Dropout Voltage | $I_{OUT2}$ ≤ 200 mA | – | 0.35 | 0.60 | V |
| Line Regulation | 6.0 V ≤ $V_{IN}$ ≤ 26 V, 1.0 mA ≤ $I_{OUT}$ ≤ 200 mA | – | – | 50 | mV |
| Load Regulation | 1.0 mA ≤ $I_{OUT2}$ ≤ 200 mA; $V_{IN}$ =14 V | – | – | 50 | mV |
| Quiescent Current | $I_{OUT2}$ = 50 mA<br>$I_{OUT2}$ = 200 mA | –<br>– | 5.0<br>20 | 10<br>35 | mA<br>mA |
| Ripple Rejection | f = 120 Hz; $I_{OUT}$ = 10 mA, $V_{IN}$ = 15 V, 2.0 $V_{RMS}$ | 42 | – | – | dB |
| Current Limit | – | 200 | – | 600 | mA |
| Short Circuit Current | – | – | – | 400 | mA |
| **ENABLE FUNCTION (ENABLE)** | | | | | |
| Input ENABLE Threshold | $V_{OUT1}$ Off<br>$V_{OUT1}$ On | –<br>2.00 | 1.30<br>1.30 | 0.80<br>– | V<br>V |
| Input ENABLE Current | $V_{ENABLE}$ = 5.5 V<br>$V_{ENABLE}$ < 0.8 V | 80<br>−10 | –<br>– | 500<br>10 | μA<br>μA |
| **OTHER FEATURES** | | | | | |
| Sleep Mode | $V_{ENABLE}$ < 0.4 V | – | 0.2 | 50 | μA |
| Thermal Shutdown | – | 150 | – | 210 | °C |
| Quiescent Current in Dropout | $I_{OUT1}$ = 100 mA, $I_{OUT2}$ = 50 mA | – | – | 60 | mA |

## PACKAGE PIN DESCRIPTION

| PACKAGE LEAD #<br>5 Lead TO−220 | LEAD SYMBOL | FUNCTION |
|---|---|---|
| 1 | $V_{IN}$ | Supply voltage, usually direct from battery. |
| 2 | $V_{OUT1}$ | Regulated output 12 V, 400 mA (typ). |
| 3 | GND | Ground connection. |
| 4 | ENABLE | CMOS compatible input lead; switches outputs on and off. When ENABLE is high $V_{OUT1}$ and $V_{OUT2}$ are active. |
| 5 | $V_{OUT2}$ | Regulated output 5.0 V, 200 mA (typ). |

## TYPICAL PERFORMANCE CHARACTERISTICS

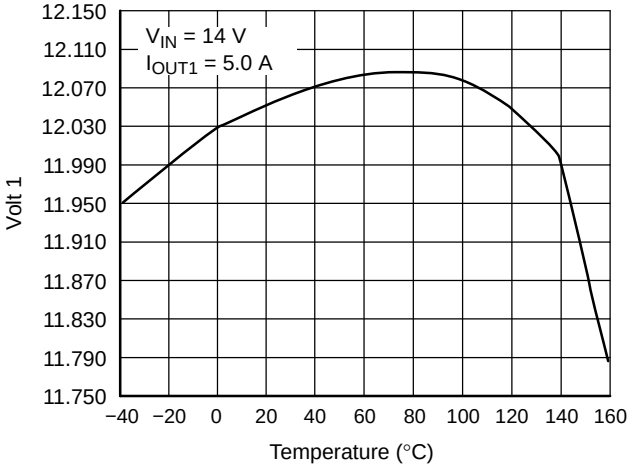



**Figure 2. Output Voltage vs. Temperature for $V_{OUT1}$**

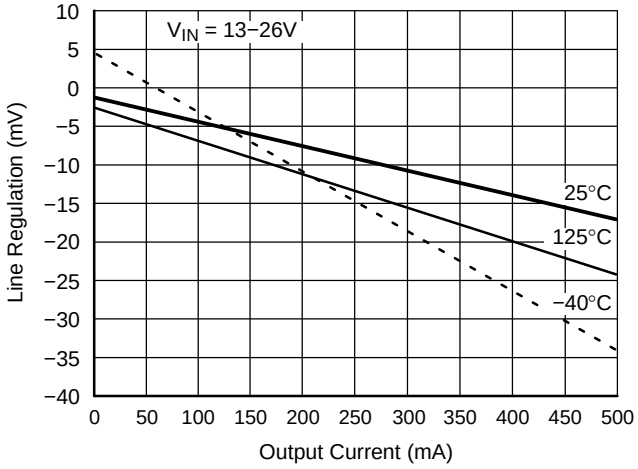



**Figure 3. Line Regulation vs. Output Current for $V_{OUT1}$**

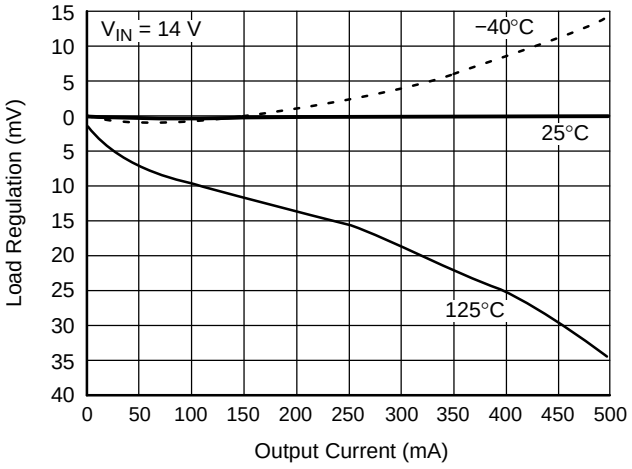



**Figure 4. Load Regulation vs. Output Current for $V_{OUT1}$**

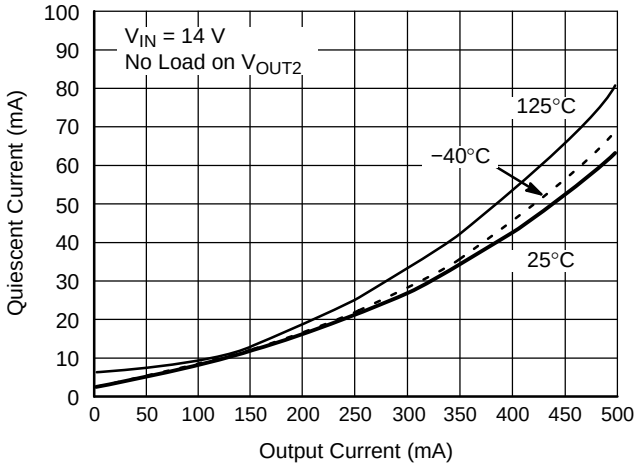



**Figure 5. Quiescent Current vs. Output Current for $V_{OUT1}$**

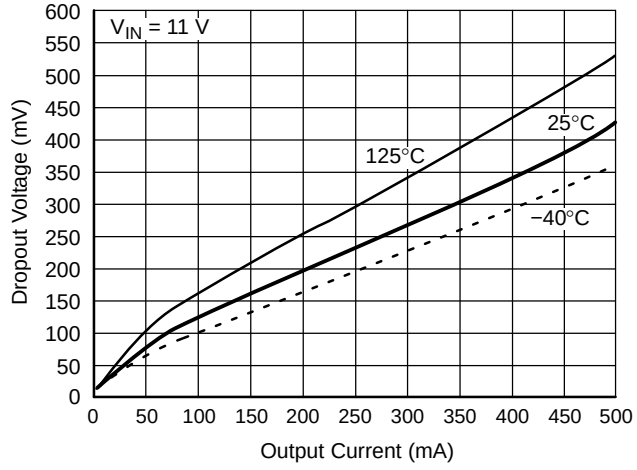



**Figure 6. Dropout Voltage vs. Output Voltage for $V_{OUT1}$**

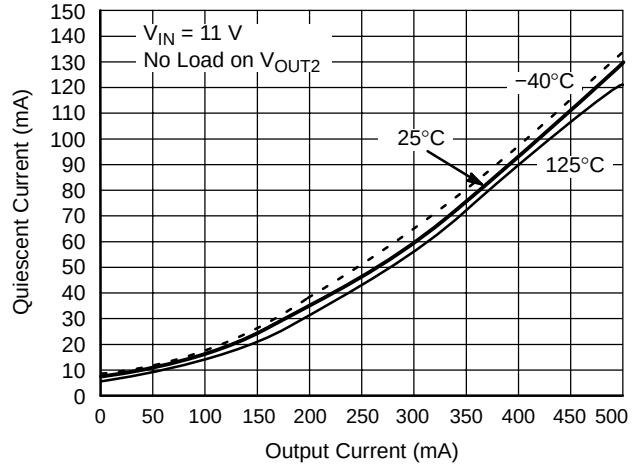



**Figure 7. Quiescent Current vs. Output Current @ Dropout for $V_{OUT1}$**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

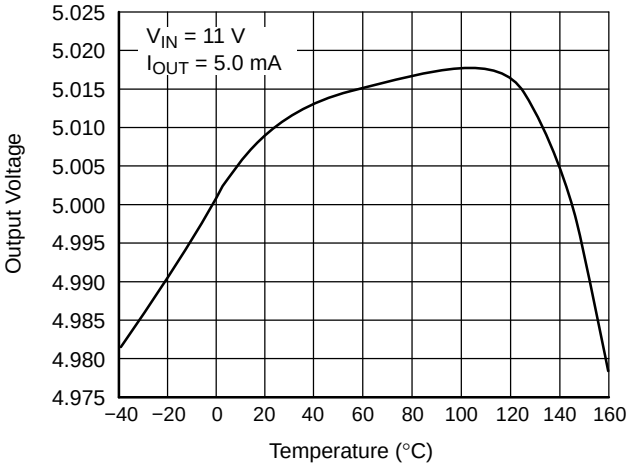



**Figure 8. Output Voltage vs. Temperature for $V_{OUT2}$**

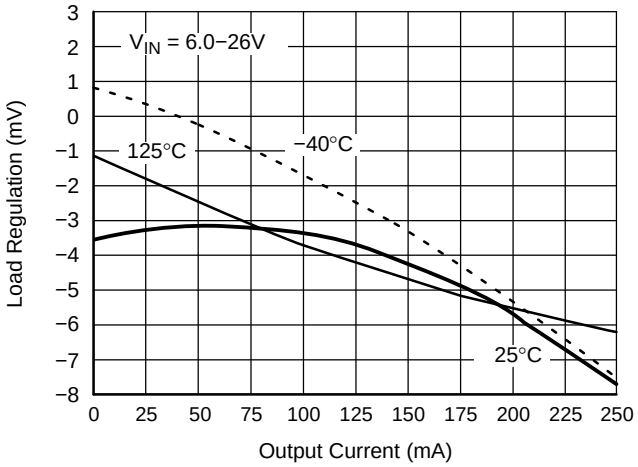



**Figure 9. Line Regulation vs. Output Current for $V_{OUT2}$**

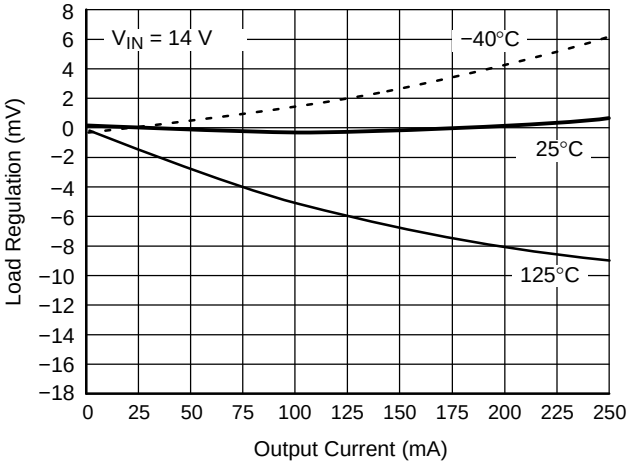



**Figure 10. Load Regulation vs. Output Current for $V_{OUT2}$**

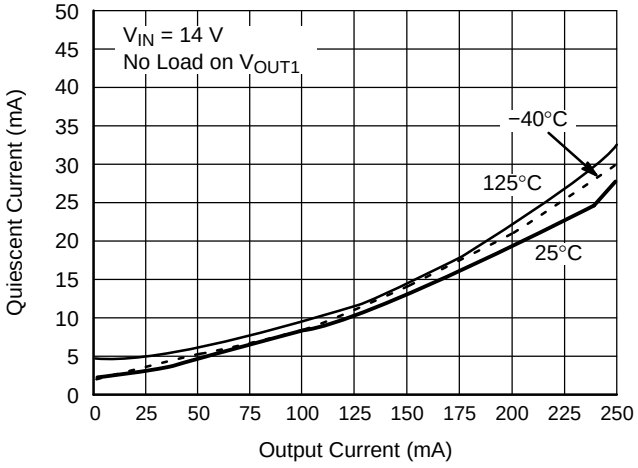



**Figure 11. Quiescent Current vs. Output Current for $V_{OUT2}$**

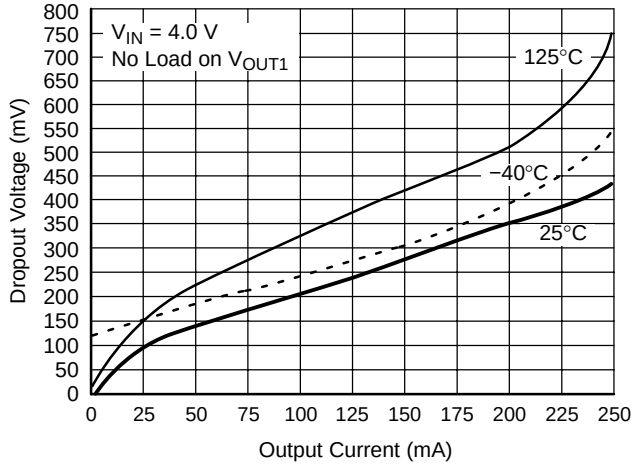



**Figure 12. Dropout Voltage vs. Output Current for $V_{OUT2}$**

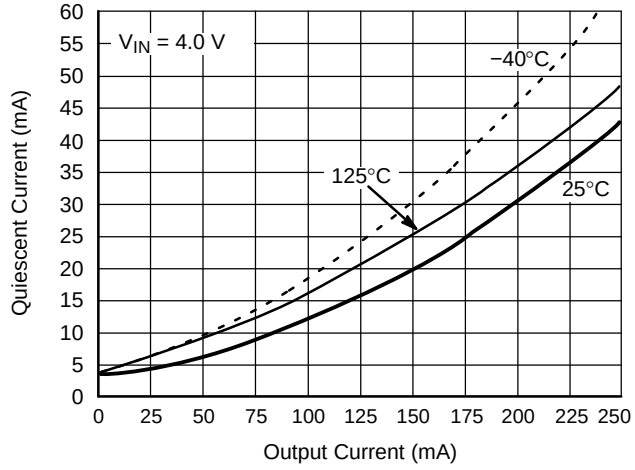



**Figure 13. Quiescent Current vs. Output Current @ Dropout for $V_{OUT2}$**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

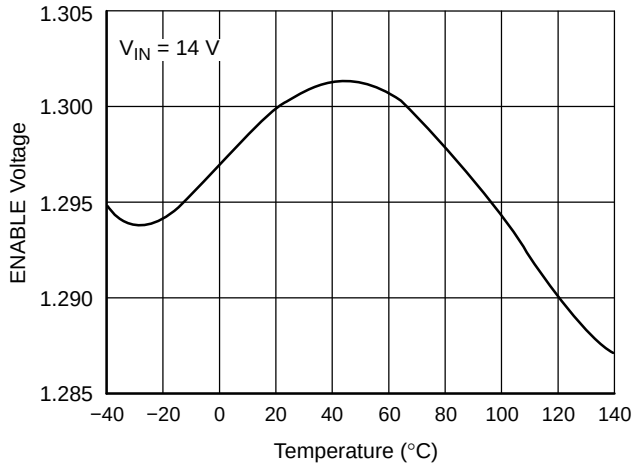



**Figure 14. Enable Threshold Voltage vs. Temperature**

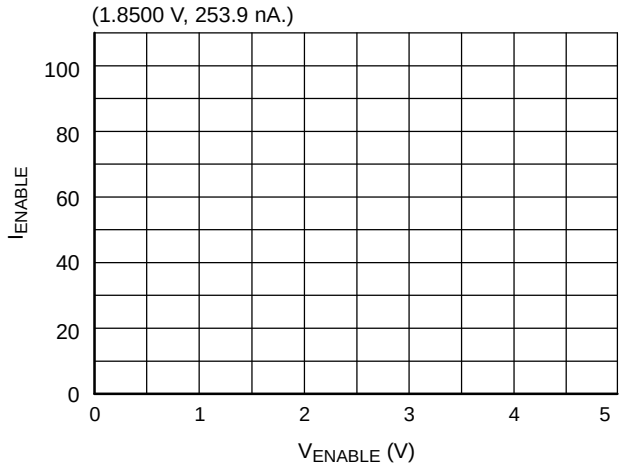



**Figure 15. ENABLE Current vs. ENABLE Voltage**

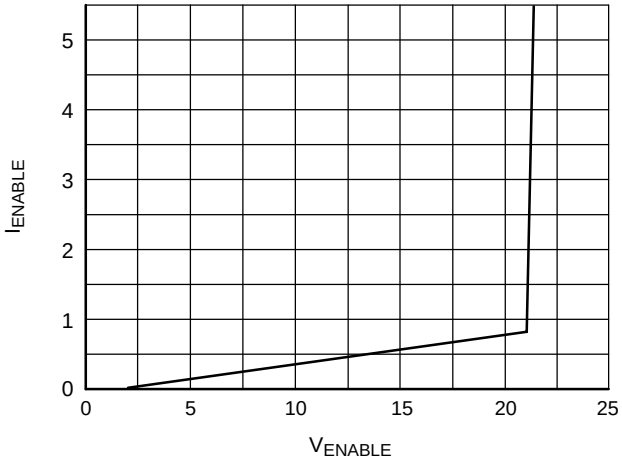



**Figure 16. 12 mA ENABLE Current vs. ENABLE Voltage**

## DEFINITION OF TERMS

**Dropout Voltage** − The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage** − The DC voltage applied to the input terminals with respect to ground.

**Input Output Differential** − The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation** − The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation** − The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability** − Output voltage stability under accelerated life−test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage** − The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current** − The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

**Ripple Rejection** − The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

**Temperature Stability of $V_{OUT}$** − The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

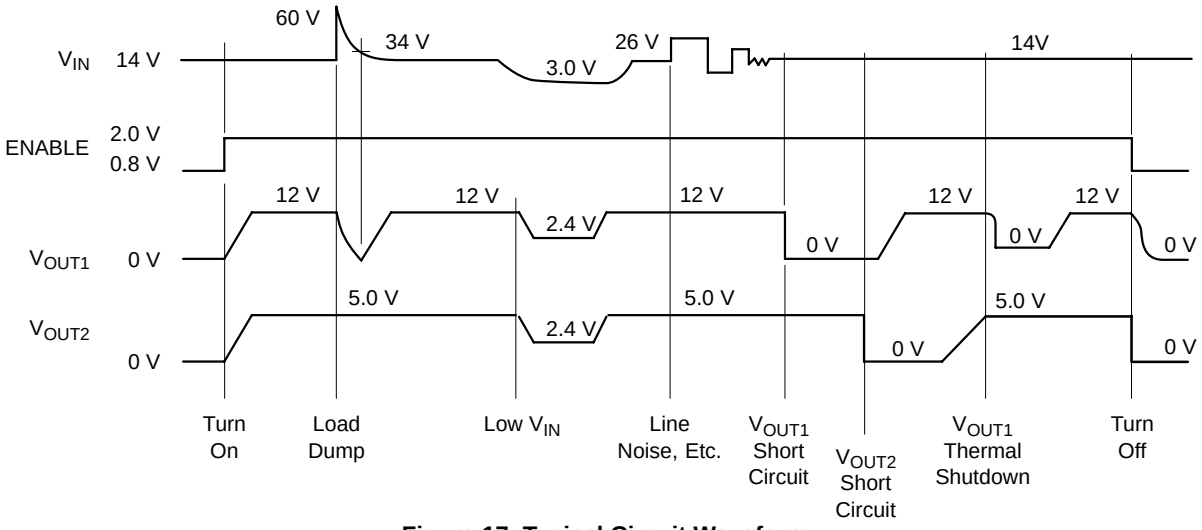
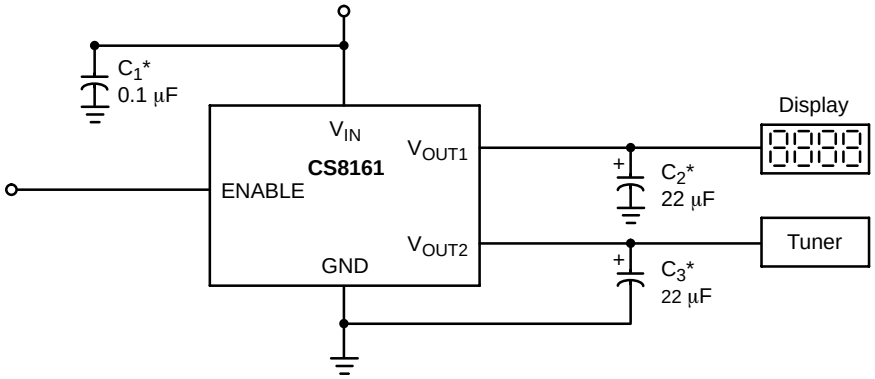



**Figure 17. Typical Circuit Waveform**

## APPLICATION DIAGRAM




* $C_1$ required if regulator is located far from power supply filter.
** $C_2$, $C_3$ required for stability, value may be increased. Capacitor must operate at minimum temperature expected.

**Figure 18. Application Diagram**

## APPLICATION NOTES

Since both outputs are controlled by the same ENABLE, the CS8161 is ideal for applications where a sleep mode is required. Using the CS8161, a section of circuitry such as a display and nonessential 5.0 V circuits can be shut down under microprocessor control to conserve energy.

The example in the Applications Diagram (Figure 18) shows an automotive radio application where the display is powered by the 12 V on $V_{OUT1}$ and the Tuner IC is powered by the 5.0 V on $V_{OUT2}$. Neither output is required unless both the ignition and the Radio On/Off switch are on.

### Stability Considerations

The output or compensation capacitor (Application diagram $C_2$ and $C_3$) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the cheapest solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The values for the output capacitors $C_2$ and $C_3$ shown in the test and applications circuit should work for most applications, however it is not necessarily the best solution.

To determine acceptable values for $C_2$ and $C_3$ for a particular application, start with tantalum capacitors of the recommended value on each output and work towards less expensive alternative parts for each output in turn.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor $C_2$ will simulate the higher ESR of an aluminum capacitor.(Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor $C_2$ is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than 50% of the maximum allowable ESR found in step 3 above. Once the value for $C_2$ is determined, repeat the steps to determine the appropriate value for $C_3$.

### Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 19) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT1(max)} + \{V_{IN(max)} - V_{OUT2(min)}\}I_{OUT2(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from $V_{OUT1}$,

$V_{OUT2(min)}$ is the minimum output voltage from $V_{OUT2}$,

$I_{OUT1(max)}$ is the maximum output current, for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application, and

$I_Q$ is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

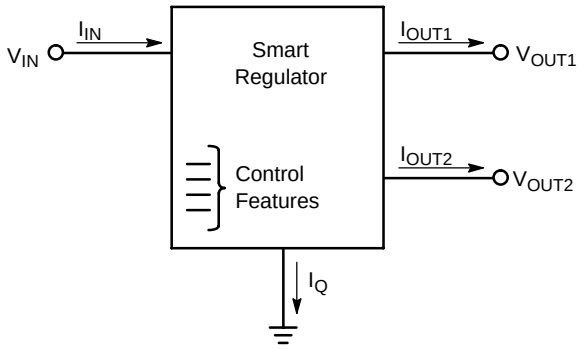



**Figure 19. Dual Output Regulator With Key Performance Parameters Labeled.**

### Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

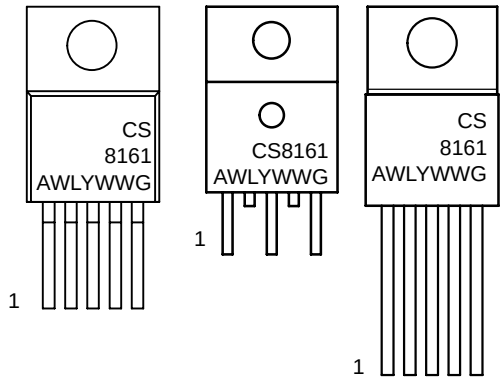
where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## MARKING DIAGRAMS

**TO−220 5−LEAD**




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

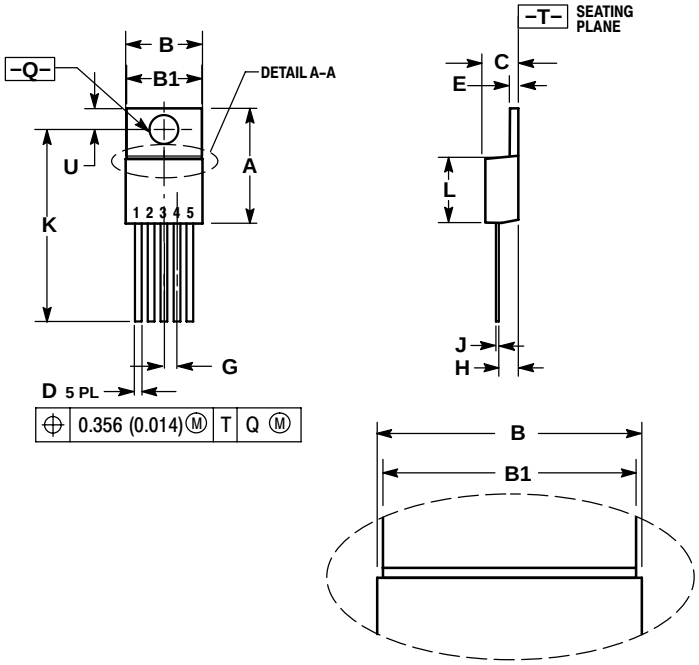
### ORDERING INFORMATION*

| Device | Package | Shipping |
|---|---|---|
| CS8161YT5 | TO−220 STRAIGHT | 50 Units / Rail |
| CS8161YT5G | TO−220 STRAIGHT (Pb−Free) | |
| CS8161YTVA5 | TO−220 VERTICAL | |
| CS8161YTVA5G | TO−220 VERTICAL (Pb−Free) | |
| CS8161YTHA5 | TO−220 HORIZONTAL | |
| CS8161YTHA5G | TO−220 HORIZONTAL (Pb−Free) | |

*Consult your local sales representative for SO−16L package option.

## PACKAGE DIMENSIONS

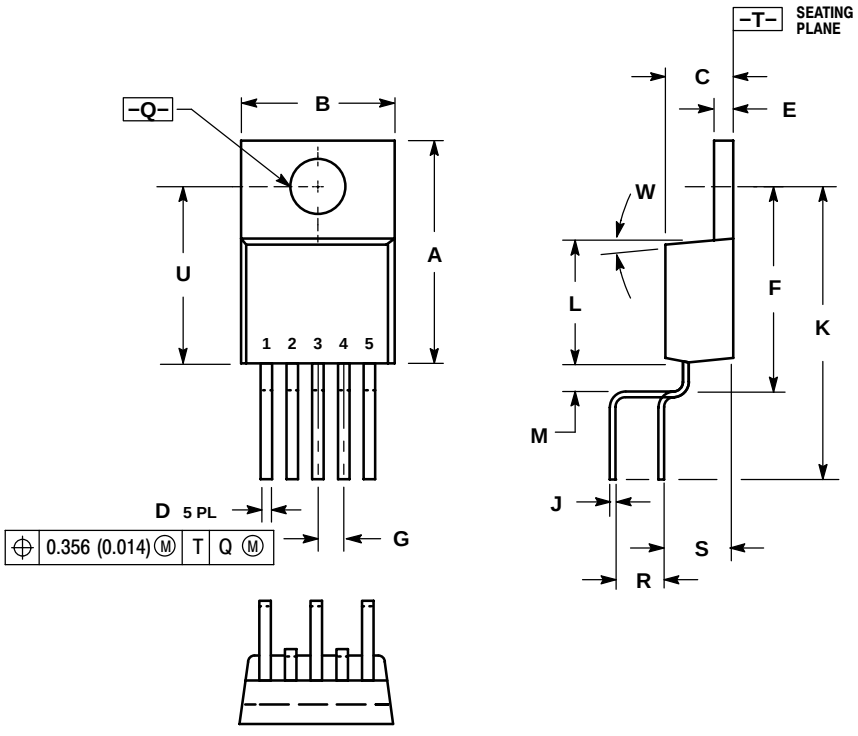
**TO−220**
CASE 314D−04
ISSUE F




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| B1 | 0.375 | 0.415 | 9.525 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.087 | 0.112 | 2.210 | 2.845 |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.977 | 1.045 | 24.810 | 26.543 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| U | 0.105 | 0.117 | 2.667 | 2.972 |

**TO−220**
**TVA SUFFIX**
CASE 314K−01
ISSUE O

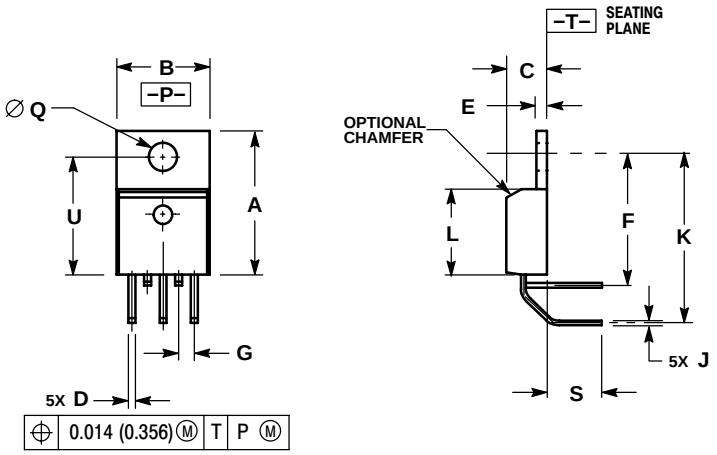



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.560 | 0.590 | 14.22 | 14.99 |
| B | 0.385 | 0.415 | 9.78 | 10.54 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.027 | 0.037 | 0.69 | 0.94 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.530 | 0.545 | 13.46 | 13.84 |
| G | 0.067 BSC | | 1.70 BSC | |
| J | 0.014 | 0.022 | 0.36 | 0.56 |
| K | 0.785 | 0.800 | 19.94 | 20.32 |
| L | 0.321 | 0.337 | 8.15 | 8.56 |
| M | 0.063 | 0.078 | 1.60 | 1.98 |
| Q | 0.146 | 0.156 | 3.71 | 3.96 |
| R | 0.271 | 0.321 | 6.88 | 8.15 |
| S | 0.146 | 0.196 | 3.71 | 4.98 |
| U | 0.460 | 0.475 | 11.68 | 12.07 |
| W | 5 ° | | 5 ° | |

## PACKAGE DIMENSIONS

**TO−220**
**THA SUFFIX**
CASE 314A−03
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| F | 0.570 | 0.585 | 14.478 | 14.859 |
| G | 0.067 BSC | | 1.702 BSC | |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.730 | 0.745 | 18.542 | 18.923 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| S | 0.210 | 0.260 | 5.334 | 6.604 |
| U | 0.468 | 0.505 | 11.888 | 12.827 |

### PACKAGE THERMAL DATA

| Parameter | | TO−220 FIVE LEAD | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Typical | 2.0 | °C/W |
| $R_{\theta JA}$ | Typical | 50 | °C/W |

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