FAIRCHILD SEMICONDUCTOR®

January 2003
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100LVELT22
3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

General Description

The 100LVELT22 is a LVTTL/LVCMOS to differential LVPECL translator operating from a single +3.3V supply.

Both outputs of a differential pair should be terminated in 50Ω to V_{CC} - 2.0V even if only one output is being used. If an output pair is unused both outputs can be left open (un-terminated).

The 100 series is temperature compensated.

Features

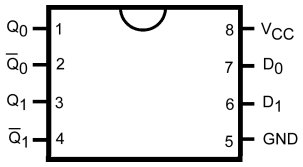
- Typical propagation delay of 350 ps
- <100 ps skew between outputs
- Max I_{CC} of 28 mA at 25°C
- When TTL input is left Open Q output defaults HIGH
- Fairchild MSOP-8 package is a drop-in replacement to ON TSSOP-8
- Flow through pinout
- Meets or exceeds JEDEC specification EIA/JESD78 IC latch-up test
- Moisture Sensitivity Level 1
- ESD Performance:
  - Human Body Model > 2000V
  - Machine Model > 200V

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description
100LVELT22M	M08A	KVT22	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
100LVELT22M8 (Preliminary)	MA08D	KR22	8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

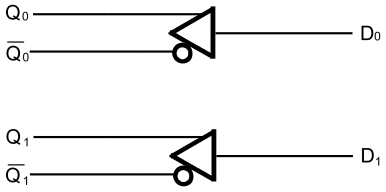
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Logic Diagram



Pin Descriptions

Pin Name	Description
Q_n, $\overline{Q}_n$	LVPECL Differential Outputs
D_0, D_1	LVTTL/LVCMOS Inputs
V_{CC}	Positive Supply
GND	Ground

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	0.0V to +7.0V
Input Voltage (V_I) $V_I \le V_{CC}$	0.0V to +7.0V
DC Output Current (I_{OUT})	
Continuous	50 mA
Surge	100 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

Power Supply Operating	V_{CC} = 3.0V to 3.8V
LVTTL/LVCMOS Input Voltage	0.0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

LVPECL DC Electrical Characteristics V_{CC} = 3.3V; GND = 0.0V (Note 2)

Symbol	Parameter	−40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			28			28			29	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215		2420	2275		2420	2275		2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470		1745	1490		1680	1490		1680	mV

Note 2: Output parameters vary 1 to 1 with V_{CC}. V_{CC} can vary ±0.15V.

Note 3: Outputs are terminated through a 50Ω resistor to V_{CC} − 2.0V.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

LVTTL/LVCMOS DC Electrical Characteristics V_{CC} = 3.3V; GND = 0.0V (Note 4)

Symbol	Parameter	T_A = −40°C to 85°C			Units	Condition
		Min	Typ	Max		
I_{IH}	Input HIGH Current			20 100	µA	V_{IN} = 2.7V V_{IN} = V_{CC}
I_{IL}	Input LOW Current			−200	µA	V_{IN} = 0.5V
V_{IK}	Clamp Diode Voltage			−1.2	V	I_{IN} = −18 mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

Note 4: V_{CC} can vary ±0.15V.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

AC Electrical Characteristics V_{CC} = 3.3V; GND = 0.0V (Note 5)

Symbol	Parameter		−40°C			25°C			85°C			Units	Figure Number
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency			TBD			TBD			TBD		MHz	
t_{JITTER}	Cycle-to-Cycle Jitter			TBD			TBD			TBD		ps	
t_{PLH} / t_{PHL}	Propagation Delay (Note 6)		200	350	600	200	350	600	200	350	600	ps	Figure 1
t_{SKEW}	Skew	Output-to-Output		30	100		30	100		30	100	ps	
		Part-to-Part			400			400			400		
t_r, t_f	Output Rise Time Q (20% to 80%)		200		550	200		500	200		500	ns	Figure 2

Note 5: V_{CC} can vary ±0.15V.

Note 6: Specifications for standard LVTTL input signal (see Figure 1).

Switching Waveforms

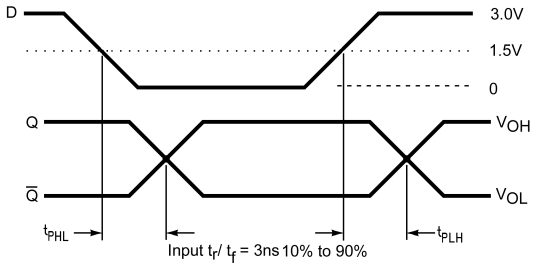


FIGURE 1. LVTTL to Differential LVPECL Propagation Delay

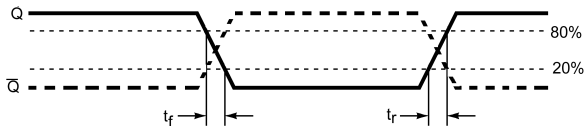
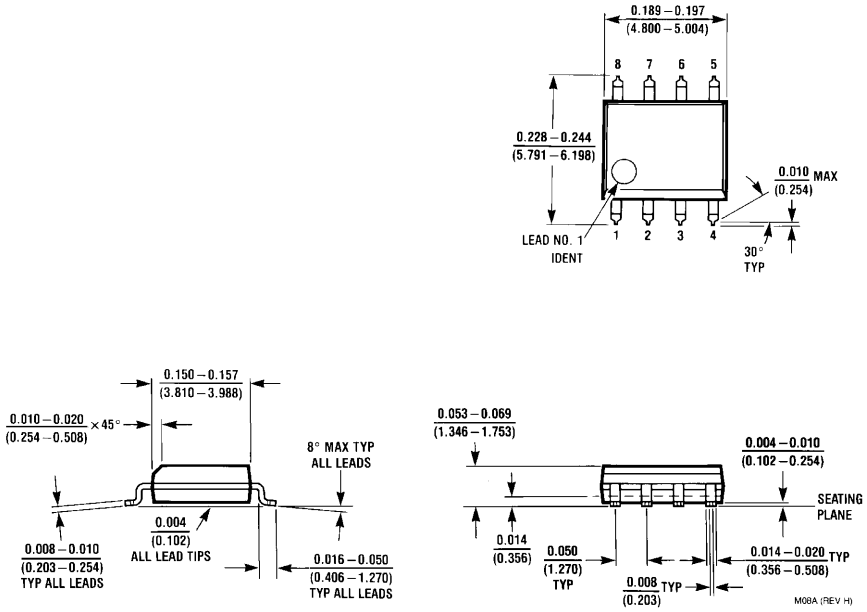


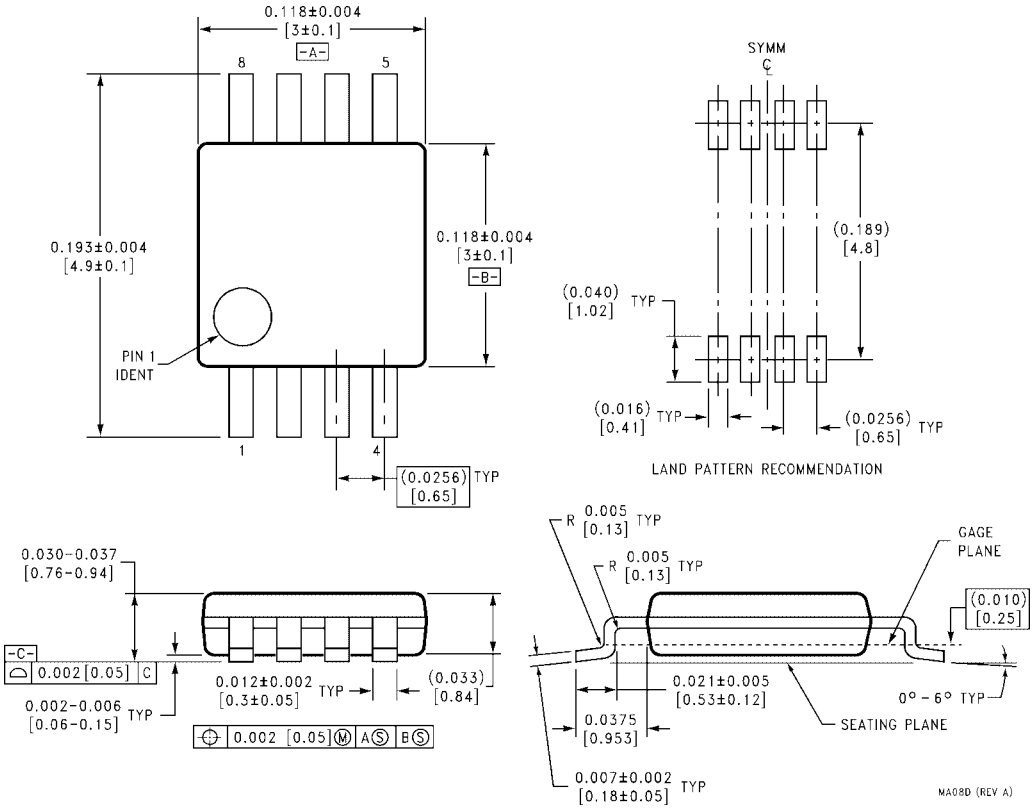
FIGURE 2. Differential Output Edge Rates

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
Package Number MA08D

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