

Product Description

The PE83511 is a high-performance static UltraCMOS™ prescaler with a fixed divide ratio of 2. Its operating frequency range is DC to 1500 MHz. The PE83511 operates on a nominal 3V supply and draws only 14 mA. It is packaged in a small 8-lead plastic MSOP and is ideal for frequency scaling and clock generation solutions.

The PE83511 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

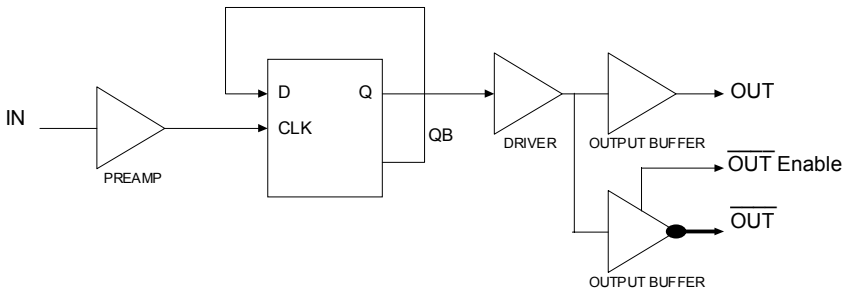


Figure 2. Package Type

8-lead MSOP



Table 1. Electrical Specifications ($Z_S = Z_L = 50 \Omega$)

2.85 V $\leq V_{DD} \leq 3.15$ V; $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current	OUTB Disabled		7	12	mA
	OUTB Enabled		14	25	mA
Input Frequency (F_{IN})		DC		1500	MHz
Input Power (P_{IN})	$100\text{ MHz} \leq F_{in} \leq 1200\text{ MHz}$ $-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-5		+10	dBm
	$100\text{ MHz} \leq F_{in} \leq 1200\text{ MHz}$ $85^\circ\text{C} \geq T_A \geq 125^\circ\text{C}$	0		+10	dBm
	$1200\text{ MHz} < F_{in} \leq 1500\text{ MHz}$ $-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	+5		+10	dBm
Output Power	$\text{DC} < F_{in} \leq 1500\text{ MHz}$	+2			dBm

Figure 3. Pin Configuration (Top View)

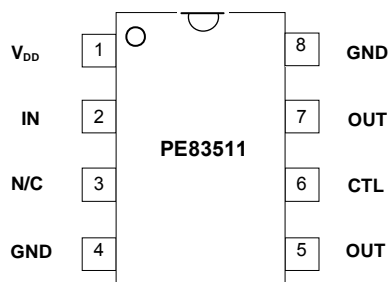


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V _{DD}	Power supply pin. Bypassing is required (eg 1000 pF & 100 pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg 1000 pF).
3	N/C	No connection. This pin should be left open.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	OUTB	Inverted divided frequency output. This pin should be coupled with a capacitor (eg 1000 pF).
6	CTL	Control pin. When grounded OUTB is enabled.
7	OUT	Divided frequency output. This pin should be coupled with a capacitor (eg 1000 pF).
8	GND	Ground Pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Supply voltage		4.0	V
P _{in}	Input Power		15	dBm
V _{IN}	Voltage on input	-0.3	V _{DD} +0.3	V
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	-55	125	°C
VESD	ESD voltage (Human Body Model, MIL-STD 883)		2000	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE83511 divides an input signal, up to a frequency of 1500 MHz, by a factor of two thereby producing an output frequency at half the input frequency. To work properly at higher frequency, the input and output signals (pins 2, 7 & optional 5) must be AC coupled via an external capacitor. The input may be DC coupled for low frequency operation with care taken to remain within the specified DC input range for the device.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 8 for a layout example.

OUTB Control

Pin 6 controls whether OUTB is enabled or disabled. Pin 6 has an internal pull-up resistor. With no connection (floating), OUTB is disabled. By grounding pin 6, OUTB is enabled. By enabling OUTB, this part will consume roughly 5 mA more current.

Typical Performance Data: $V_{DD} = 3.0\text{ V}$

Figure 4. Input Sensitivity

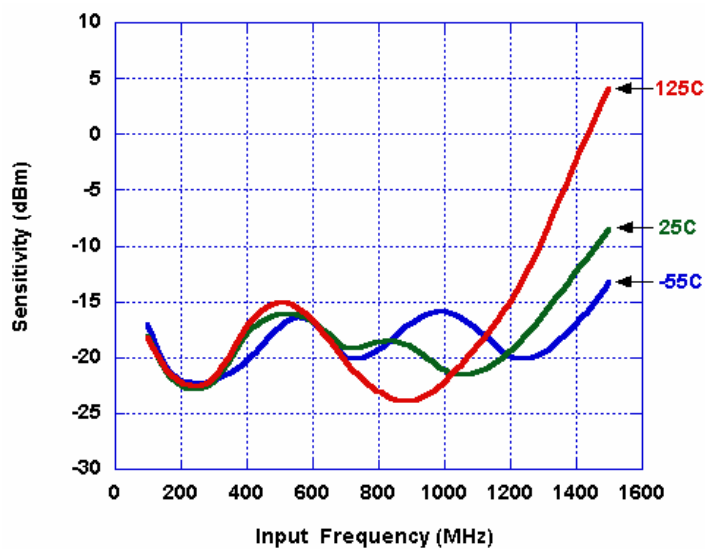


Figure 5. Device Current (OUTB Enabled)

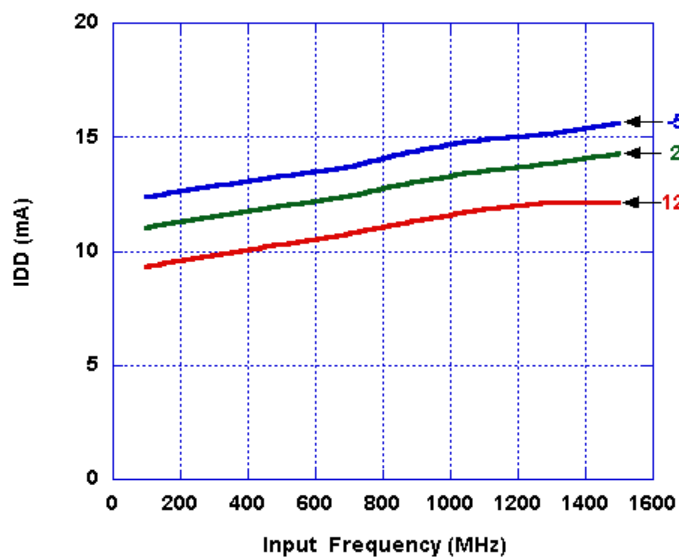


Figure 6. Output Power (OUT or OUTB)

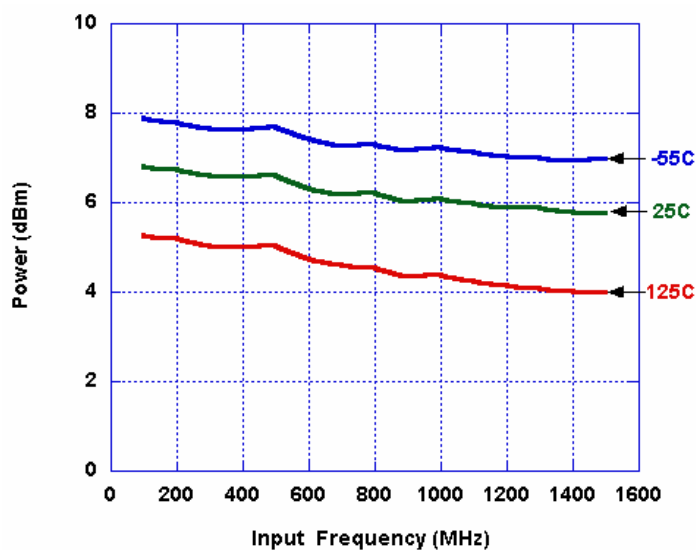
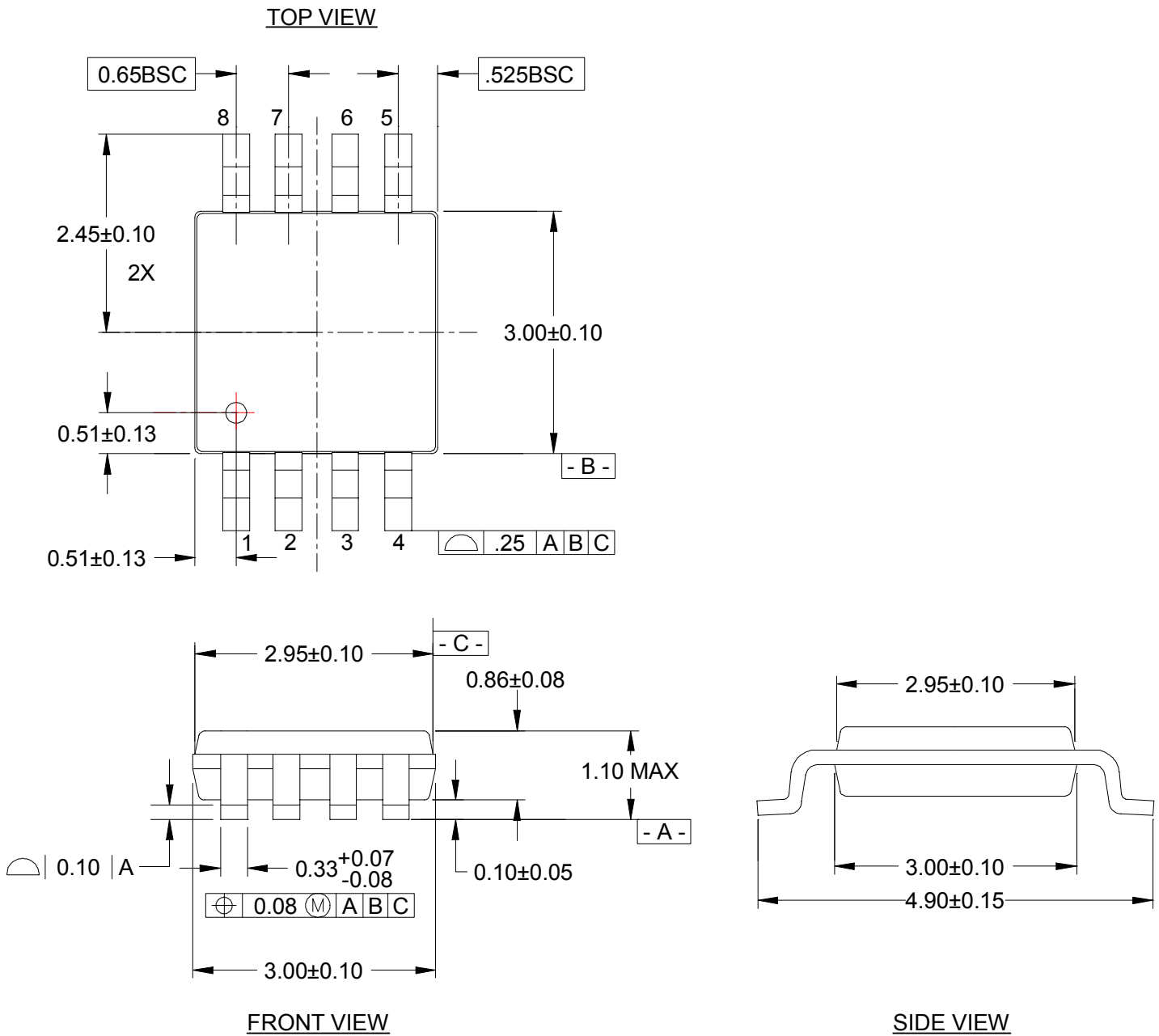
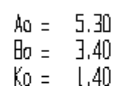


Figure 9. Package Drawing

8-lead MSOP



8-lead MSOP



NOTES:

1. TO SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
83511-01	PE83511	PE83511-08MSOP-50A	8-lead MSOP	50 units / Tube
83511-02	PE83511	PE83511-08MSOP-2000C	8-lead MSOP	2000 units / T&R
83511-00	PE83511-EK	PE83511-08MSOP-EK	Evaluation Kit	1 / Box

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Preliminary Specification

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