This X25040 device has been acquired by
IC MICROSYSTEMS from Xicor, Inc.

4K X25040 512 x 8 Bit

SPI Serial E²PROM with Block Lock™ Protection

FEATURES

- 1MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 512 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150µA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Lead PDIP Package
- 8-Lead SOIC Package

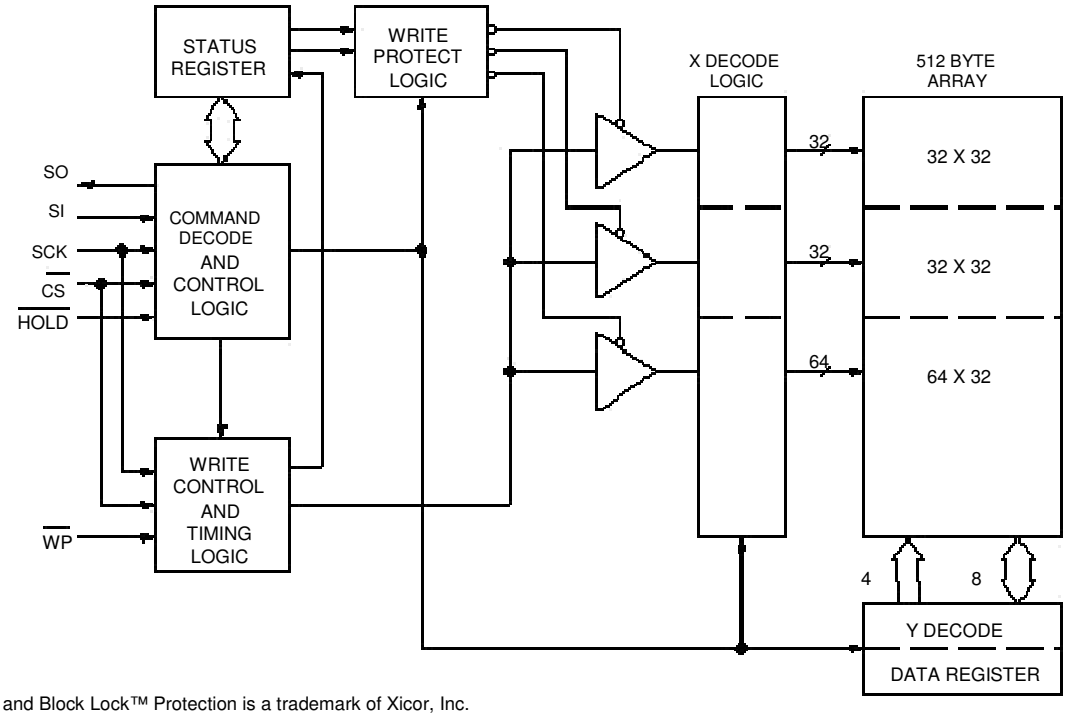
DESCRIPTION

The X25040 is a CMOS 4096-bit serial E²PROM, internally organized as 512 x 8. The X25040 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25040 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25040 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25040 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25040 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



6451 FHD F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

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6451-3.6 6/10/96 T5/C1/D0 NS

Characteristics subject to change without notice

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25040 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25040 will be in the standby power mode. $\overline{CS}$ LOW enables the X25040, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

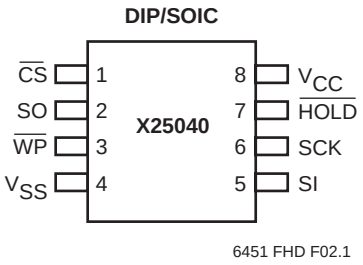
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25040 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25040. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



6451 FHD F02.1

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

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PRINCIPLES OF OPERATION

The X25040 is a 512 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25040 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25040 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25040 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25040 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

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BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25040 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25040 is divided into four 1024-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$180–$1FF
1	0	$100–$1FF
1	1	$000–$1FF

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Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 $A_8$011	Read Data from Memory Array beginning at selected address
WRITE	0000 $A_8$010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

6451 PGM T04.2

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^{2}PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25040, followed by the 8-bit address. Bit 3 of the Read Data instruction contains address A_8. This bit is used to select the upper or lower half of the address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FF) the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^{2}PROM array operation sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25040, the “write enable” latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25040. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 4 bytes of data to the X25040. The only restriction is the 4 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5, 6 and 7 must be “0”. Figure 6 illustrates this sequence.

While the write is in progress following a status register or E^{2}PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25040 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The “write enable” latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The “write enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “write enable” latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

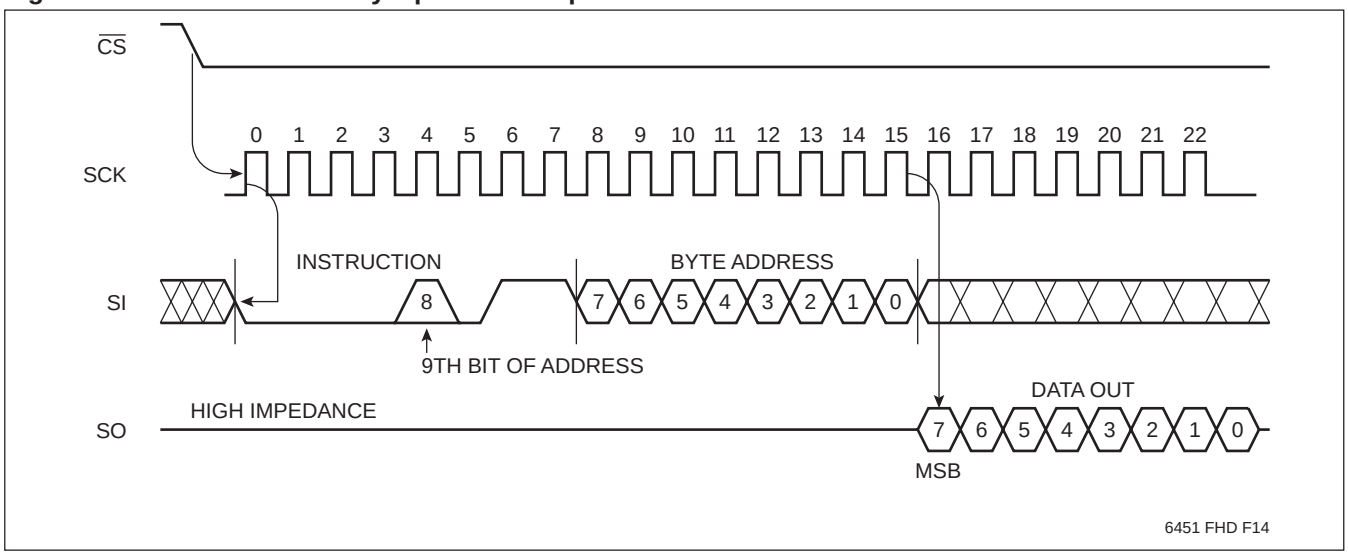


Figure 2. Read Status Register Operation Sequence

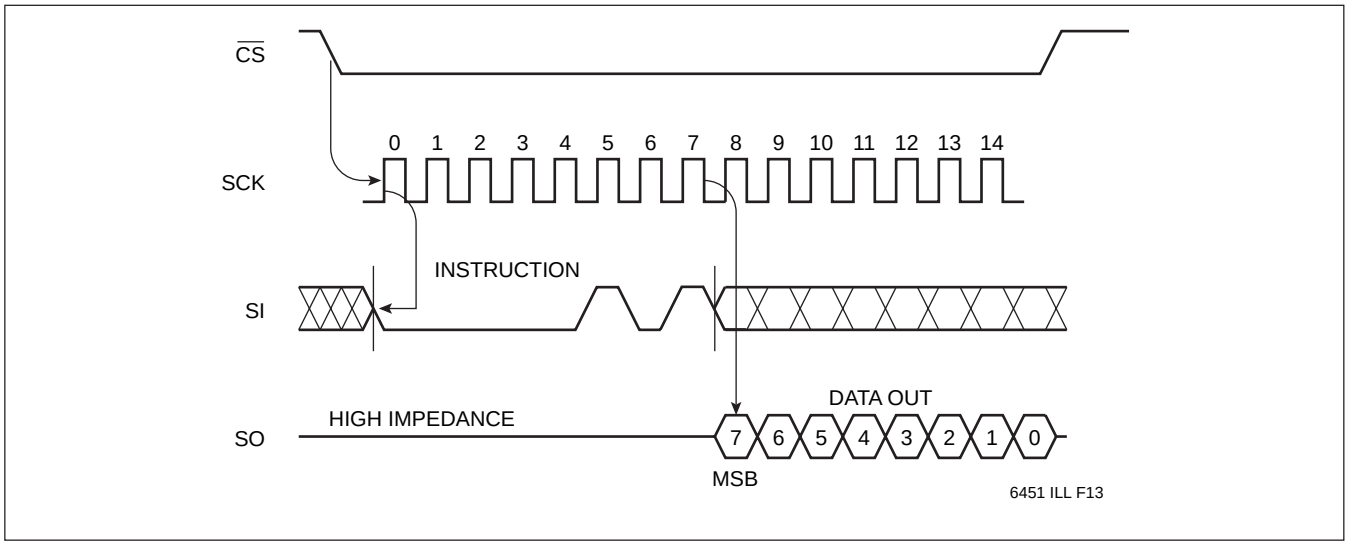


Figure 3. Write Enable Latch Sequence

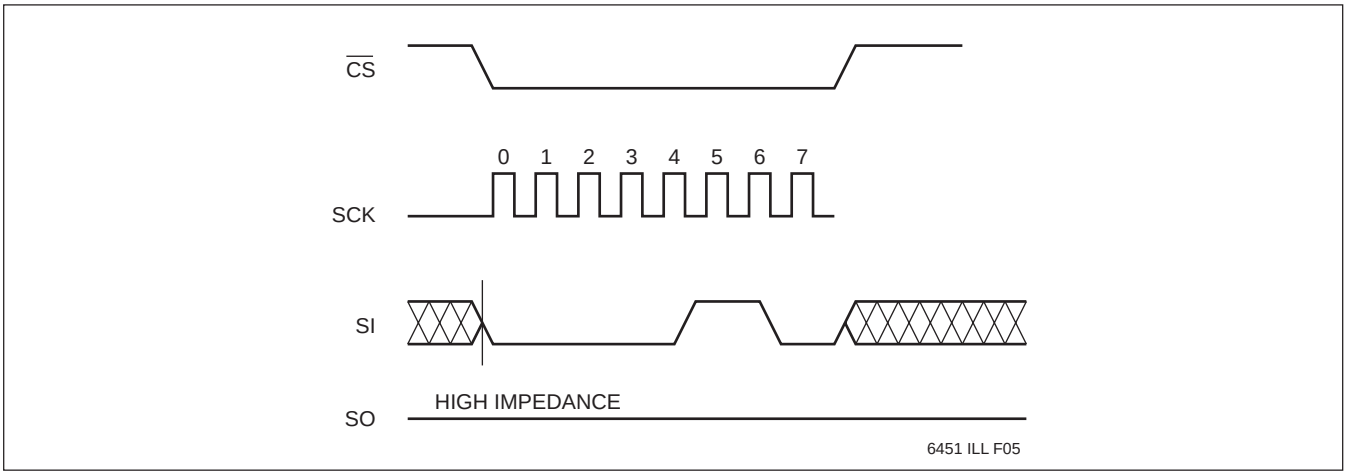


Figure 4. Byte Write Operation Sequence

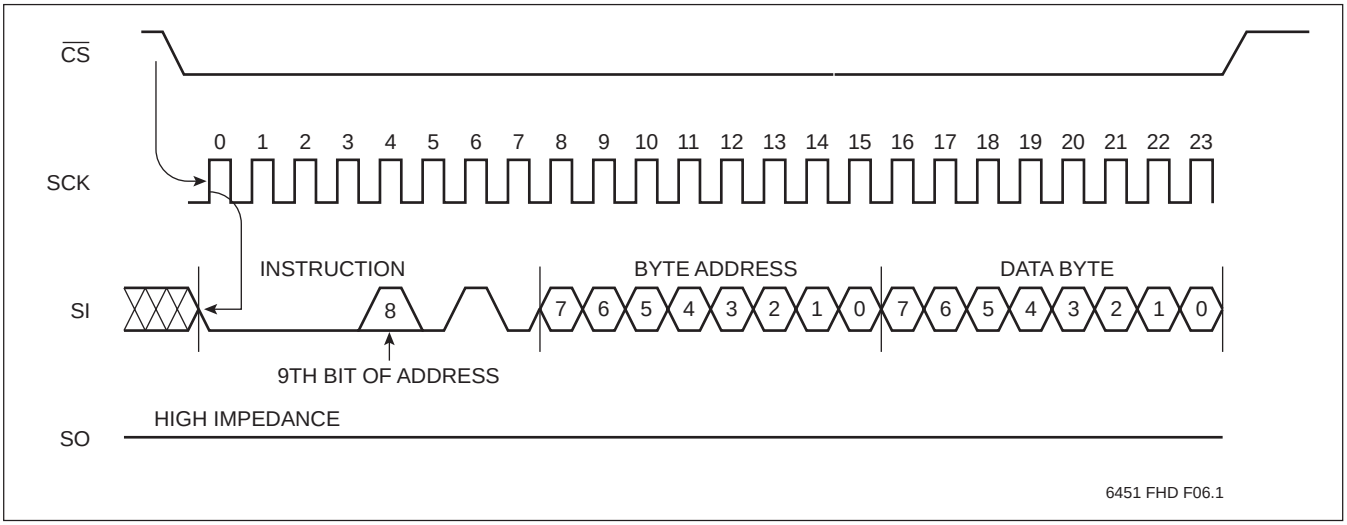


Figure 5. Page Write Operation Sequence

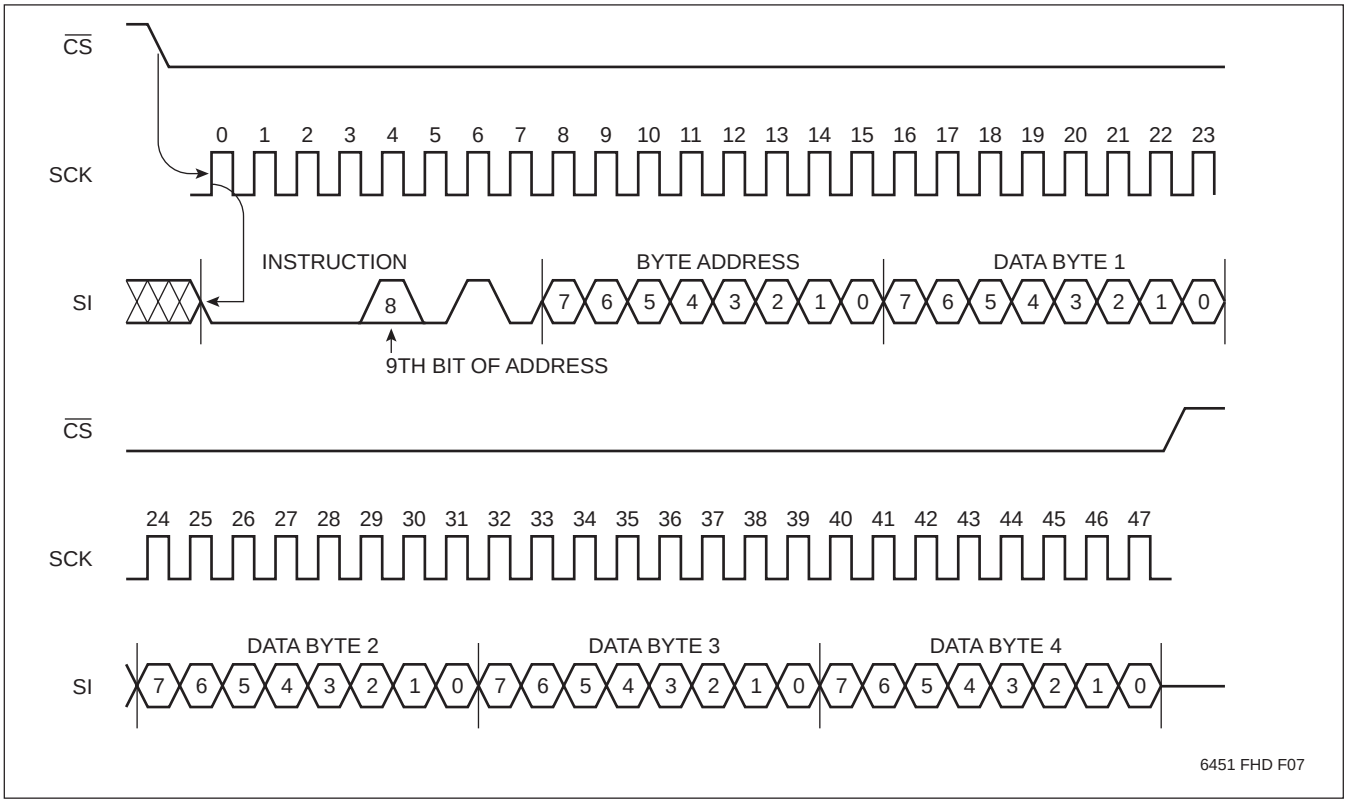
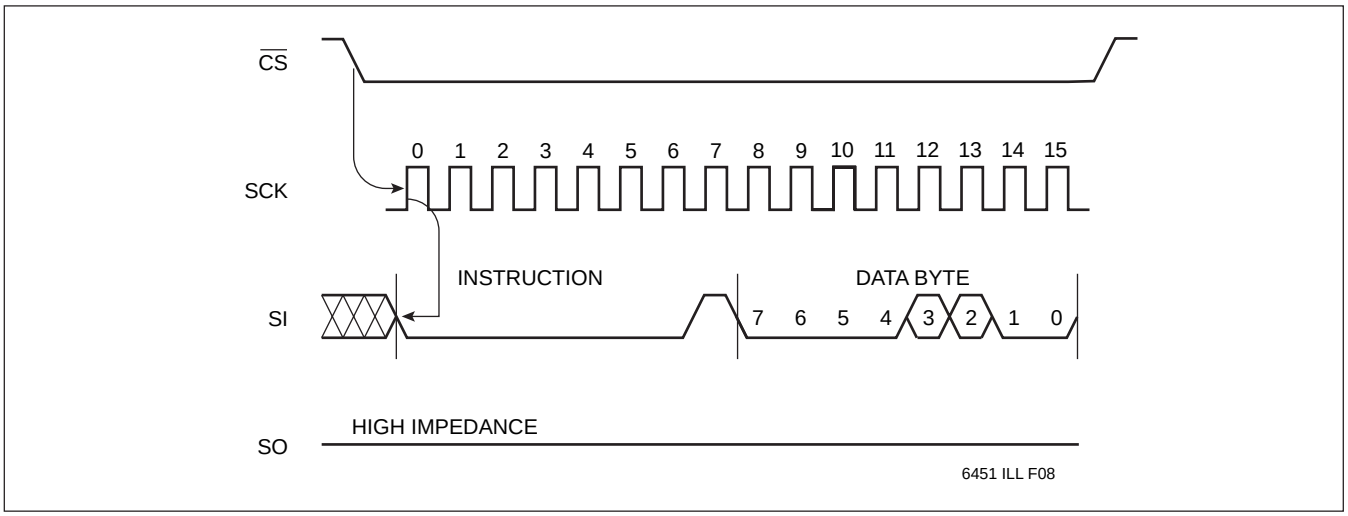


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X25040	5V ±10%
X25040-3	3V to 5.5V
X25040-2.7	2.7 to 5.5V

6451 PGM T06.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

6451 PGM T07.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

6451 PGM T08

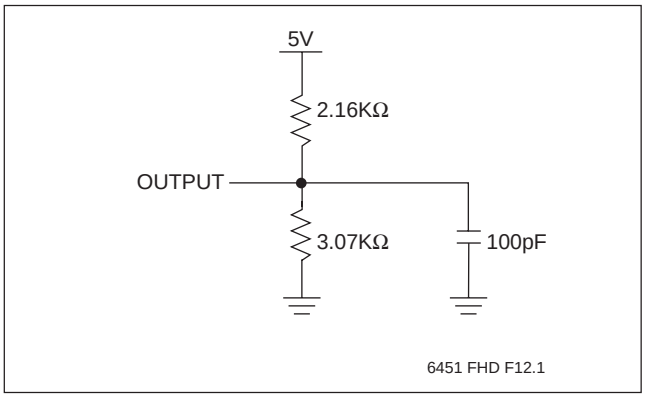
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6451 PGM T09.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6451 PGM T10

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

6451 PGM T11.1

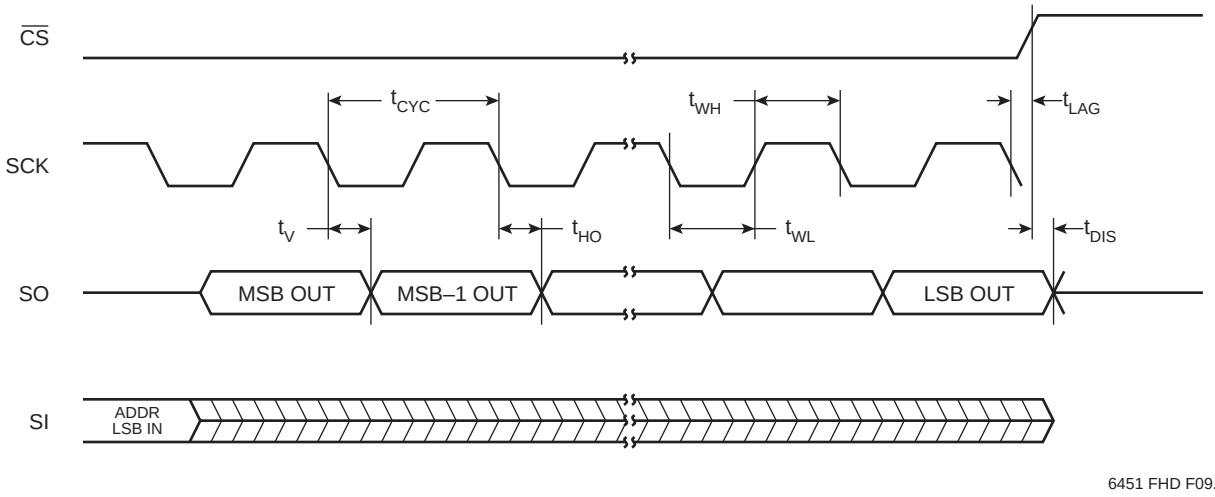
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ LOW to Output in High Z	100		ns

6451 PGM T12.1

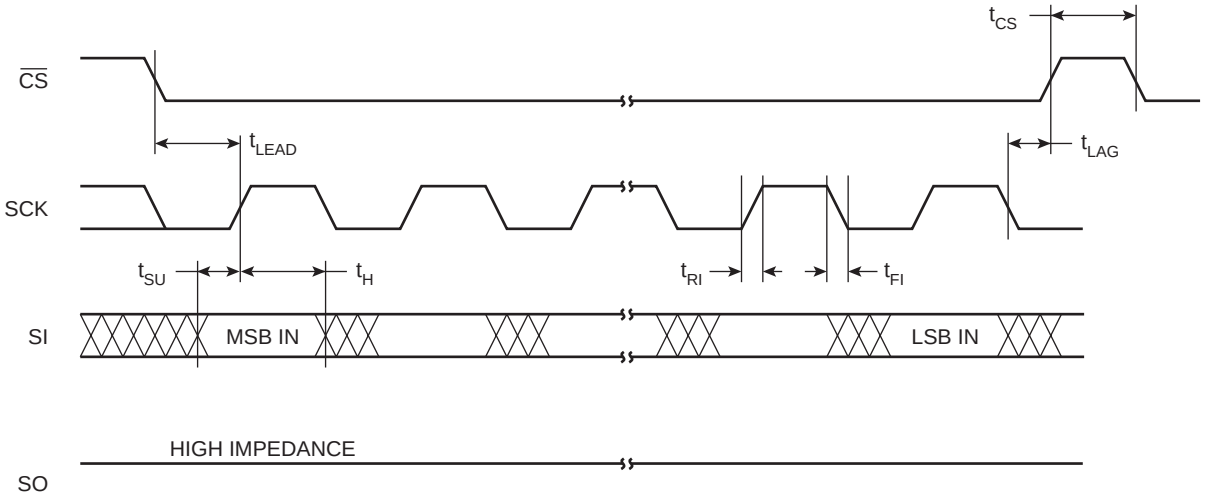
Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



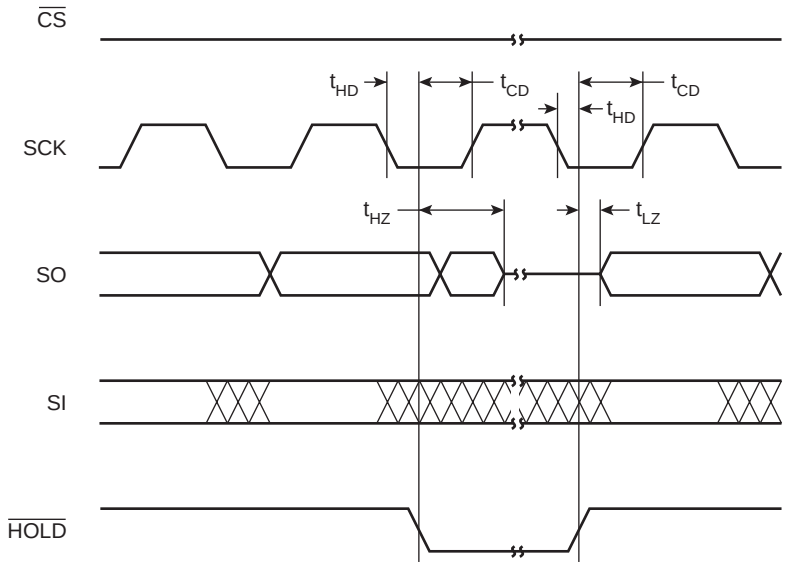
6451 FHD F09.1

Serial Input Timing



6451 FHD F10

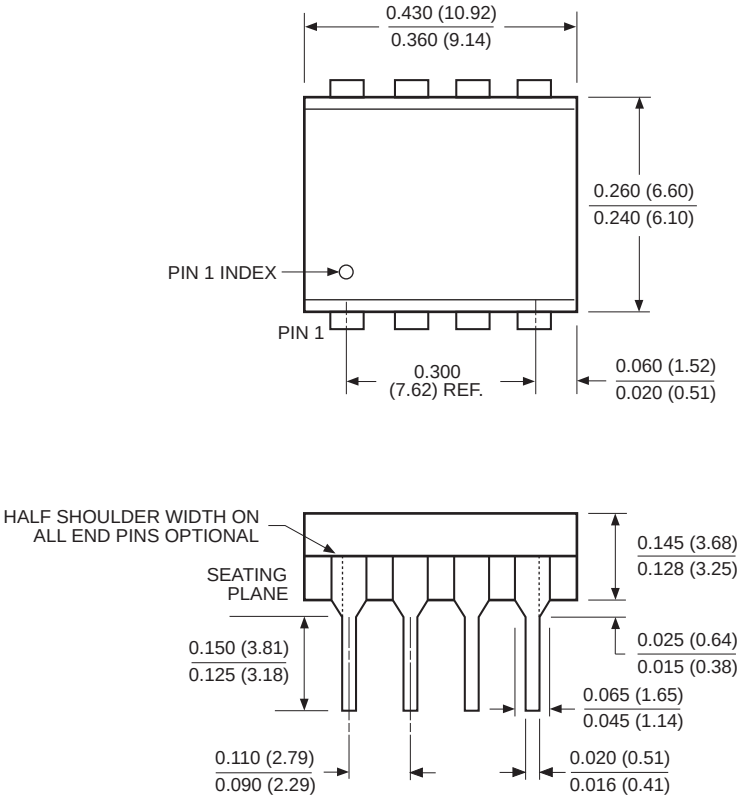
Hold Timing



6451 FHD F11

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



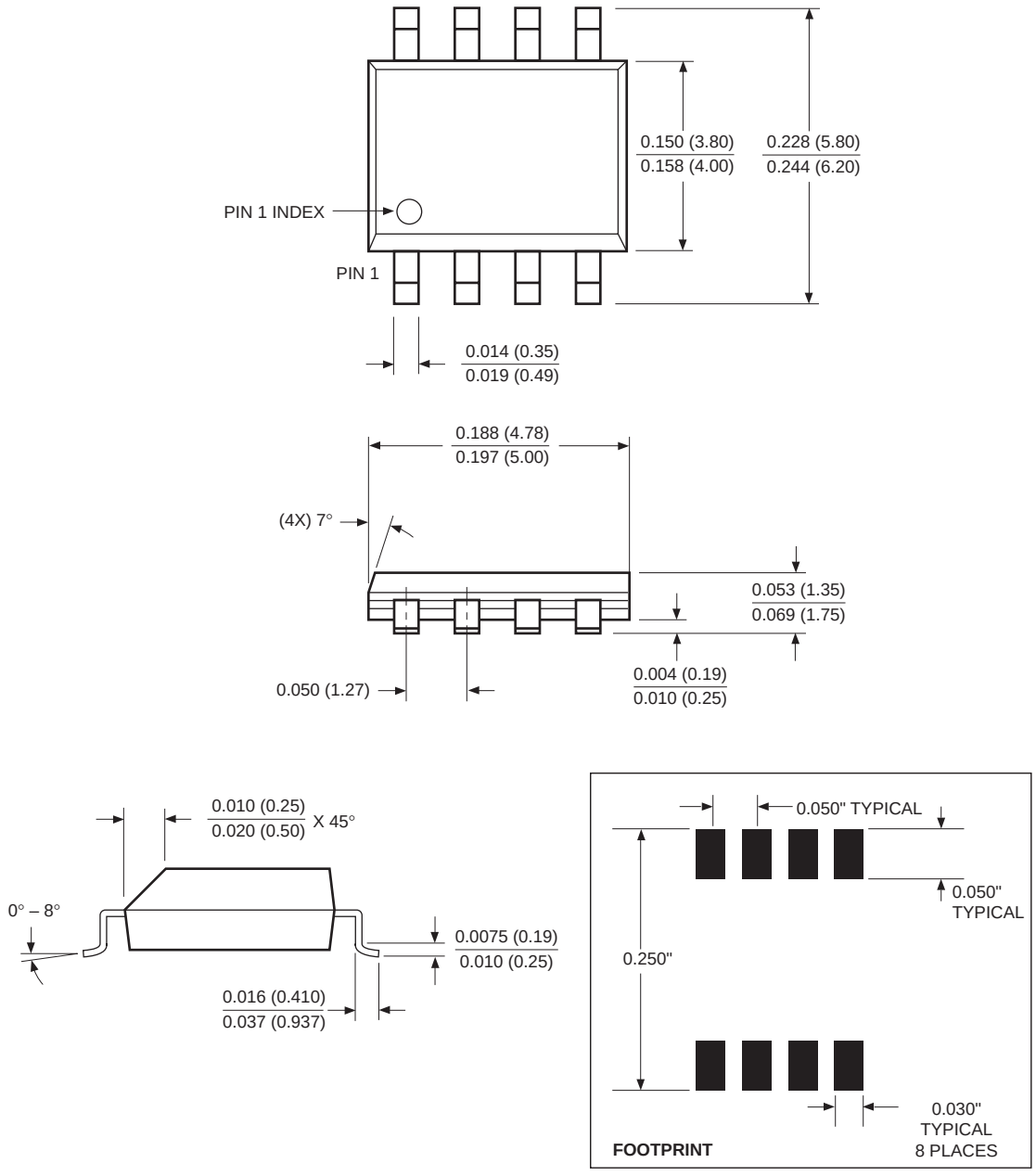
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

PACKAGING INFORMATION

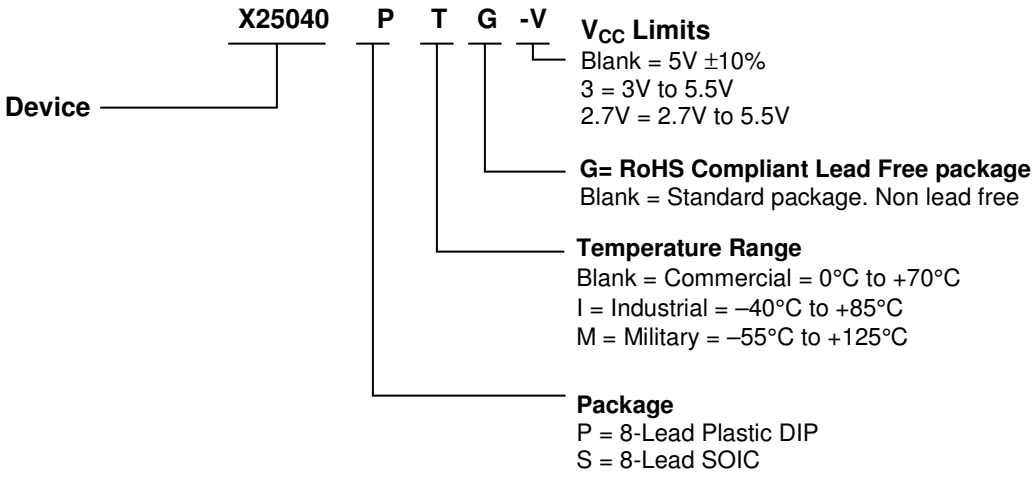
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



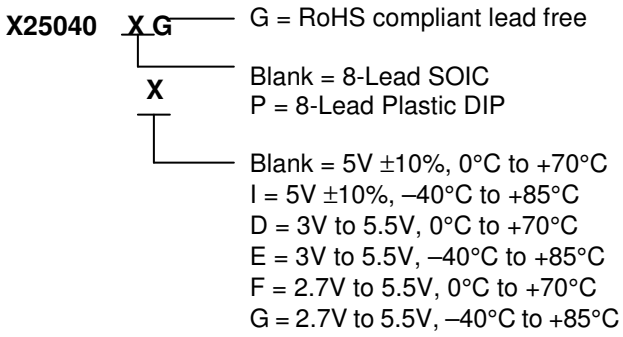
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

ORDERING INFORMATION



Part Mark Convention



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U.S. PATENTS

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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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- Индивидуальный подход
- Гибкое ценообразование
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