AN-8027

FAN480X PFC+PWM Combination Controller Application

FAN4800A / FAN4800C / FAN4801 / FAN4802 / FAN4802L

Introduction

This application note describes step-by-step design considerations for a power supply using the FAN480X controller. The FAN480X combines a PFC controller and a PWM controller. The PFC controller employs average current mode control for Continuous Conduction Mode (CCM) boost converter in the front end. The PWM controller can be used in either current mode or voltage mode for the downstream converter. In voltage mode, feed-forward from the PFC output bus can be used to improve the line transient response of PWM stage. In either mode, the PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This proprietary leading/trailing-edge modulation technique can significantly reduce the ripple current of the PFC output capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). In addition to power factor correction, a number of protection features have been built in to the FAN480X. These include programmable soft-start, PFC over-voltage protection, pulse-by-pulse current limiting, brownout protection, and under-voltage lockout.

FAN4801/2/2L feature programmable two-level PFC output to improve efficiency at light-load and low-line conditions.

FAN480X is pin-to-pin compatible with FAN4800 and ML4800, only requiring adjustment of some peripheral components. The FAN480X series comparison is summarized in the Appendix A.

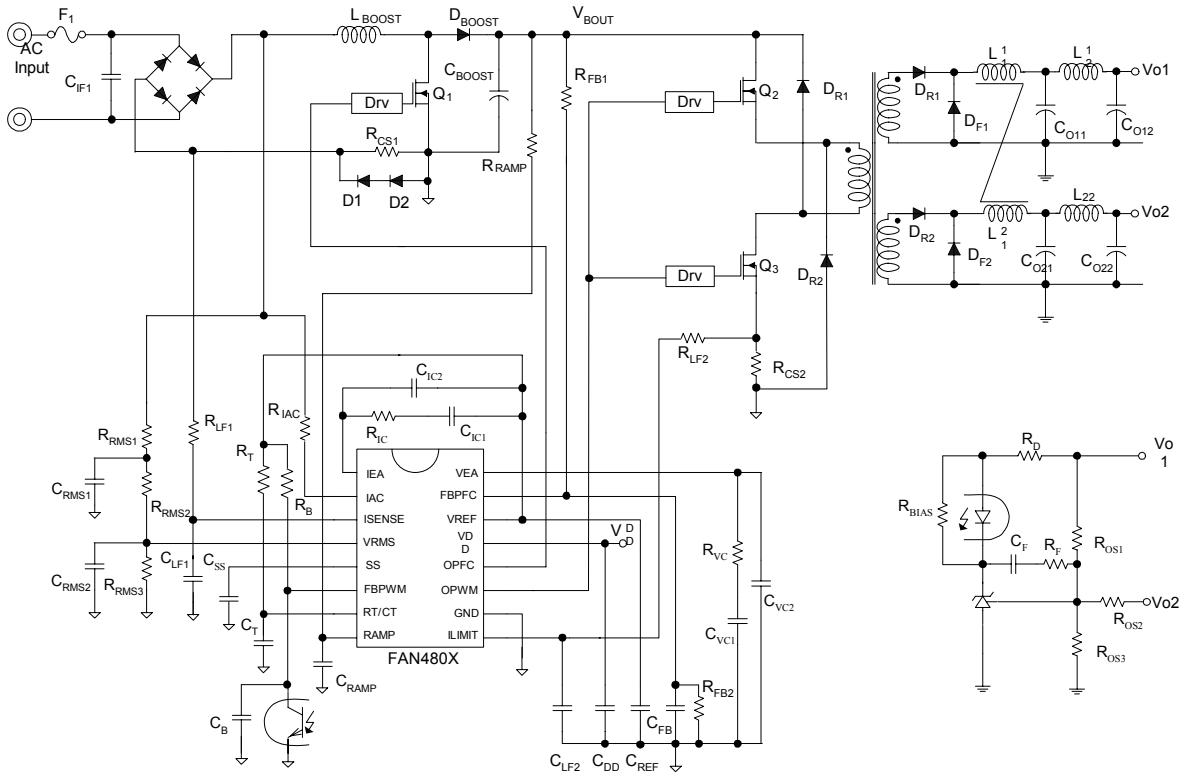


Figure 1. Typical Application Circuit of FAN480X

Functional Description

Gain Modulator

The gain modulator is the key block for PFC stage because it provides the reference to the current control error amplifier for the input current shaping, as shown in Figure 2. The output current of gain modulator is a function of V_{EA}, I_{AC} , and V_{RMS}. The gain of the gain modulator is given in the datasheet as a ratio between I_{MO} and I_{AC} with a given V_{RMS} when V_{EA} is saturated to HIGH. The gain is inversely proportional to V_{RMS}^2, as shown in Figure 3, to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage such that the input power of PFC converter is not changed with line voltage.

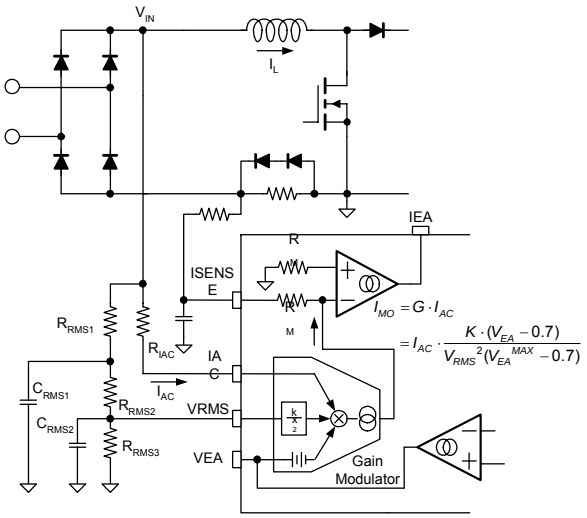


Figure 2. Gain Modulator Block

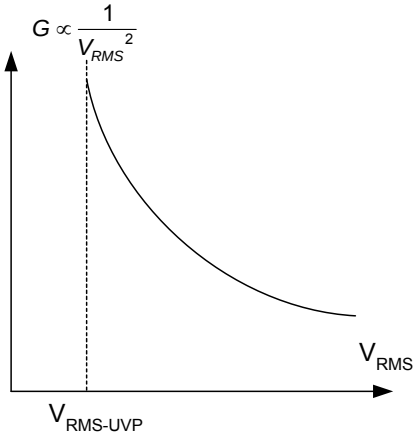


Figure 3. Modulation Gain Characteristics

To sense the RMS value of the line voltage, an averaging circuit with two poles is typically employed, as shown in Figure 2. The voltage of VRMS pin in normal PFC operation is given as:

$$V_{RMS} = V_{LINE} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \cdot \frac{2}{\pi} \quad (1)$$

where V_{LINE} is RMS value of line voltage.

However, once PFC stops switching operation, the junction capacitance of bridge diode is not discharged and V_{IN} of Figure 2 is clamped at the peak of the line voltage. Then, the voltage of VRMS pin is given by:

$$V_{RMS}^{NS} = V_{LINE} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \quad (2)$$

Therefore, the voltage divider for VRMS should be designed considering the brownout protection trip point and minimum operation line voltage.

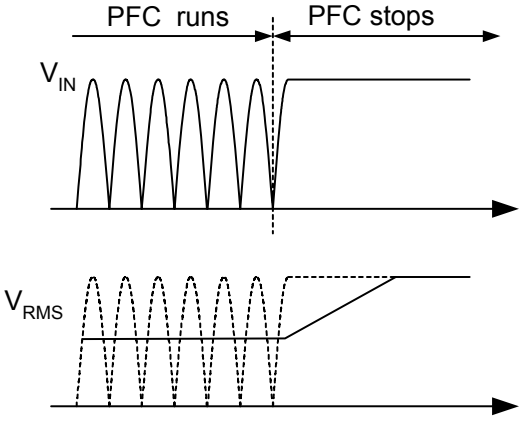


Figure 4. V_{RMS} According to the PFC Operation

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator as:

$$\frac{\sqrt{2}V_{LINE.BO}}{R_{IAC}} \cdot G^{MAX} < 159\mu A \quad (3)$$

where $V_{LINE.BO}$ is the line voltage that trips brownout protection, G^{MAX} is the maximum modulator gain when V_{RMS} is 1.08V (which can be found in the datasheet), and 159μA is the maximum output current of the gain modulator.

Current and Voltage Control of Boost Stage

As shown in Figure 5, the FAN480X employs two control loops for power factor correction: a current control loop and a voltage control loop. The current control loop shapes inductor current, as shown in Figure 6, based on the reference signal obtained at the IAC pin as:

$$I_L \cdot R_{CS1} = I_{MO} \cdot R_M = I_{AC} \cdot G \cdot R_M \quad (4)$$

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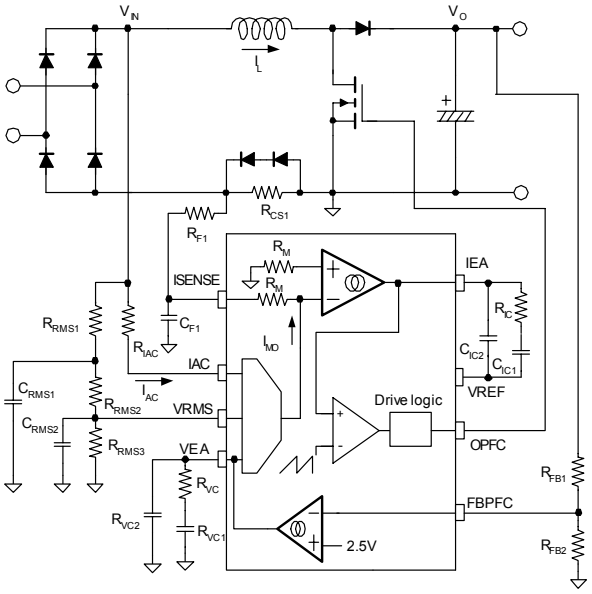


Figure 5. Gain Modulation Block

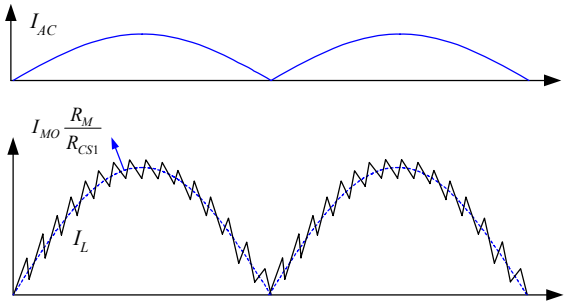


Figure 6. Inductor Current Shaping

The voltage control loop regulates PFC output voltage using internal error amplifier such that the FBPFC voltage is same as internal reference of 2.5V.

Brownout Protection

FAN480X has a built-in internal brownout protection comparator monitoring the voltage of the VRMS pin. Once the VRMS pin voltage is lower than 1.05V (0.9V for FAN4802L), the PFC stage is shutdown to protect the system from over current. The FAN480X starts up the boost stage once the V_{RMS} voltage increases above 1.9V (1.65V for FAN4802L).

Two-Level PFC Output

To improve system efficiency at low AC line voltage and light load condition, FAN480X provides two-level PFC output voltage. As shown in Figure 7, FAN480X monitors V_{EA} and V_{RMS} voltages to adjust the PFC output voltage. When V_{EA} and V_{RMS} are lower than the thresholds, an internal current source of 20μA is enabled that flows through R_{FB2}, increasing the voltage of the FBPFC pin. This causes the PFC output voltage to reduce when 20μA is enabled, calculated as:

$$V_{OPFC2} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times (2.5 - 20\mu A \times R_{FB2}) \quad (5)$$

It is typical to set the second boost output voltage as 340V~300V.

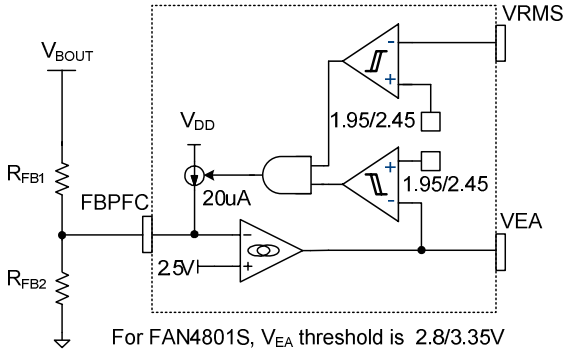


Figure 7. Block of Two-Level PFC Output

Oscillator

The internal oscillator frequency of FAN480X is determined by the timing resistor and capacitor on RT/CT pin. The frequency of the internal oscillator is given by:

$$f_{OSC} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360 C_T} \quad (6)$$

Because the PWM stage of FAN480X generally uses a forward converter, it is required to limit the maximum duty cycle at 50%. To have a small tolerance of the maximum duty cycle, a frequency divider with toggle flip-flops is used, as illustrated in Figure 8. The operation frequency of PFC and PWM stage is one quarter (1/4) of the oscillator frequency. (For FAN4800C and FAN4802/2L, the operation frequencies for PFC and PWM stages are one quarter (1/4) and one half (1/2) of the oscillator frequency, respectively).

The dead time for the PFC gate drive signal is determined by the equation:

$$t_{DEAD} = 360 C_T \quad (7)$$

The dead time should be smaller than 2% of switching period to minimize line current distortion around line zero crossing.

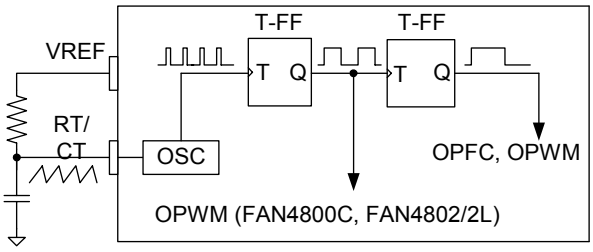


Figure 8. Oscillator Configuration

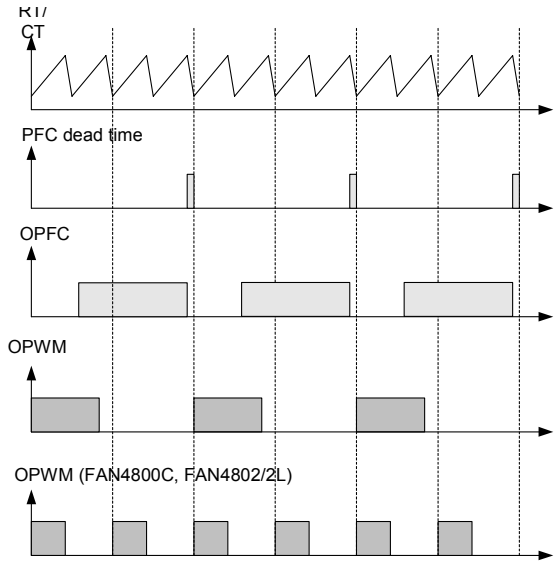


Figure 9. FAN480X Timing Diagram

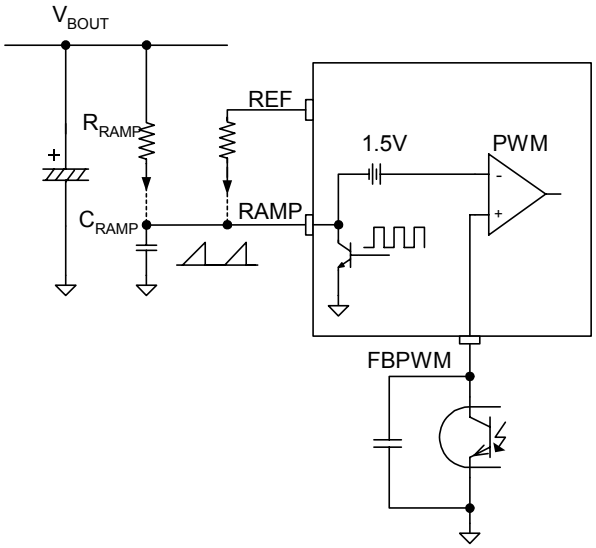


Figure 10. PWM Ramp Generation Circuit

PWM Stage

The PWM stage is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage and is thereby representative of the current flowing in the converter's output stage. I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP in such applications.

For voltage-mode operation, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which FBPWM voltage is compared. Under these conditions, the use of voltage feed-forward from the PFC bus can be used for better line transient response.

No voltage error amplifier is included in the PWM stage, as this function is generally performed by a programmable shunt regulator, such as KA431, in the secondary-side. To facilitate the design of opto-coupler feedback circuitry, an offset voltage is built into the inverting input of PWM comparator that allows FBPWM to command a zero percent duty cycle when its pin voltage is below 1.5V.

PWM Current Limit

The ILIMIT pin is a direct input to the cycle-by-cycle current limiter for the PWM section. If the input voltage at this pin exceeds 1V, the output of the PWM is disabled until the start of the next PWM clock cycle.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the output of the PFC stage and inhibits the PWM stage if this voltage is less than 2.4V (96% of its nominal value). Once this voltage goes above 2.4V, the PWM stage begins to soft-start.

PWM Soft-Start (SS)

PWM startup is controlled by the soft-start capacitor. A 10μA current source supplies the charging current for the soft-start capacitor. Startup of the PWM is prohibited until the soft-start capacitor voltage reaches 1.5V.

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Design Considerations

In this section, a design procedure is presented using the schematic in Figure 11 as reference. A 300W PC power supply application with universal input range is selected as a design example. The design specifications are summarized in 0. The two-switch forward converter is used for DC/DC converter stage.

Design Specifications

Rated Voltage of Output 1	V_{OUT1} = 5V		PWM Stage Efficiency	η_{PWM} = 0.86
Rated Current of Output 1	I_{OUT1} = 9A		Hold-up Time	t_{HLD} = 20ms
Rated Voltage of Output 2	V_{out2} = 12V		Minimum PFC Output Voltage	310V
Rated Current of Output 2	I_{OUT2} = 16.5A		Nominal PFC output voltage	V_{O_PFC} = 387V
Rated Voltage of Output 3	V_{OUT3} = -12V		PFC Output Voltage Ripple	$12V_{PP}$
Rated Current of Output 3	I_{OUT3} = 0.8A		PFC Inductor Ripple Current	dI = 40%
Rated Voltage of Output 4	V_{OUT4} = 3.3V		AC Input Voltage Frequency	f_{line} = 50 ~ 60Hz
Rated Current of Output 4	I_{OUT4} = 13.5A		Switching Frequency	f_S = 65KHz
Rated Output Power	P_O = 300W		Total Harmonic Distortion	α = 4%
Line Voltage Range	85~264V_{AC}		Magnetic Flux Density	ΔB = 0.27T
Line Frequency	50Hz		Current Density	D_{cma} = 400C-m/A
Brownout Protection Line Voltage	$72V_{AC}$		PWM Maximum Duty Cycle	D_{max} = 0.35
Overall Stage Efficiency	η = 0.82		5V Output Current Ripple	I_{Lo1} = 44%
			12V Output Current Ripple	I_{Lo2} = 10%

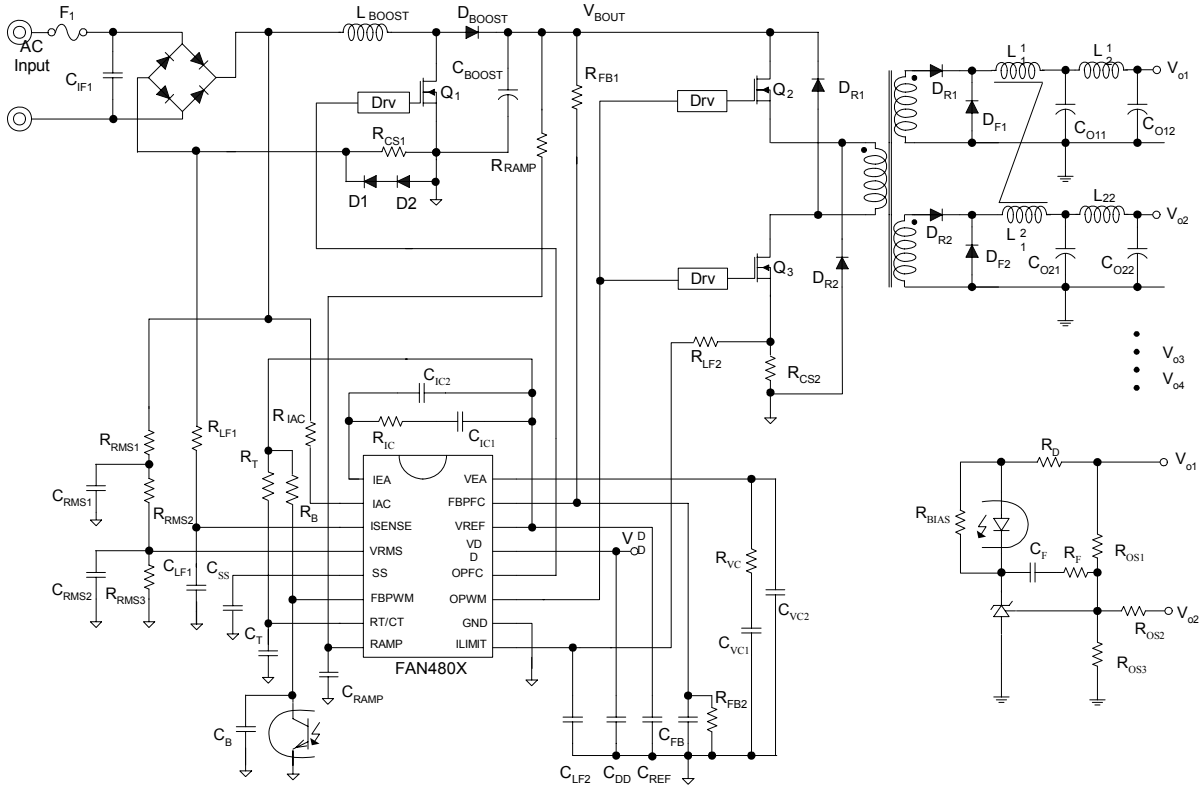


Figure 11. Reference Circuit for Design Example

[STEP-1] Define System Specifications

Since the overall system is comprised of two stages (PFC and DC/DC), as shown in Figure 12, the input power and output power of the boost stage are given as:

$$P_{IN} = \frac{P_{OUT}}{\eta} \tag{8}$$

$$P_{BOUT} = \frac{P_{OUT}}{\eta_{PWM}} \tag{9}$$

where η is the overall efficiency and η_{PWM} is the forward converter efficiency.

The nominal output current of boost PFC stage is given as:

$$I_{BOUT} = \frac{P_{OUT}}{\eta_{PWM} V_{BOUT}} \tag{10}$$

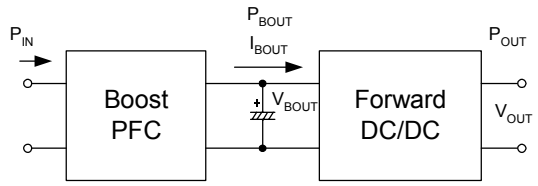


Figure 12. Two Stage Configuration

(Design Example)

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{300}{0.82} = 366W$$

$$P_{BOUT} = \frac{P_{OUT}}{\eta_{PWM}} = \frac{300}{0.86} = 349W$$

$$I_{BOUT} = \frac{P_{OUT}}{\eta_{PWM} V_{BOUT}} = \frac{300}{0.86 \cdot 387} = 0.9A$$

[STEP-2] Frequency Setting

The switching frequency is determined by the timing resistor and capacitor (R_T and C_T) as:

$$f_{SW} \cong \frac{1}{4} \cdot \frac{1}{0.56 \cdot R_T \cdot C_T} \tag{11}$$

It is typical to use a 470pF~1nF capacitor for 50~75kHz switching frequency operation since the timing capacitor value determines the maximum duty cycle of PFC gate drive signal as:

$$D_{MAX.PFC} = 1 - \frac{T_{OFF.}^{MIN}}{T_{SW}} = 1 - 360 \cdot C_T \cdot f_{SW} \tag{12}$$

(Design Example) Since the switching frequency is 65kHz, C_T is selected as 1nF. Then the maximum duty cycle of PFC gate drive signal is obtained as:

$$D_{MAX.PFC} = 1 - 360 \cdot C_T \cdot f_{SW} = 0.98$$

The timing resistor is determined as:

$$R_T = \frac{1}{4} \cdot \frac{1}{0.56 f_{SW} C_T} = 6.9k\Omega$$

[STEP-3] Line Sensing Circuit Design

FAN480X senses the RMS value and instantaneous value of line voltage using the VRMS and IAC pins, respectively, as shown in Figure 13. The RMS value of the line voltage is obtained by an averaging circuit using low pass filter with two poles. Meanwhile, the instantaneous line voltage information is obtained by sensing the current flowing into IAC pin through R_{IAC}.

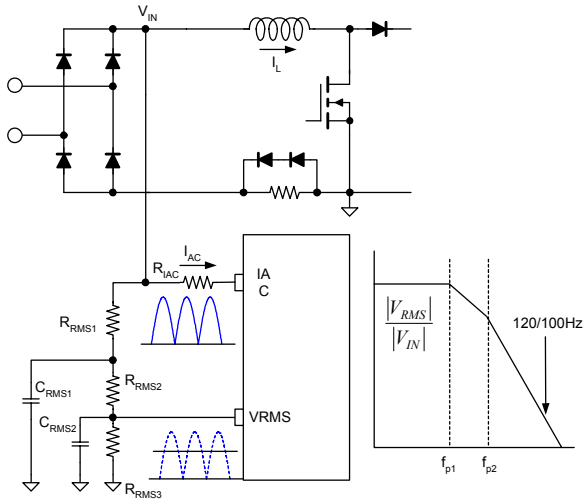


Figure 13. Line Sensing Circuits

RMS sensing circuit should be designed considering the nominal operation range of line voltage and brownout protection trip point as:

$$V_{RMS-UVL} = V_{LINE.BO} \frac{\sqrt{2} R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \cdot \frac{2}{\pi} \tag{13}$$

$$V_{RMS-UVH} < V_{LINE.MIN} \frac{\sqrt{2} R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \tag{14}$$

where $V_{RMS-UVL}$ and $V_{RMS-UVH}$ are the brown OUT/IN thresholds of V_{RMS}.

It is typical to set R_{RMS2} as 10% of R_{RMS1}. The poles of the low pass filter are given as:

$$f_{P1} \cong \frac{1}{2\pi \cdot C_{RMS1} \cdot R_{RMS2}} \tag{15}$$

$$f_{P2} \cong \frac{1}{2\pi \cdot C_{RMS2} \cdot R_{RMS3}} \tag{16}$$

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To properly attenuate the twice line frequency ripple in V_{RMS}, it is typical to set the poles around 10~20Hz.

The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator as:

$$\frac{\sqrt{2}V_{LINE.BO}}{R_{IAC}} \cdot G^{MAX} < 159\mu A \quad (17)$$

where $V_{LINE.BO}$ is the brownout protection line voltage, G^{MAX} is the maximum modulator gain when V_{RMS} is 1.08V (which can be found in the datasheet), and 159μA is the maximum output current of the gain modulator.

(Design Example) The brownout protection threshold is 1.05V ($V_{RMS-UVL}$) and 1.9V ($V_{RMS-UVH}$), respectively. Then, the scaling down factor of the voltage divider is:

$$\frac{R_{RMS3}}{R_{RMS1}+R_{RMS2}+R_{RMS3}} = \frac{V_{RMS-UVL}}{V_{LINE.BO}} \cdot \frac{\pi}{2\sqrt{2}} = \frac{1.05}{72} \cdot \frac{\pi}{2\sqrt{2}} = 0.0162$$

Then the startup of the PFC stage at the minimum line voltage is checked as:

$$\frac{V_{LINE.MIN} \cdot \sqrt{2}R_{RMS3}}{R_{RMS1}+R_{RMS2}+R_{RMS3}} = 85 \cdot \sqrt{2} \cdot 0.0162 = 1.95 > 1.9V$$

The resistors of the voltage divider network are selected as R_{RMS1}=2MΩ, R_{RMS1}=200kΩ, and R_{RMS1}=36kΩ.

To place the poles of the low pass filter at 15Hz and 22Hz, the capacitors are obtained as:

$$C_{RMS1} = \frac{1}{2\pi \cdot f_{P1} \cdot R_{RMS2}} = \frac{1}{2\pi \cdot 15 \cdot 200 \times 10^3} = 53nF$$

$$C_{RMS2} \cong \frac{1}{2\pi \cdot f_{P2} \cdot R_{RMS3}} = \frac{1}{2\pi \cdot 22 \cdot 36 \times 10^3} = 200nF$$

The condition for Resistor R_{IAC} is:

$$R_{IAC} > \frac{\sqrt{2}V_{LINE.BO}}{159 \times 10^{-6}} \cdot G^{MAX} = \frac{\sqrt{2} \cdot 72 \cdot 9}{159 \times 10^{-6}} = 5.8M\Omega$$

Therefore, 6MΩ resistor is selected for R_{IAC}.

[STEP-4] PFC Inductor Design

The duty cycle of boost switch at the peak of line voltage is given as:

$$D_{LP} = \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \quad (18)$$

Then, the maximum current ripple of the boost inductor at the peak of line voltage for low line is given as:

$$\Delta I_L = \frac{\sqrt{2}V_{LINE.MIN}}{L_{BOOST}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} \quad (19)$$

The average of boost inductor current over one switching cycle at the peak of the line voltage for low line is given as:

$$I_{L.AVG} = \frac{\sqrt{2}P_{OUT}}{V_{LINE.MIN} \cdot \eta} \quad (20)$$

Therefore, with a given current ripple factor ($K_{RB}=\Delta I_L/I_{LAVG}$), the boost inductor value is obtained as:

$$L_{BOOST} = \frac{V_{LINE.MIN}^2 \cdot \eta}{K_{RB} \cdot P_{OUT}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} \quad (21)$$

The maximum current of boost inductor is given as:

$$I_L^{PK} = I_{L.AVG} \cdot (1 + \frac{K_{RB}}{2}) = \frac{\sqrt{2}P_{OUT}}{V_{LINE.MIN} \cdot \eta} \cdot (1 + \frac{K_{RB}}{2}) \quad (22)$$

(Design Example) With the ripple current specification (40%), the boost inductor is obtained as:

$$L_{BOOST} = \frac{V_{LINE.MIN}^2 \cdot \eta}{K_{RB} \cdot P_{OUT}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} = \frac{85^2 \cdot 0.82}{0.4 \cdot 300} \cdot \frac{387 - \sqrt{2} \cdot 85}{387} \cdot \frac{10^{-3}}{65} = 524\mu H$$

The average of boost inductor current over one switching cycle at the peak of the line voltage for low line is obtained as:

$$I_{L.AVG} = \frac{\sqrt{2}P_{OUT}}{V_{LINE.MIN} \cdot \eta} = \frac{\sqrt{2} \cdot 300}{85 \cdot 0.82} = 6.09A$$

The maximum current of the boost inductor is given as:

$$I_L^{PK} = \frac{\sqrt{2}P_{OUT}}{V_{LINE.MIN} \cdot \eta} \cdot (1 + \frac{K_{RB}}{2}) = \frac{\sqrt{2} \cdot 300}{85 \cdot 0.82} \cdot (1 + \frac{0.4}{2}) = 7.31A$$

[STEP-5] PFC Output Capacitor Selection

The output voltage ripple should be considered when selecting the PFC output capacitor. Figure 14 shows the twice line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{BOUT} > \frac{I_{BOUT}}{2\pi \cdot f_{LINE} \cdot V_{BOUT,RIPPLE}} \quad (23)$$

where I_{BOUT} is nominal output current of boost PFC stage and $V_{BOUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

The hold-up time also should be considered when determining the output capacitor as:

$$C_{BOUT} > \frac{P_{BOUT} \cdot t_{HOLD}}{V_{BOUT}^2 - V_{BOUT,MIN}^2} \quad (24)$$

where P_{BOUT} is nominal output power of boost PFC stage, t_{HOLD} is the required holdup time, and $V_{BOUT,MIN}$ is the allowable minimum PFC output voltage during hold-up time.

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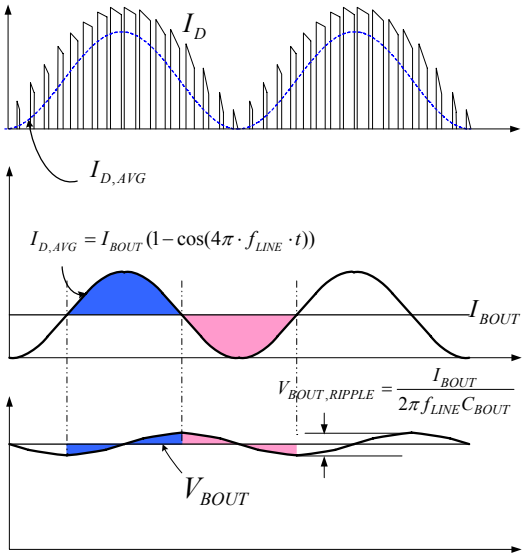


Figure 14. PFC Output Voltage Ripple

(Design Example) With the ripple specification of $12V_{PP}$, the capacitor should be:

$$C_{BOUT} > \frac{I_{BOUT}}{2\pi \cdot f_{LINE} \cdot V_{BOUT,RIPPLE}} = \frac{0.9}{2\pi \cdot 50 \cdot 12} = 239\mu F$$

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 310V, the capacitor should be:

$$C_{BOUT} > \frac{P_{BOUT} \cdot t_{HOLD}}{V_{OUT}^2 - V_{OUT,MIN}^2} = \frac{2 \cdot 349 \cdot 20 \times 10^{-3}}{387^2 - 310^2} = 260\mu F$$

Thus, 270µF capacitor is selected for the PFC output capacitor.

[STEP-6] PFC Output Sensing Circuit

To improve system efficiency at low line and light load condition, FAN480X provides two-level PFC output voltage. As shown in Figure 15, FAN480X monitors V_{EA} and V_{RMS} voltages to adjust the PFC output voltage.

The PFC output voltage when 20µA is enabled is given as:

$$V_{BOUT2} = V_{BOUT} \times (1 - \frac{20\mu A \times R_{FB2}}{2.5}) \quad (25)$$

It is typical second boost output voltage as 340V~300V.

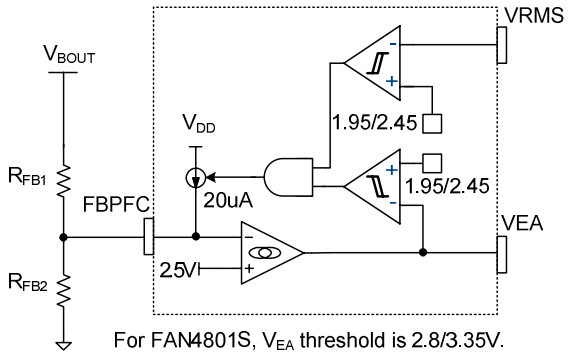


Figure 15. Two-Level PFC Output Block

The voltage divider network for the PFC output voltage sensing should be designed such that FBPFC voltage is 2.5V at nominal PFC output voltage:

$$V_{BOUT} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = 2.5V \quad (26)$$

(Design Example) Assuming the second level of PFC output voltage is 347V:

$$R_{FB2} = (1 - \frac{V_{BOUT2}}{V_{BOUT}}) \cdot \frac{2.5}{20 \times 10^{-6}}$$

$$= (1 - \frac{347}{387}) \cdot \frac{2.5}{20 \times 10^{-6}} = 12.9k\Omega$$

13kΩ is selected for R_{FB2}.

$$R_{FB1} = (\frac{V_{BOUT}}{2.5} - 1) \cdot R_{FB2}$$

$$= (\frac{387}{2.5} - 1) \cdot 13 \times 10^3 = 1999k\Omega$$

2MΩ is selected for R_{FB1}.

[STEP-7] PFC Current-Sensing Circuit Design

Figure 16 shows the PFC compensation circuits. The first step in compensation network design is to select the current-sensing resistor of PFC converter considering the control window of voltage loop. Since line feed-forward is used in FAN480X, the output power is proportional to the voltage control error amplifier voltage as:

$$P_{BOUT}(V_{EA}) = P_{BOUT}^{MAX} \cdot \frac{V_{EA} - 0.6}{V_{EA}^{SAT} - 0.6} \quad (27)$$

where V_{EA}^{SAT} is 5.6V and the maximum power limit of PFC is:

$$P_{BOUT}^{MAX} = \frac{V_{LINE.BO}^2 \cdot G^{MAX} \cdot R_M}{R_{IAC} R_{CS1}} \quad (28)$$

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It is typical to set the maximum power limit of PFC stage around 1.2~1.5 of its nominal power such that the V_{EA} is around 4~4.5V at nominal output power. By adjusting the current-sensing resistor for PFC stage, the maximum power limit of PFC stage can be programmed.

To filter out the current ripple of switching frequency, an RC filter is typically used for ISENSE pin. R_{LF1} should not be larger than 100Ω and the cut-off frequency of filter should be 1/2~1/6 of the switching frequency.

Diodes D_1 and D_2 are required to prevent over-voltage on ISENSE pin due to the inrush current that might damage the IC. A fast recovery diode or ultra fast recovery diode is recommended.

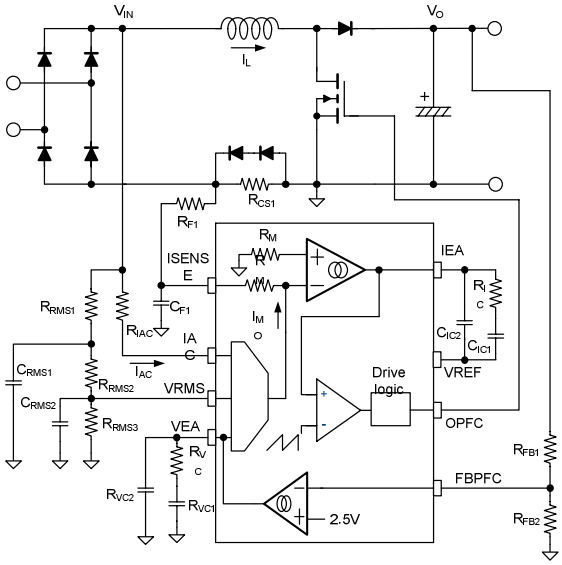


Figure 16. Gain Modulation Block

(Design Example) Setting the maximum power limit of PFC stage as 450W, the current sensing resistor is obtained as:

$$R_{CS1} = \frac{V_{LINE.BO}^{\ 2} \cdot G^{MAX} \cdot R_M}{R_{IAC} P_{BOUT}^{\ MAX}} = \frac{72^2 \cdot 9 \cdot 5.7 \times 10^3}{6 \times 10^6 \cdot 450} = 0.098\Omega$$

Thus, 0.1Ω resistor is selected.

[STEP-8] PFC Current Loop Design

The transfer function from duty cycle to the inductor current of boost power stage is given as:

$$\frac{\hat{i}_L}{\hat{d}} = \frac{V_{BOUT}}{sL_{BOOST}} \tag{29}$$

The transfer function from the output of the current control error amplifier to the inductor current-sensing voltage is obtained as:

$$\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}} = \frac{R_{CS1} \cdot V_{BOUT}}{V_{RAMP} \cdot sL_{BOOST}} \tag{30}$$

where V_{RAMP} is the peak to peak voltage of ramp signal for current control PWM comparator, which is 2.55V.

The transfer function of the compensation circuit is given as:

$$\frac{\hat{v}_{IEA}}{\hat{v}_{CS1}} = \frac{2\pi f_{II}}{s} \cdot \frac{1+\frac{s}{2\pi f_{IC}}}{1+\frac{s}{2\pi f_{IP}}} \tag{31}$$

where:

$$f_{II} = \frac{G_{MI}}{2\pi \cdot C_{IC1}},\ f_{IZ} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC1}}\ and\ f_{IP} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC2}} \tag{32}$$

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_{IC}) around 1/10~1/6 of the switching frequency. Then calculate the gain of the transfer function of Equation (30) at crossover frequency as:

$$\left|\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}} = \frac{R_{CS1} \cdot V_{BOUT}}{V_{RAMP} \cdot 2\pi f_{IC} \cdot L_{BOOST}} \tag{33}$$

(b) Calculate R_{IC} that makes the closed loop gain unity at crossover frequency:

$$R_{IC} = \frac{1}{G_{MI} \cdot \left|\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}}} \tag{34}$$

(c) Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency is 0dB, as shown in Figure 17; it is necessary to place the zero of the compensation network (f_{IZ}) around 1/3 of the crossover frequency so that more than 45° phase margin is obtained. Then the capacitor C_{IC1} is determined as:

$$C_{IC1} = \frac{1}{R_{IC} \cdot 2\pi f_C / 3} \tag{35}$$

(d) Place compensator high-frequency pole (f_{CP}) at least a decade higher than f_{IC} to ensure that it does not interfere with the phase margin of the current loop at its crossover frequency.

$$C_{IC2} = \frac{1}{2\pi \cdot f_{IP} \cdot R_{IC}} \tag{36}$$

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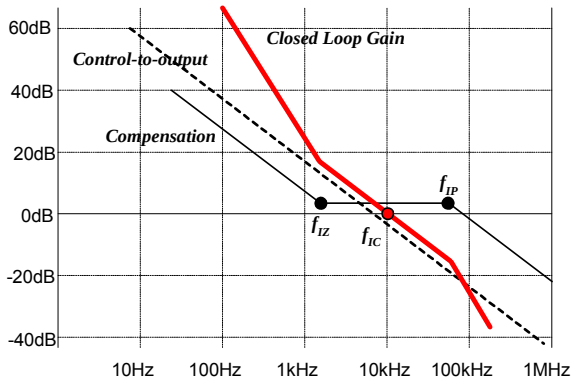


Figure 17. Current Loop Compensation

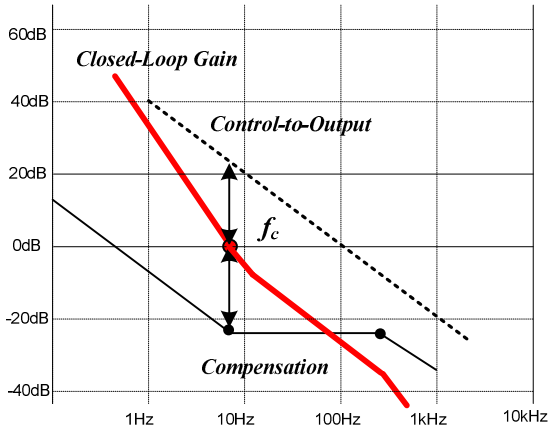


Figure 18. Voltage Loop Compensation

(Design Example) Setting the crossover frequency as 7kHz:

$$\left|\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}} = \frac{R_{CS1}\cdot V_{BOUT}}{V_{RAMP}\cdot 2\pi f_{IC}\cdot L_{BOOST}} = \frac{0.1\cdot 387}{2.55\cdot 2\pi\cdot 7\times 10^{3}\cdot 524\times 10^{-6}} = 0.66$$

$$R_{IC} = \frac{1}{G_{MI}\cdot\left|\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}}} = \frac{1}{88\times 10^{-6}\cdot 0.66} = 17k\Omega$$

$$C_{IC1} = \frac{1}{R_{IC}\cdot 2\pi f_C/3} = \frac{1}{17\times 10^{3}\cdot 2\pi\cdot 7\times 10^{3}/3} = 4nF$$

Setting the pole of the compensator at 70kHz,

$$C_{IC2} = \frac{1}{2\pi\cdot f_{IP}\cdot R_{IC}} = \frac{1}{2\pi\cdot 70\times 10^{3}\cdot 17\times 10^{3}} = 0.13nF$$

[STEP-9] PFC Voltage Loop Design

Since FAN480X employs line feed-forward, the power stage transfer function becomes independent of the line voltage. Then, the low-frequency, small-signal, control-to-output transfer function is obtained as:

$$\frac{\hat{v}_{BOUT}}{\hat{v}_{EA}} \cong \frac{I_{BOUT}\cdot K_{MAX}}{5}\cdot\frac{1}{sC_{BOUT}} \quad (37)$$

where:

$$\frac{\hat{v}_{BOUT}}{\hat{v}_{EA}} \cong \frac{I_{BOUT}\cdot K_{MAX}}{5}\cdot\frac{1}{sC_{BOUT}} \quad (38)$$

Proportional and integration (PI) control with high-frequency pole is typically used for compensation. The compensation zero (f_{VZ}) introduces phase boost, while the high-frequency compensation pole (f_{VP}) attenuates the switching ripple, as shown in Figure 18.

The transfer function of the compensation network is obtained as:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{OUT}} = \frac{2\pi f_{VI}}{s}\cdot\frac{1+\frac{s}{2\pi f_{VZ}}}{1+\frac{s}{2\pi f_{VP}}} \quad (39)$$

where:

$$f_{VI} = \frac{2.5}{V_{BOUT}}\cdot\frac{G_{MV}}{2\pi\cdot C_{VC1}},\ f_{VZ} = \frac{1}{2\pi\cdot R_{VC}\cdot C_{VC1}}\ \ and\ \ f_{VP} = \frac{1}{2\pi\cdot R_{VC}\cdot C_{VC2}} \quad (40)$$

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_{VC}) around 1/10~1/5 of the line frequency. Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency, as shown in Figure 18 as 0dB; it is necessary to place the zero of the compensation network (f_{VZ}) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitor C_{VC1} is determined as:

$$C_{VC1} = \frac{G_{MV}\cdot I_{BOUT}\cdot K_{MAX}}{5\cdot C_{BOUT}\cdot(2\pi f_{VC})^2}\cdot\frac{2.5}{V_{BOUT}} \quad (41)$$

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

$$R_{VC} = \frac{1}{2\pi\cdot f_{VC}\cdot C_{VC1}} \quad (42)$$

(b) Place compensator high-frequency pole (f_{VP}) at least a decade higher than f_C to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor C_{VC2} is determined as:

$$C_{VC2} = \frac{1}{2\pi\cdot f_{VP}\cdot R_{VC}} \quad (43)$$

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(Design Example) Setting the crossover frequency as 22Hz:

$$C_{VC1} = \frac{G_{MV} \cdot I_{BOUT} \cdot K_{MAX}}{5 \cdot C_{BOUT} \cdot (2\pi f_{VC})^2} \cdot \frac{2.5}{V_{BOUT}}$$
$$= \frac{70\times10^{-6} \cdot 0.9 \cdot 1.27}{5 \cdot 270\times10^{-6} \cdot (2\pi \cdot 22)^2} \cdot \frac{2.5}{387} = 20nF$$

$$R_{VC} = \frac{1}{2\pi \cdot f_{VC} \cdot C_{VC1}} = \frac{1}{2\pi \cdot 22 \cdot 20\times10^{-9}} = 362k\Omega$$

Setting the pole of the compensator at 120Hz:

$$C_{VC2} = \frac{1}{2\pi \cdot f_{VP} \cdot R_{VC}} = \frac{1}{2\pi \cdot 120 \cdot 362\times10^{3}} = 3.7nF$$

[STEP-10] Transformer Design for PWM Stage

Figure 19 shows the typical secondary-side circuit of forward converter for multi-output of PC power application.

A common technique for winding multiple outputs with the same polarity sharing a common ground is to stack the secondary windings instead of winding each output winding separately. This approach improves the load regulation of the stacked outputs. The winding N_{S1} in Figure 19 must be sized to accommodate its output current, plus the current of the output (+12V) stacked on top of it. To get tight regulation of 3.3V output, magnetic amplifier (MAG-AMP) is used. The saturable core of MAG-AMP prevents the diode D_{REC} from fully conducting by introducing high impedance until it is saturated. This allows the effective duty cycle of V_{REC} to be controlled to be regulated the output voltage.

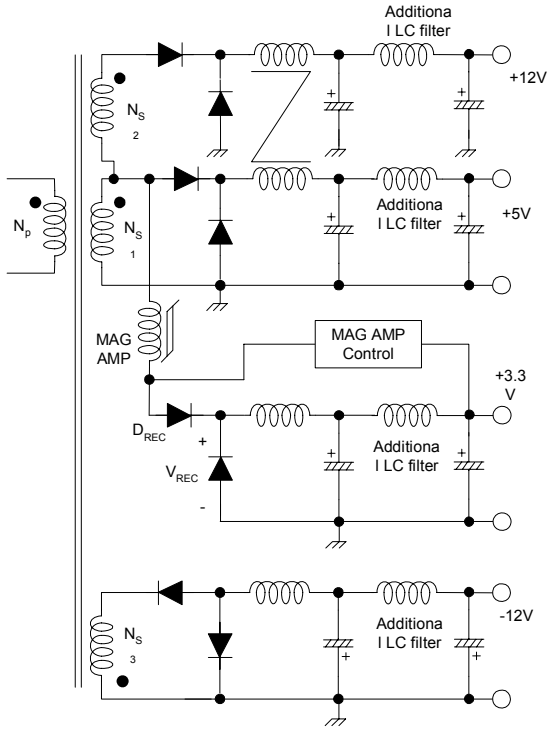


Figure 19. Typical Secondary-Side Circuit

Once the core for the transformer is determined, the minimum number of turns for the transformer primary-side to avoid saturation is given by:

$$N_P^{MIN} = \frac{V_{BOUT}^{MIN} D_{MAX}}{A_e f_{SW} \Delta B} \quad (44)$$

where A_e is the cross sectional area of the core in m^2, f_{SW} is the switching frequency, and ΔB is the maximum flux density swing in Tesla for normal operation. ΔB is typically 0.2-0.3 T for most power ferrite cores in the case of a forward converter.

The turn ratio between the primary-side and secondary-side winding for the first output is determined by:

$$n = \frac{N_P}{N_{S1}} = \frac{V_{BOUT}^{MIN} D_{MAX}}{(V_{O1} + V_{F1})} \quad (45)$$

where V_F is the diode forward-voltage drop.

Next, determine the proper integer for N_{S1} resulting in N_p larger than N_p^{min}. Once the number of turns of the first output is determined, the number of turns of other output (n-th output) can be determined by:

$$N_{S(n)} = \frac{V_{O(n)} + V_{F(n)}}{V_{O1} + V_{F1}} \cdot N_{S1} \quad (46)$$

The golden ratio between the secondary-side windings for the best regulation of 3.3V, 5V, and 12V is known as 2:3:7.

(Design Example) The minimum PFC output voltage is 310V and the maximum duty cycle of PWM controller is 50%. By adding 5% margin to the maximum duty cycle, D_{MAX}=0.45 is used for transformer design. Assuming ERL35 ($Ae=107mm^2$) core is used and ΔB=0.28, the minimum turns for the transformer primary side is obtained as:

$$N_P^{MIN} = \frac{V_{BOUT}^{MIN} D_{MAX}}{A_e f_{SW} \Delta B} = \frac{310 \cdot 0.45}{107\times10^{-6} \cdot 65\times10^{3} \cdot 0.28} = 72$$

The turns ratio for 5V output is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{BOUT}^{MIN} D_{MAX}}{(V_O + V_F)} = \frac{310 \cdot 0.45}{(5 + 0.45)} = 25.6$$

The number of turns for the primary-side winding is determined as:

$$N_p = n \cdot N_{S1} = 2 \times 25.6 = 51.2 < N_P^{MIN}$$

$$N_p = n \cdot N_{S1} = 3 \times 25.6 = 76.8 > N_P^{MIN} \quad \therefore N_{S1} = 3$$

Then, the turns ratio for 12V output is obtained as:

$$N_{S2} = \frac{V_{O2} + V_{F2}}{V_{O1} + V_{F1}} \cdot N_{S1} = \frac{12 + 0.7}{5 + 0.45} \cdot 3 = 6.99 \cong 7$$

Therefore, the number of turns for each winding is obtained as:

Np=78, N_{S1}=3, N_{S2}=7 (3+4 stack) and N_{S3}=7.

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[STEP-11] Coupled Inductor Design for the PWM Stage

When the forward converter has more than one output, as shown in Figure 20, coupled inductors are usually employed to improve the cross regulation and to reduce the ripple. They are implemented by winding their separate coils on a single, common core. The turns ratio should be the same as the transformer turns ratio of the two outputs as:

$$\frac{N_{S2}}{N_{S1}} = \frac{N_{L2}}{N_{L1}} \tag{47}$$

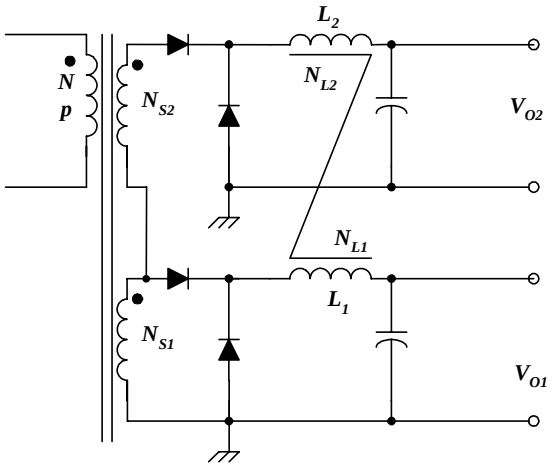


Figure 20. Coupled Inductor

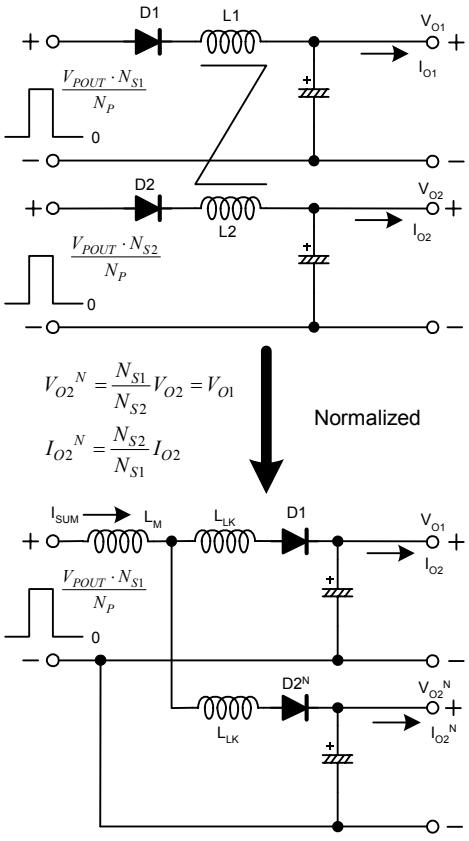


Figure 21. Normalized Coupled Inductor Circuit

One way to understand the operation of coupled inductor is to normalize the outputs to one output. Figure 21 shows how to normalize the second output (V_{O2}) to the first output (V_{O1}). The transformer and inductor turns are divided by N_{S2}/N_{S1}, the voltage and current are adjusted by N_{S2}/N_{S1}. It is assumed that the leakage inductances of the coupled inductor are much smaller than the magnetizing inductance and evenly distributed for each winding.

The inductor value of the first output can be obtained by:

$$L_1 = \frac{V_{O1}(V_{O1}+V_{F1})}{f_{SW}(P_{O1}+P_{O2})\dfrac{\Delta I_{SUM}}{I_{SUM}}} \cdot (1 - D_{MIN}) \tag{48}$$

where:

$$D_{MIN} = D_{MAX}\frac{V_{BOUT}^{MIN}}{V_{BOUT}}$$
$$I_{SUM} = \frac{P_{O1}+P_{O2}}{V_{O1}} \tag{49}$$

Then, the ripple current for each output is given as:

$$\frac{\Delta I_{O1}}{I_{O1}} = \frac{\Delta I_{SUM}}{2} \cdot \frac{1}{I_{O1}} \tag{50}$$

$$\frac{\Delta I_{O2}}{I_{O2}} = \frac{\Delta I_{SUM}}{2} \cdot \frac{N_{S1}}{N_{S2}} \cdot \frac{1}{I_{O2}} \tag{51}$$

(Design Example) The minimum duty cycle of PWM stage at nominal input (PFC output) voltage is:

$$D_{MIN} = D_{MAX}\frac{V_{BOUT}^{MIN}}{V_{BOUT}} = 0.45\frac{310}{389} = 0.36$$

The sum of two normalize output current is:

$$I_{SUM} = \frac{P_{O1}+P_{O2}}{V_{O1}} = \frac{243}{5} = 48.6A$$

Assuming 16% p-p ripple current in L_{SUM}, the inductor for the first output is obtained as:

$$L_1 = \frac{V_{O1}(V_{O1}+V_{F1})}{f_{SW}(P_{O1}+P_{O2})\dfrac{\Delta I_{SUM}}{I_{SUM}}} \cdot (1 - D_{MIN})$$
$$= \frac{5(5+0.45)}{65\times10^3(5\times9+12\times16.5)\cdot0.16}\cdot(1-0.36) = 6.9uH$$

Then, the ripple current for each output is given as:

$$\frac{\Delta I_{O1}}{I_{O1}} = \frac{\Delta I_{SUM}}{2}\cdot\frac{1}{I_{O1}} = \frac{48.6\times0.16}{2}\cdot\frac{1}{9} = 43\%$$

$$\frac{\Delta I_{O2}}{I_{O2}} = \frac{\Delta I_{SUM}}{2}\cdot\frac{N_{S1}}{N_{S2}}\cdot\frac{1}{I_{O2}} = \frac{48.6\times0.16}{2}\cdot\frac{3}{7}\cdot\frac{1}{16.5} = 10\%$$

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[STEP-12] PWM Ramp Circuit Design

For voltage-mode operation, the RAMP pin can be connected to a DC voltage through a resistor. When it is connected to the input of forward converter, ramp signal slope is automatically adjusted according to the input voltage providing line feed-forward operation. However, it can cause more power dissipation in the resistor. For better efficiency and lower standby power consumption, it is recommended to connect the RAMP pin to the VREF pin.

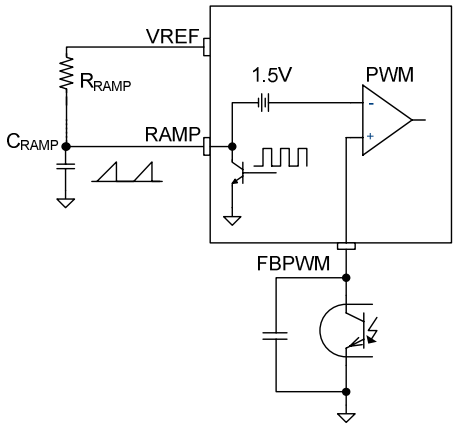


Figure 22. Ramp Generation Circuit for PWM

It is typical to use 470pF~1nF capacitor on the RAMP pin and to have the peak of the ramp signal around 2~3V.

The peak of the ram voltage is given as:

$$V_{RAMP}^{PK} = \frac{1}{C_{RAMP}} \cdot \frac{V_{REF}}{R_{RAMP}} \cdot \frac{1}{2f_{SW}} \quad (52)$$

(Design Example) Selecting C_{RAMP} and R_{RAMP} as 1nF and 22k, the PWM ramp voltage is obtained as:

$$V_{RAMP}^{PK} = \frac{1}{C_{RAMP}} \cdot \frac{V_{REF}}{R_{RAMP}} \cdot \frac{1}{2f_{SW}} = \frac{1}{1\times10^{-9}} \cdot \frac{7.5}{22\times10^{3}} \cdot \frac{1}{2\cdot65\times10^{3}} = 2.6V$$

[STEP-13] Feedback Compensation Design for PWM Stage

Figure 21 shows the typical cross regulation compensation circuit configuration for multi-output converters. The small signal characteristics of the compensation network is given as:

$$\hat{v}_{FBPWM} = -\frac{R_B}{1+s/\omega_{CP}} \cdot \left(\frac{1+s/\omega_{CZ1}}{R_{OS1}R_DC_Fs}\hat{v}_{O1} + \frac{1+s/\omega_{CZ2}}{R_{OS2}R_DC_Fs}\hat{v}_{O2}\right) \quad (53)$$

where:

$$\omega_{CP} = \frac{1}{(R_{B1} // R_{B2})C_B}$$
$$\omega_{CZ1} = \frac{1}{R_FC_F} \quad (54)$$
$$\omega_{CZ2} = \frac{1}{(R_F + R_{OS2})C_F}$$

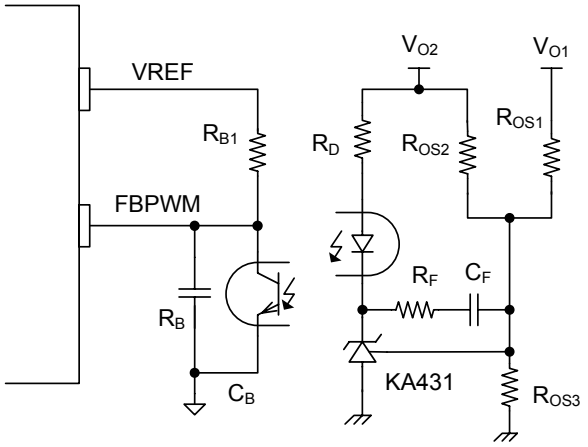


Figure 23. Feedback Compensation Circuit for PWM Stage

The small signal equivalent circuit for control-to-output transfer function of the PWM power stage can be simplified as shown in Figure 24. The transfer function is fourth-order system because additional LC filters are used to meet the output voltage ripple specification. Therefore, it is recommended to use engineering software, such as PSPICE or Mathlab, to design the feedback loop.

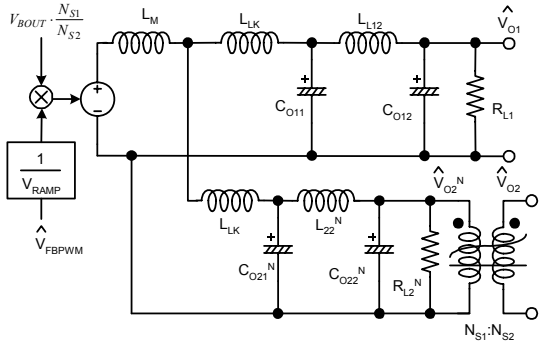


Figure 24. Simplified Small Signal Equivalent Circuit for Control-to-Output Transfer Function

Design Summary

Application	Output Power	Input Voltage	Output Voltage / Output Current
ATX Power	300W	85~264V_{AC}	12V/16.5A；5V/9A；-12V/0.8A ；3.3V/13.5A

Features

- Meets 80+ specification
- FAN4800A fully pin-to-pin compatible with ML4800 and FAN4800 (needs few parts modify)
- Switch-charge technique of gain modulator can provide better PF and lower THD
- Leading and trailing modulation technique for reduce output ripple
- Protections: OVP (Over-Voltage Protection), UVP (Under-Voltage Protection), OLP (Open-Loop Protection), and maximum current limit

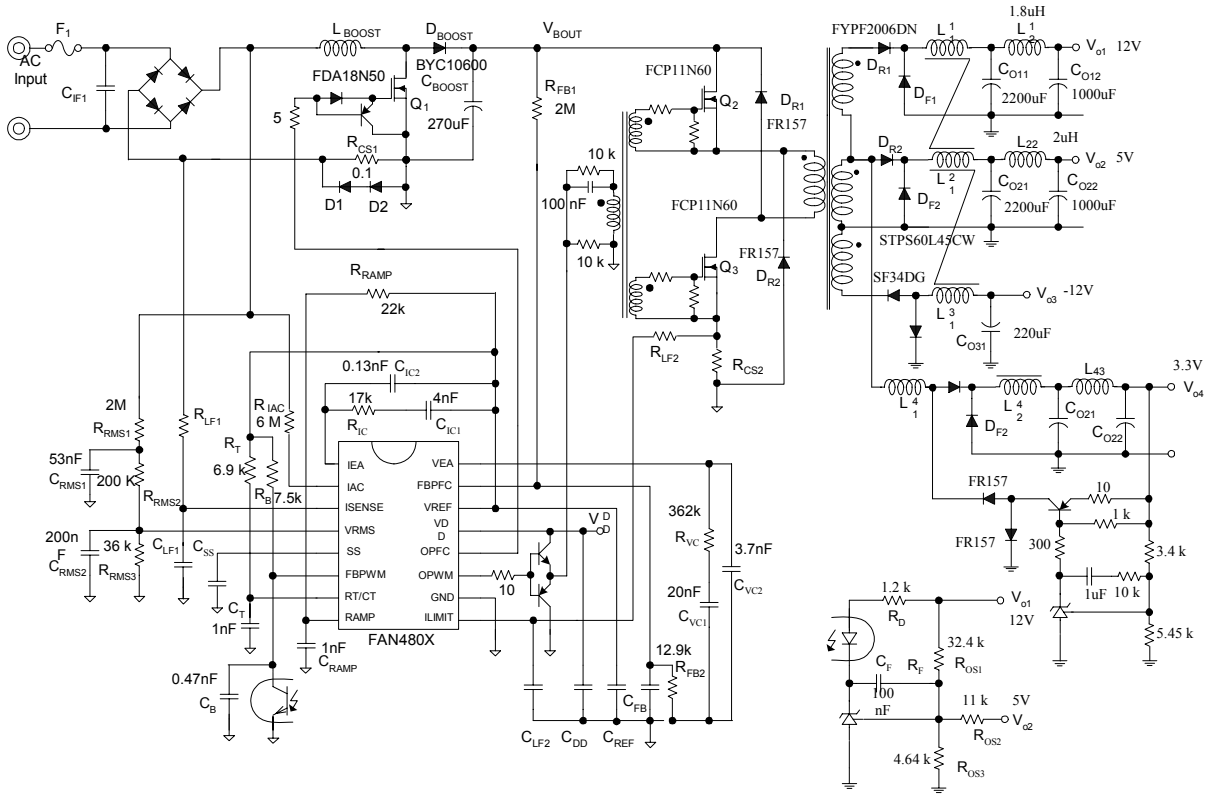


Figure 25. Final Schematic of Design Example

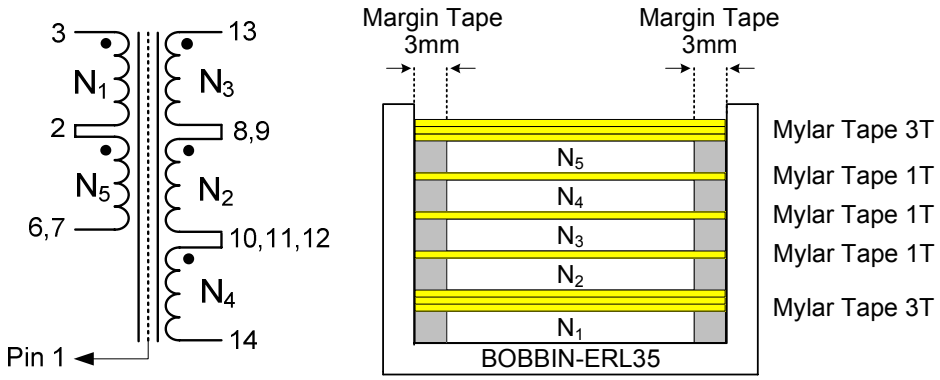


Figure 26. Forward Converter Transformer Structure

Winding Specification

No	Pin(s-f)	Wire	Turns	Winding Method
N_1	3-2	0.6Φ	37Ts	Solenoid Winding
Insulation: Mylar Tape t = 0.03mm, 3 Layers				
N2	8,9-10,11,12	Copper-Foil 10mil	3Ts	Copper-Foil Width 18mm
Insulation: Mylar Tape t = 0.03mm, 1 Layers				
N_3	13-8,9	1.0Φ*4	4Ts	Solenoid Winding
Insulation: Mylar Tape t = 0.03mm, 1 Layers				
N_4	10,11,12-14	0.4Φ	6Ts	Solenoid Winding
Insulation: Mylar Tape t = 0.03mm, 1 Layers				
N_5	2-6,7	0.6Φ	37Ts	Solenoid Winding
Insulation: Mylar Tape t = 0.03mm, 3 Layers				
Core-ERL35				
Insulation: Mylar Tape t = 0.03mm, 3 Layers				
Insulation: Copper-Foil Tape t = 0.05mm-pin1 Open Loop				
Insulation: Mylar Tape t = 0.03mm, 3 Layers				

Core: ERL35 (Ae=107 mm^2)
Bobbin: ERL35
Inductance: 13mH

Appendix A

FAN480X Series Comparison Table of Relevant Parameters

	FAN4800	New Generation FAN4800A	New Generation FAN4800C	New Generation FAN4801	New Generation FAN4802/2L
V_{DD} Maximum Rating	20V	30V			
V_{DD} OVP	17.9V/Clamp	28/Auto-Recover			
V_{CC} UVLO	10V/13V	9.3/11V			
Two-Level PFC Output	NO	NO		YES	
PFC Soft-Start	NO	YES			
Brownout	NO	YES			
PFC：PWM Frequency	1：1	1：1	1：2	1：1	1：2
Frequency Range	68kHz~81kHz	50kHz~75kHz			
Gate Clamp	NO	16V			
PFC Multiplier	Traditional	Switching Charge			
V_{IN}OK	2.25V/1.1V	2.40V/1.15V			
PWM Maximum Duty	42%~49%	49.5%~50%			
Startup Current	100μA	30μA			
Soft-Start Current	20μA	10μA			
PWM Comparator Level Shift	1.0V	1.5V			
R_{AC}	1~2MΩ	5~8 MΩ			

MOSFET and Diode Reference Specification

PFC MOSFETs	
Voltage Rating	**Part Number**
500V	FQP13N50C, FQPF13N50C, FDP18N50, FDPF18N50, FDA18N50, FDP20N50(T), FDPF20N50(T)
600V	FCP11N60, FCPF11N60, FCP16N60, FCPF16N60, FCP20N60S, FCPF20N60S, FCA20N60S, FCP20N60, FCPF20N60
Boost Diodes	
600V	FFP08H60S, FFPF10H60S, FFP08S60S, FPF08S60SN, BYC10600
PWM MOSFETs	
500V	FQP/PF9N50C, FQPF9N50C, FQP13N50C, FQPF13N50C, FQA13N50C, FDP18N50, FDPF18N50, FDP20N50(T), FDPF20N50(T)
600V	FCP11N60, FCPF11N60, FCP16N60, FCPF16N60, FCA16N60, FCP20N60S, FCPF20N60S, FCA20N60S, FCP20N60, FCPF20N60, FCA20N60

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References

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ATX 300W 80+ Evaluation Board of FAN4800A+SG6520+FSQ0170

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