Rev 0; 2/07

DALLAS SEMICONDUCTOR MAXIM

12.8MHz to 51.84MHz TCXO

General Description

The DS4026 is a temperature-compensated crystal oscillator (TCXO) that provides ±1ppm frequency stability over the -40°C to +85°C industrial temperature range. Each device is factory calibrated over temperature to achieve the ±1ppm frequency stability. Standard frequencies for the device include 12.8, 19.44, 20.0, 38.88, 40.0, and 51.84MHz. Contact the factory for custom frequencies.

The DS4026 provides excellent phase-noise characteristics. The output is a push-pull CMOS square wave with symmetrical rise and fall times. In addition, the DS4026 is designed to provide a maximum frequency deviation of less than ±4.6ppm over 10 years. The device also provides an I²C interface to allow pushing and pulling of the output frequency by a minimum of ±15ppm typical with typical 1ppb resolution.

The DS4026 implements a temperature-to-voltage conversion with a nonlinear relationship. The output from the temperature-to-voltage converter is used to drive the voltage-controlled crystal oscillator to compensate for frequency change.

The device implements an on-chip temperature sensor lookup table, and a digital-to-analog converter (DAC) to adjust the frequency. An I²C interface used to communicate with the DS4026 performs temperature readings and frequency push-pull.

Applications

Reference Clock Generation

Telecom/Datacom/SATCOM

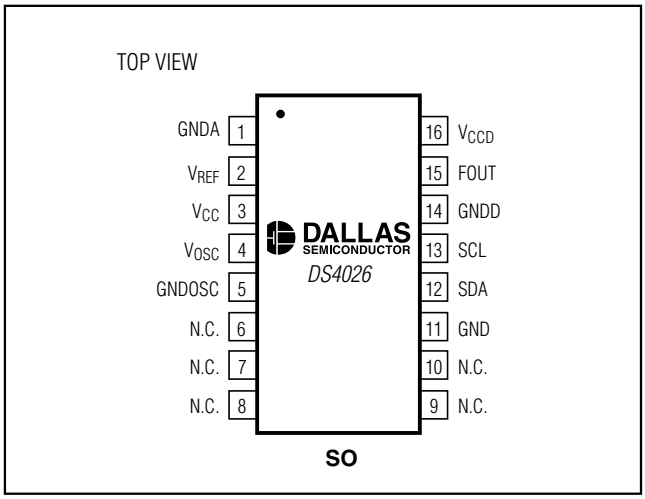
Wireless

Test and Measurement

Features

- **±1ppm Frequency Accuracy Over -40°C to +85°C**
- **Standard Frequencies: 12.8, 19.44, 20.0, 38.88, 40.0, 51.84MHz**
- **Maximum ±4.6ppm Deviation Over 10 Years**
- **Minimum ±8ppm Digital Frequency Tuning Through I²C Interface**
- **Surface-Mount 16-Pin SO Package**
- **Pb Free/RoHS Compliant**

Pin Configuration



Ordering Information

PART	TEMP RANGE	OUTPUT (f_{NOM}) (MHz, CMOS)	PIN-PACKAGE	TOP MARK*
DS4026S+BCC	0°C to +70°C	12.8	16 SO	DS4026-BCC
DS4026S+BCN	-40°C to +85°C	12.8	16 SO	DS4026-BCN
DS4026S+HCC	0°C to +70°C	19.44	16 SO	DS4026-HCC
DS4026S+HCN	-40°C to +85°C	19.44	16 SO	DS4026-HCN
DS4026S+JCC	0°C to +70°C	20.0	16 SO	DS4026-JCC
DS4026S+JCN	-40°C to +85°C	20.0	16 SO	DS4026-JCN

Ordering Information continued at end of data sheet.

+Lead-free package.

**The top mark will include a "+" for a lead-free/RoHS-compliant device.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, V_{CCD}, and V_{OSC} Relative to Ground.....-0.3V to +3.8V
Voltage Range on SDA, SCL, and FOUT Relative to Ground.....-0.3V to (V_{CC} + 0.3V)
Operating Temperature Range (noncondensing)....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC}		3.135	3.3	3.465	V
Oscillator Power Supply	V_{OSC}		3.135	3.3	3.465	V
Driver Power Supply	V_{CCD}		3.135	3.3	3.465	V

DC ELECTRICAL CHARACTERISTICS (Note 1)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Active-Supply Current	I_{CC}	(Note 4)		1.5	2.5	mA
V_{OSC} Oscillator Active-Supply Current	I_{OSC}	FOUT CMOS output on, CL = 10pF, frequency < 25MHz		3	4	mA
		FOUT CMOS output on, CL = 10pF, frequency ≥ 25MHz		5	9	
V_{CCD} Driver Active-Supply Current	I_{CCD}	FOUT CMOS output on, CL = 10pF, frequency < 25MHz		2	3	mA
		FOUT CMOS output on, CL = 10pF, frequency ≥ 25MHz		3	5	
SCL Input Leakage	I_{LI}		-1		+1	µA
SDA Leakage	I_{LO}	Output off	-1		+1	µA
SCL, SDA High Input Voltage	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
SCL, SDA Low Input Voltage	V_{IL}		-0.3		+0.3 x V_{CC}	V
SDA Logic 0 Output	I_{OL}	V_{CC} = 3.0V, V_{OL} = 0.4V			3	mA
FOUT High Output Voltage	V_{OH}	V_{CCD} = 3V, I_{OH} = -2mA	2.4			V
FOUT Low Output Voltage	V_{OL}	V_{CCD} = 3V, I_{OL} = 2.0mA			0.4	V
FOUT Rise/Fall Time	t_R/t_F	(0.1 x V_{CCD}) - (0.9 x V_{CCD})		2		ns
FOUT Duty Cycle	t_D	0.5 x V_{CCD} (Note 5)	45		55	%

AC ELECTRICAL CHARACTERISTICS (Note 1)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Stability vs. Temperature	$\Delta f_1/T_A$	CL = 10pF to ground	f_{NOM} – 1ppm	f_{NOM}	f_{NOM} + 1ppm	ppm
Frequency Stability vs. Voltage	$\Delta f_1/V$	CL = 10pF	-2		+2	ppm/V
Aging, First Year	$\Delta f_1/Yr$	(Note 5)	-1		+1	ppm
Aging, Years 2–15	$\Delta f_1/Yr$	(Note 5)	-2		+2	ppm
Frequency Pull Range	Δf	FTUNEH = 3Fh and FTUNEL = FFh; FTUNEH = 40h and FTUNEL = 00h	±8	±15		ppm
Frequency Pull Resolution	Δf_{RES}			1		ppb

PHASE NOISE

	PHASE NOISE (dBc/Hz) (TYPICAL, +25°C, 3.3V)						
	OFFSET (MHz)	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz
CARRIER FREQUENCY	12.80	-88.41	-130.16	-147.84	-150.84	-151.71	-151.87
	19.44	-82.63	-125.12	-145.03	-146.87	-151.69	-151.52
	20.00						
	38.88	-79.01	-120.06	-141.75	-150.59	-152.50	-153.06
	40.00	-80.80	-115.44	-141.17	-151.59	-152.37	-153.00
	51.84	-74.09	-120.39	-142.33	-151.14	-153.21	-153.94

TEMPERATURE SENSOR ELECTRICAL CHARACTERISTICS (Note 1)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Sensor Accuracy	ΔT		-3		+3	°C
Temperature Sensor Conversion Time	t_{CONVT}				11	ms
Temperature Sensor Resolution	N2				12	Bits

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	0		100	kHz
		Fast mode	100		400	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Standard mode	4.7			µs
		Fast mode	1.3			
Hold Time (Repeated) START Condition (Note 6)	$t_{HD:STA}$	Standard mode	4.0			µs
		Fast mode	0.6			
Low Period of SCL Clock	t_{LOW}	Standard mode	4.7			µs
		Fast mode	1.3			
High Period of SCL Clock	t_{HIGH}	Standard mode	4.0			µs
		Fast mode	0.6			
Data Hold Time (Notes 7, 8)	$t_{HD:DAT}$	Standard mode	0		0.9	µs
		Fast mode	0		0.9	
Data Setup Time (Note 9)	$t_{SU:DAT}$	Standard mode	250			ns
		Fast mode	100			
Start Setup Time	$t_{SU:STA}$	Standard mode	4.7			µs
		Fast mode	0.6			
Rise Time of Both SDA and SCL Signals (Note 10)	t_R	Standard mode	$20 + 0.1C_B$		1000	ns
		Fast mode	$20 + 0.1C_B$		300	
Fall Time of Both SDA and SCL Signals (Note 10)	t_F	Standard mode	$20 + 0.1C_B$		300	ns
		Fast mode	$20 + 0.1C_B$		300	

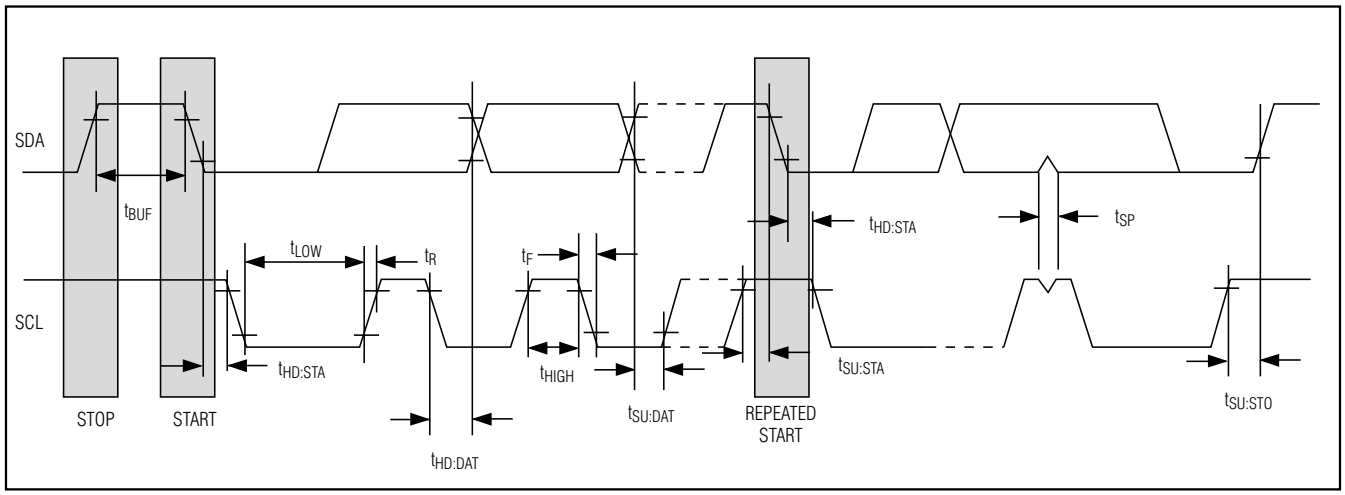
AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	$t_{SU:STO}$	Standard mode	4.7			µs
		Fast mode	0.6			
Pin Capacitance SDA, SCL (Note 5)	$C_{I/O}$				10	pF
Capacitive Load for Each Bus Line (Note 10)	C_B				400	pF
Pulse Width of Spikes That Must Be Suppressed by the Input Filter	t_{SP}	Fast mode		30		ns

Note 1: Typical values are at +25°C, nominal supply voltages, unless otherwise indicated.
Note 2: Voltages referenced to ground.
Note 3: Limits at -40°C are guaranteed by design and not production tested.
Note 4: Specified with I^2C bus inactive.
Note 5: Guaranteed by design and not production tested.
Note 6: After this period, the first clock pulse is generated.
Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 8: The maximum tHD:DAT need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 9: A fast-mode device can be used in a standard-mode system, but the requirement that $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does not stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 10: C_B—total capacitance of one bus line in pF.

Data Transfer on I^2C Serial Bus

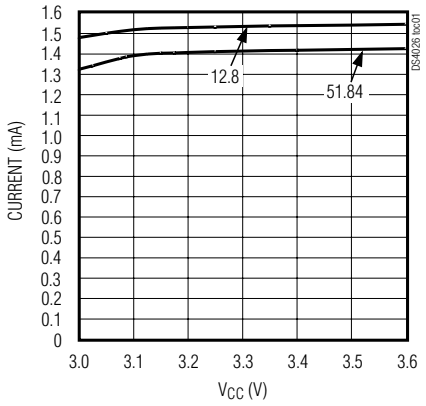


12.8MHz to 51.84MHz TCXO

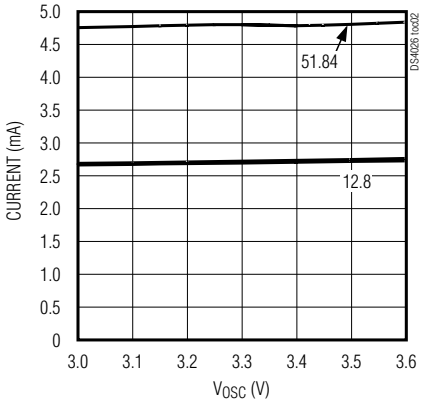
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

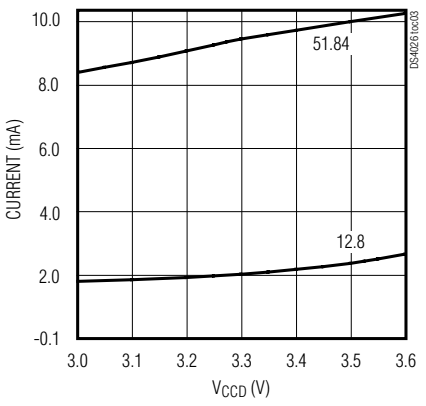
ACTIVE-SUPPLY CURRENT vs. POWER-SUPPLY CURRENT



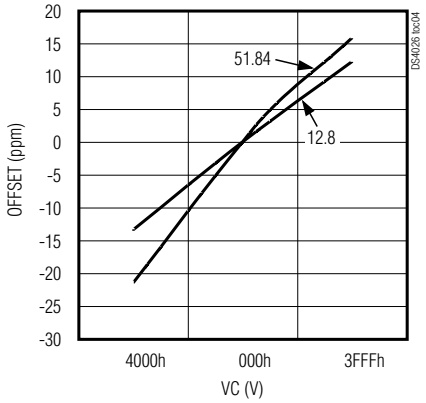
ACTIVE-SUPPLY CURRENT vs. OSCILLATOR POWER SUPPLY



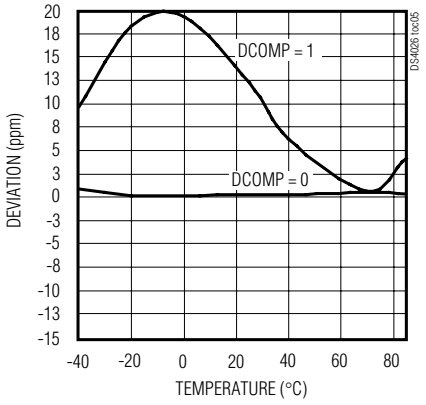
ACTIVE-SUPPLY CURRENT vs. DRIVER POWER SUPPLY



FREQUENCY vs. FTUNE



FREQUENCY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	GNDA	Ground for DAC
2	V_{REF}	Voltage Reference Output. This pin must be decoupled with a 100µF ceramic capacitor to ground.
3	V_{CC}	Power Supply for Digital Control and Temperature Sensor. This pin must be decoupled with a 100nF capacitor to ground.
4	V_{OSC}	Power Supply for Oscillator Circuit. This pin must be decoupled with a 100nF capacitor to ground.
5	GNDOSC	Ground for Oscillator Circuit
6–10	N.C.	No Connection. Must be connected to ground.
11	GND	Ground for Digital Control, Temperature Sensor, and Controller Substrate
12	SDA	Serial Data Input/Output. SDA is the data input/output for the I^2C interface. This open-drain pin requires an external pullup resistor.
13	SCL	Serial Clock Input. SCL is the clock input for the I^2C Interface and is used to synchronize data movement on the serial interface.
14	GNDD	Ground for Oscillator Output Driver
15	FOUT	Frequency Output, CMOS Push-Pull
16	V_{CCD}	Power Supply for Oscillator Output Driver. This pin must be decoupled with a 100nF capacitor to ground. A 20Ω resistor must be placed in series between the power supply and V_{CCD}.

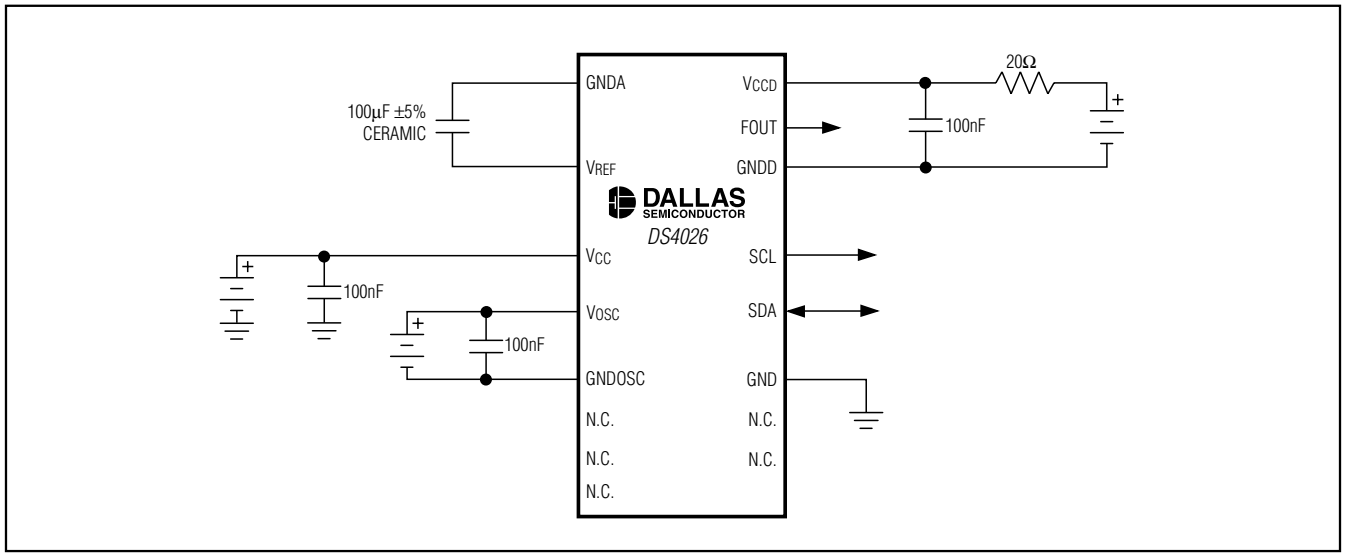


Figure 1. Typical Operating Circuit

12.8MHz to 51.84MHz TCXO

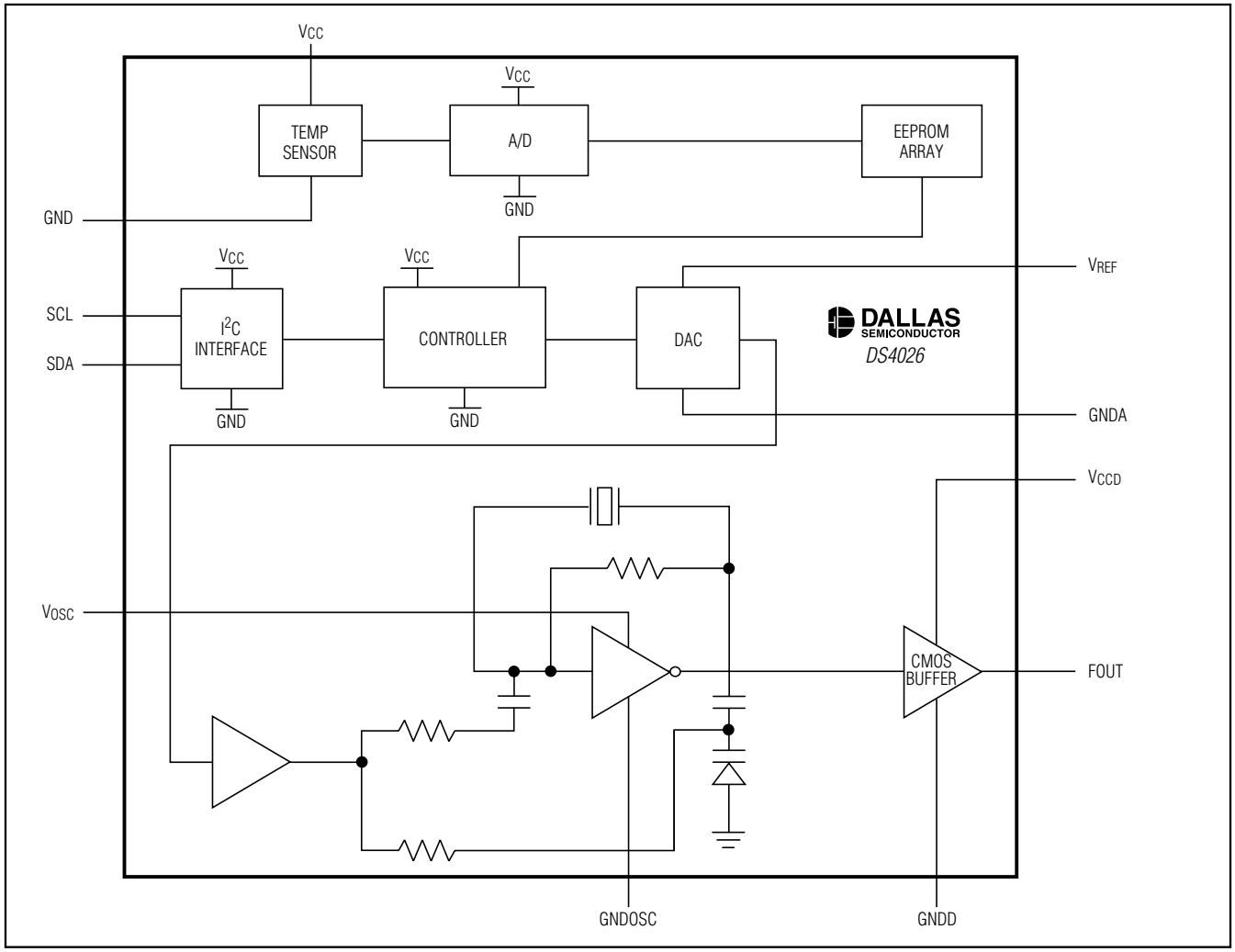


Figure 2. Functional Diagram

Detailed Description

The DS4026 is a TCXO capable of operating at 3.3V ±10%, and it allows digital tuning of the fundamental frequency. The device is calibrated in the factory to achieve an accuracy of ±1ppm over the industrial temperature range, and its minimum pullability is ±8ppm with a typical resolution of 1ppb (typ) per LSB.

The DS4026 contains the following blocks:

- Oscillator block with variable capacitor for compensation
- Output driver block
- Temperature sensor
- Controller to read the temperature, control lookup table, and adjust the DAC input
- DAC output to adjust the capacitive load
- I^2C interface to communicate with the chip

The oscillator block consists of an amplifier and variable capacitor in a Pierce crystal oscillator with a crystal resonator of fundamental mode. The oscillator amplifier is a single transistor amplifier and its transconductance is temperature compensated. The variable capacitor is adjusted by the DAC to provide temperature compensation. With the FTUNEH and FTUNEL registers, a minimum pullability of ±15ppm (typ) is achieved with a typical resolution of 1ppb (typ) per LSB.

The output driver is a CMOS square-wave output with symmetrical rise and fall time.

The temperature sensor provides a 12-bit temperature reading with a resolution of 0.0625°C. The sensor is in continuous conversion mode unless the DCOMP bit in the control register is set to disable temperature updates.

The controller coordinates the conversion of temperature into digital codes. When the temperature reading is different from the previous one or the frequency tuning register is changed, the controller looks up the two corresponding capacitance trim codes from the lookup table at a 0.5°C increment. The trim codes are interpolated to 0.0625°C resolution.

The result is added with the tuning value from the frequency tuning register and loaded into the DAC registers to adjust voltage output. The monotonic DAC provides an analog voltage based on temperature compensation to drive the variable capacitor.

The DS4026 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed.

Address Map

Disable Compensation Update (DCOMP)

DCOMP is bit 7 of the frequency tuning register (see the *Frequency Tuning Register (00h–01h), POR = 00h* table). When set to logic 1, this bit's temperature-compensation function is disabled. This disabling prevents the variable capacitor in the oscillator block from changing. However, the temperature register still performs temperature conversions. The temperature trim code from the last temperature conversion before DCOMP is enabled is used for temperature compensation. The FTUNE registers are still functional when DCOMP is disabled.

The frequency tuning registers adjust the base frequency. The frequency tuning value is represented in two's complement data. Bit 6 of FTUNEH is the sign, bit 5 is the MSB, and bit 0 of FTUNEL is the LSB (see Table 1). When the tuning register low (01h) is programmed with a value, the next temperature update cycle sums the programmed value with the factory compensated value. This allows the user to digitally control the base frequency using the I^2C protocol.

These frequency tuning register bits allow the tuning of the base frequency. Each bit typically represents about 1ppb (typ). For FTUNEH = 3Fh and FTUNEL = FFh, the device pushes the base frequency by approximately +15ppm.

Frequency Tuning Register (00h–01h), POR = 00h

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	DCOMP	Sign	Data	Data	Data	Data	Data	Data
POR	0	0	0	0	0	0	0	0
01h	Data	Data	Data	Data	Data	Data	Data	Data
POR	0	0	0	0	0	0	0	0

Temperature Register (02h–03h)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
02h	Sign	Data	Data	Data	Data	Data	Data	Data
POR	0	0	0	0	0	0	0	0
03h	Data	Data	Data	Data	0	0	0	0
POR	0	0	0	0	0	0	0	0

Table 1. Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
00	DCOMP	SIGN	FTUNEH						Frequency Tuning High
01	FTUNEL								Frequency Tuning Low
02	SIGN	TREGH							Temperature MSB
03	TREGL								Temperature LSB

Read Mode

In the temperature register (see the *Temperature Register (02h–03h)* table), temperature is represented as a 12-bit code and is accessible at location 02h and 03h. The upper 8 bits are at location 02h and the lower 4 bits are in the upper nibble of the byte at location 03h. Upon power reset, the registers are set to a +25°C default temperature and the controller starts a temperature conversion. The temperature register stores new temperature readings.

The current temperature is loaded into the (user) temperature registers when a valid I²C slave address and write is received and when a word address is received. Consequently, if the two temperature registers are read in individual I²C transactions, it is possible for a temperature conversion to occur between reads, and the results can be inaccurate. To prevent this from occurring, the registers should be read using a single, multibyte read operation (Figure 5). I²C reads do not affect the internal temperature registers.

I²C Serial Data Bus

The DS4026 supports a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS4026 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS4026 works in both modes.

The following bus protocol has been defined (Figure 3):

- Data transfer can be initiated only when the bus is not busy.

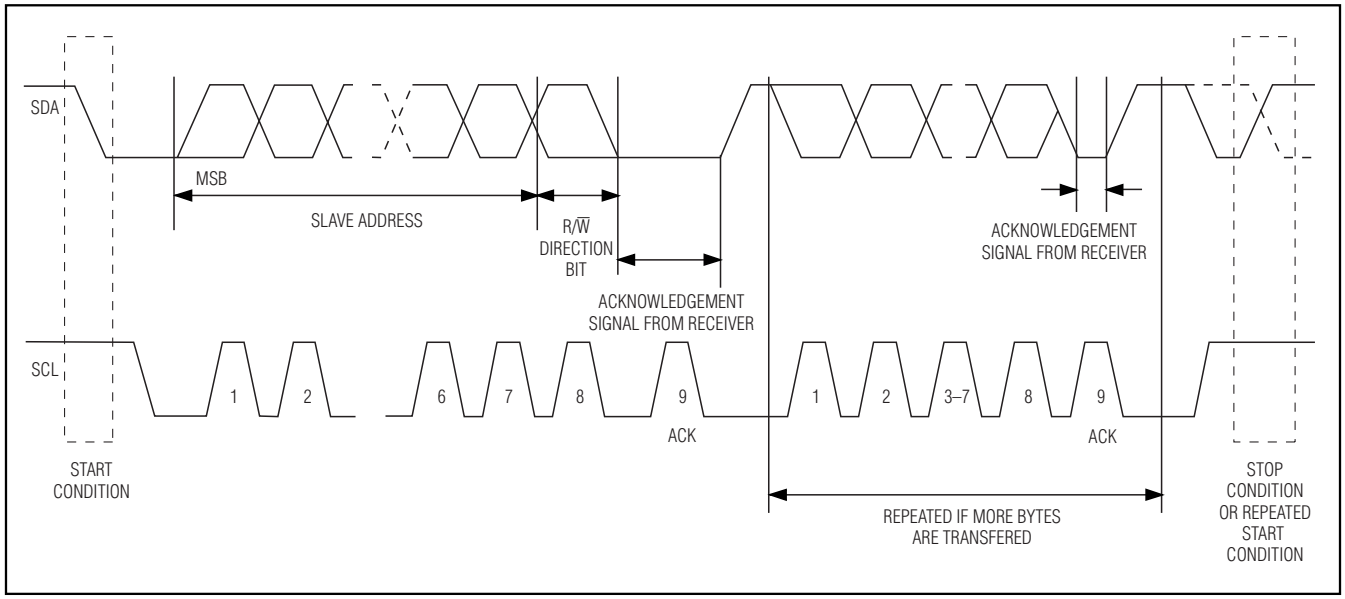


Figure 3. I²C Data Transfer Overview

- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge (ACK) after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figures 4 and 5 detail how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge (ACK) bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge (NACK) is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

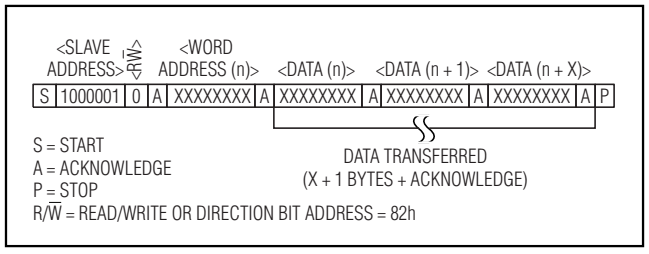


Figure 4. Slave Receiver Mode (Write Mode)

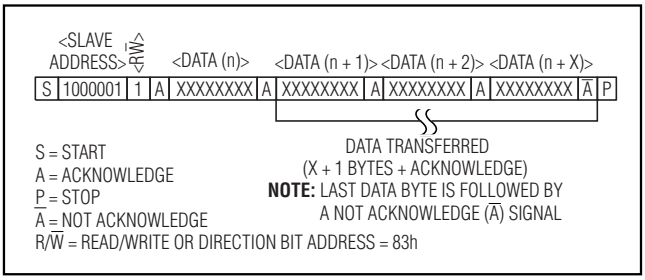


Figure 5. Slave Transmitter Mode (Read Mode)

12.8MHz to 51.84MHz TCXO

The DS4026 can operate in the following two modes:

Slave receiver mode (write mode): Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS4026 address, which is 1000001, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte, the DS4026 outputs an acknowledge on SDA. After the DS4026 acknowledges the slave address and write bit, the master transmits a word address to the DS4026. This sets the register pointer on the DS4026, with the DS4026 acknowledging the transfer. The master can then transmit zero or more bytes of data, with the DS4026 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

Slave transmitter mode (read mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS4026 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS4026 address, which is 1000001, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte, the DS4026 outputs an acknowledge on SDA. The DS4026 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS4026 must receive a not acknowledge to end a read.

Ordering Information (continued)

PART	TEMP RANGE	OUTPUT (f_{NOM}) (MHz, CMOS)	PIN-PACKAGE	TOP MARK*
DS4026S+MCC	0°C to +70°C	38.88	16 SO	DS4026-MCC
DS4026S+MCN	-40°C to +85°C	38.88	16 SO	DS4026-MCN
DS4026S+PCC	0°C to +70°C	40.0	16 SO	DS4026-PCC
DS4026S+PCN	-40°C to +85°C	40.0	16 SO	DS4026-MCN
DS4026S+QCC	0°C to +70°C	51.84	16 SO	DS4026-QCC
DS4026S+QCN	-40°C to +85°C	51.84	16 SO	DS4026-QCN

+Lead-free package.

**The top mark will include a "+" for a lead-free/RoHS-compliant device.*

Chip Information

TRANSISTOR COUNT: 77, 712

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

PACKAGE TYPE	DOCUMENT NO.
16-pin SO (300 mils)	**56-G4009-001**

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