

FDS3570

80V N-Channel PowerTrench® MOSFET

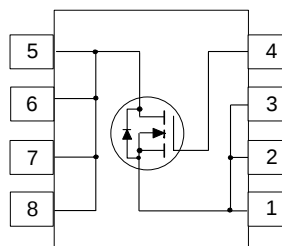
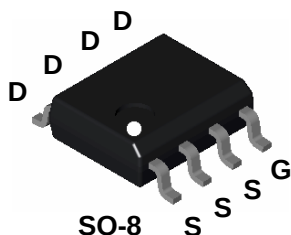
General Description

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(on)}$ specifications resulting in DC/DC power supply designs with higher overall efficiency.

Features

- 9 A, 80 V. $R_{DS(on)} = 0.020 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(on)} = 0.023 \Omega @ V_{GS} = 6 \text{ V}$.
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.
- High power and current handling capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	9	A
	- Pulsed	50	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS3570	FDS3570	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 40\text{ V}$, $I_D = 9\text{ A}$			360	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				9	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_1}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		77		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	2.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_1}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-7		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}$, $I_D = 8.4\text{ A}$		0.015 0.027 0.016	0.020 0.038 0.023	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	25			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 7.6\text{ A}$		40		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		2750		pF
C_{oss}	Output Capacitance			280		pF
C_{rss}	Reverse Transfer Capacitance			140		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		20	32	ns
t_r	Turn-On Rise Time			12	24	ns
$t_{d(off)}$	Turn-Off Delay Time			60	95	ns
t_f	Turn-Off Fall Time			24	38	ns
Q_g	Total Gate Charge	$V_{DS} = 40\text{ V}$, $I_D = 9\text{ A}$, $V_{GS} = 10\text{ V}$		54	76	nC
Q_{gs}	Gate-Source Charge			9.6		nC
Q_{gd}	Gate-Drain Charge			14		nC

Drain-Source Diode Characteristics and Maximum Ratings

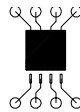
I _S	Maximum Continuous Drain-Source Diode Forward Current					2.1	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.1 A	(Note 2)		0.72	1.2	V

Notes:

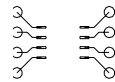
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50° C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 105° C/W when mounted on a 0.04 in^2 pad of 2 oz. copper.



c) 125° C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

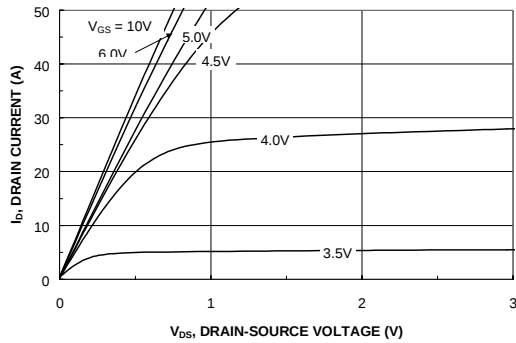


Figure 1. On-Region Characteristics.

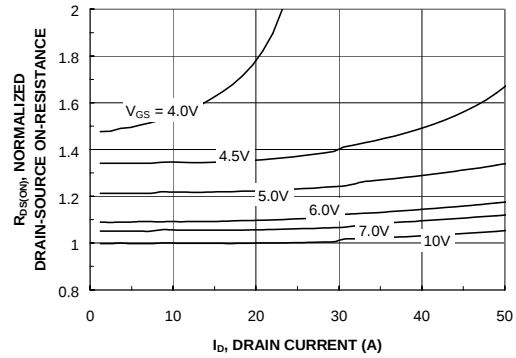


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

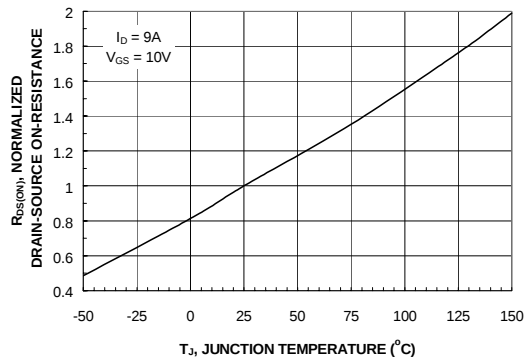


Figure 3. On-Resistance Variation with Temperature.

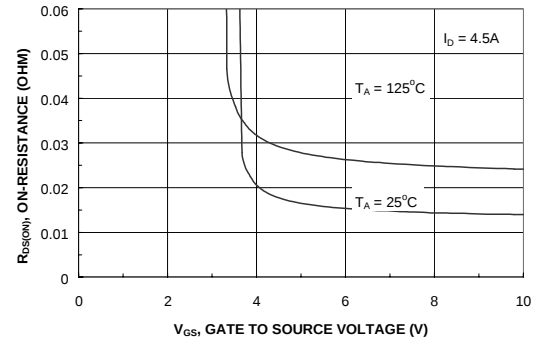


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

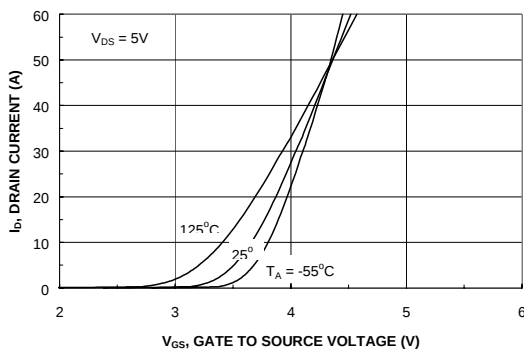


Figure 5. Transfer Characteristics.

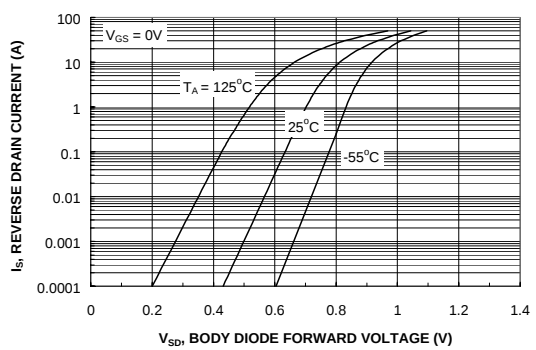
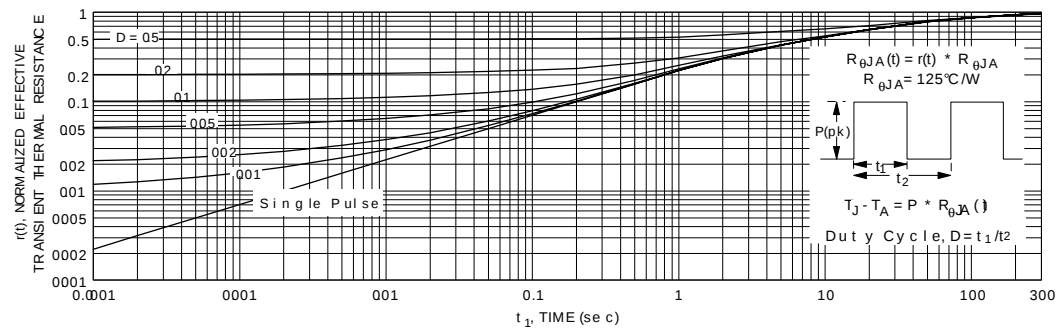
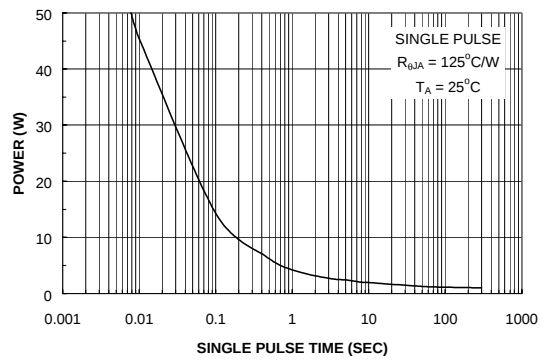
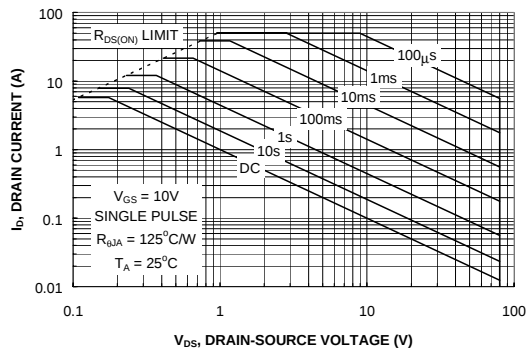
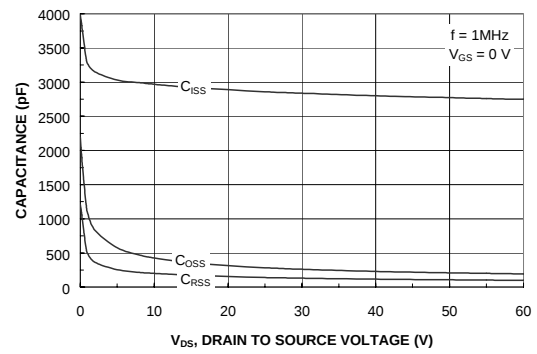
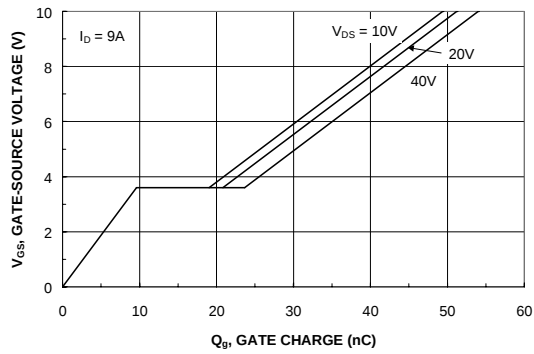


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



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