Features

- **High Density, High Performance Electrically Erasable Complex Programmable Logic Device**
  - **64 Macrocells**
  - **5 Product Terms per Macrocell, Expandable up to 40 per Macrocell**
  - **44, 68, 84, 100 pins**
  - **7 ns Maximum Pin-to-Pin Delay**
  - **Registered Operation Up To 100 MHz**
  - **Enhanced Routing Resources**
- **In-System Programmability (ISP) via JTAG**
- **Flexible Logic Macrocell**
  - **D/T/Latch Configurable Flip Flops**
  - **Global and Individual Register Control Signals**
  - **Global and Individual Output Enable**
  - **Programmable Output Slew Rate**
  - **Programmable Output Open Collector Option**
  - **Maximum Logic utilization by burying a register within a COM output**
- **Advanced Power Management Features**
  - **Automatic 100 µA Stand-By for "Z" Version**
  - **Pin-Controlled 4 mA Stand-By Mode (Typical)**
  - **Programmable Pin-Keeper Inputs and I/Os**
  - **Reduced-Power Feature Per Macrocell**
- **Available in Commercial and Industrial Temperature Ranges**
- **Available in 44-, 68-, and 84-pin PLCC; 44- and 100-pin TQFP; and 100-pin PQFP**
- **Advanced EE Technology**
  - **100% Tested**
  - **Completely Reprogrammable**
  - **100 Program/Erase Cycles**
  - **20 Year Data Retention**
  - **2000V ESD Protection**
  - **200 mA Latch-Up Immunity**
- **JTAG Boundary-Scan Testing to IEEE Std. 1149.1-1990 and 1149.1a-1993 Supported**
- **PCI-compliant**
- **3.3 or 5.0V I/O pins**
- **Security Fuse Feature**

Enhanced Features

- **Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)**
- **Output Enable Product Terms**
- **D - Latch Mode**
- **Combinatorial Output with Registered Feedback within any Macrocell**
- **Three Global Clock Pins**
- **ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O**
- **Fast Registered Input from Product Term**
- **Programmable "Pin-Keeper" Option**
- **V_{CC} Power-Up Reset Option**
- **Pull-Up Option on JTAG Pins TMS and TDI**
- **Advanced Power Management Features**
  - **Edge Controlled Power Down "L"**
  - **Individual Macrocell Power Option**
  - **Disable ITD on Global Clocks, Inputs and I/O**

Description

The ATF1504AS is a high performance, high density Complex Programmable Logic Device (CPLD) which utilizes Atmel's proven electrically erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several

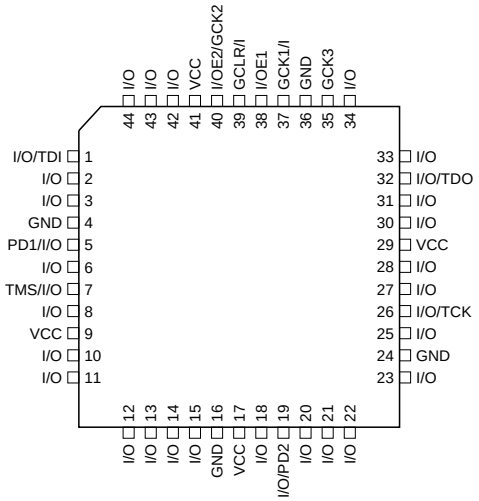
(continued)

High-Performance EE CPLD

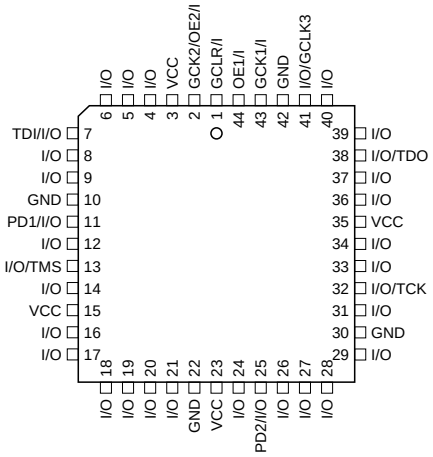
ATF1504AS
ATF1504ASZ

Rev. 0950D–07/98

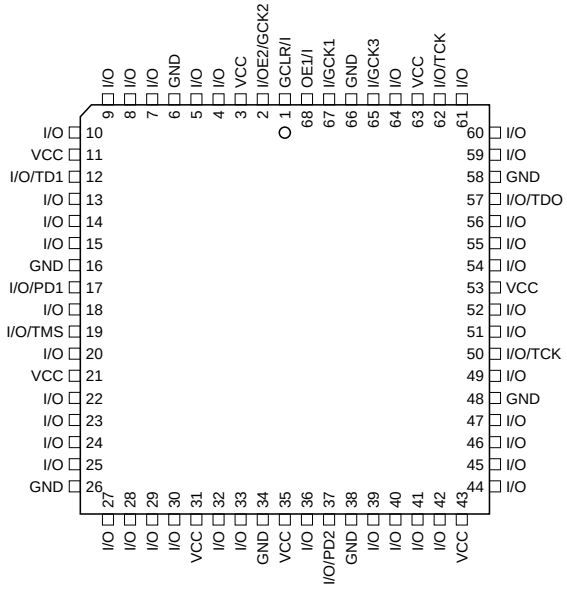
44-Lead TQFP
Top View



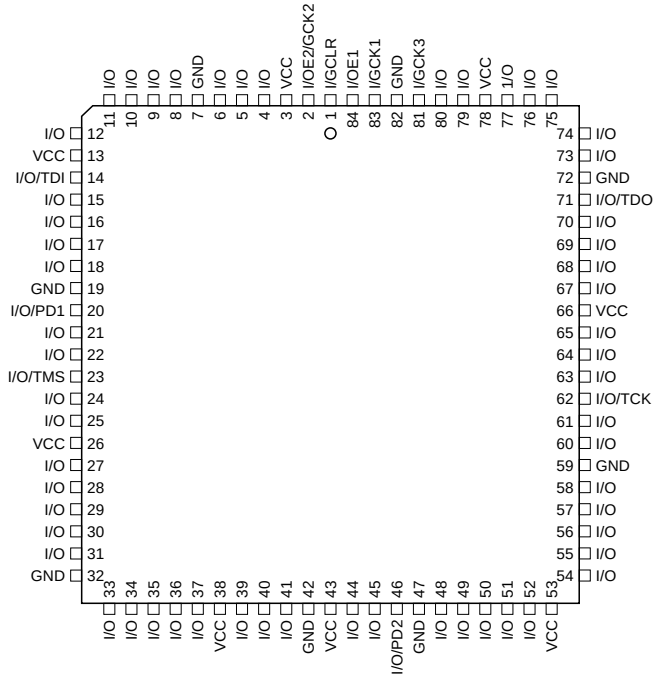
44-Lead PLCC
Top View



68-Lead PLCC
Top View

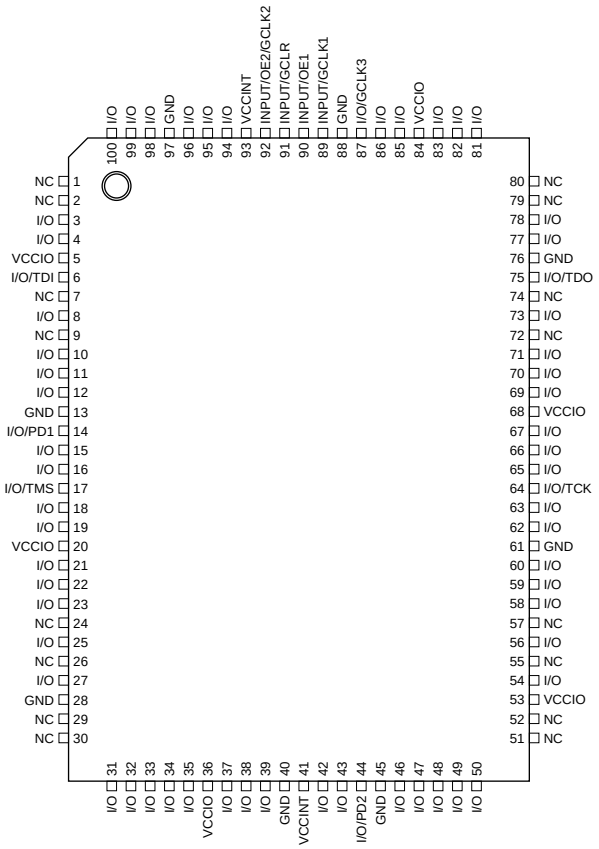


84-Lead PLCC
Top View



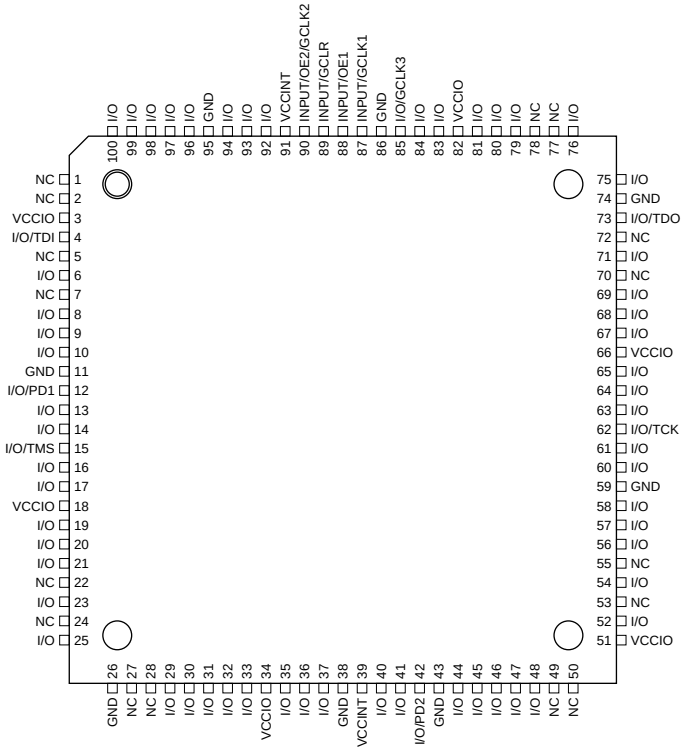
100-Lead PQFP

Top View



100-Lead TQFP

Top View



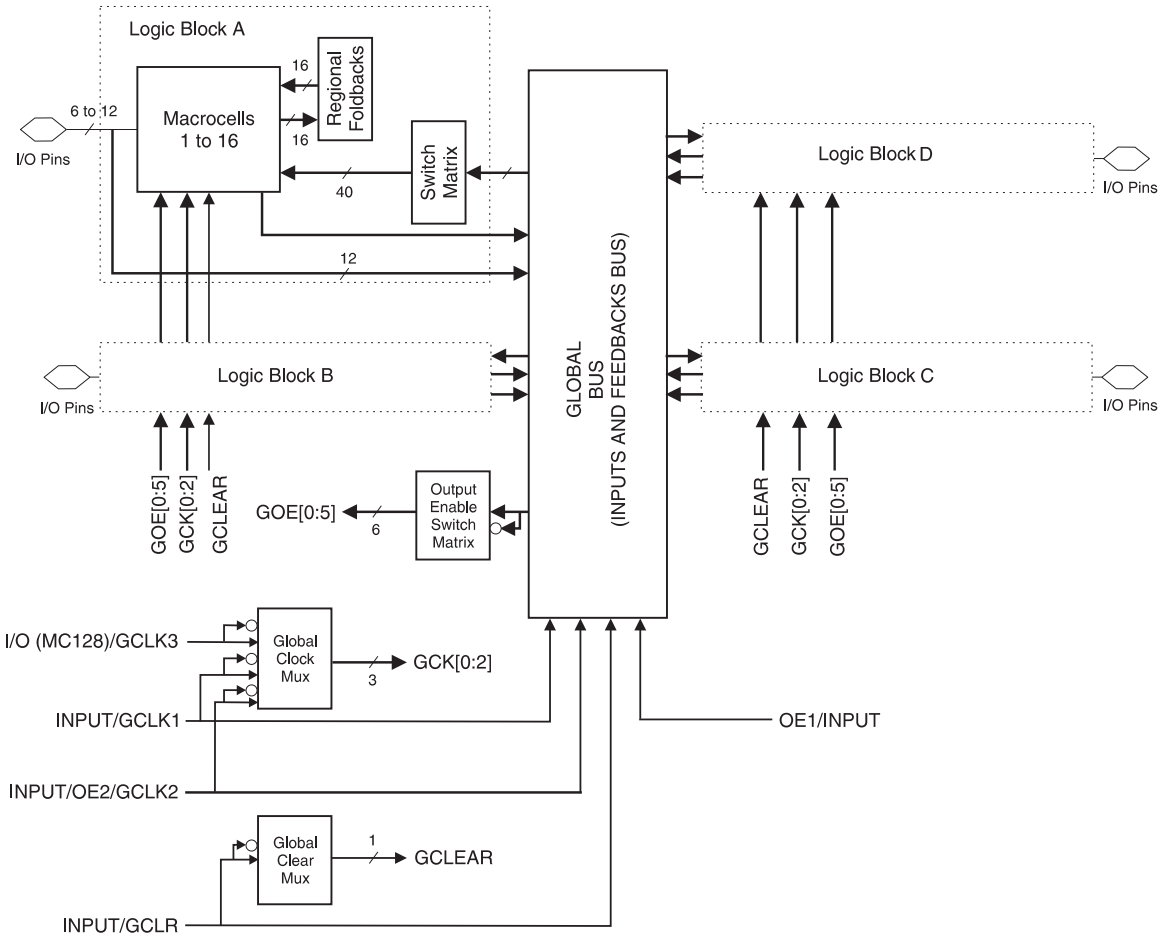
TTL, SSI, MSI, LSI and classic PLDs. The ATF1504AS's enhanced routing switch matrices increase usable gate count, and the odds of successful pin-locked design modifications.

The ATF1504AS has up to 68 bi-directional I/O pins and 4 dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal; register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term, which goes to a regional bus. Cascade logic between macrocells in the ATF1504AS allows fast, efficient generation of complex logic functions. The ATF1504AS contains four such logic chains, each capable of creating sum term logic with a fan in of up to 40 product terms.

The ATF1504AS macrocell shown in Figure 1, is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic; a flip-flop; output select and enable; and logic array inputs.

Block Diagram



Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF1504AS. Two bytes (16-bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

The ATF1504AS device is an In-System Programmable (ISP) device. It uses the industry standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary Scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select MUX

Each ATF1504AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1504AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a very small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip Flop

The ATF1504AS's flip flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can either be one of the Global CLK Signal GCK[0 : 2] or an individual product term. The flip flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1504AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

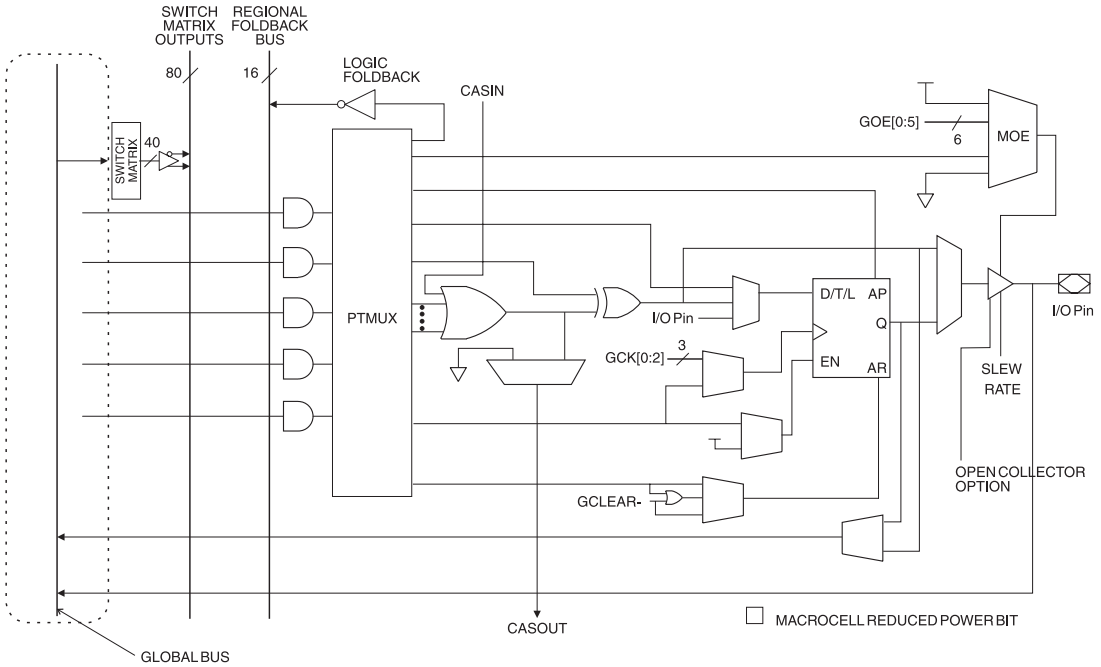
Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The Switch Matrix in each Logic Block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the Logic Block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 4 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 4 foldback terms in each region allows generation of high fan-in sum terms (up to 9 product terms) with a small additional delay.

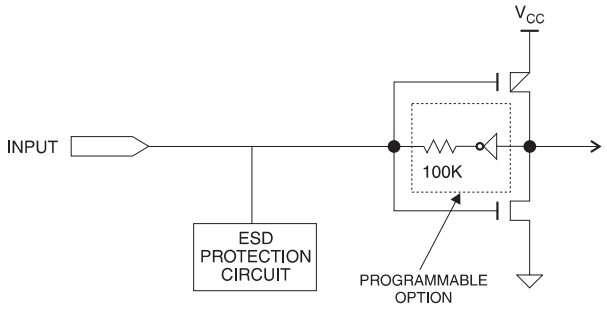
Figure 1. ATF1504AS Macrocell



Programmable Pin-Keeper Option for Inputs and I/Os

The ATF1504AS offers the option of programming all input and I/O pins so that pin keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

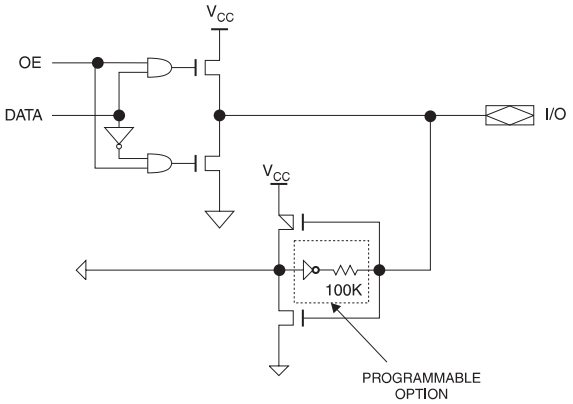
Input Diagram



Speed/Power Management

The ATF1504AS has several built-in speed and power management features. The ATF1504AS contains circuitry that automatically puts the device into a low power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides a proportional power savings for most applications running at system speeds below 50 MHz. This feature may be selected as a design option.

I/O Diagram



To further reduce power, each ATF1504AS macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504ASs also have an optional power down mode. In this mode, current drops to below 10 mA. When the power down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power down option is selected in the design source file. When enabled,

the device goes into power down when either PD1 or PD2 is high. In the power down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All Power-Down AC Characteristic parameters are computed from external input or I/O pins, with Reduced Power Bit turned on. For macrocells in reduced-power mode (Reduced power bit turned on), the reduced power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

The ATF1504AS macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power down option, macrocells that are not used in an application can be turned down thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1504AS designs are supported by several third party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

Power Up Reset

The ATF1504AS has a power-up reset option at two different voltage trip levels when the device is being powered down. Within the fitter, or during a conversion, if the "power-reset" option is turned "on" (which is the default option), the trip levels during power up or power down is at 2.8V. The user can change this default option from "on" to "off" (within the fitter or specify it as a switch during conversion). When this is done, the voltage trip level during power-down changes from 2.8V to 0.7V. This is to ensure a robust operating environment.

The registers in the ATF1504AS are designed to reset during power up. At a point delayed slightly from V_{CC} crossing Vrst, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin-high, and,
3. The clock must remain stable during T_D.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504AS fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

Programming

ATF1504AS devices are In-System Programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for program and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS via the PC. ISP is performed by using either a download cable, or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided Software utilities.

ATF1504AS devices can also be programmed using standard 3rd party programmers. With 3rd party programmer the JTAG ISP port can be disabled thereby allowing 4 additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1504AS has a special feature which locks the device and prevents the inputs and I/O from driving if the programming process is interrupted due to any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin keeper option preserves the former state during device programming.

All ATF1504AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CCINT} or V_{CCIO} (5V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Stand-by	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		120		mA
				Ind.		150		mA
			"Z" Mode	Com.			100	µA
				Ind.			100	µA
I_{CC2}	Power Supply Current, Power Down Mode	V_{CC} = Max V_{IN} = 0, V_{CC}	"PD" Mode			4	10	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-150	mA
V_{CCIO}	Supply Voltage	5.0V Device Output		Com.	4.75		5.25	V
				Ind.	4.5		5.5	V
V_{CCIO}	Supply Voltage	3.3V Device Output			3.0		3.6	V
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCINT} + 0.3	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OL} = 12 mA		Com.			0.45	V
				Ind.				
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OH} = -4.0 mA				2.4		V

Note: Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

Pin Capacitance

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pf.

Absolute Maximum Ratings*

Temperature Under Bias ..... -40°C to +85°C

Storage Temperature ..... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground .....-2.0V to +7.0V(1)

Voltage on Input Pins
with Respect to Ground
During Programming.....-2.0V to +14.0V(1)

Programming Voltage with
Respect to Ground .....-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

AC Characteristics

		-7		-10		-15		-20		-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD1}	Input or Feedback to Non-Registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-Registered Feedback		7		9	3	12		16		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

(continued)

= Preliminary Information

AC Characteristics (Continued)

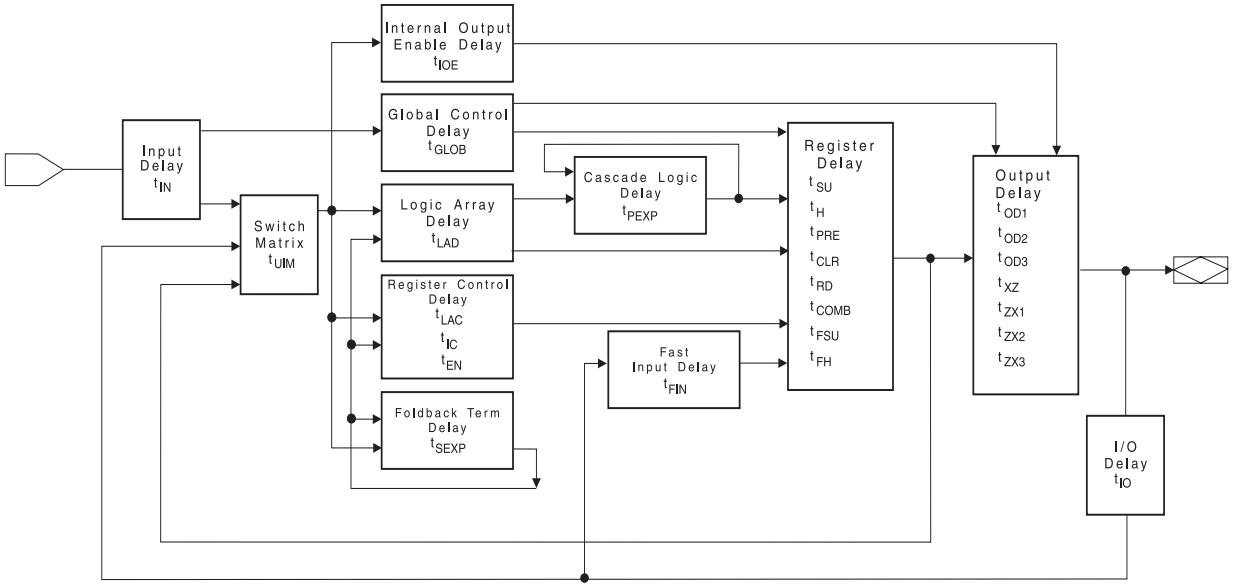
Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
F_{MAX}	Maximum Clock Frequency	166.7		125		100		83.3		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		2		1.5		4		5		6	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		5.5		8		10		10	ns

Note: See ordering information for valid part numbers.

(continued)

= Preliminary Information

Timing Model



AC Characteristics (Continued)

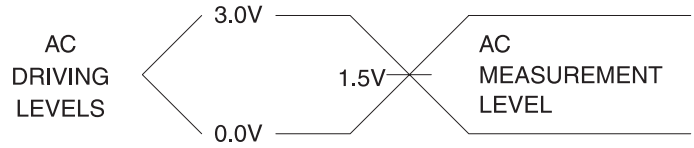
Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		4.0		5.0		7		9		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		4.5		5.5		7		9		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		9		9		10		11		12	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		4		5		6		7		8	ns
t_{SU}	Register Setup Time	3		3		4		5		6		ns
t_H	Register Hold Time	2		3		4		5		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t_{RD}	Register Delay		1		2		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		6		7		8	ns
t_{EN}	Register Enable Time		3		5		6		7		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		5		6	ns
t_{CLR}	Register Clear Time		2		3		4		5		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t_{RPA}	Reduced-Power Adder(2)		10		11		13		14		15	ns

Notes: 1. See ordering information for valid part numbers.

2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

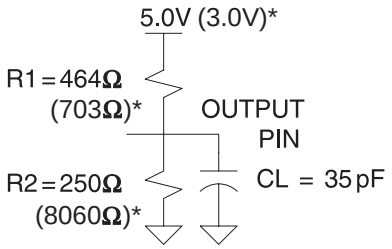
= Preliminary Information

Input Test Waveforms and Measurement Levels



t_R, t_F = 1.5 ns typical

Output AC Test Loads



Note: *Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

Power Down Mode

The ATF1504AS includes an optional pin controlled power down feature.When this mode is enabled, the PD pin acts as the power down pin. When the PD pin is high, the device supply current is reduced to less than 3 mA. During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in a Hi-Z state at the onset will remain at Hi-Z. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using the power down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power Down AC Characteristics(1)(2)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O Before PD High	7		10		15		20		25		ns
t_{GVDH}	Valid OE(2) Before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock(2) Before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care After PD High		12		15		25		30		35	ns
t_{DHGX}	OE(2) Don't Care After PD High		12		15		25		30		35	ns
t_{DHCX}	Clock(2) Don't Care After PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or Product Term.

= Preliminary Information

JTAG-BST/ISP Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary scan cell (BSC) in order to support boundary scan testing. The ATF1504AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504AS's ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504AS programming to be described and implemented using any one of the 3rd party development tools supporting this standard.

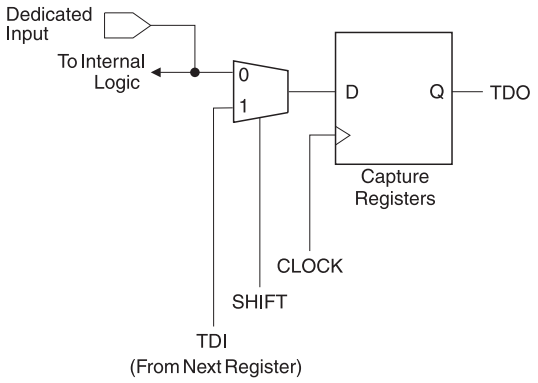
The ATF1504AS has the option of using four JTAG-standard I/O pins for boundary scan testing (BST) and in-system programming (ISP) purposes. The ATF1504AS is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary Scan Cell (BSC) Testing

The ATF1504AS contains up to 68 I/O pins and 4 input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary scan cell (BSC) in order to support boundary scan testing as described in detail by IEEE Standard 1149.1. Typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to

load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

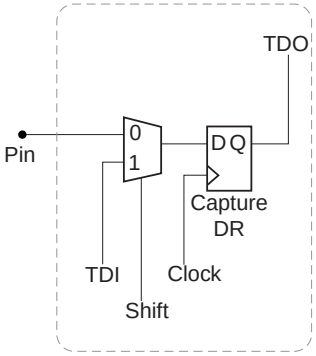
BSC Configuration for Input and I/O Pins (except JTAG TAP Pins)

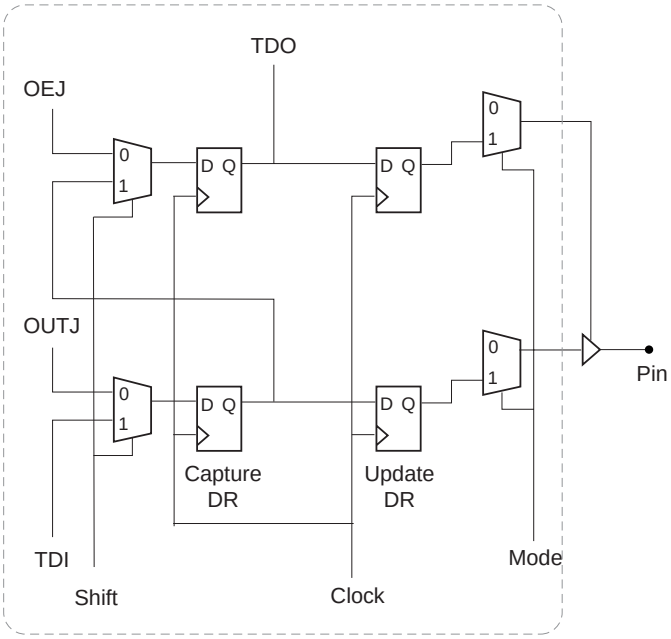


Note: The ATF1504AS has pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell

Pin BSC



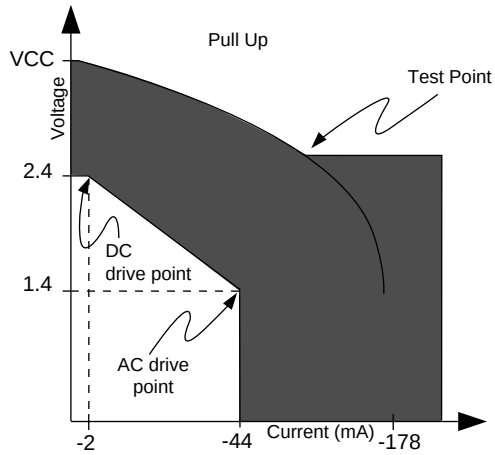


Macrocell BSC

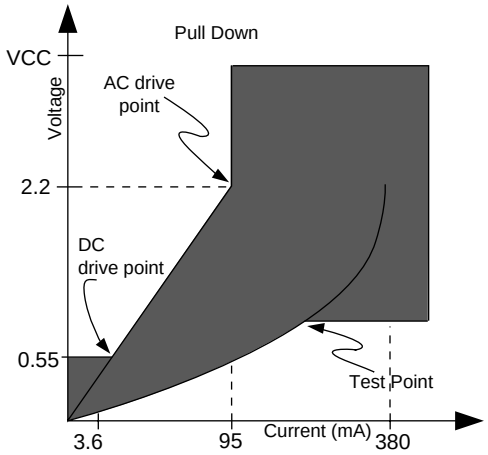
PCI Compliance

The ATF1504AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS allows this without contributing to system noise while delivering low output to output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance. The PCI electrical characteristics appear on the next page.

PCI Voltage-to-Current Curves for +5V Signaling in Pull-Up Mode



PCI Voltage-to-Current Curves for +5V Signaling in Pull-Down Mode



PCI DC Characteristics (Preliminary)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5V		-70	µA
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: Leakage Current is with Pin-Keeper off.

PCI AC Characteristics (Preliminary)

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching	$0 < V_{OUT} \leq 1.4$	-44		mA
	Current High	$1.4 < V_{OUT} < 2.4$	$-44+(V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
	(Test High)	V_{OUT} = 3.1V		-142	µA
$I_{OL(AC)}$	Switching	$V_{OUT} > 2.2V$	95		mA
	Current Low	$2.2 > V_{OUT} > 0$	$V_{OUT}/0.023$		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
	(Test Point)	V_{OUT} = 0.71		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25+(V_{IN} + 1)/0.015$		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V load	0.5	3	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V load	0.5	3	V/ns

Notes: 1. Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

ATF1504AS Dedicated Pinouts

Dedicated Pin	44-Pin TQFP	44-Pin J-Lead	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP
INPUT/OE2/GCLK2	40	2	2	2	92	90
INPUT/GCLR	39	1	1	1	91	89
INPUT/OE1	38	44	68	84	90	88
INPUT/GCLK1	37	43	67	83	89	87
I/O /GCLK3	35	41	65	81	87	85
I/O / PD (1,2)	5, 19	11, 25	17, 37	20, 46	14, 44	12, 42
I/O / TDI (JTAG)	1	7	12	14	6	4
I/O / TMS (JTAG)	7	13	19	23	17	15
I/O / TCK (JTAG)	26	32	50	62	64	62
I/O / TDO (JTAG)	32	38	57	71	75	73
GND	4, 16, 24, 36	10, 22, 30, 42	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86, 95
V_{CCINT}	9, 17, 29, 41	3, 15, 23, 35	3, 35	3, 43	41, 93	39, 91
V_{CCIO}	-	-	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	3, 18, 34, 51, 66, 82
N/C	-	-	-	-	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	52	68	68	68
# User I/O Pins	32	32	48	64	64	64

OE (1, 2)	Global OE Pins
GCLR	Global Clear Pin
GCLK (1, 2, 3)	Global Clock Pins
PD (1, 2)	Power down pins
TDI, TMS, TCK, TDO	JTAG pins used for Boundary Scan Testing or In-System Programming
GND	Ground Pins
V_{CCINT}	V_{CC} pins for the device (+5V - Internal)
V_{CCIO}	V_{CC} pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)

ATF1504AS I/O Pinouts

MC	PLC	44-Pin PLCC	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	MC	PLC	44-Pin PLCC	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP
1	A	12	6	18	22	16	14	33	C	24	18	36	44	42	40
2	A	-	-	-	21	15	13	34	C	-	-	-	45	43	41
3	A/ **PD1**	11	5	17	20	14	12	35	C/ **PD2**	25	19	37	46	44	42
4	A	9	3	15	18	12	10	36	C	26	20	39	48	46	44
5	A	8	2	14	17	11	9	37	C	27	21	40	49	47	45
6	A	-	-	13	16	10	8	38	C	-	-	41	50	48	46
7	A	-	-	-	15	8	6	39	C	-	-	-	51	49	47
8/ **TDI**	A	7	1	12	14	6	4	40	C	28	22	42	52	50	48
9	A	-	-	10	12	4	2	41	C	29	23	44	54	54	52
10	A	-	-	-	11	3	1	42	C	-	-	-	55	56	54
11	A	6	44	9	10	100	98	43	C	-	-	45	56	58	56
12	A	-	-	8	9	99	97	44	C	-	-	46	57	59	57
13	A	-	-	7	8	98	96	45	C	-	-	47	58	60	58
14	A	5	43	5	6	96	94	46	C	31	25	49	60	62	60
15	A	-	-	-	5	95	93	47	C	-	-	-	61	63	61
16	A	4	42	4	4	94	92	48/ **TCK**	C	32	26	50	62	64	62
17	B	21	15	33	41	39	37	49	D	33	27	51	63	65	63
18	B	-	-	-	40	38	36	50	D	-	-	-	64	66	64
19	B	20	14	32	39	37	35	51	D	34	28	52	65	67	65
20	B	19	13	30	37	35	33	52	D	36	30	54	67	69	67
21	B	18	12	29	36	34	32	53	D	37	31	55	68	70	68
22	B	-	-	28	35	33	31	54	D	-	-	56	69	71	69
23	B	-	-	-	34	32	30	55	D	-	-	-	70	73	71
24	B	17	11	27	33	31	29	56/ **TDO**	D	38	32	57	71	75	73
25	B	16	10	25	31	27	25	57	D	39	33	59	73	77	75
26	B	-	-	-	30	25	22	58	D	-	-	-	74	78	76
27	B	-	-	24	29	23	21	59	D	-	-	60	75	81	79
28	B	-	-	23	28	22	20	60	D	-	-	61	76	82	80
29	B	-	-	22	27	21	19	61	D	-	-	62	77	83	81
30	B	14	8	20	25	19	17	62	D	40	34	64	79	85	83
31	B	-	-	-	24	18	16	63	D	-	-	-	80	86	84
32/ **TMS**	B	13	7	19	23	17	15	64	D/ **GCLK3**	41	35	65	81	87	85

Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1504AS-7 AC44 ATF1504AS-7 JC44 ATF1504AS-7 JC68 ATF1504AS-7 JC84 ATF1504AS-7 QC100 ATF1504AS-7 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AC44 ATF1504AS-10 JC44 ATF1504AS-10 JC68 ATF1504AS-10 JC84 ATF1504AS-10 QC100 ATF1504AS-10 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AI44 ATF1504AS-10 JI44 ATF1504AS-10 JI68 ATF1504AS-10 JI84 ATF1504AS-10 QI100 ATF1504AS-10 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)
15	8	100	ATF1504AS-15 AC44 ATF1504AS-15 JC44 ATF1504AS-15 JC68 ATF1504AS-15 JC84 ATF1504AS-15 QC100 ATF1500AS-15 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
15	8	100	ATF1504AS-15 AI44 ATF1504AS-15 JI44 ATF1504AS-15 JI68 ATF1504AS-15 JI84 ATF1504AS-15 QI100 ATF1504AS-15 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

Package Type	
44A	44-Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68J	68-Lead, Plastic J-Leaded Chip Carrier (PLCC)
84J	84-Lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q1	100-Lead, Plastic Quad Flat Pack (PQFP)
100A	100-Lead, Thin Quad Flat Pack (TQFP)

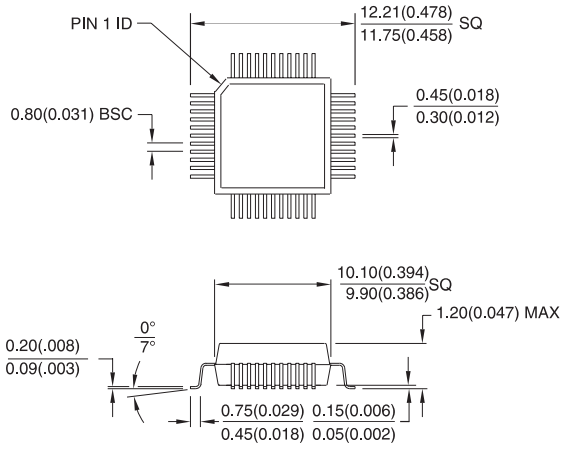
Ordering Information (Continued)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1504ASZ-20 AC44 ATF1504ASZ-20 JC44 ATF1504ASZ-20 JC68 ATF1504ASZ-20 JC84 ATF1504ASZ-20 QC100 ATF1504ASZ-20 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
25	15	70	ATF1504ASZ-25 AC44 ATF1504ASZ-25 JC84 ATF1504ASZ-25 JC68 ATF1504ASZ-25 JC84 ATF1504ASZ-25 QC100 ATF1504ASZ-25 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
25	15	70	ATF1504ASZ-25 AI44 ATF1504ASZ-25 JI84 ATF1504ASZ-25 JI68 ATF1504ASZ-25 JI84 ATF1504ASZ-25 QI100 ATF1504ASZ-25 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

Package Type	
44A	44-Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68J	68-Lead, Plastic J-Leaded Chip Carrier (PLCC)
84J	84-Lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q1	100-Lead, Plastic Quad Flat Pack (PQFP)
100A	100-Lead, Thin Quad Flat Pack (TQFP)

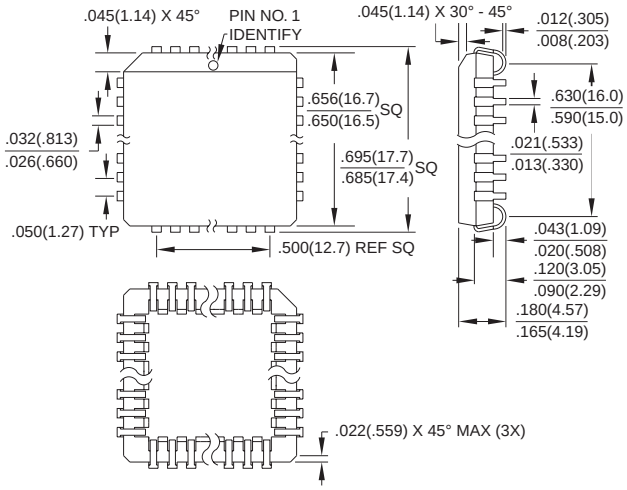
Packaging Information

44A, 44-Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

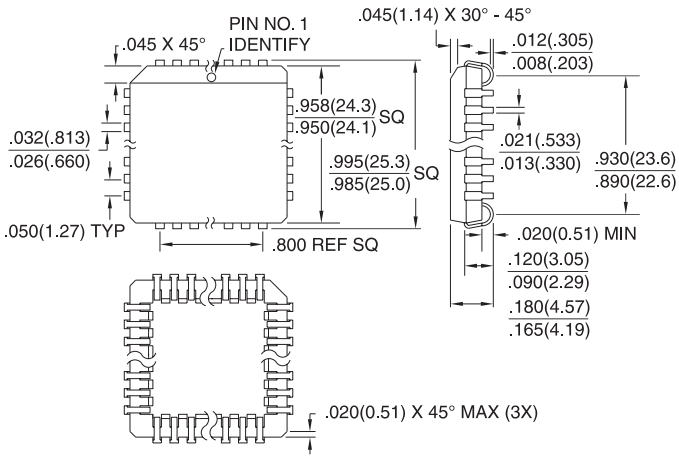


* Controlling dimension: millimeters

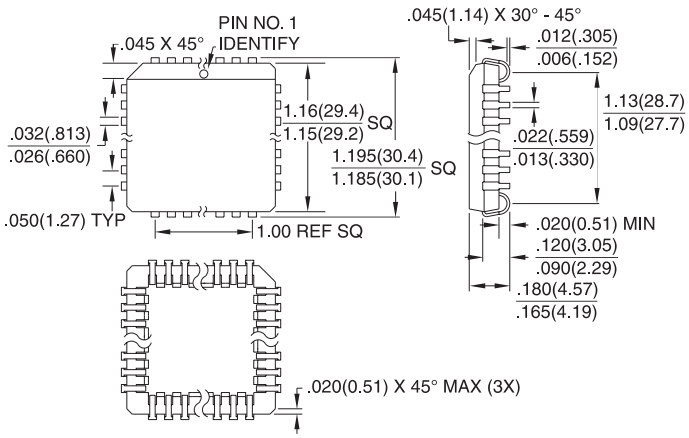
44J, 44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



68J, 68-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AE

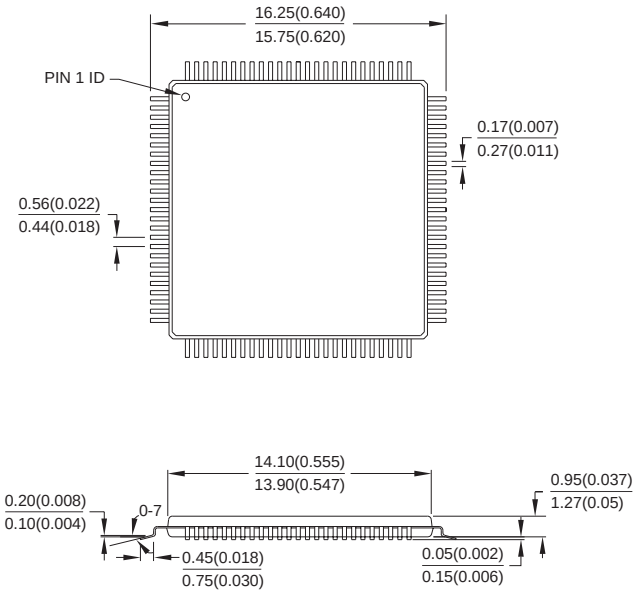


84J, 84-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AF



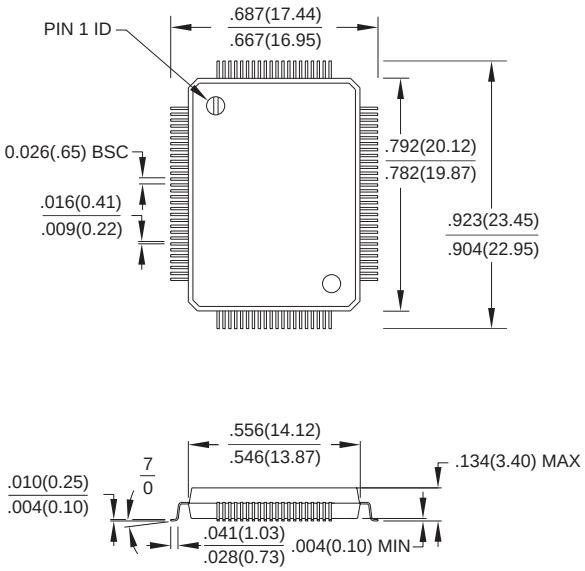
Packaging Information

100A, 100-Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

100Q1, 100-Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)



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