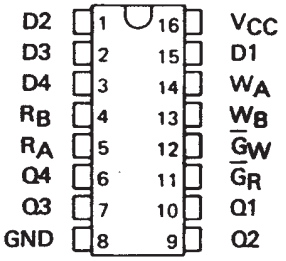
SN54170, SN54LS170, SN74170, SN74LS170
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

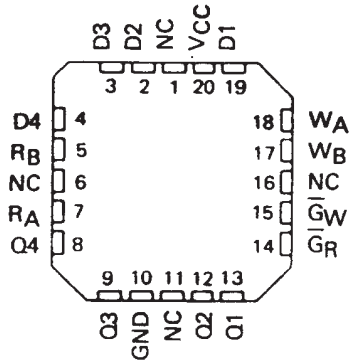
SDLS065 – MARCH 1974 – REVISED MARCH 1988

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
  - Scratch-Pad Memory
  - Buffer Storage between Processors
  - Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current:
  - '170 . . . 30 μA
  - 'LS170 . . . 20 μA
- SN54LS670 and SN74LS670 Are Similar But Have 3-State Outputs

SN54170, SN54LS170 . . . J OR W PACKAGE
SN74170 . . . N PACKAGE
SN74LS170 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS170 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

The '170 and 'LS170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $\overline{G}_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $\overline{G}_R$, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

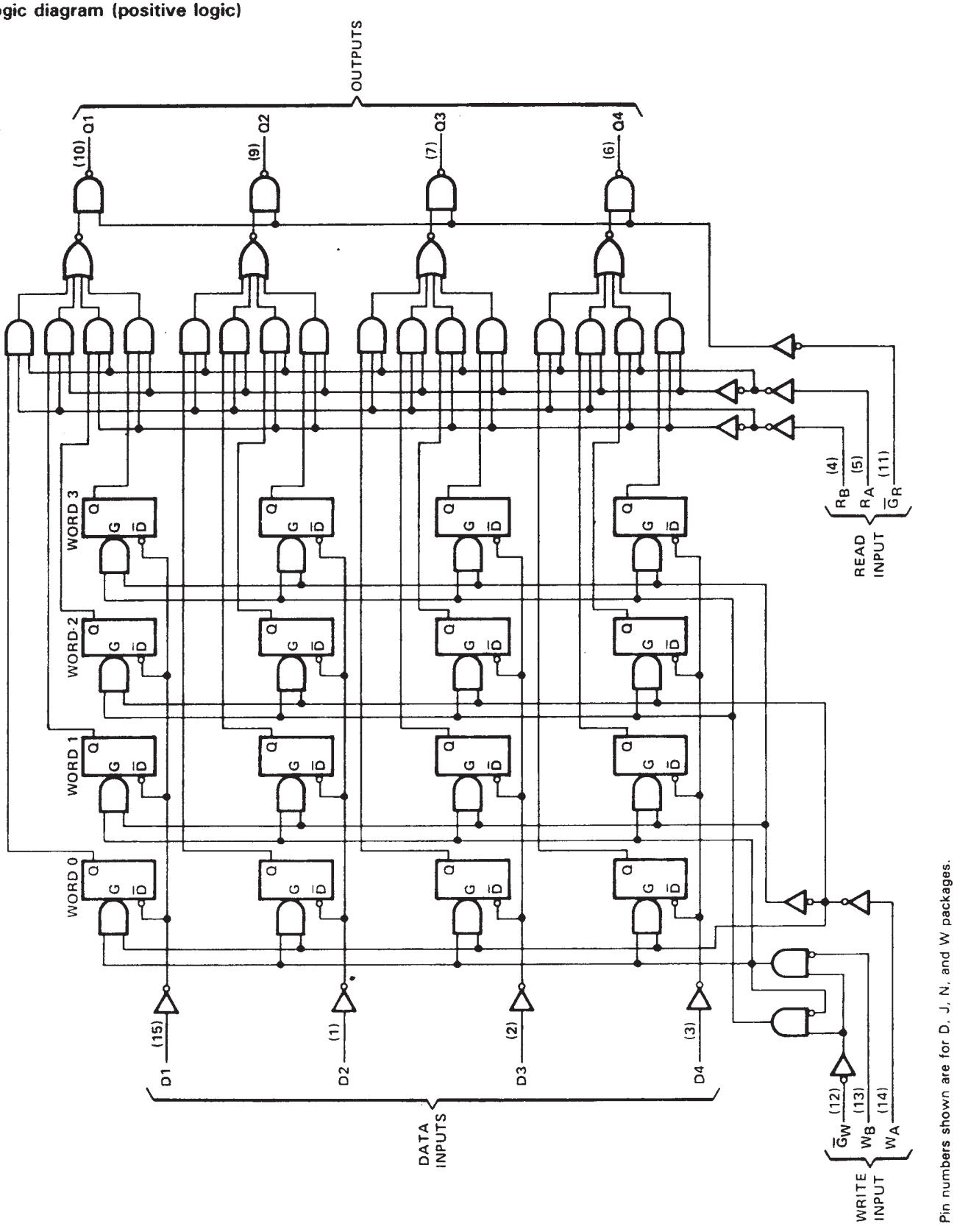
All '170 inputs and all inputs except the read enable and write enable of the 'LS170 are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54170 and SN54LS170 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 and SN74LS170 are characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

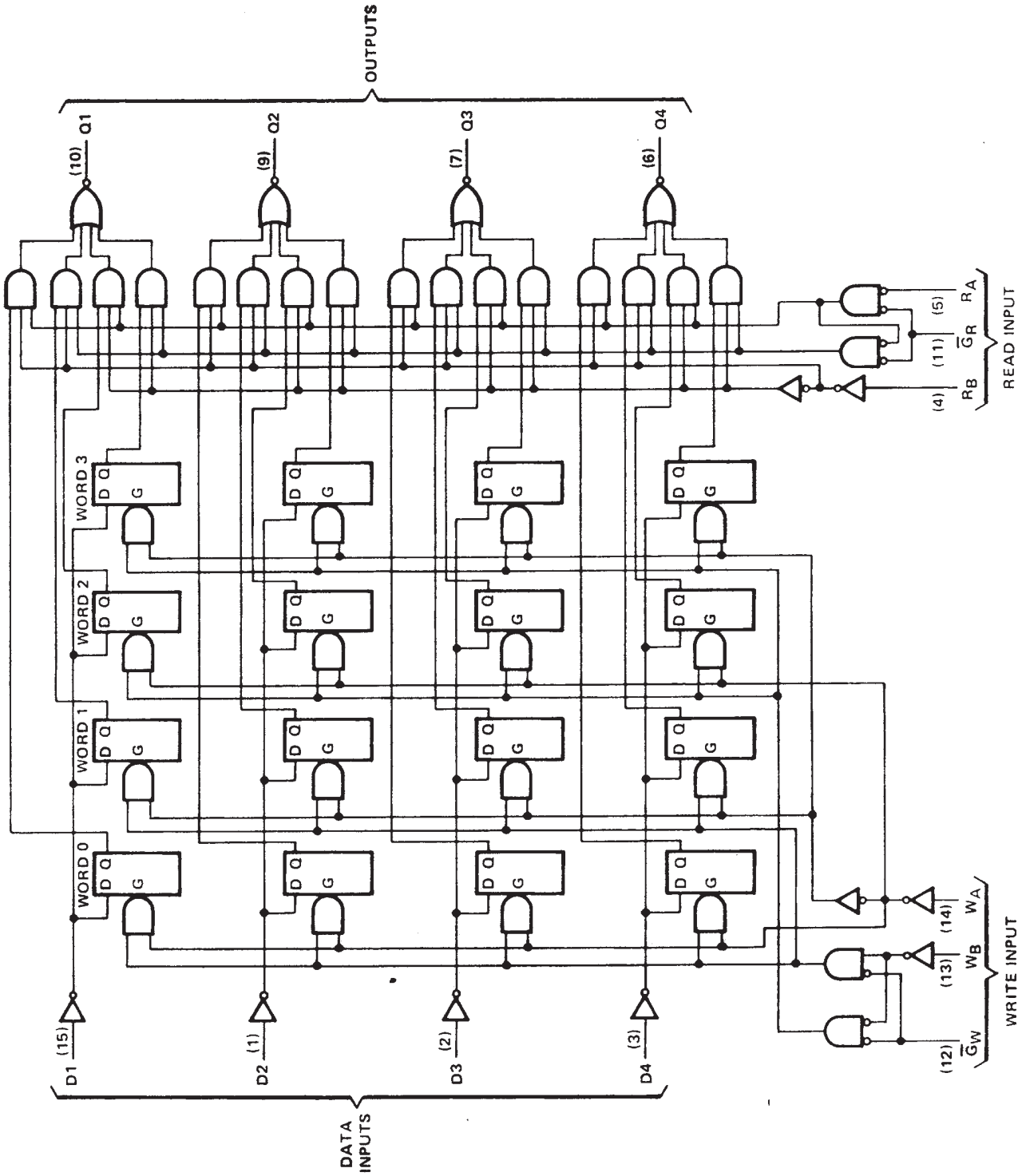
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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

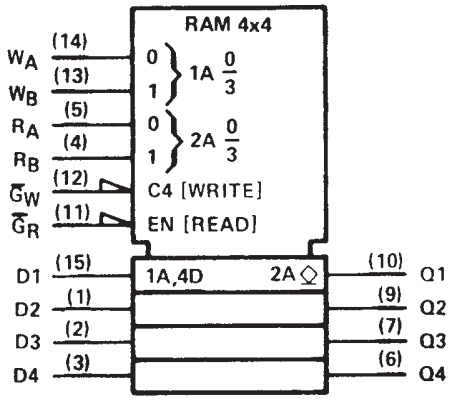
NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '170 . . . . . 5.5 V
'LS170 . . . . . 7 V
Off-state output voltage: '170 . . . . . 5.5 V
'LS170 . . . . . 7 V
Operating free-air temperature range: SN54170, SN54LS170 (see Note 2) . . . . . −55°C to 125°C
SN74170, SN74LS170 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W

logic symbols†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A (see Note 2)		−55		125	0		70	°C

NOTES: 2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W.

3. Write select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V				30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 5	SN54170		127§	140	mA
			SN74170		127§	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Typical supply current shown is an average for 50% duty cycle.
NOTE 5: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

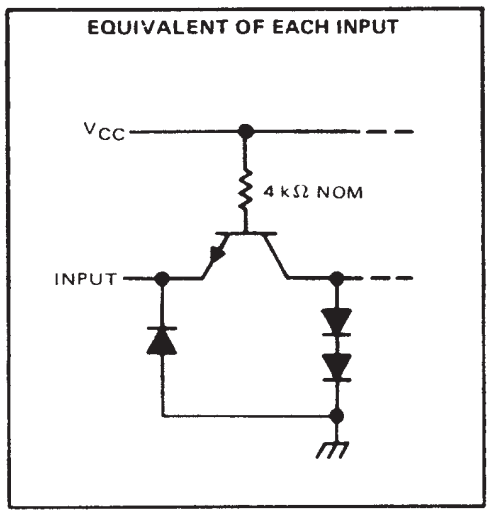
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2		10	15	ns
t_{PHL}					20	30	
t_{PLH}	Read Select	Any Q			23	35	ns
t_{PHL}					30	40	
t_{PLH}	Write enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 3		25	40	ns
t_{PHL}					34	45	
t_{PLH}	Data	Any Q			20	30	ns
t_{PHL}					30	45	

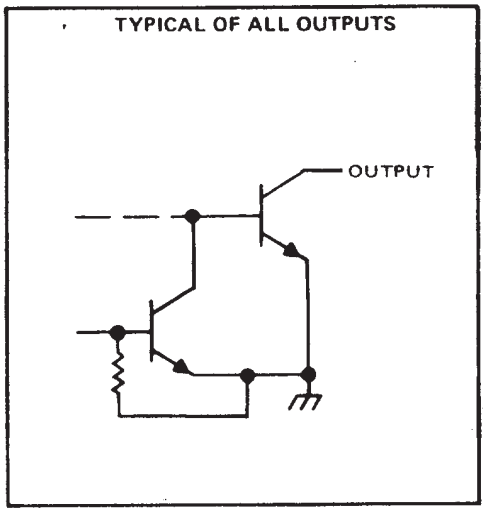
†t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

schematics of inputs and outputs

'170



'170



recommended operating conditions

		SN54LS170			SN74LS170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS170			SN74LS170			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{OH} = 5.5 V, V_{IH} = 2 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any D, R, or W	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		$\overline{G}_R$ or $\overline{G}_W$					0.2			0.2	
I_{IH}	High-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		$\overline{G}_R$ or $\overline{G}_W$					40			40	
I_{IL}	Low-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		$\overline{G}_R$ or $\overline{G}_W$					−0.8			−0.8	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 5		25	40		25	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 5: I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are ground, and all outputs are open.

recommended operating conditions

		SN54LS170			SN74LS170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS170			SN74LS170			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{OH} = 5.5 V, V_{IH} = 2 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any D, R, or W	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		$\overline{G}_R$ or $\overline{G}_W$					0.2			0.2	
I_{IH}	High-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		$\overline{G}_R$ or $\overline{G}_W$					40			40	
I_{IL}	Low-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		$\overline{G}_R$ or $\overline{G}_W$					−0.8			−0.8	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 5		25	40		25	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 5: I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are ground, and all outputs are open.

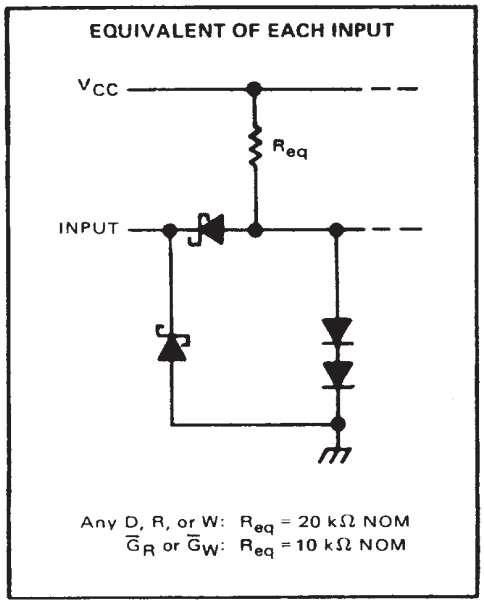
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Read select	Any Q			25	40	ns
t_{PHL}					24	40	
t_{PLH}	Write enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 3		30	45	ns
t_{PHL}					26	40	
t_{PLH}	Data	Any Q			30	45	ns
t_{PHL}					22	35	

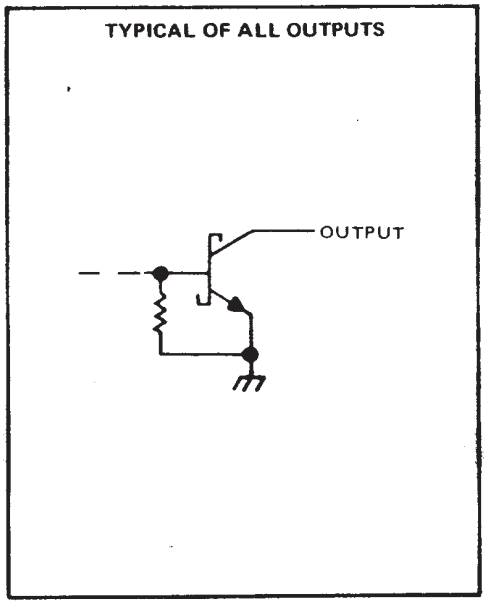
†t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

schematics of inputs and outputs

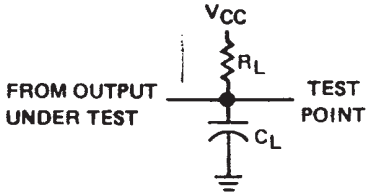
'LS170



'LS170



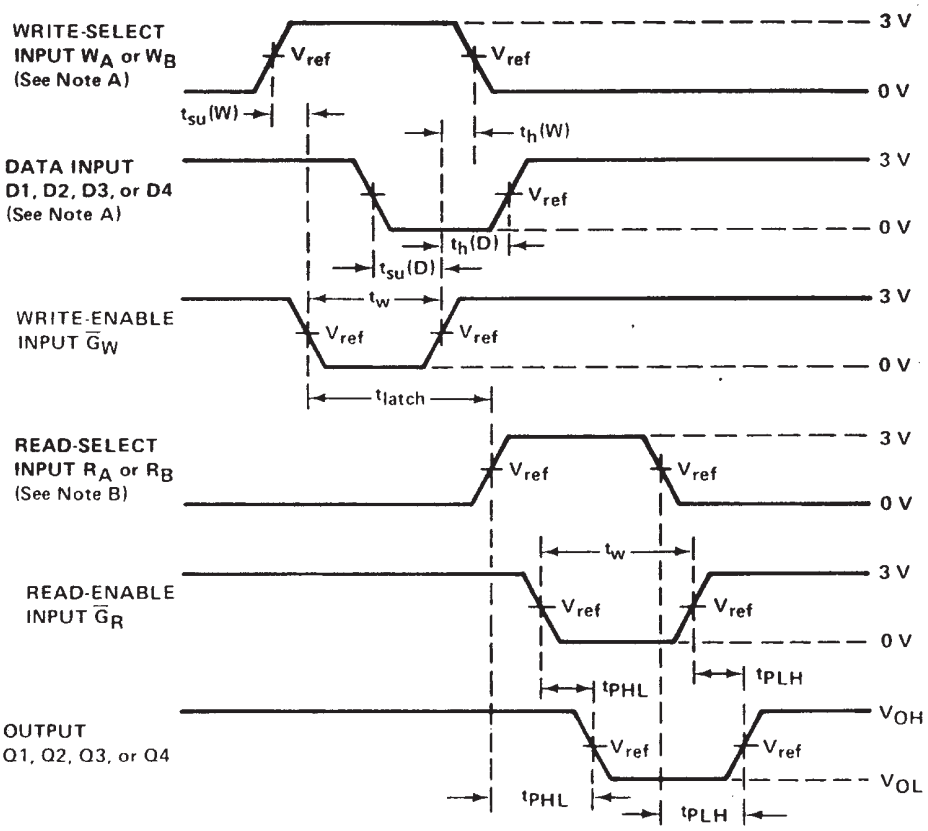
PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance

LOAD CIRCUIT

FIGURE 1

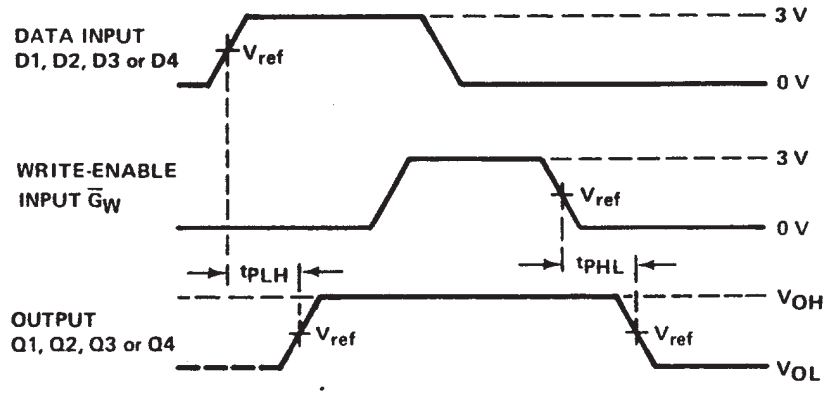


VOLTAGE WAVEFORMS

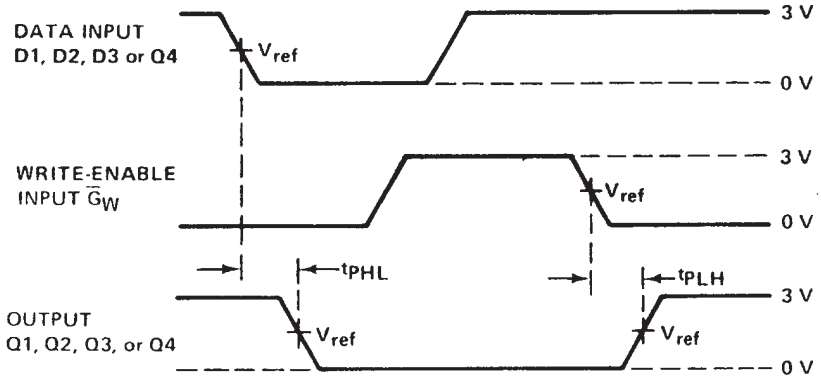
FIGURE 2

NOTES:
A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
C. In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stablized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
D. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 10$ ns and $t_f \leq 10$ ns for '170, and $t_r \leq 15$ ns and $t_f \leq 6$ ns for 'LS170.
E. For '170, $V_{ref} = 1.5$ V; for 'LS170, $V_{ref} = 1.3$ V.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM 1



VOLTAGE WAVEFORM 2

FIGURE 3

NOTES: A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

D. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 10$ ns and $t_f \leq 10$ ns for '170, and $t_r \leq 15$ ns and $t_f \leq 6$ ns for 'LS170.

E. For '170, $V_{ref} = 1.5$ V; for 'LS170, $V_{ref} = 1.3$ V.

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
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Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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8002501FA	OBSOLETE			16		TBD	Call TI	Call TI
SN54LS170J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS170J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74170N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74170N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS170D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS170D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS170N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS170N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54LS170J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54LS170J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54LS170W	OBSOLETE			16		TBD	Call TI	Call TI
SNJ54LS170W	OBSOLETE			16		TBD	Call TI	Call TI

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

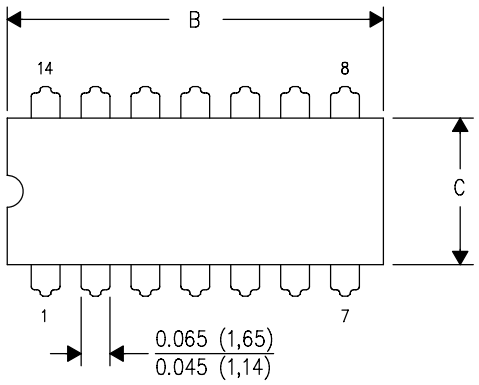
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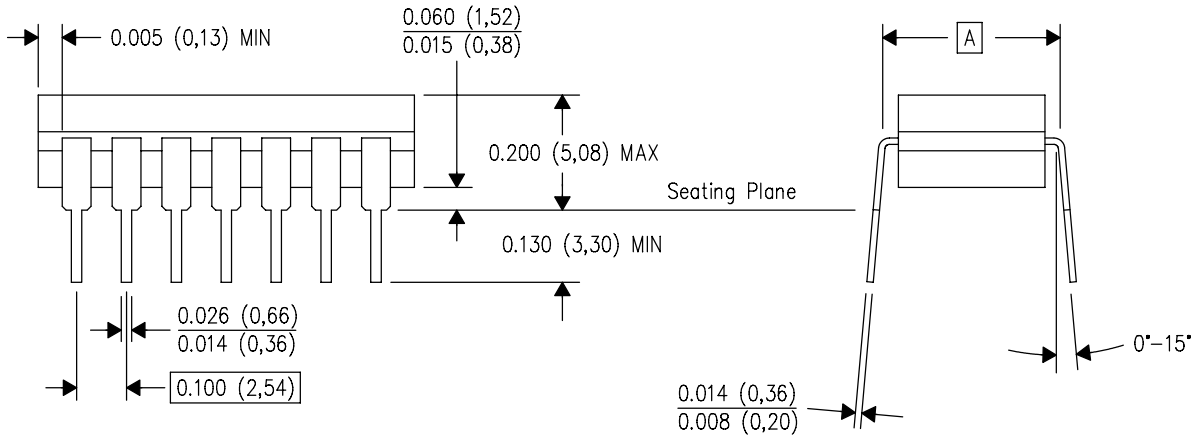
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



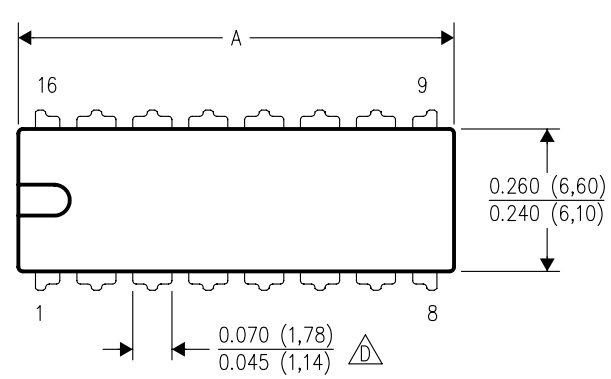
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

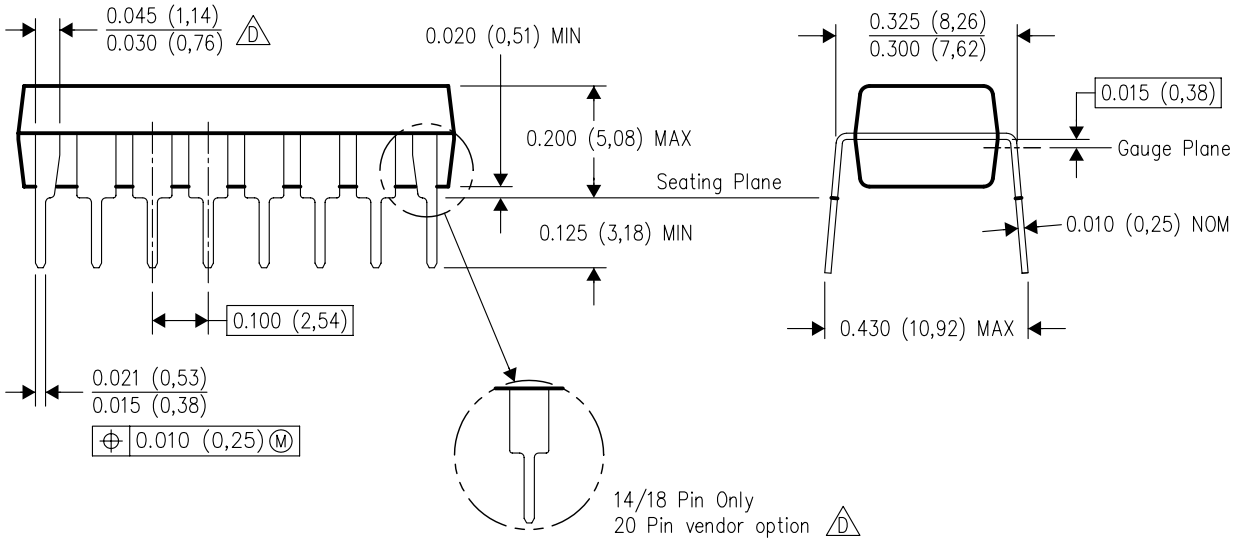
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



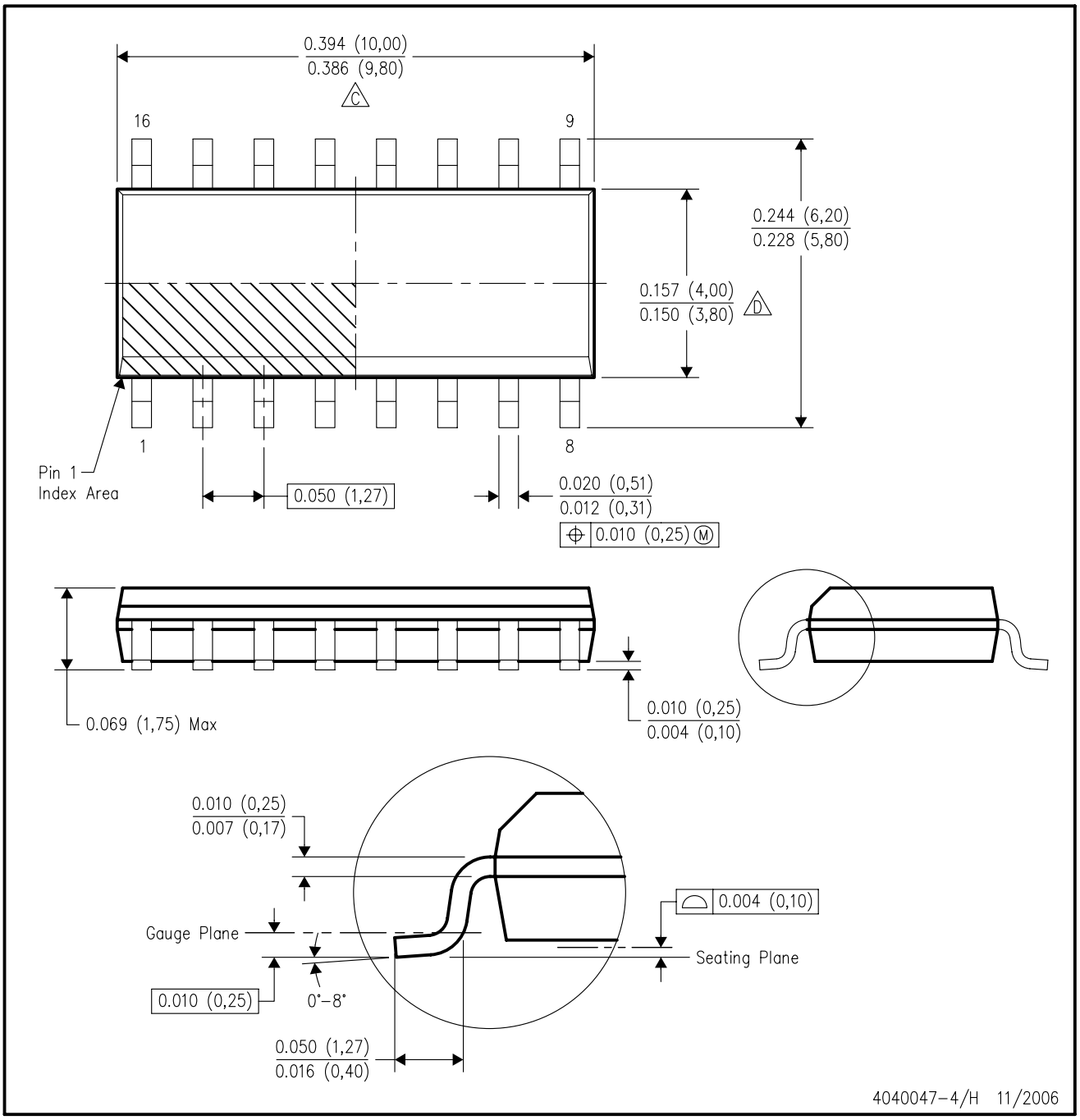
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

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ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
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