

# FDS7064A

## 30V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

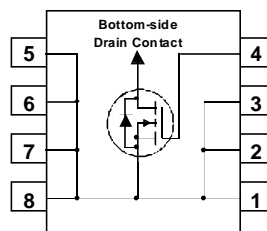
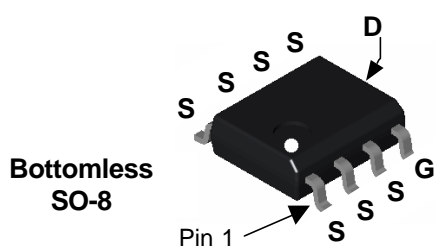
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low  $R_{DS(ON)}$  in a small package.

### Applications

- Synchronous rectifier
- DC/DC converter

### Features

- 19 A, 30 V  $R_{DS(ON)} = 6.5 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability
- Fast switching
- Bottomless™ SO-8 package: Enhanced thermal performance in industry-standard package size



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a)	19	A
	– Pulsed	60	
$P_D$	Power Dissipation for Single Operation (Note 1a)	3.9	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	38	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7064A	FDS7064A	13"	12mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		20		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.8	1.2	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 21\text{ A}$			6.5 5.5	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	50			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 19\text{ A}$		75		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		5070		pF
$C_{oss}$	Output Capacitance			550		pF
$C_{rss}$	Reverse Transfer Capacitance			230		pF

**Switching Characteristics (Note 2)**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		17	25	ns
$t_r$	Turn–On Rise Time			18	25	ns
$t_{d(off)}$	Turn–Off Delay Time			69	100	ns
$t_f$	Turn–Off Fall Time			29	42	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 19\text{ A},$ $V_{GS} = 4.5\text{ V}$		33	46	nC
$Q_{gs}$	Gate–Source Charge			7.5		nC
$Q_{gd}$	Gate–Drain Charge			6.8		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

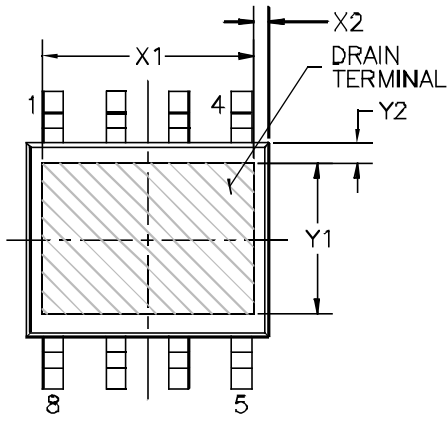
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.2\text{ A}$ (Note 2)			1.2	V

**Notes:**

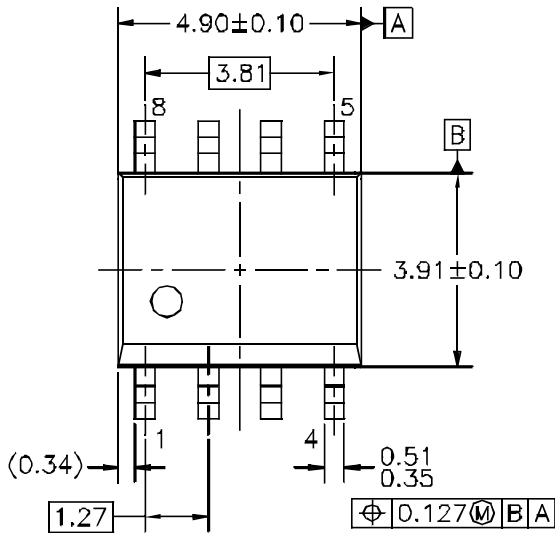
1.  $R_{\theta JA}$  is the junction-to-ambient thermal resistance.  $R_{\theta JA}$  depends on the user's board design.

a)  $38^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

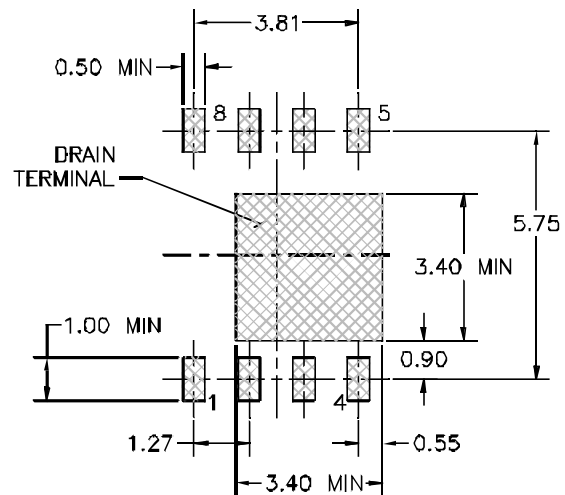
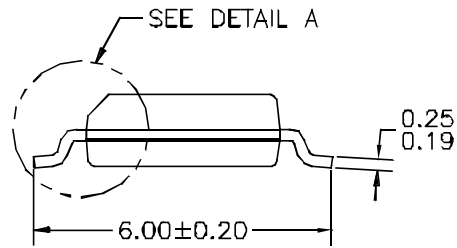
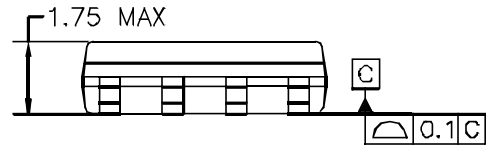
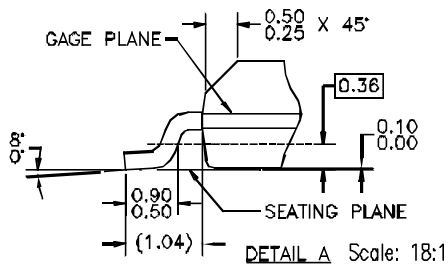
### Dimensional Outline and Pad Layout



**Bottom View**



**Top View**



### Minimum Recommended Landing Pattern

**Notes** Unless otherwise Specified

- a) All dimensions in mm
- b) Standard lead finish:  
20 – 80 μ inches nickel /  
6 μ inches palladium
- c) Chip Size Dimensional Table

Chip Size		X2	Y2
X1	Y1		
2.36	2.36	0.75	0.67

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