

# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32$ -mA  $I_{OH}$ ,  $64$ -mA  $I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

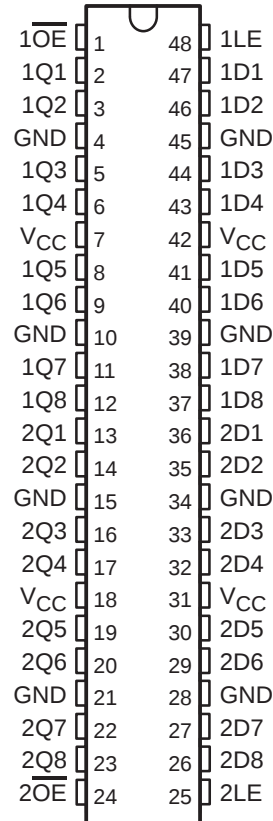
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16373A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT16373A . . . WD PACKAGE  
SN74ABT16373A . . . DGG OR DL PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

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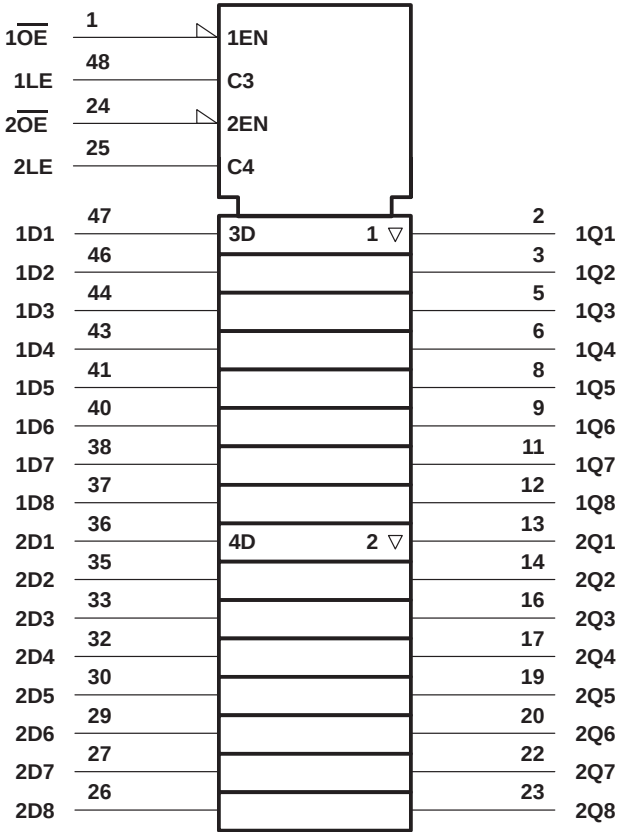
SN54ABT16373A, SN74ABT16373A  
 16-BIT TRANSPARENT D-TYPE LATCHES  
 WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
 (each 8-bit section)

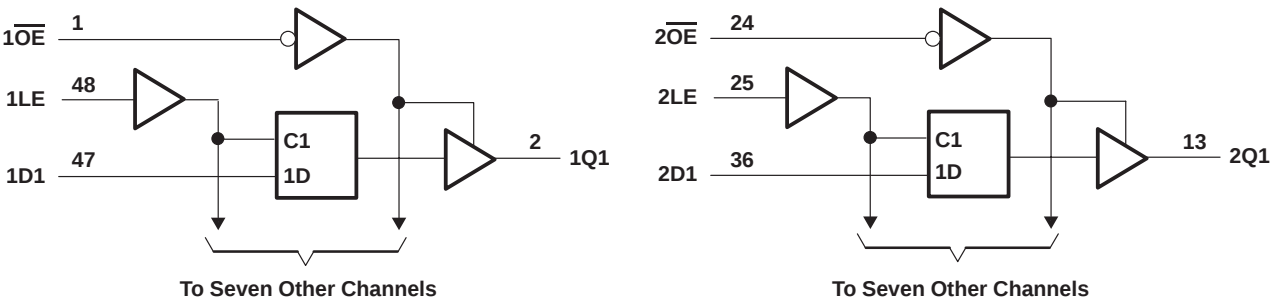
| INPUTS          |    |   | OUTPUT<br>Q    |
|-----------------|----|---|----------------|
| $\overline{OE}$ | LE | D |                |
| L               | H  | H | H              |
| L               | H  | L | L              |
| L               | L  | X | Q <sub>0</sub> |
| H               | X  | X | Z              |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT16373A           | 96 mA           |
| SN74ABT16373A                                                             | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package        | 89°C/W          |
| DL package                                                                | 94°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

|                          |                                    | SN54ABT16373A   |          | SN74ABT16373A |          | UNIT |
|--------------------------|------------------------------------|-----------------|----------|---------------|----------|------|
|                          |                                    | MIN             | MAX      | MIN           | MAX      |      |
| $V_{CC}$                 | Supply voltage                     | 4.5             | 5.5      | 4.5           | 5.5      | V    |
| $V_{IH}$                 | High-level input voltage           | 2               |          | 2             |          | V    |
| $V_{IL}$                 | Low-level input voltage            |                 | 0.8      |               | 0.8      | V    |
| $V_I$                    | Input voltage                      | 0               | $V_{CC}$ | 0             | $V_{CC}$ | V    |
| $I_{OH}$                 | High-level output current          |                 | –24      |               | –32      | mA   |
| $I_{OL}$                 | Low-level output current           |                 | 48       |               | 64       | mA   |
| $\Delta t/\Delta v$      | Input transition rise or fall rate | Outputs enabled |          |               | 10       | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200             |          | 200           |          | μs/V |
| $T_A$                    | Operating free-air temperature     | –55             | 125      | –40           | 85       | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# SN54ABT16373A, SN74ABT16373A

## 16-BIT TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER           | TEST CONDITIONS                                                                     | T <sub>A</sub> = 25°C                           |      |       | SN54ABT16373A |      | SN74ABT16373A |      | UNIT |
|---------------------|-------------------------------------------------------------------------------------|-------------------------------------------------|------|-------|---------------|------|---------------|------|------|
|                     |                                                                                     | MIN                                             | TYP† | MAX   | MIN           | MAX  | MIN           | MAX  |      |
| V <sub>IK</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA                                    |                                                 |      | –1.2  |               | –1.2 |               | –1.2 | V    |
| V <sub>OH</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA                                    | 2.5                                             |      |       | 2.5           |      | 2.5           |      | V    |
|                     | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA                                      | 3                                               |      |       | 3             |      | 3             |      |      |
|                     | V <sub>CC</sub> = 4.5 V                                                             | I <sub>OH</sub> = –24 mA                        | 2    |       | 2             |      |               |      |      |
|                     |                                                                                     | I <sub>OH</sub> = –32 mA                        | 2*   |       |               |      | 2             |      |      |
| V <sub>OL</sub>     | V <sub>CC</sub> = 4.5 V                                                             | I <sub>OL</sub> = 48 mA                         |      | 0.55  |               | 0.55 |               |      | V    |
|                     |                                                                                     | I <sub>OL</sub> = 64 mA                         |      | 0.55* |               |      |               | 0.55 |      |
| V <sub>hys</sub>    |                                                                                     |                                                 | 100  |       |               |      |               |      | mV   |
| I <sub>I</sub>      | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND               |                                                 |      | ±1    |               | ±1   |               | ±1   | μA   |
| I <sub>OZPU</sub> ‡ | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |                                                 |      | ±50   |               | ±50  |               | ±50  | μA   |
| I <sub>OZPD</sub> ‡ | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |                                                 |      | ±50   |               | ±50  |               | ±50  | μA   |
| I <sub>OZH</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V  |                                                 |      | 10    |               | 10   |               | 10   | μA   |
| I <sub>OZL</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V  |                                                 |      | –10   |               | –10  |               | –10  | μA   |
| I <sub>off</sub>    | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                       |                                                 |      | ±100  |               |      |               | ±100 | μA   |
| I <sub>CEX</sub>    | Outputs high                                                                        | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V |      | 50    |               | 50   |               | 50   | μA   |
| I <sub>O</sub> §    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                     | –50                                             | –100 | –180  | –50           | –180 | –50           | –180 | mA   |
| I <sub>CC</sub>     | Outputs high                                                                        |                                                 |      | 2     |               | 2    |               | 2    | mA   |
|                     | Outputs low                                                                         |                                                 |      | 85    |               | 85   |               | 85   |      |
|                     | Outputs disabled                                                                    |                                                 |      | 2     |               | 2    |               | 2    |      |
| ΔI <sub>CC</sub> ¶  | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND |                                                 |      | 1.5   |               | 1.5  |               | 1.5  | mA   |
| C <sub>i</sub>      | V <sub>I</sub> = 2.5 V or 0.5 V                                                     |                                                 |      | 3.5   |               |      |               |      | pF   |
| C <sub>O</sub>      | V <sub>O</sub> = 2.5 V or 0.5 V                                                     |                                                 |      | 9.5   |               |      |               |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

|                 |                             | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C# |     | SN54ABT16373A |     | SN74ABT16373A |     | UNIT |
|-----------------|-----------------------------|-----------------------------------------------|-----|---------------|-----|---------------|-----|------|
|                 |                             | MIN                                           | MAX | MIN           | MAX | MIN           | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high     | 3.3                                           |     | 3.3           |     | 3.3           |     | ns   |
| t <sub>su</sub> | Setup time, data before LE↓ | 1.5                                           |     | 2.4           |     | 1.5           |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE↓   | 1                                             |     | 2.2           |     | 1             |     | ns   |

# These values apply only to the SN74ABT16373A.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54ABT16373A                                   |     |     |     |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                 |                | MIN                                             | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | D               | Q              | 1.4                                             | 3.7 | 5.3 | 1.4 | 6.5 | ns   |
| t <sub>PHL</sub> |                 |                | 2                                               | 4   | 5.4 | 2   | 6.5 |      |
| t <sub>PLH</sub> | LE              | Q              | 1.7                                             | 4.1 | 5.7 | 1.7 | 7   | ns   |
| t <sub>PHL</sub> |                 |                | 2.3                                             | 4.3 | 5.6 | 2.3 | 6.3 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Q              | 1.1                                             | 3.4 | 5   | 1.1 | 6.4 | ns   |
| t <sub>PZL</sub> |                 |                | 1.5                                             | 3.5 | 4.9 | 1.5 | 5.8 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Q              | 2.4                                             | 5.1 | 7.1 | 2.4 | 8.3 | ns   |
| t <sub>PLZ</sub> |                 |                | 1.6                                             | 4.4 | 6.3 | 1.6 | 8   |      |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN74ABT16373A                                   |     |     |     |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                 |                | MIN                                             | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | D               | Q              | 1.4                                             | 3.7 | 5.3 | 1.4 | 6.3 | ns   |
| t <sub>PHL</sub> |                 |                | 2                                               | 4   | 5.4 | 2   | 6.2 |      |
| t <sub>PLH</sub> | LE              | Q              | 1.7                                             | 4.1 | 5.7 | 1.7 | 6.7 | ns   |
| t <sub>PHL</sub> |                 |                | 2.3                                             | 4.3 | 5.6 | 2.3 | 6.1 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Q              | 1.1                                             | 3.4 | 5   | 1.1 | 6.1 | ns   |
| t <sub>PZL</sub> |                 |                | 1.5                                             | 3.5 | 4.9 | 1.5 | 5.6 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Q              | 2.4                                             | 5.1 | 7.1 | 2.4 | 8.1 | ns   |
| t <sub>PLZ</sub> |                 |                | 1.6                                             | 4.4 | 5.8 | 1.6 | 6.5 |      |

# SN54ABT16373A, SN74ABT16373A

## 16-BIT TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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