National Semiconductor

ADVANCE INFORMATION
May 2003

FPD94128
528-Ch Small Format a-Si AMLCD Controller / Column Driver with Integrated Frame Buffer

General Description

The FPD94128 is a Controller/Column Driver for use in low-power small format color TFT LCD displays. The FPD94128 contains a frame buffer, display refresh controller, programmable gamma reference, 528-channel column driver, and a backlight intensity modulator. The FPD94128 and the companion FPD93140 (gate driver with power supply) form a complete 2-chip solution for driving TFT LCD panels containing up to 176RGB x 240 pixels with versatile mounting and scan options. 262,144 colors are supported in 18-bit color mode, and 12-bit, 9-bit, and 3-bit color modes are provided for reduced power. Data may be loaded via serial, 8/16-bit parallel, and video interfaces (18-bit NTSC R'G'B' or 8/16-bit BT.601 4:2:2 Y'CbCr).

The video frame rate and the refresh rate of the LCD panel are independent. The LCD panel refresh rate and the polarity inversion interval are programmable. The LCD panel refresh rate may be up to 125 fps. Two partial-display regions, reduced-color modes, and an automatic backlight control are provided to minimize total system power consumption. The FPD94128 requires no external components.

Parts are provided as gold bumped flip-chip devices. The nominal range for VDD is [1.8V-3.3] V, and the nominal range for the LCD drive voltage is [3.3-5.5] V.

Features

- Video port accepts 18-bit video (NTSC R'G'B') or 8/16-bit video (BT.601 Y'CbCr 4:2:2) at up to 150 QCIF fps (4 Mpix/s).
- CPU port accepts packed graphics data (1.1.1, 3.3.2, 4.4.4, 5.6.5, 6.6.6 RGB) via SPI or parallel 8/16-bit (80x/68x) interfaces
- Internal frame buffer supports up to 176RGB x 240 (18-bit pixels).
- Flexible mounting/scan options provide for symmetric display layout
- Programmable for smaller display resolutions such as 176RGB x 220, 144RGB x 176, 132RGB x 176, etc.
- No external components.
- Quiescent power ~2.5mW in 18-bit mode
- Programmable color-depth allows selection of 3, 9, 12, or 18-bit color modes to further reduce power.
- Power-saving automatic backlight intensity reduction based on statistics of image data or by direct system control.
- Two-region partial display option for ultra-low power in handset stand-by mode.
- Frame, line, or n-line inversion modes.
- Programmable gamma curve control allows easy adjustment for optimum gray level placement and minimum flicker.
- Programmable line rate supports up to 125Hz display refresh rate.
- Separate addressing of two memory regions allows simultaneous loading of both streaming video and graphic/icon data
- Versatile auto-increment addressing modes allow horizontal or vertical raster scanning.
- Factory-calibrated internal clock provides accurate refresh control with no external components.

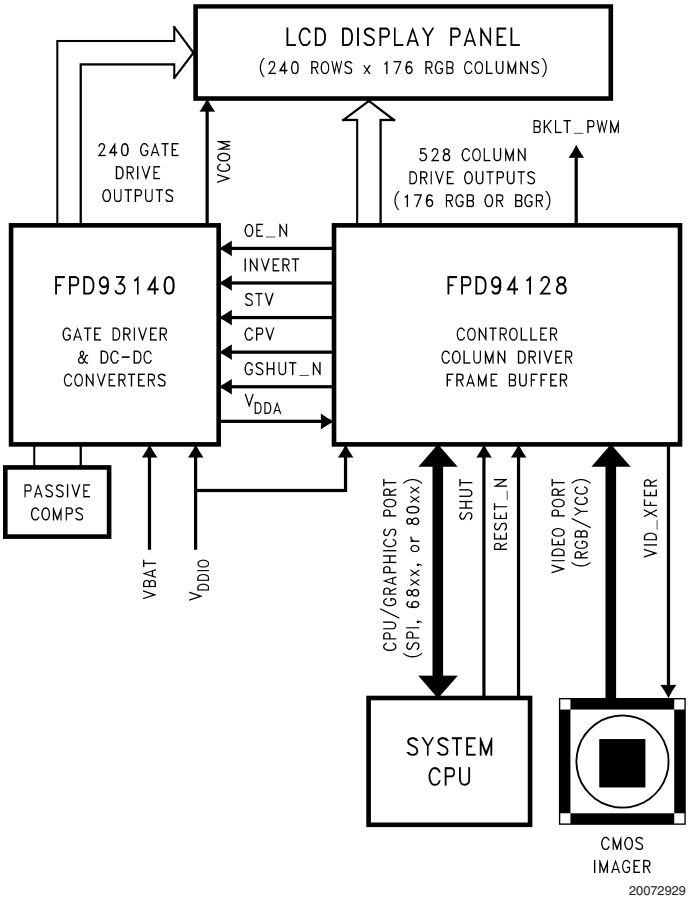
Ordering Information

NSID	Function	Package
FPD93140	Gate Driver (see Datasheet)	COG
FPD94128	Column Driver	COG

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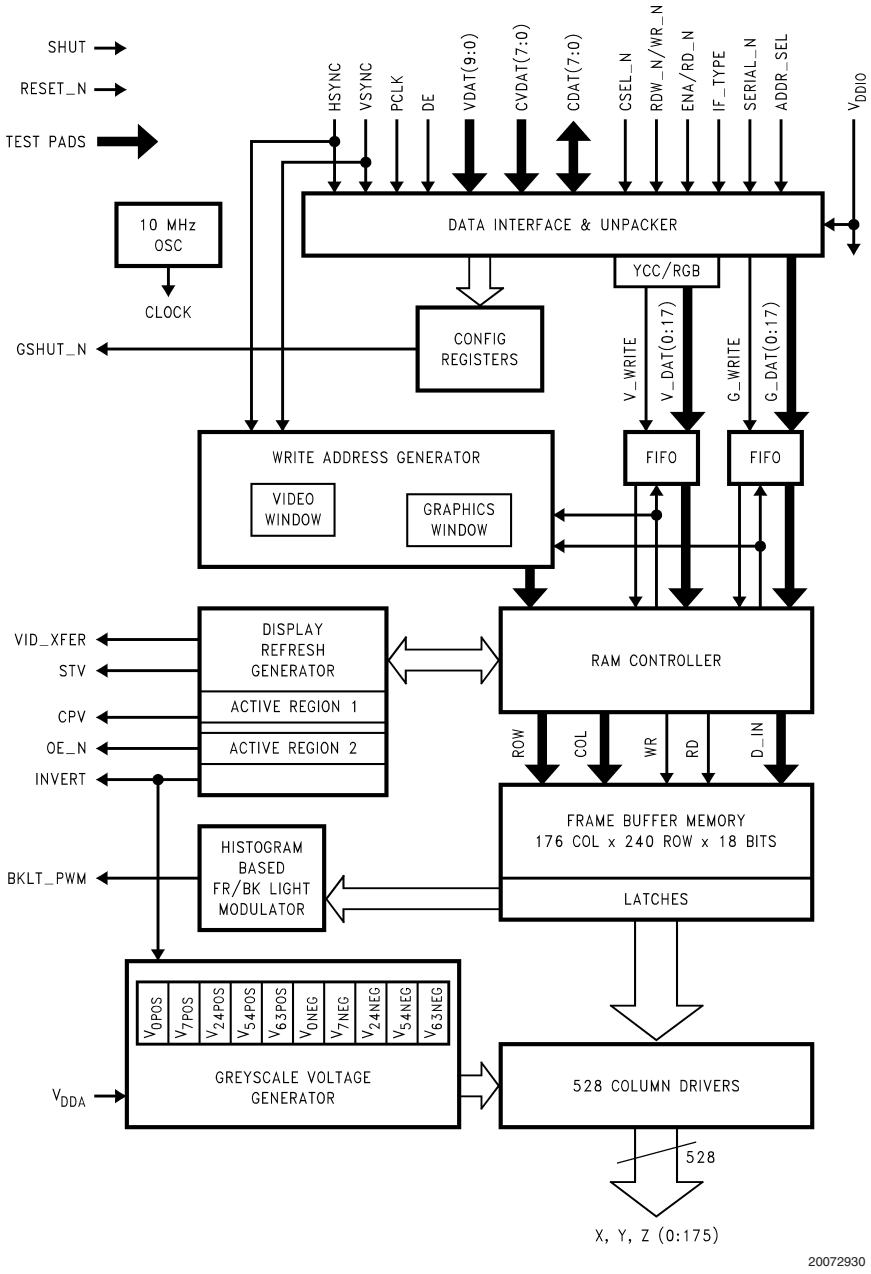
Block Diagrams

Typical Application



Block Diagrams (Continued)

FPD94128 Block Diagram



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Notes

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