DS1384
Watchdog Timekeeping Controller

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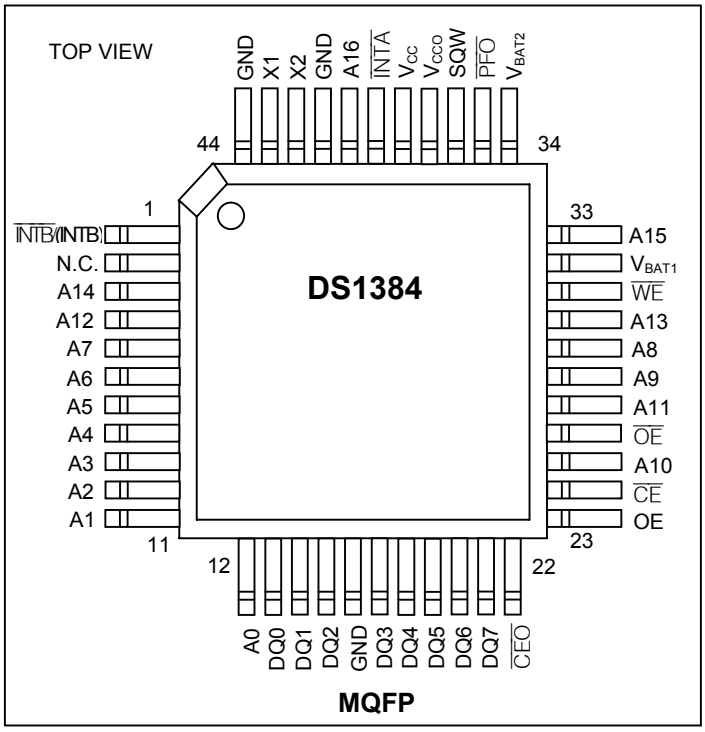
FEATURES

- **Keeps Track of Hundredths of Seconds, Seconds, Minutes, Hours, Days, Date of the Month, Months, and Years with Leap Year Compensation Valid Up to 2100**
- **Watchdog Timer Restarts an Out-of-Control Processor**
- **Alarm Function Schedules Real-Time Related Activities**
- **Programmable Interrupts and Square-Wave Outputs**
- **Bytewide RAM-Like Access**
- **50 Bytes of On-Board User RAM**
- **Greater Than 10 Years Timekeeping and Data Retention in the Absence of Power with Small Lithium Coin Cells**
- **Supports Up to 128k x 8 of External Static RAM**
- **All Timekeeping Registers and On-Board RAM are Individually Addressable via the Address and Data Bus**

PIN CONFIGURATION



ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1384FP-12	0°C to +70°C	5.0	44 MQFP	DS1384FP
DS1384FP-12+	0°C to +70°C	5.0	44 MQFP	DS1384FP

+ Denotes lead-free/RoHS-compliant device.
** A "+" anywhere on the top mark indicates a lead-free/RoHS-compliant device.*

DETAILED DESCRIPTION

The DS1384 watchdog timekeeping controller is a self-contained real-time clock, alarm, watchdog timer, and interval timer that provides control of up to 128k x 8 of external low-power CMOS static RAM in a 44-pin quad flat-pack package. An external crystal and battery are the only components required to maintain time of day and RAM memory contents in the absence of power. Access to all RTC functions and the external RAM is the same as conventional bytewide SRAM. Data is maintained in the watchdog timekeeper by intelligent control circuitry, which detects the status of V_{CC} and write protects both memory and timekeeping functions when V_{CC} is out of tolerance. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap year. The timekeeper operates in either 12- or 24-hour format with an AM/PM indicator. The watchdog internal timer provides watchdog alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. All the RTC functions and the internal 50 bytes of RAM reside in the lower 64 bytes of the attached RAM memory map. The externally attached static RAM is controlled by the DS1384 via the $\overline{OER}$ and $\overline{CEO}$ signals.

Automatic backup and write protection for an external SRAM is provided through the V_{CCO}, $\overline{CEO}$, and $\overline{OER}$ pins. The lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{CCO} pin. The chip enable output to RAM ($\overline{CEO}$) and the output enable to RAM ($\overline{OER}$) are controlled during power transients to prevent data corruption. The DS1384 is a complete one-chip solution in that an external crystal and battery are the only components required to maintain time of day memory status in the absence of power.

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{INTB}$/(INTB)	Interrupt Output B (Active High or Low). $\overline{INTB}$ outputs the alarm (time of day or watchdog) that is not selected for $\overline{INTA}$. This pin is programmable high or low. Both $\overline{INTA}$ and $\overline{INTB}$/(INTB) are open-drain outputs. The two interrupts and the internal clock continue to run regardless of the V_{CC} level. However, it is important to ensure that the pullup resistors used with the interrupt pins are never pulled up to a value that is greater than V_{CC} + 0.3V. As V_{CC} falls below approximately 3.0V, a power-switching circuit turns the lithium energy source on to maintain the clock and timer data functionality. It is also required to ensure that during this time (battery-backup mode) the voltage present at $\overline{INTA}$ and $\overline{INTB}$/(INTB) never exceeds V_{BAT}. At all times the current on each should not exceed +2.1mA or -1.0mA.
2	N.C.	No Connection
3	A14	Address Bus (Input). The address bus inputs qualified by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and V_{CC} are used to select the on-chip 64 timekeeping/RAM registers within the memory map of the external SRAM controlled as nonvolatile storage. When the qualified address bus value is within the range of 00000H–0003FH, one of the internal registers is selected and $\overline{OER}$ remains inactive. When the value is outside the range, $\overline{OE}$ is passed through to $\overline{OER}$.
4	A12	
5–12	A7–A0	
25	A10	
27	A11	
28	A9	
29	A8	
30	A13	
33	A15	
40	A16	

PIN	NAME	FUNCTION
13, 14, 15, 17–21	DQ0, DQ1, DQ2, DQ3–DQ7	Data Bus (Bidirectional). When a qualified address from 00000H–0003FH is presented to the device, data is passed to or from the on-chip 64 timekeeping/RAM registers via the data bus lines. Data is written on the rising edge of $\overline{WE}$ when $\overline{CE}$ is active. If $\overline{CE}$ is active without $\overline{WE}$, data is read from the device and driven onto the data bus pins when $\overline{OE}$ is low.
16, 41, 44	GND	Ground. DC power input.
22	$\overline{CEO}$	Active-Low RAM Chip-Enable Output. When power is good, the $\overline{CE}$ input is passed through to $\overline{CEO}$. If V_{CC} is below V_{PF}, $\overline{CEO}$ remains at an inactive high level.
23	$\overline{OER}$	Active-Low RAM Output Enable (Output). When power is good and the address value is not within the range of 00000H and 0003FH, and $\overline{CE}$ is active, the $\overline{OE}$ input is passed through to $\overline{OER}$. If these conditions are not met, $\overline{OER}$ remains at an inactive high level.
24	$\overline{CE}$	Active-Low Chip Enable (Input). This signal must be asserted low during a bus cycle to access the on-chip timekeeping RAM registers, or to access the external RAM via $\overline{CEO}$.
26	$\overline{OE}$	Active-Low Output Enable (Input). This signal identifies the time period when either the RTC or the external SRAM drives the bus with read data, provided that $\overline{CE}$ is valid with $\overline{WE}$ disabled. When one of the 64 on-chip registers is selected during a read cycle, the $\overline{OE}$ is the enable signal for the DS1384 output buffers and the data bus is driven with read data. When the external RAM is selected during a read cycle, the $\overline{OE}$ signal is passed through to the $\overline{OER}$ pin so that read data is driven by the external SRAM.
31	$\overline{WE}$	Active-Low Write Enable (Input). This signal identifies the time period during which data is written to either the on-chip registers or to an external SRAM location. When one of the on-chip 64 registers is addressed, data is written to the selected register on the rising edge of $\overline{WE}$.
32, 34	V_{BAT1}, V_{BAT2}	Battery Inputs for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between 2.4V and 4V for proper operation. In the absence of power, the DS1384 has a maximum load of 0.5µA at +25°C. This should be added to the amount of current drawn from the external RAM in standby mode at +25°C to size the external energy source. The DS1384 samples V_{BAT1} and V_{BAT2} and always selects the battery with the higher voltage. If only one battery is used, the unused battery input must be grounded.
35	$\overline{PFO}$	Power-Fail Signal (Output, Active Low when V_{WP} Occurs). High state occurs t_{REC} after power-up and $V_{CC} \geq 4.5V$.
36	SQW	Square-Wave Output. This pin can be programmed to output a 1024Hz square-wave signal. When the signal is turned off, the pin is high impedance.
37	V_{CCO}	Switched DC Power for SRAM (Output). This pin is connected to V_{CC} when V_{CC} voltage is above V_{SO} (the greater of V_{BAT1} or V_{BAT2}). When V_{CC} voltage falls below this level, V_{CCO} is connected to the higher voltage battery pin.

PIN	NAME	FUNCTION
38	V_{CC}	DC Power Input. DC operating voltage is provided to the device on this pin. V_{CC} is the +5V input.
39	$\overline{INTA}$	Active-Low Interrupt Output A. $\overline{INTA}$ can be programmed as a time-of-day alarm or as a watchdog alarm. ($\overline{INTB}$ becomes the alternate function). $\overline{INTA}$ can also be programmed to output either a pulse or a level.
42, 43	X1, X2	Connections for Standard 32.768kHz Quartz Crystal. When ordering, request a load capacitance (C_L) of 6pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real Time Clocks*.

ADDRESS DECODING

The DS1384 accommodates 17 address lines, which allows direct connection of up to 128k bytes of static RAM. The lower 14 bytes of RAM, regardless of the density used, will always contain the timekeeping, alarm, and watchdog registers. The 14 clock registers reside in the lower 14 RAM locations without conflict by inhibiting the $\overline{OER}$ (output enable RAM) signal during clock access. Since the watchdog timekeeping chip actually contains 64 registers (14 RTC and 50 user RAM), the lower 64 bytes of any attached memory resides within the DS1384. However, the RAM's physical location is transparent to the user and the memory map looks continuous from the first clock address to the upper most attached RAM address.

OPERATION—READ CYCLE

The DS1384 executes a read cycle whenever $\overline{WE}$ is inactive (high) and $\overline{CE}$ and $\overline{OE}$ are active (low). The unique address specified by the address inputs (A0-A16) defines which of the on-chip 64 RTC/RAM or external SRAM locations is to be accessed. When the address value presented to the DS1384 is in the range of 00000H through 0003FH, one of the 64 on-chip registers will be selected and valid data will be available to the eight data output drivers within t_{ACC} (access time) after the address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If they are not, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than the address access time. When one of the on-chip registers is selected for read, the $\overline{OER}$ signal will remain inactive throughout the read cycle.

When the address value presented to the DS1384 is in the range of 00040H through 1FFFFH, an external SRAM location will be selected. In this case the $\overline{OE}$ signal will be passed to the $\overline{OER}$ pin, with the specified delay times of t_{AOEL} or t_{OERL}.

OPERATION—WRITE CYCLE

The DS1384 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus

contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{WEZ} from its falling edge.

When the address value presented to the DS1384 during the write is in the range of 00000H through 0003FH, one of the 64 on-chip registers will be selected and data will be written into the device.

When the address value presented to the DS1384 during the write is in the range of 00040H through 1FFFFH, an external SRAM location will be selected.

DATA RETENTION MODE

When V_{CCI} is within nominal limits (V_{CC} > 4.5V) the DS1384 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power-fail point, V_{PF}, (point at which write protection occurs) the internal clock registers and external RAM is blocked from access. This is accomplished internally by inhibiting access to the clock registers via the $\overline{CE}$ signal. At this time the power fail output signal ($\overline{PFO}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{CEO}$ to high level. This level is within 0.2 volts of the V_{CCI} input. $\overline{CEO}$ will remain at this level as long as V_{CCI} remains at an out-of-tolerance condition. When V_{CCI} falls below the level of the battery (V_{BAT1} or V_{BAT2}), power input is switched from the V_{CCI} pin to the V_{BAT} pin and the clock registers are maintained from the attached battery supply. External RAM is also powered by the V_{BAT} input when V_{CCI} is below V_{BAT} pin through the V_{CCO} pin. The V_{CCO} pin is capable of supplying 100µA of current to the attached memory with less than 0.3V drop under this condition. On power-up, when V_{CCI} returns to in-tolerance conditions, write protection continues for 150ms by inhibiting $\overline{CEO}$. The $\overline{PFO}$ signal also remains active during this time. The DS1384 is capable of supporting two batteries which are used in a redundant fashion for applications which require added reliability or increased battery capacity. When two batteries are used, the higher of the two is selected for use. A selected battery will remain as backup supply until it is significantly below the other. When the selected battery voltage falls below the alternate battery by about 0.6V, the alternate battery is selected and then becomes the backup supply. This switching occurs transparently to the user and continues until both batteries are exhausted. When only a single battery is required, both battery inputs can be connected together. However, a more effective method of using a single battery supply is to ground the unused battery input. When using a single battery, V_{BAT1} is the preferred input.

WATCHDOG TIMEKEEPER REGISTERS

The DS1384 Watchdog Timekeeper Controller has 14 internal registers, which are 8 bits wide and contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm and Watchdog Registers are memory locations, which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers are accessed from the external address and data bus and reside or overlay external static RAM. Registers 0, 1, 2, 4, 6, 8, 9 and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the time of day alarm information. Time of day alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Register C and D are the Watchdog Alarm Registers and information, which is stored in these two registers, is in BCD. Registers 0000EH through register 0003FH are on-chip user bytes and can be used to contain data at the user's discretion.

Figure 1. DS1384 Block Diagram

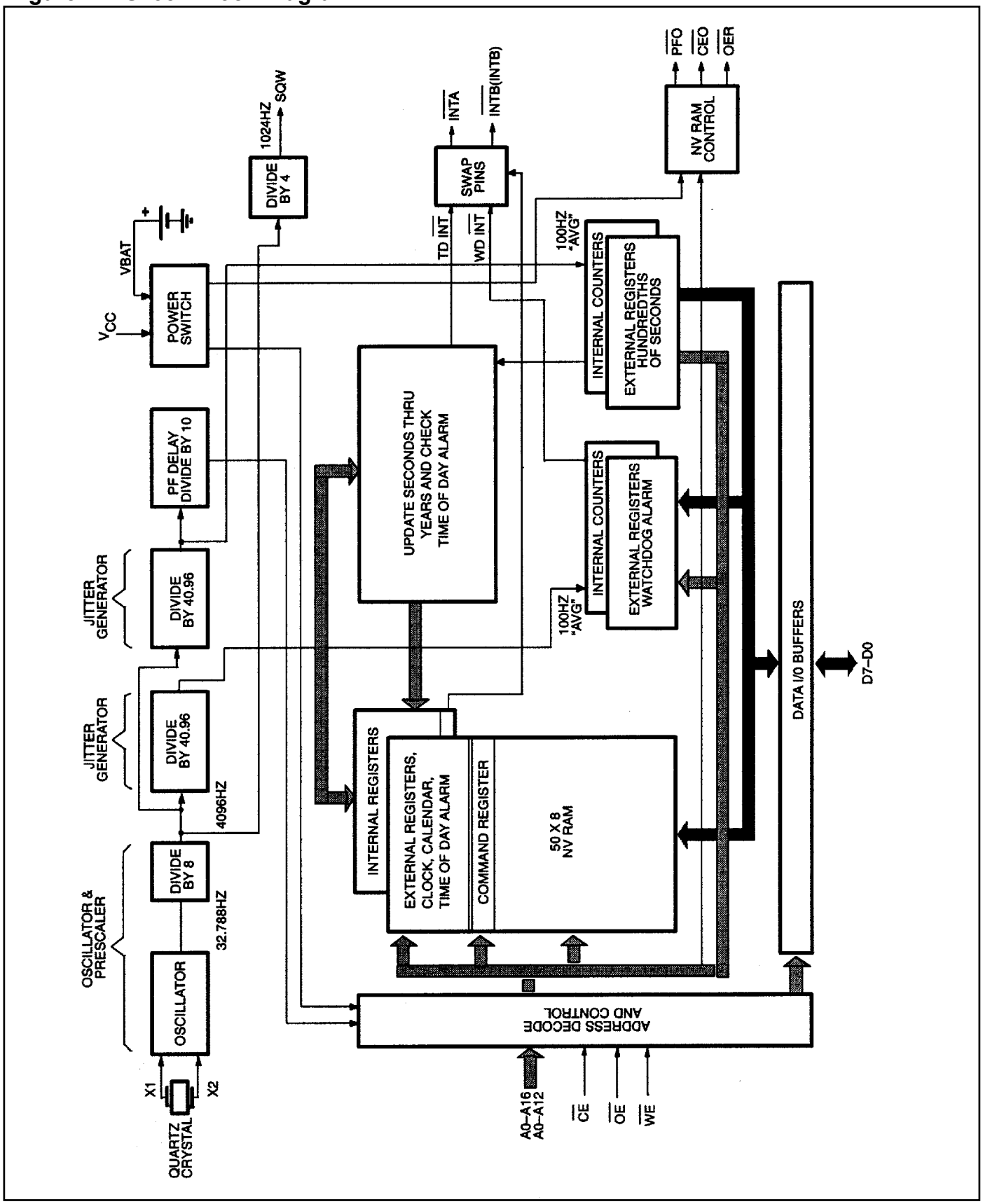


Figure 2. DS1384 Watchdog Timekeeper Registers

	ADDRESS	BIT 7							BIT 0	RANGE
CLOCK, CALENDAR, TIME OF DAY ALARM REGISTERS	0	0.1 SECONDS				0.01 SECONDS				00–99
	1	0	10 SECONDS			SECONDS				00–59
	2	0	10 MINUTES			MINUTES				00–59
	3	M	10 MIN ALARM			MIN ALARM				00–59
	4	0	12/24	10 A/P	10 HR	HOURS				01–12+A/P 00–23
	5	M	12/24	10 A/P	10 HR	HR ALARM				01–12+A/P 00–23
	6	0	0	0	0	0	DAYS			01–07
	7	M	0	0	0	0	DAY ALARM			01–07
	8	0	0	10 DATE		DATE				01–31
	9	$\overline{\text{EOSC}}$	$\overline{\text{ESQW}}$	0	10 MO	MONTHS				01–12
	A	10 YEARS				YEARS				00–99
COMMAND REGISTERS	B	TE	IPSW	IBH LO	PU LVL	WAM	TDM	WAF	TDF	
WATCHDOG ALARM REGISTERS	C	0.1 SECONDS				0.01 SECONDS				00–99
	D	10 SECONDS				SECONDS				00–99
USER REGISTERS	E									
	1FFFF									

Table 1. Time Of Day Alarm Mask Bits

REGISTER			DESCRIPTION
MINUTES	HOURS	DAYS	
1	1	1	Alarm Once Per Minute
0	1	1	Alarm When Minutes Match
0	0	1	Alarm When Hours And Minutes Match
0	0	0	Alarm When Hours, Minutes, And Days Match

Note: *any other bit combinations of mask bit settings produce illogical operation.*

TIME-OF-DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9 and A contain time of day data in BCD. Ten bits within these eight registers are not used and will always read 0 regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits.

When set to logical 0, $\overline{\text{EOSC}}$ (bit 7) enables the real-time clock oscillator. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level.

Bit 6 of this same byte controls the square wave output (pin 24). When set to logical 0, the square wave output pin will output a 1024 Hz square wave signal. When set to logic 1 the square wave output pin is in a high impedance state.

Bit 6 of the Hours Register is defined as the 12- or 24-Hour Select Bit. When set to logic 1, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/ PM bit with logical one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The time of day registers are updated every 0.01 seconds from the real time clock, except when the TE bit (bit 7 of register B) is set low or the clock oscillator is not running.

The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic 0. This will freeze the external time of day registers at the present recorded time allowing access to occur without danger of simultaneous update. When the watch registers have been read or written a second write cycle to location 0B, setting the TE bit to a logic 1, will put the time of day registers back to being updated every 0.01 second. No time is lost in the real time clock because the internal copy of the time of day register buffers are continually incremented while the external memory registers are frozen. An alternate method of reading and writing the time of day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read.

The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundredths of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME-OF-DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the time of day alarm registers. Bits 3, 4, 5, and 6 of register 7 will always read 0 regardless of how they are written. Bit 7 of registers 3, 5, and 7 are mask bits (Table 1). When all of the mask bits are logic 0, a time of day alarm will only occur when registers 2, 4, and 6 match the values stored in registers 3, 5, and 7. An alarm will be generated every day when bit 7 of register 7 is set to a logic 1. Similarly, an alarm is generated every hour when bit 7 of registers 7 and 5 is set to a logic 1. When bit 7 of registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when register 1 (seconds) rolls from 59 to 00.

Time of day alarm registers are written and read in the same format as the time of day registers. The time of day alarm flag and interrupt is always cleared when alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 seconds to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to 0. When 0 is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count down register is internal and is not readable. Writing registers C and D to 0 will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

Bit 7: TE (Transfer Enable). This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

Bit 6: IPSW (Interrupt Switch). When set to a logic 1, $\overline{\text{INTA}}$ is the Time of Day Alarm and $\overline{\text{INTB}}$/(INTB) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{\text{INTA}}$ is now the Watchdog Alarm output and $\overline{\text{INTB}}$ /(INTB) is the Time of Day Alarm output.

Bit 5: IBH/LO (Interrupt B Sink or Source Current). When this bit is set to a logic 1 and V_{CC} is applied, $\overline{\text{INTB}}$ /(INTB) will source current (see DC characteristics I_{OH}). When this bit is set to a logic 0, $\overline{\text{INTB}}$ will sink current (see DC characteristics I_{OL}).

Bit 4: PU/LVL (Interrupt Pulse Mode or Level Mode). This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ /(INTB) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. $\overline{\text{INTB}}$ /(INTB) will either sink or source current, depending on the condition of bit 5, for a minimum of 3 ms and then release.

Bit 3: WAM (Watchdog Alarm Mask). When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the Command Register. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

Bit 2: TDM (Time-of-Day Alarm Mask). When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0, 4, 5, and 6 of the Command Register. When this bit is set to a logic 1, the Time of Day Alarm interrupt output is deactivated.

Bit 1: WAF (Watchdog Alarm Flag). This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read-only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

Bit 0: TDF (Time-of-Day Flag). This is a read-only bit. This bit is set to a logic 1 when a time of day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers is accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Operating Temperature Range……..0°C to +70°C
Storage Temperature Range……..-20°C to +70°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.0		V_{CC} + 0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	
Battery Input Voltage	V_{BAT}	2.4		4.0V	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power-Supply Current	I_{CC1}		7	15	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}		2	5	mA	2, 3
CMOS Standby Current ($\overline{CE}$ < V_{CC} - 0.2V)	I_{CC3}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	1		+1	µA	
Output Leakage Current	I_{IO}	-1		+1	µA	
Output Logic 1 Voltage (I_{OH} = -1.0mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OH} = +2.1mA)	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	V_{CC} - 0.3			V	4
Output Current	I_{CCO1}			85	mA	4
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	5
Output Voltage	V_{CCO2}	V_{BAT} -0.3			V	6
Output Current	I_{CCO2}			100	µA	6
Battery Leakage OSC ON	I_{BAT1}			500	nA	
Battery Leakage OSC OFF	I_{BAT2}			100	nA	
Switchover Voltage	V_{SO}		V_{BAT1}, V_{BAT2}		V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{ACC}			120	ns	
$\overline{CE}$ Access Time	t_{CO}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
Output Enable Access Time	t_{OE}			60	ns	
Output Enable Data Off Time	t_{OEZ}			40	ns	
Output Enable to DQ Low-Z	t_{OEL}	5			ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	10			ns	
Output Hold from Address	t_{OH}	5			ns	
$\overline{CE}$ to $\overline{CEO}$ Low or High	t_{CEPD}			25	ns	
$\overline{OE}$ Low to $\overline{OER}$ Low A0–A16 ≥ 00040h	t_{OERL}			20	ns	
$\overline{OE}$ High to $\overline{OER}$ High Time	t_{RO}			20	ns	
Address 00040h–1FFFFh to $\overline{OER}$ Low	t_{AOEL}			50	ns	
Address 00000h–0003Fh to $\overline{OER}$ High	t_{AOEH}			40	ns	
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AW}	0			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	120			ns	
Address Hold from End of Write	t_{AH}	10			ns	
Write Pulse Width	t_{WP}	80			ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10			ns	
Data Setup Time	t_{DS}	45			ns	
Data Hold Time High	t_{DH}	0			ns	
$\overline{INTA}$ and $\overline{INTB}$ Pulse Width	t_{IPW}	3			ms	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5ns

CAPACITANCE

(T_A = +25°C)

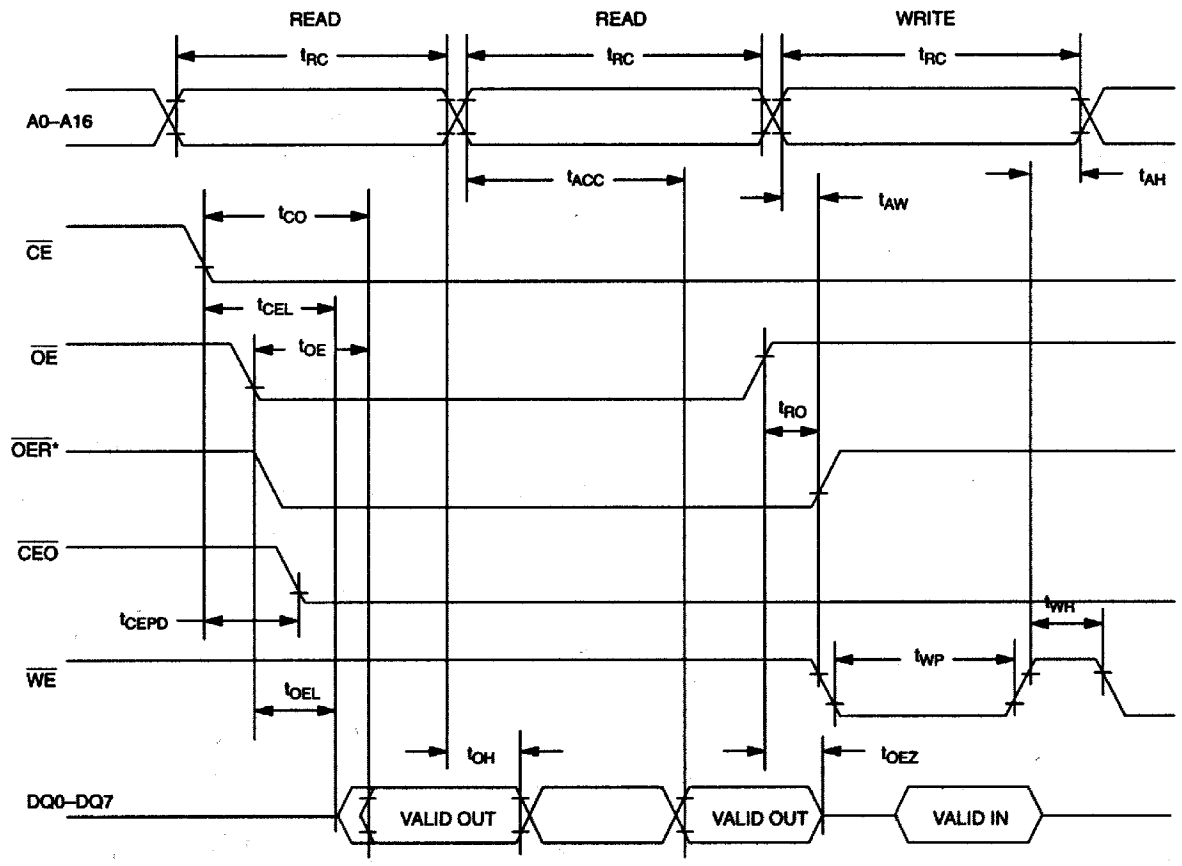
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins (Except DQ)	C_I		7	15	pF	
Capacitance on DQ Pins	C_{DQ}		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C)

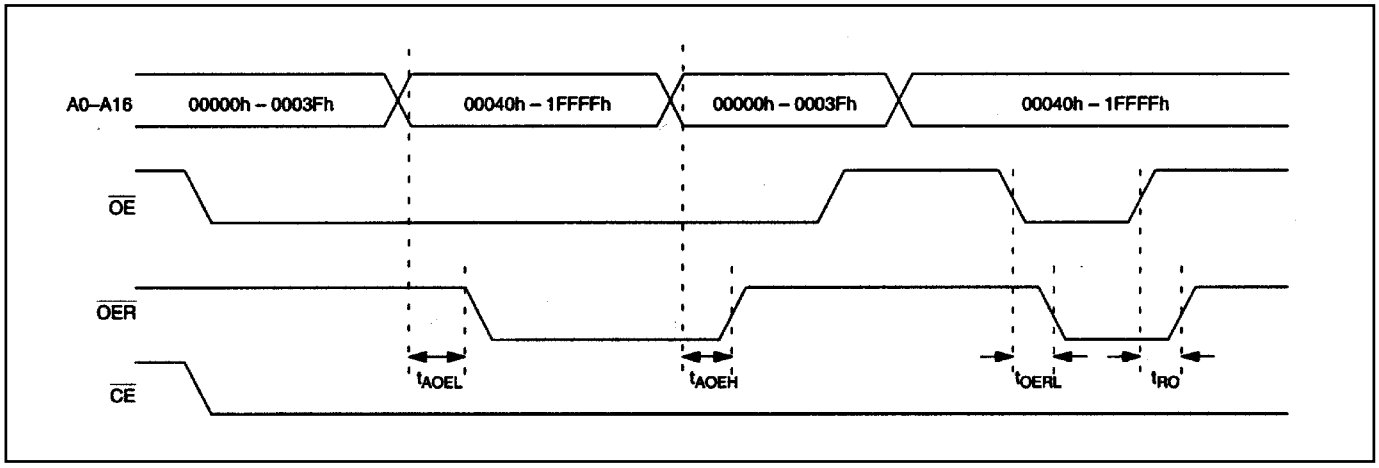
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power-Up	t_{REC}	10		150	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	7

READ CYCLE TIMING—RTC AND EXTERNAL SRAM CONTROL SIGNALS

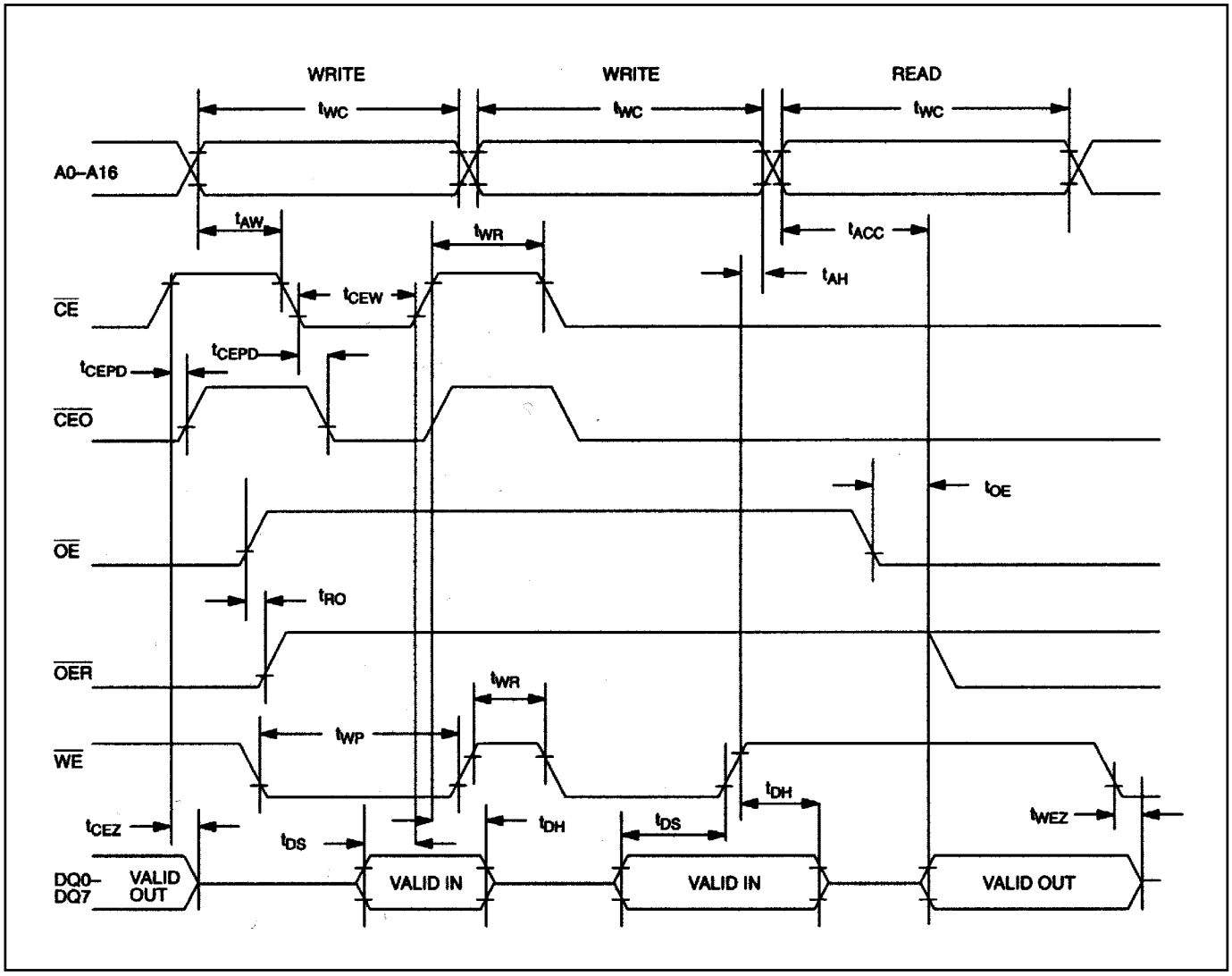


* See the following timing diagram for more specifics on $\overline{OER}$ timing.

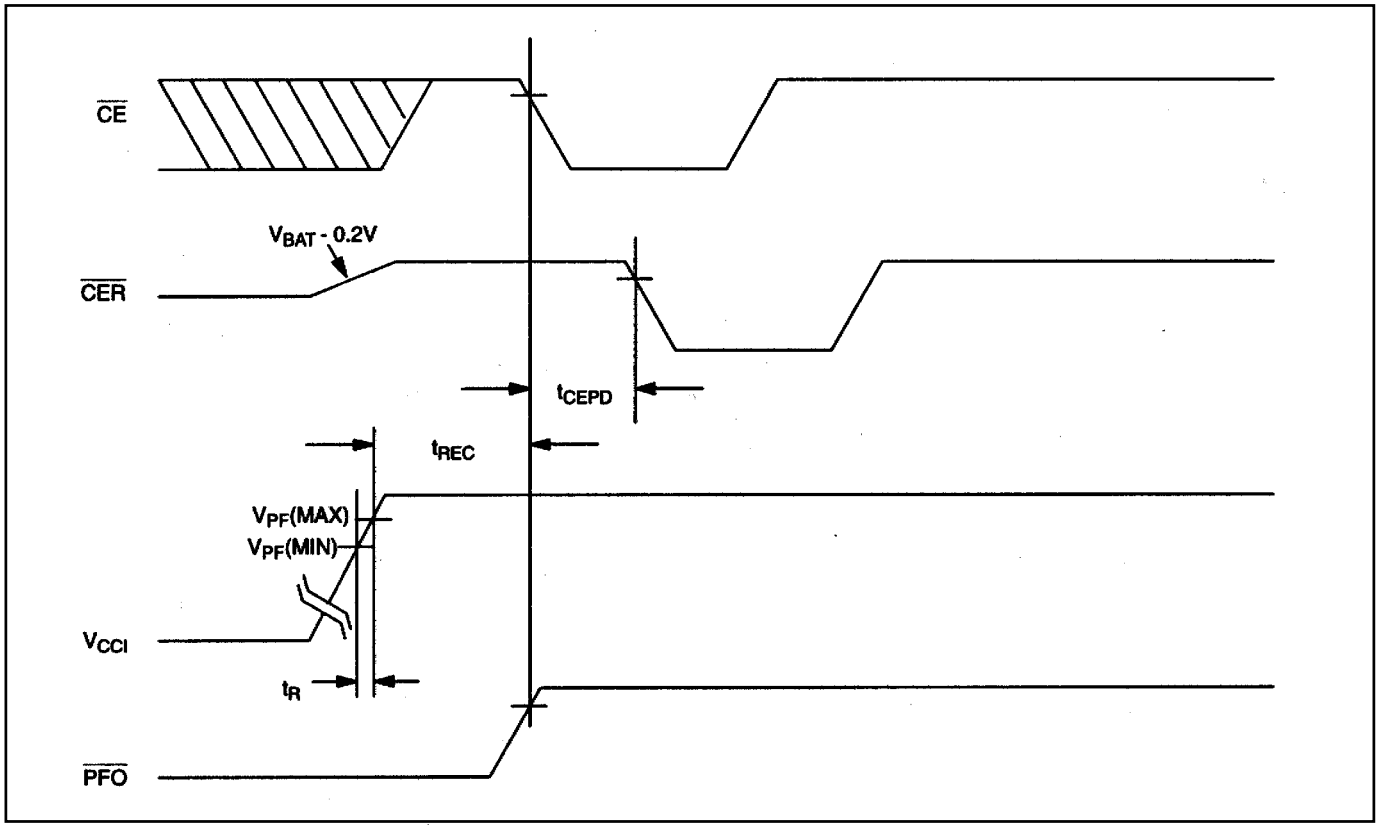
$\overline{\text{OER}}$ TIMING WHEN SWITCHING BETWEEN LOWER MEMORY (00000h–0003Fh) AND UPPER MEMORY (00040h–1FFFFh)



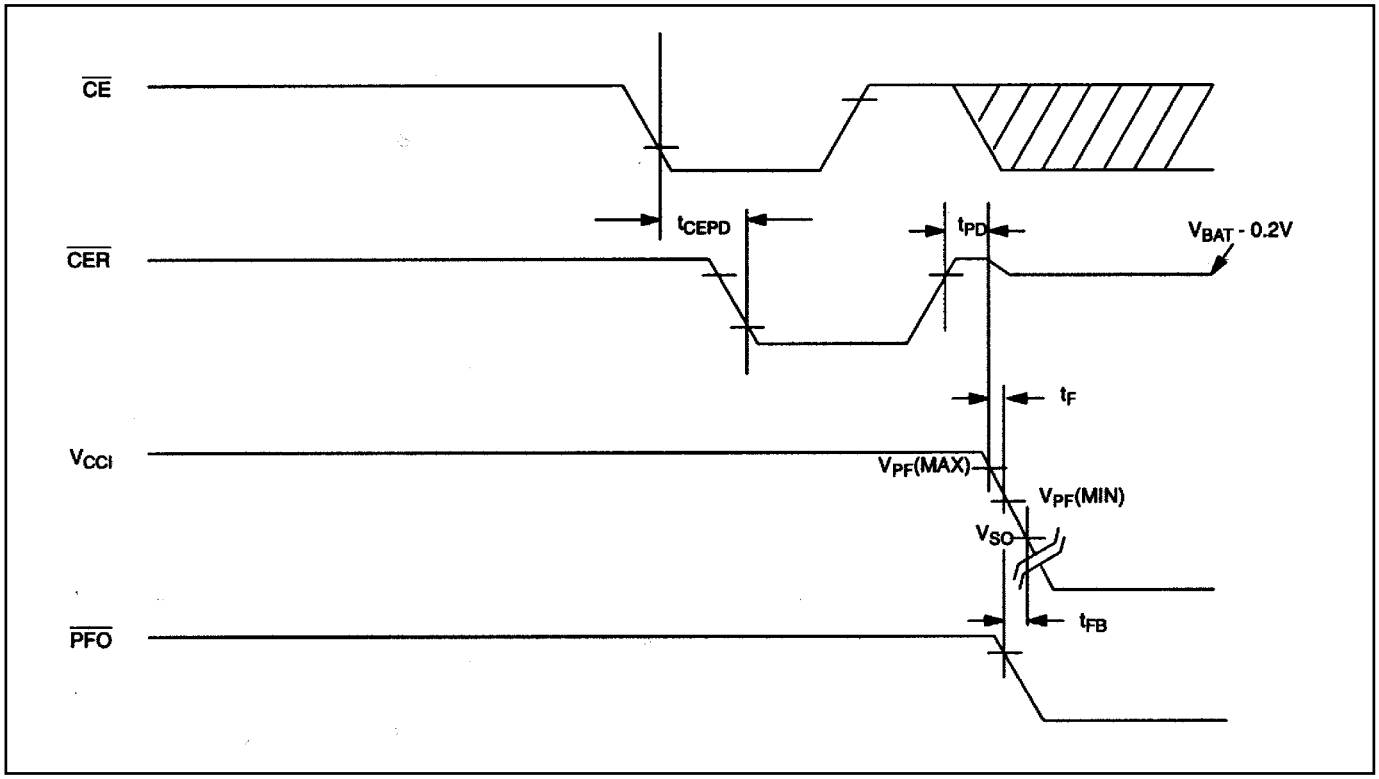
WRITE CYCLE TIMING—RTC AND EXTERNAL SRAM CONTROL SIGNALS



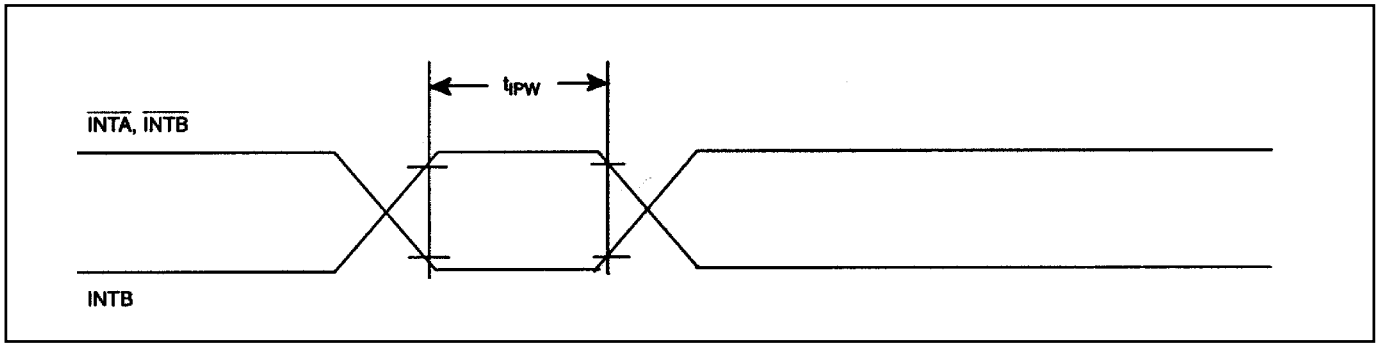
POWER-UP TIMING DIAGRAM



POWER-DOWN TIMING DIAGRAM



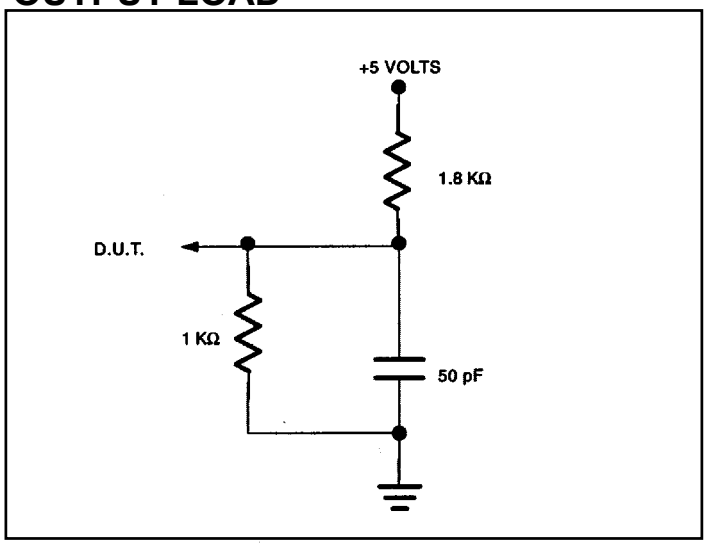
INTERRUPT OUTPUTS PULSE MODE TIMING DIAGRAM (See Notes 8 and 9)



NOTES:

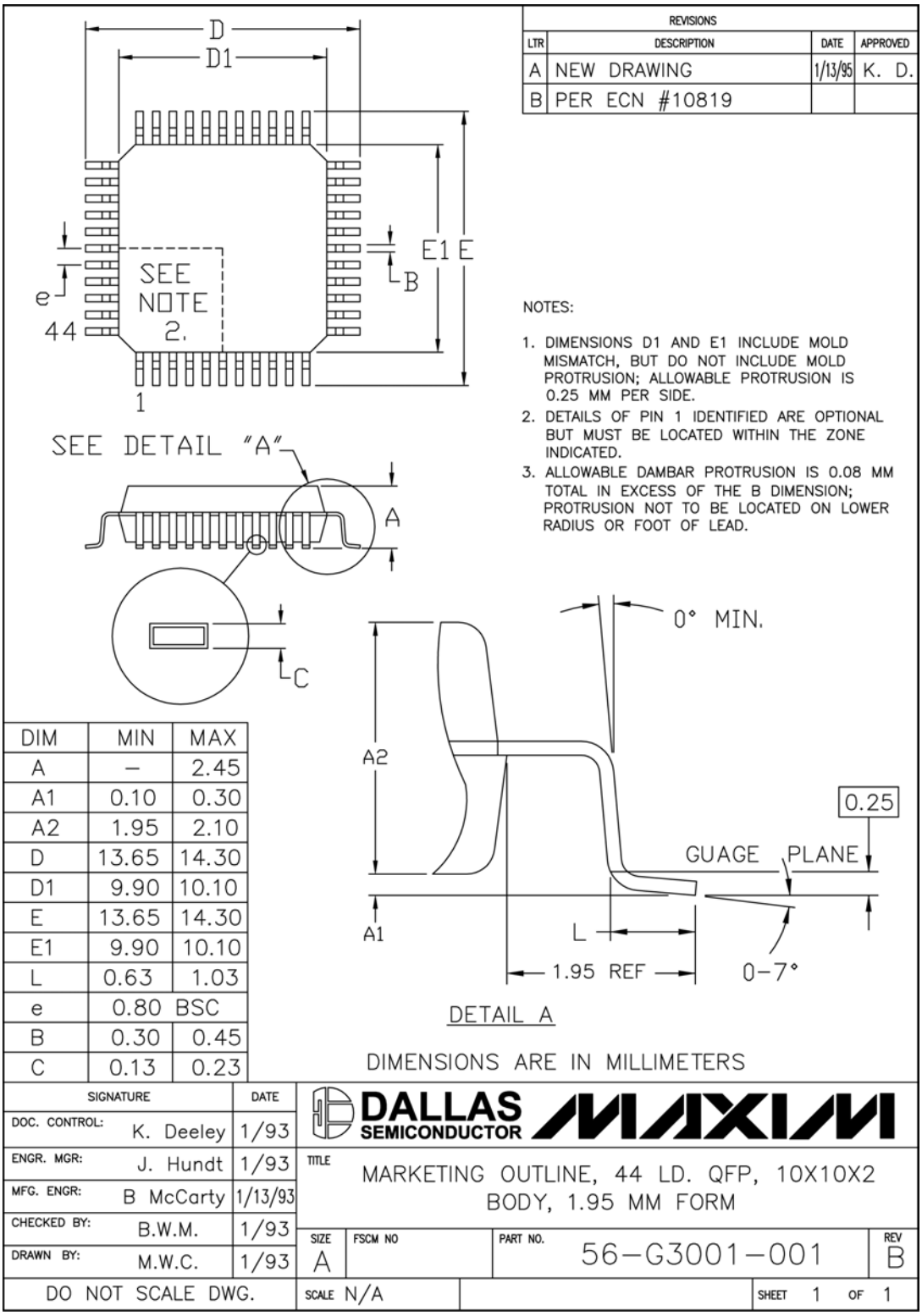
1) All voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Value for voltage and currents is from the V_{CCI} input pin to the V_{CCO} pin.
5) Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
6) Value for voltage and currents is from the V_{BAT} input pin to the V_{CCO} pin.
7) Data retention time depends on the size of battery selected and the amount of current demanded by the static RAM in backup mode. The battery capacity (mA • hr) to achieve a t_{DR} of 10 years is given by the formula: $C = (I_{BAT1} + I_{RAM}) \times 24 \times 365 \times 10$, where I_{RAM} is the standby current of the static RAM at the battery voltage. For the DS1384 chip alone, a standard 48mAh lithium cell battery will provide greater than 10 years of data retention in the absence of power.
8) Applies to both interrupt pins when the alarms are set to pulse.
9) Interrupt output occurs within 100ns of the alarm condition existing.

OUTPUT LOAD



PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



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