FAIRCHILD SEMICONDUCTOR®

April 2006

74AC240, 74ACT240
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The AC/ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inverting 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- ACT240 has TTL-compatible inputs

Ordering Information

Order Number	Package Number	Package Description
74AC240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT240SC_NL(1)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT240PC_NL(1)	N20A	Pb-Free 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

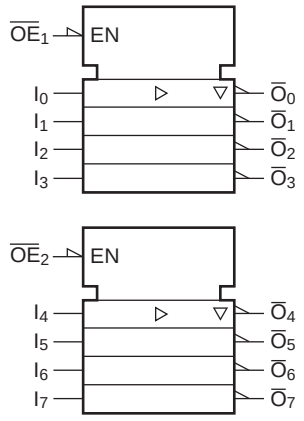
Note:
1. “_NL” indicates Pb-Free package (per JEDEC J-STD-020B). Please use order number as indicated.

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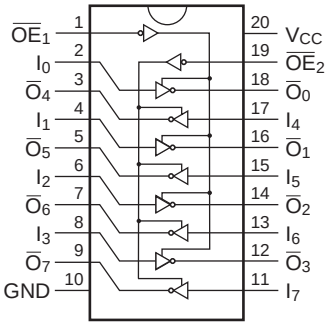
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Logic Symbol

IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Symbol	Parameter	Value	Units
V_{CC}	Supply Voltage	–0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_I = –0.5V$ $V_I = V_{CC} + 0.5V$	 –20 +20	mA
V_I	DC Input Voltage	–0.5 to $V_{CC} + 0.5$	V
I_{OK}	DC Output Diode Current $V_O = –0.5V$ $V_O = V_{CC} + 0.5V$	 –20 +20	mA
V_O	DC Output Voltage	–0.5 to $V_{CC} + 0.5$	V
I_O	DC Output Source or Sink Current	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50	mA
T_{STG}	Storage Temperature	–65°C to +150°C	°C
T_J	Junction Temperature, PDIP	140°	°C

Recommended Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply Voltage AC ACT	 2.0 to 6.0 4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature	–40 to +85°	°C
$\Delta V/\Delta t$	Minimum Input Edge Rate AC Devices, V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125	mV/ns
$\Delta V/\Delta t$	Minimum Input Edge Rate ACT Devices, V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125	mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1V	3.0	1.5	2.1	2.1	V
			4.5	2.25	3.15	3.15	
			5.5	2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1V	3.0	1.5	0.9	0.9	V
			4.5	2.25	1.35	1.35	
			5.5	2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	I_{OUT} = –50µA	3.0	2.99	2.9	2.9	V
			4.5	4.49	4.4	4.4	
			5.5	5.49	5.4	5.4	
		$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = –12mA	3.0		2.56	2.46	
		I_{OH} = –24mA	4.5		3.86	3.76	
		I_{OH} = –24mA[2]	5.5		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	I_{OUT} = 50µA	3.0	0.002	0.1	0.1	V
			4.5	0.001	0.1	0.1	
			5.5	0.001	0.1	0.1	
		$V_{IN} = V_{IL}$ or V_{IH} I_{OL} = 12mA	3.0		0.36	0.44	
		I_{OL} = 24mA	4.5		0.36	0.44	
		I_{OL} = 24mA[2]	5.5		0.36	0.44	
I_{IN}[4]	Maximum Input Leakage Current	$V_I = V_{CC}$, GND	5.5		± 0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND	5.5		±0.25	±2.5	µA
I_{OLD}	Minimum Dynamic Output Current[3]	V_{OLD} = 1.65V Max	5.5			75	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.5			–75	mA
I_{CC}[4]	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5		4.0	40.0	µA

Notes:

2. All outputs loaded; thresholds on input associated with output under test.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1V	4.5	1.5	2.0	2.0	V
			5.5	1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1V	4.5	1.5	0.8	0.8	V
			5.5	1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	I_{OUT} = –50μA	4.5	4.49	4.4	4.4	V
			5.5	5.49	5.4	5.4	
		$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = –24mA	4.5		3.86	3.76	
		I_{OH} = –24mA[5]	5.5		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	I_{OUT} = 50μA	4.5	0.001	0.1	0.1	V
			5.5	0.001	0.1	0.1	
		$V_{IN} = V_{IL}$ or V_{IH} I_{OL} = 24mA	4.5		0.36	0.44	
		I_{OL} = 24mA[5]	5.5		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	$V_I = V_{CC}$, GND	5.5		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Leakage Current	$V_I = V_{IL}$, V_{IH}, $V_O = V_{CC}$, GND	5.5		±0.25	±2.5	μA
I_{CCT}	Maximum I_{CC}/Input	$V_I = V_{CC}$ – 2.1V	5.5	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[6]	V_{OLD} = 1.65V Max	5.5			75	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.5			–75	mA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5		4.0	40.0	μA

Notes:

5. All outputs loaded; thresholds on input associated with output under test.
6. Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	6.0	8.0	1.0	9.0	ns
		5.0	1.5	4.5	6.5	1.0	7.0	
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	5.5	8.0	1.0	8.5	ns
		5.0	1.5	4.5	6.0	1.0	6.5	
t_{PZH}	Output Enable Time	3.3	1.5	6.0	10.5	1.0	11.0	ns
		5.0	1.5	5.0	7.0	1.0	8.0	
t_{PZL}	Output Enable Time	3.3	1.5	7.0	10.0	1.0	11.0	ns
		5.0	1.5	5.5	8.0	1.0	8.5	
t_{PHZ}	Output Disable Time	3.3	1.5	7.0	10.0	1.0	10.5	ns
		5.0	1.5	6.5	9.0	1.0	9.5	
t_{PLZ}	Output Disable Time	3.3	1.5	7.5	10.5	1.0	11.5	ns
		5.0	1.5	6.5	9.0	1.0	9.5	

Notes:

7. Voltage Range 3.3 is 3.3V ± 0.3V, Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[8]	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Data to Output	5.0	1.5	6.0	8.5	1.5	9.5	ns
t_{PHL}	Propagation Delay Data to Output	5.0	1.5	5.5	7.5	1.5	8.5	ns
t_{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.0	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns
t_{PHZ}	Output Disable Time	5.0	2.0	8.0	9.5	2.0	10.5	ns
t_{PLZ}	Output Disable Time	5.0	2.5	6.5	10.0	2.0	10.5	ns

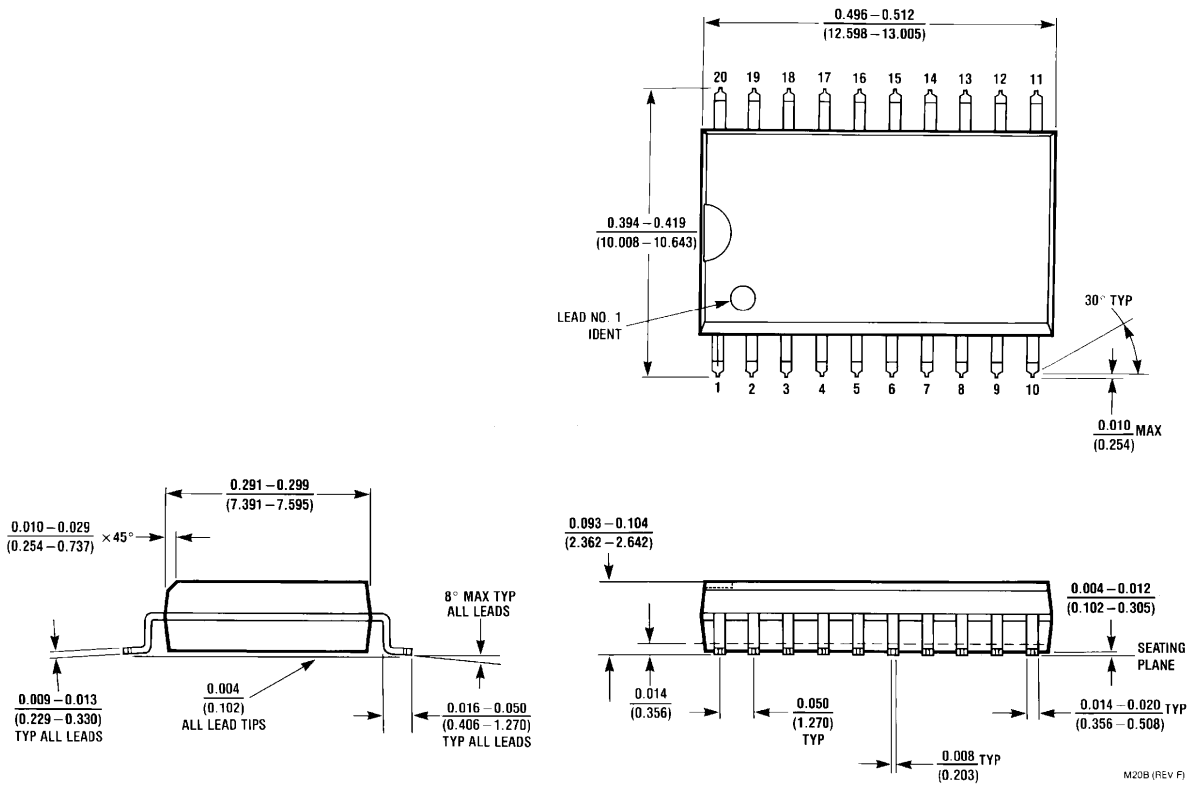
Notes:

8. Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

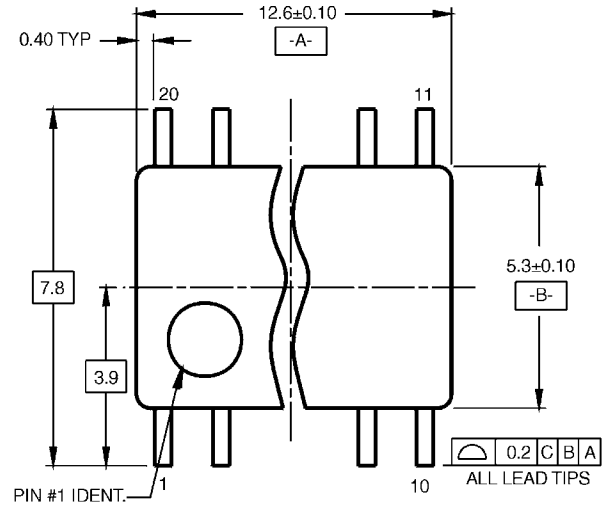
Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	45.0	pF

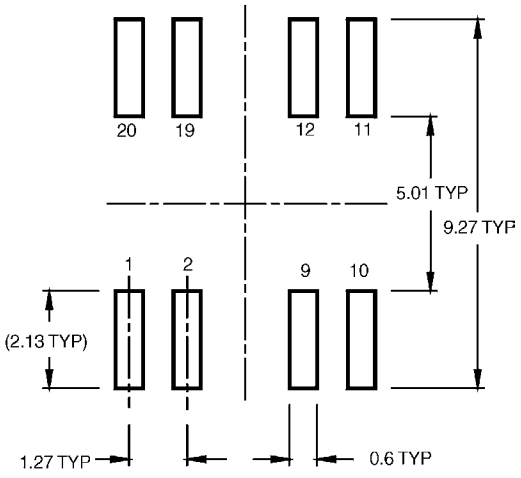
Physical Dimensions inches (millimeters) unless otherwise noted



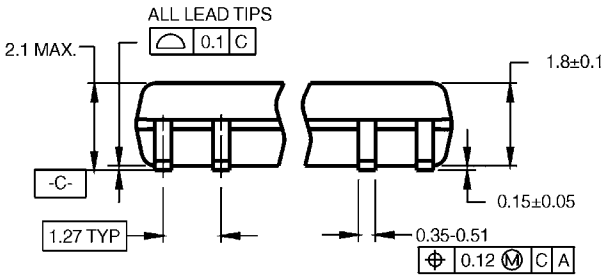
20-Lead Small Outline Integrated Circuit (SOIC),
JEDEC MS-013, 0.300" Wide Package Number M20B

Physical Dimensions (Continued) millimeters unless otherwise noted

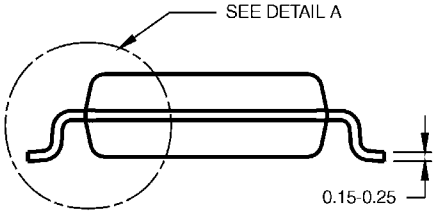


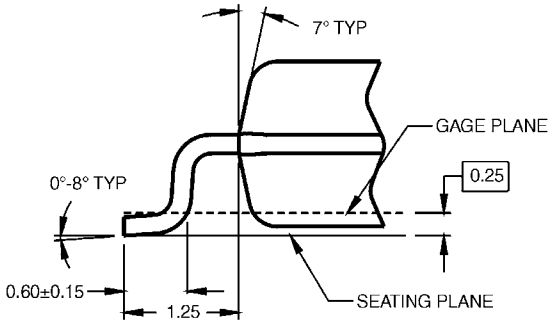


LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS





DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

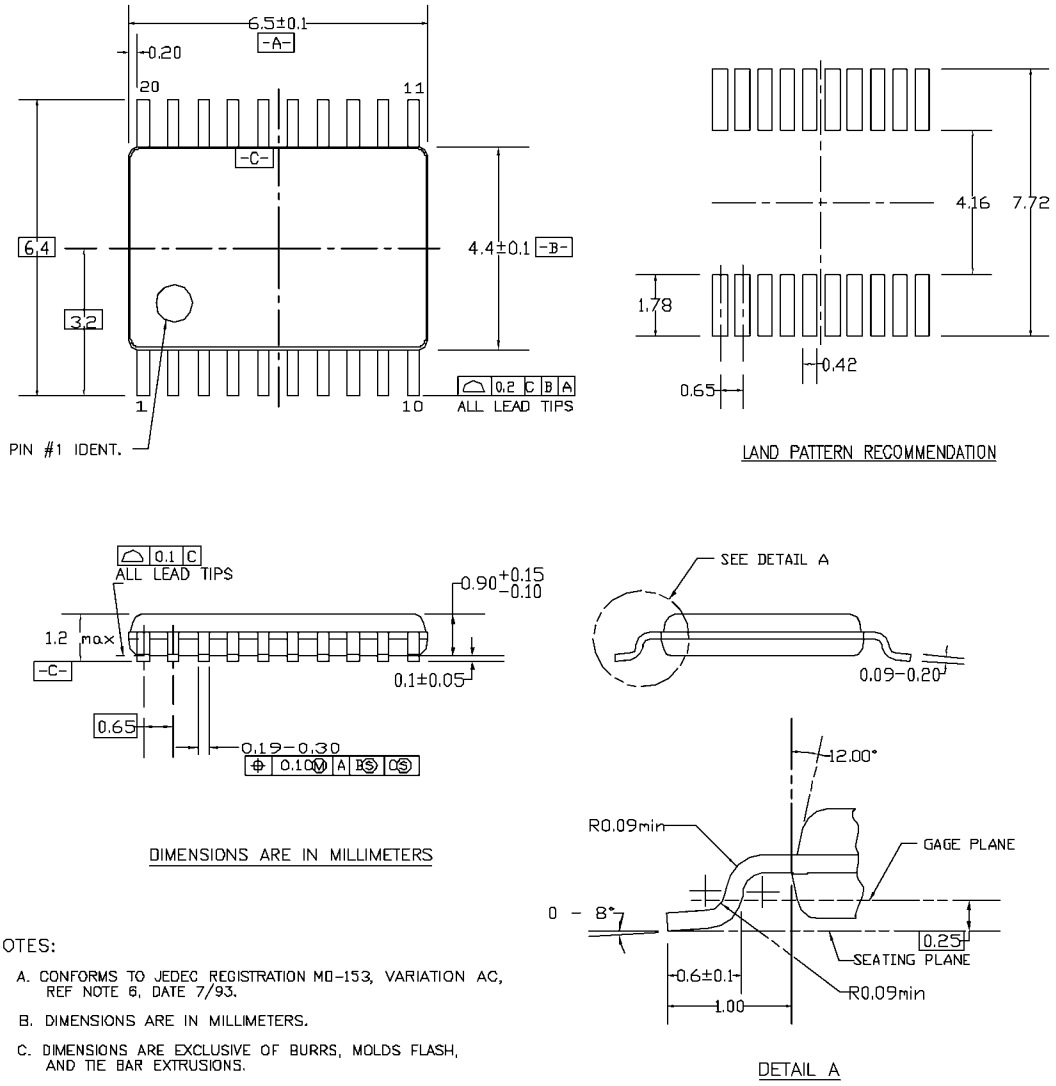
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions (Continued) millimeters unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

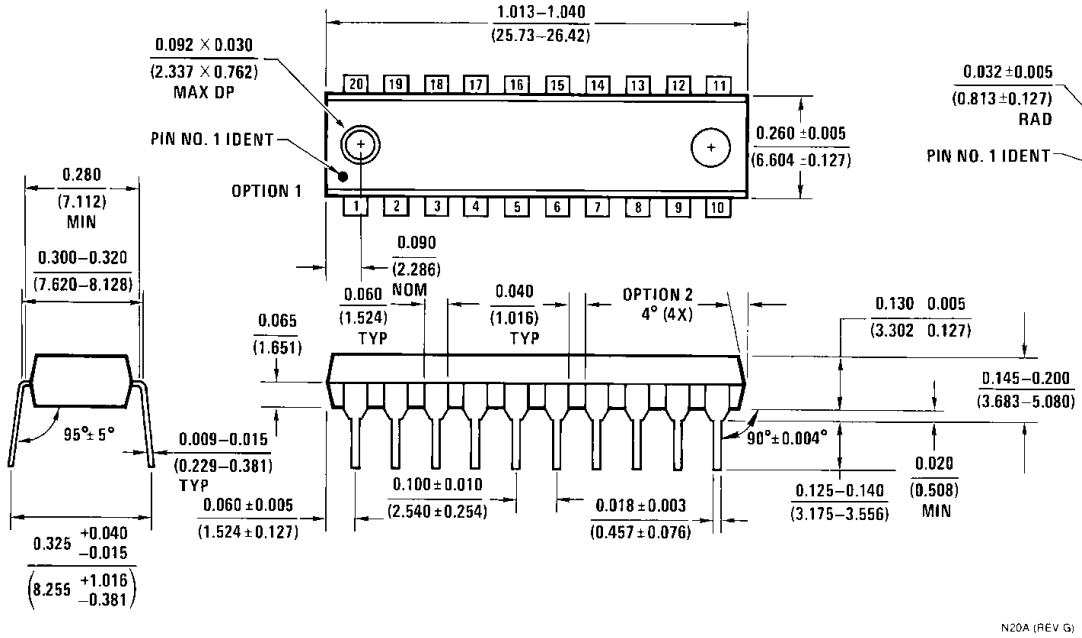
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP),
JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions (Continued) inches (millimeters) unless otherwise noted



20-Lead Plastic Dual-In-Line Package (PDIP),
JEDEC MS-001, 0.300" Wide Package Number N20A

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Rev. I18

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