

- **Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry**
- **Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges**

DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT	R _{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

description

These voltage-controlled oscillators (VCOs) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCOs in a single monolithic chip. The 'LS624, 'LS625, 'LS626, and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external component (either a capacitor or crystal) in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

The 'LS628 offers more precise temperature compensation than its 'LS624 counterpart. The 'LS624 features a 600 ohm internal timing resistor. The 'LS628 requires a timing resistor to be connected externally across R_{ext} pins. Temperature compensation will be improved due to the temperature coefficient of the external resistor.

Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

A single 5-volt supply can be used; however, one set of supply voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (OSC V_{CC} and OSC GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS626 and 'LS627 can be achieved by removing the appropriate OSC V_{CC}. An enable input is provided on the 'LS624, 'LS626, 'LS628, and 'LS629. When the enable input is low, the output is enabled; when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627 and 'LS629) when both VCOs are operated simultaneously. To minimize crosstalk, either of the following are recommended: (A) If frequencies are widely separated, use a 10-μh inductor between V_{CC} pins. (B) If frequencies are closely spaced, use two separate V_{CC} supplies or place two series diodes between the V_{CC} pins.

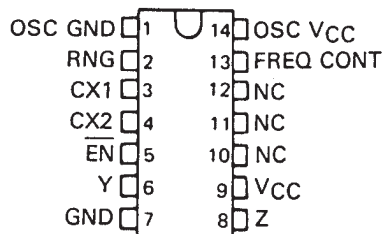
The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LS624 thru SN74LS629 are characterized for operation from 0°C to 70°C.

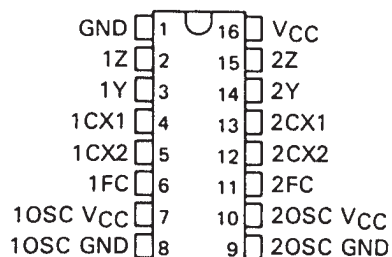
SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

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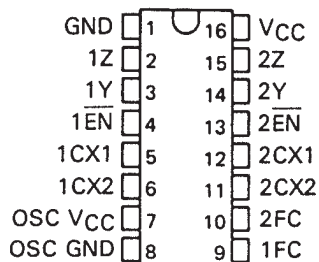
**SN54LS624 . . . J OR W PACKAGE
SN74LS624 . . . D OR N PACKAGE
(TOP VIEW)**



**SN54LS625 . . . J OR W PACKAGE
SN74LS625 . . . D OR N PACKAGE
(TOP VIEW)**

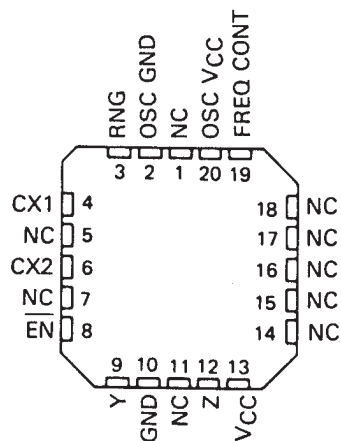


**SN54LS626 . . . J OR W PACKAGE
SN74LS626 . . . D OR N PACKAGE
(TOP VIEW)**

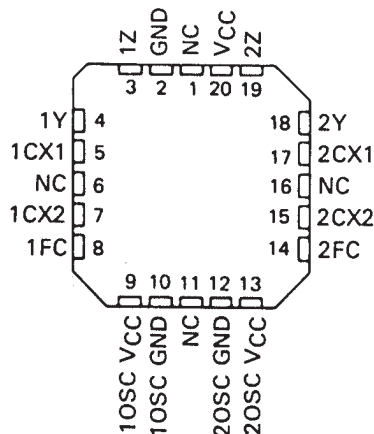


NC – No internal connection

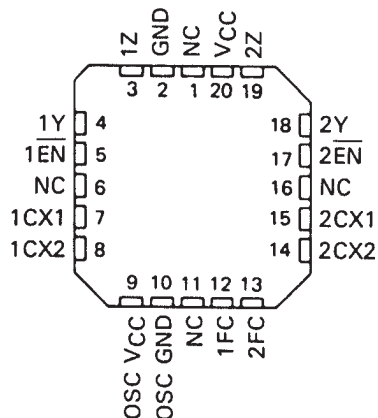
**SN54LS624 . . . FK PACKAGE
(TOP VIEW)**



**SN54LS625 . . . FK PACKAGE
(TOP VIEW)**



**SN54LS626 . . . FK PACKAGE
(TOP VIEW)**



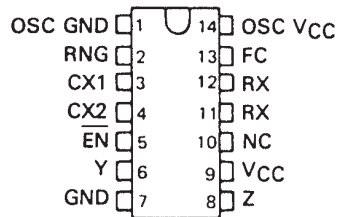
SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

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**SN54LS627 . . . J OR W PACKAGE
SN74LS627 . . . D OR N PACKAGE
(TOP VIEW)**



**SN54LS628 . . . J OR W PACKAGE
SN74LS628 . . . D OR N PACKAGE
(TOP VIEW)**

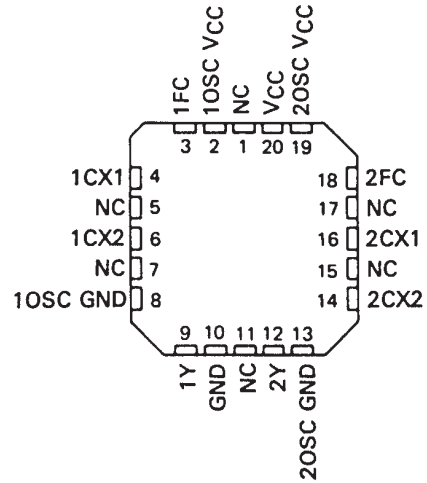


**SN54LS629 . . . J OR W PACKAGE
SN74LS629 . . . D OR N PACKAGE
(TOP VIEW)**



NC-No internal connection

**SN54LS627 . . . FK PACKAGE
(TOP VIEW)**



**SN54LS628 . . . FK PACKAGE
(TOP VIEW)**



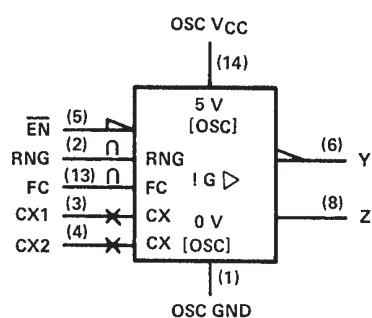
**SN54LS629 . . . FK PACKAGE
(TOP VIEW)**



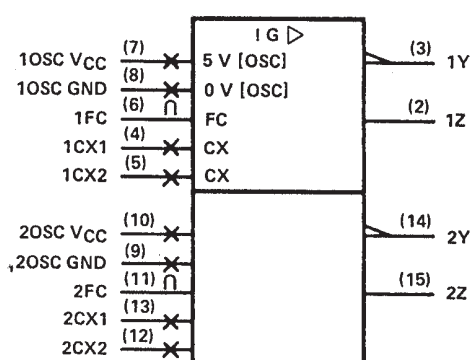
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The logic diagram shows a 4-bit counter implemented using a 74LS629 decoder and a 74LS624/628/629 decoder. The 74LS629 decoder has inputs Cx, FC, RC, and EN, and outputs G, FC, RC, and EN. The 74LS624/628/629 decoder has inputs G, FC, RC, and EN, and outputs Z, Y, and three other outputs. The circuit uses several logic gates (AND, OR, NOT) and a flip-flop (T, R) to generate the outputs Z, Y, and the three other outputs. The EN input is connected to the EN input of both decoders. The Cx input is connected to the Cx input of the 74LS629 decoder. The FC input is connected to the FC input of both decoders. The RC input is connected to the RC input of both decoders. The G output of the 74LS629 decoder is connected to the G input of the 74LS624/628/629 decoder. The FC output of the 74LS629 decoder is connected to the FC input of the 74LS624/628/629 decoder. The RC output of the 74LS629 decoder is connected to the RC input of the 74LS624/628/629 decoder. The EN output of the 74LS629 decoder is connected to the EN input of the 74LS624/628/629 decoder. The Z output of the 74LS624/628/629 decoder is connected to the Z output of the circuit. The Y output of the 74LS624/628/629 decoder is connected to the Y output of the circuit. The three other outputs of the 74LS624/628/629 decoder are connected to the three other outputs of the circuit.

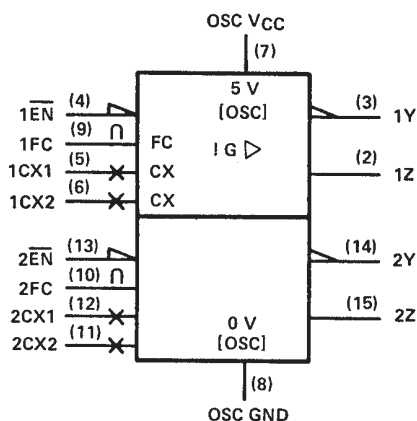
'LS624



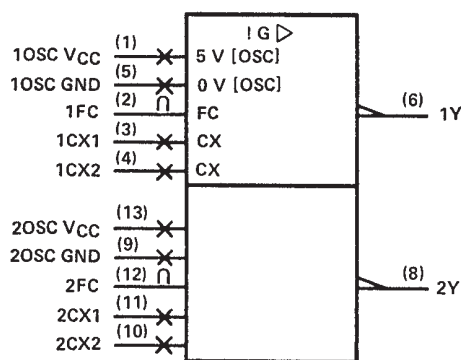
'LS625



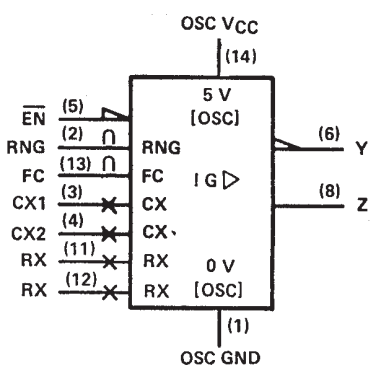
'LS626



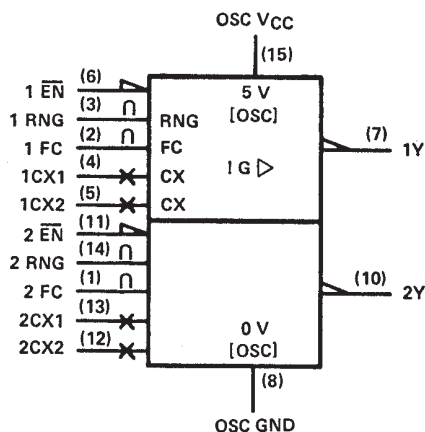
'LS627.



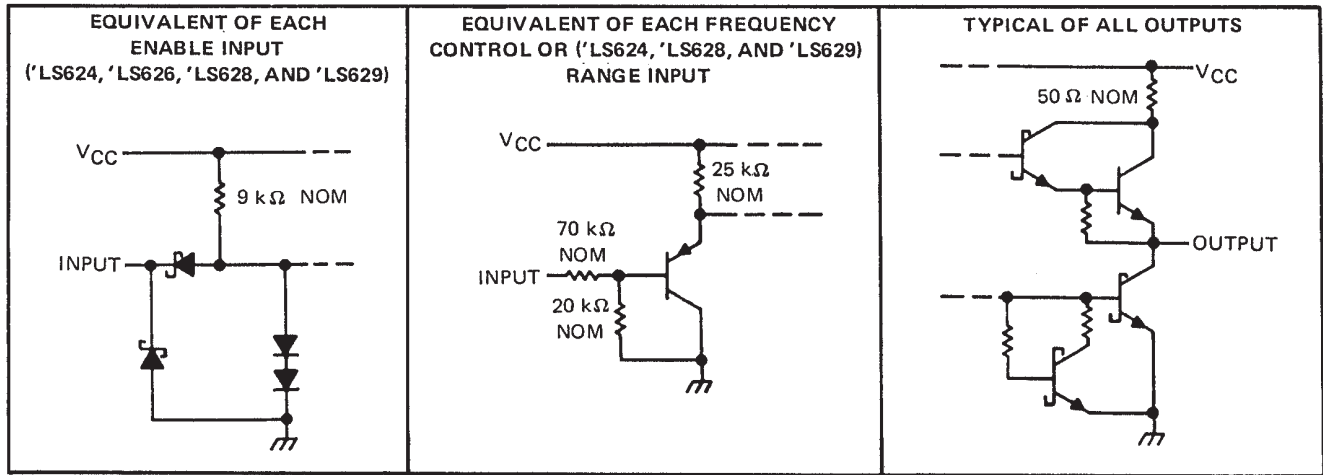
'LS628



'LS629



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)	7 V
Input voltage: Enable input [†]	7 V
Frequency control or range input [‡]	V_{CC}
Operating free-air temperature range: SN54LS' Circuits	–55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] The enable input is provided only on the ‘LS624, ‘LS626, ‘LS628, and ‘LS629.

[‡] The range input is provided only on ‘LS624, ‘LS628, and ‘LS629.

NOTE: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout the data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and OSC V_{CC} terminals, unless otherwise noted.

SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	0		5	0		5	V
High-level output current, I_{OH}			-1.2			-1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency, f_o	1			1			Hz
			20			20	MHz
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage at enable#					2			2			V
V_{IL}	Low-level input voltage at enable#							0.7			0.8	V
V_{IK}	Input clamp voltage at enable#		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}, \overline{EN}$ at V_{IL} max, $I_{OH} = -1.2 \text{ mA}$, See Note 3			2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, \overline{EN}$ at V_{IL} max, See Note 3	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4		V
				$I_{OL} = 24 \text{ mA}$					0.35	0.5		
I_I	Input current	Freq control or range†	$V_{CC} = \text{MAX}$	$V_I = 5 \text{ V}$		50	250		50	250		μA
				$V_I = 1 \text{ V}$		10	50		10	50		
I_I	Input current at maximum input voltage	Enable#	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.2			0.2		mA
I_{IH}	High-level input current	Enable#	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				40			40		μA
I_{IL}	Low-level input current	Enable#	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.8			-0.8		mA
I_{OS}	Short-circuit output current§		$V_{CC} = \text{MAX}$			-40	-225		-40	-225		mA
I_{CC}	Supply current, total into V_{CC} and OSC V_{CC} pins		$V_{CC} = \text{MAX}, \text{Enable\#} = 4.5 \text{ V}$ See Note 4	'LS624		20	35		20	35		mA
				'LS625		35	55		35	55		
				'LS626		35	55		35	55		
				'LS627		35	55		35	55		
				'LS628		20	35		20	35		
				'LS629		35	55		35	55		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†The range input is provided only on the 'LS624, 'LS628, and 'LS629.

#The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3. V_{OH} for Y outputs and V_{OL} for Z outputs are measured while enable inputs are at V_{IL} MAX, with individual 1-k Ω resistors connected from CX1 to V_{CC} and from CX2 to ground. The resistor connections are reversed for testing V_{OH} for Z outputs and V_{OL} for Y inputs.

4. For 'LS624, 'LS626, 'LS628, and 'LS629, I_{CC} is measured with the outputs disabled and open. For 'LS625 and 'LS627, I_{CC} is measured with one OSC $V_{CC} = \text{MAX}$, and with the other OSC V_{CC} and outputs open.



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switching characteristics, $V_{CC} = 5\text{ V}$ (unless otherwise noted), $R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		'LS624, 'LS628, 'LS629			'LS625, 'LS626, 'LS627			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _O	Output frequency	C _{ext} = 50 pF	V _I {freq} = 5 V, V _I {rng} = 0 V	15	20	25				MHz
			V _I {freq} = 1 V, V _I {rng} = 5 V	1.1	1.6	2.1				
			V _I {freq} = 5 V				7	9.5	12	
			V _I {freq} = 0 V				0.9	1.2	1.5	

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE†

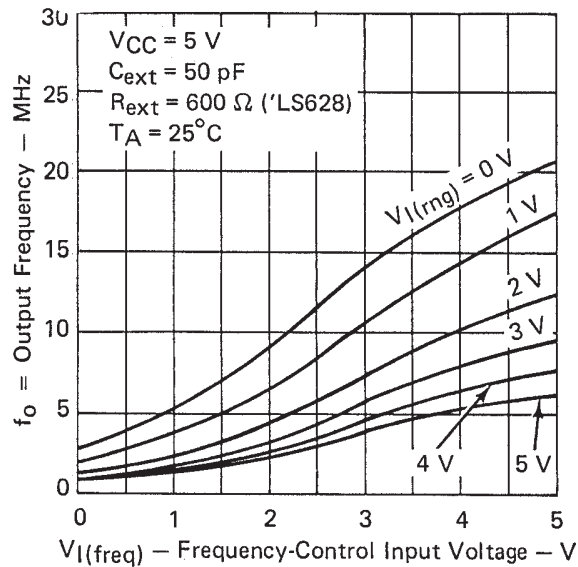


FIGURE 1

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE†

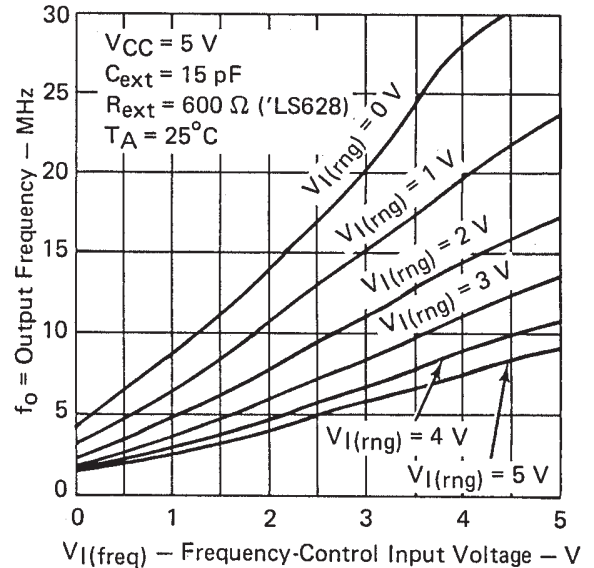


FIGURE 2

† Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

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TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY

vs

EXTERNAL CAPACITANCE

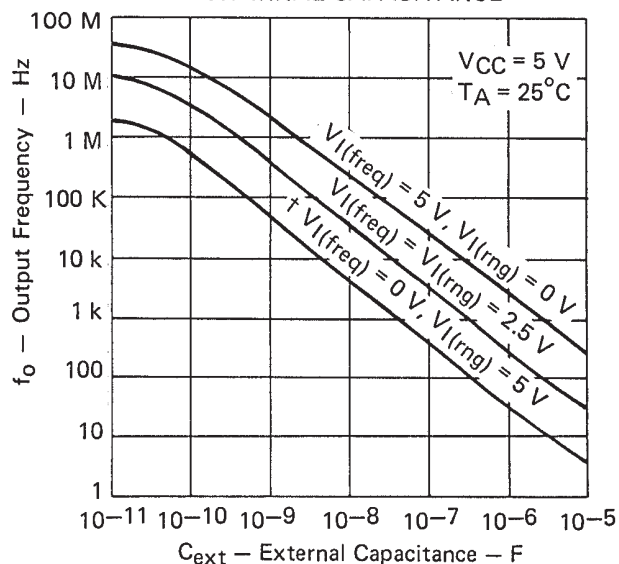


FIGURE 3

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE†

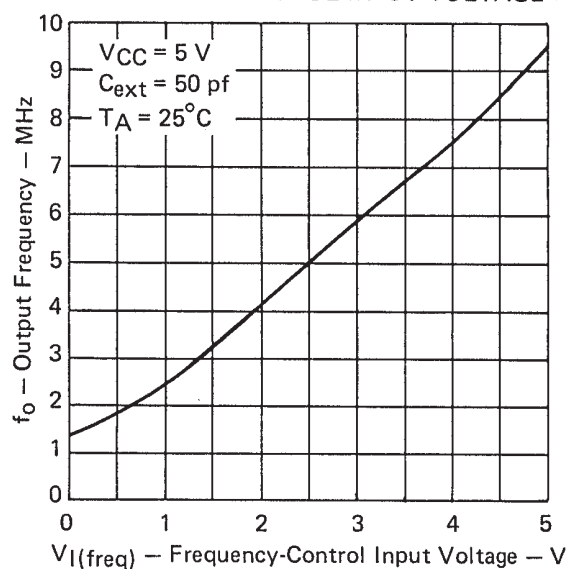


FIGURE 4

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE

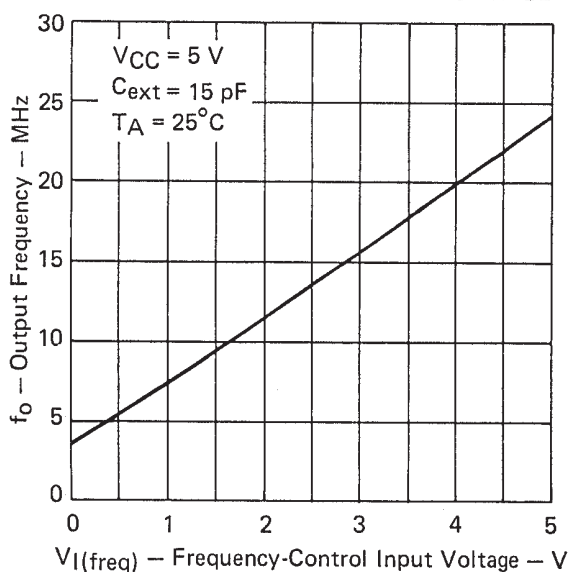


FIGURE 5

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY

vs

EXTERNAL CAPACITANCE

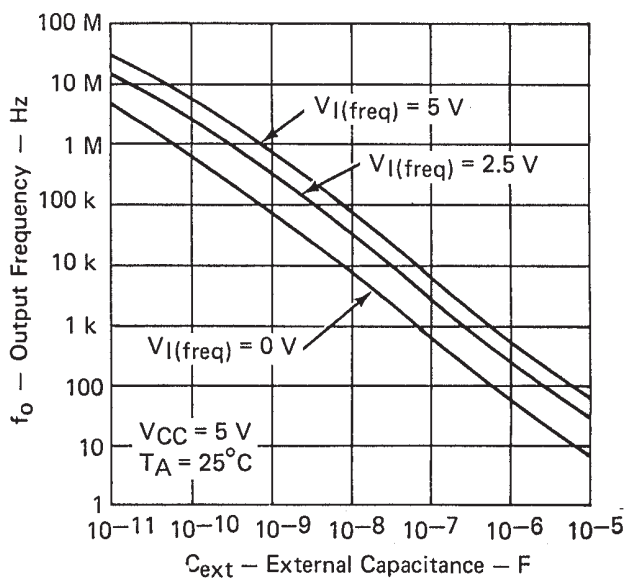


FIGURE 6

† Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

TYPICAL CHARACTERISTICS

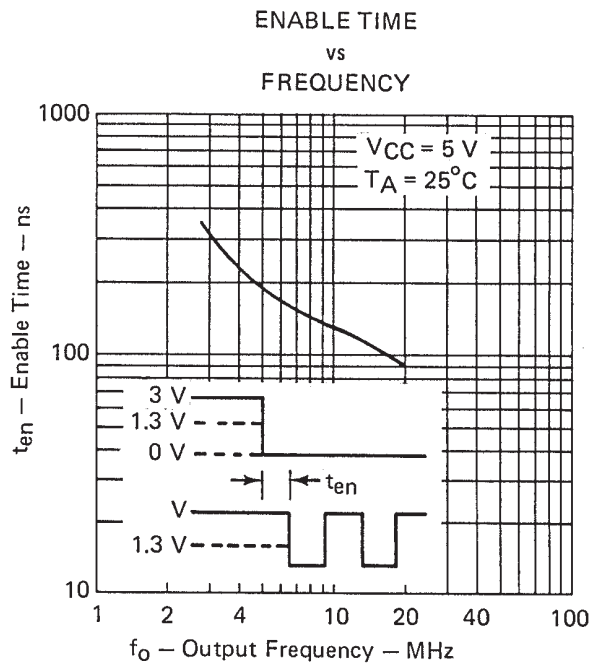
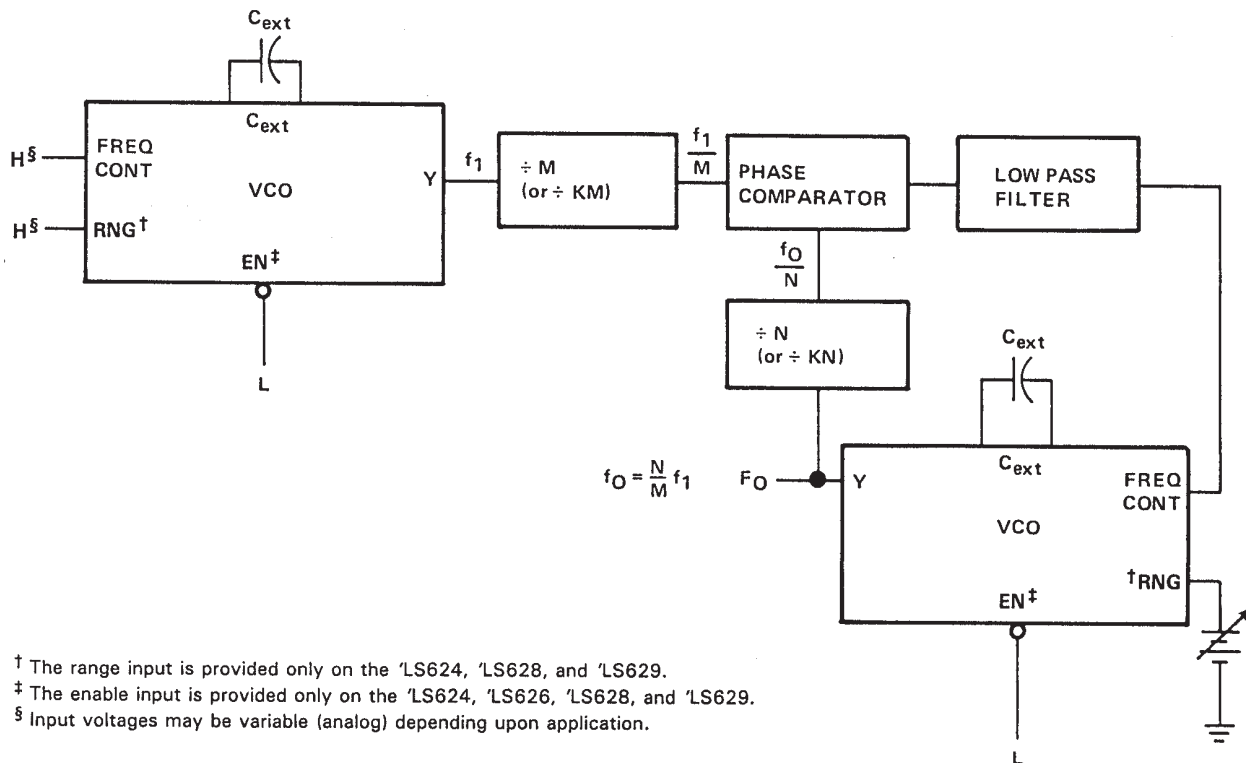


FIGURE 7

TYPICAL APPLICATIONS DATA



[†] The range input is provided only on the 'LS624, 'LS628, and 'LS629.

[‡] The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

[§] Input voltages may be variable (analog) depending upon application.

FIGURE A—PHASE-LOCKED LOOP.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS624DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS624NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS628DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS624DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS624NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LS628DR	SOIC	D	14	2500	367.0	367.0	38.0

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