# DS1553

# 64kB, Nonvolatile, Year-2000-Compliant Timekeeping RAM

www.maxim-ic.com

## GENERAL DESCRIPTION

The DS1553 is a full-function, year-2000-compliant (Y2KC) real-time clock/calendar (RTC) with an RTC alarm, watchdog timer, power-on reset, battery monitor, and 8k x 8 nonvolatile static RAM. User access to all registers within the DS1553 is accomplished with a byte-wide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for day of month and leap year are made automatically.

***Pin Configurations appear at end of data sheet.***

## FEATURES

- Integrated NV SRAM, RTC, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM; These Registers are Resident in the 16 Top RAM Locations
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- Precision Power-On Reset
- Programmable Watchdog Timer and RTC Alarm
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid Up to the Year 2100
- Battery Voltage Level Indicator Flag
- Power-Fail Write Protection Allows for ±10% $V_{CC}$ Power-Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time

## ORDERING INFORMATION

| PART | VOLTAGE (V) | TEMP RANGE | PIN-PACKAGE | TOP MARK** |
|---|---|---|---|---|
| DS1553-85+ | 5.0 | 0°C to +70°C | 28 EDIP (0.740) | DS1553+85 |
| DS1553-100+ | 5.0 | 0°C to +70°C | 28 EDIP (0.740) | DS1553+100 |
| DS1553W-120+ | 3.3 | 0°C to +70°C | 28 EDIP (0.740) | DS1553W+120 |
| DS1553W-150+ | 3.3 | 0°C to +70°C | 28 EDIP (0.740) | DS1553W+150 |
| DS1553P-85+ | 5.0 | 0°C to +70°C | 34 PowerCap* | DS1553P+85 |
| DS1553P-100+ | 5.0 | 0°C to +70°C | 34 PowerCap* | DS1553P+100 |
| DS1553WP-120+ | 3.3 | 0°C to +70°C | 34 PowerCap* | DS1553WP+120 |
| DS1553WP-150+ | 3.3 | 0°C to +70°C | 34 PowerCap* | DS1553WP+150 |
| DS9034PCX+ | 3 | 0°C to +70°C | — | DS9034PCX |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**PowerCap required, must be ordered separately*

***A "+" symbol anywhere on the top mark indicates a lead(Pb)-free package.*

***Note:*** *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

## PIN DESCRIPTION

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| EDIP | PowerCap | | |
| 1 | 2 | $\overline{RST}$ | Active-Low Power-On Reset Output (Open Drain) |
| 2 | 30 | A12 | Address Inputs |
| 3 | 25 | A7 | |
| 4 | 24 | A6 | |
| 5 | 23 | A5 | |
| 6 | 22 | A4 | |
| 7 | 21 | A3 | |
| 8 | 20 | A2 | |
| 9 | 19 | A1 | |
| 10 | 18 | A0 | |
| 21 | 28 | A10 | |
| 23 | 29 | A11 | |
| 24 | 27 | A9 | |
| 25 | 26 | A8 | |
| 11 | 16 | DQ0 | Data Input/Outputs |
| 12 | 15 | DQ1 | |
| 13 | 14 | DQ2 | |
| 15 | 13 | DQ3 | |
| 16 | 12 | DQ4 | |
| 17 | 11 | DQ5 | |
| 18 | 10 | DQ6 | |
| 19 | 9 | DQ7 | |
| 20 | 8 | $\overline{CE}$ | Active-Low Chip Enable |
| 22 | 7 | $\overline{OE}$ | Active-Low Output Enable |
| 26 | 1 | $\overline{IRQ}$/FT | Active-Low Interrupt/Frequency Test Output (Open Drain) |
| 27 | 6 | $\overline{WE}$ | Active-Low Write Enable |
| 28 | 5 | $V_{CC}$ | Power-Supply Input |
| | 17 | GND | Ground |
| — | 2, 3, 31–34 | N.C | No Connection |

## DETAILED DESCRIPTION

The RTC registers in the DS1553 are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is turned on, the internal set of registers is continuously updated. This occurs regardless of external registers settings to guarantee that accurate RTC information is always maintained.

The DS1553 has interrupt ($\overline{IRQ}$/FT) and reset ($\overline{RST}$) outputs that can be used to control CPU activity. The $\overline{IRQ}$/FT interrupt output can be used to generate an external interrupt when the RTC register values match user-programmed alarm values. The interrupt is always available while the device is powered from the system supply, and it can be programmed to occur when in the battery-backed state to serve as a system wakeup. Either the $\overline{IRQ}$/FT or $\overline{RST}$ outputs can also be used as a CPU watchdog timer. CPU activity is monitored and an interrupt or reset output is activated if the correct activity is not detected within programmed limits. The DS1553 power-on reset can be used to detect a system power-down or failure and can hold the CPU in a safe reset state until normal power returns and stabilizes. The $\overline{RST}$ output is used for this function.

The DS1553 also contains its own power-fail circuitry, which automatically deselects the device when the $V_{CC}$ supply enters an out-of-tolerance condition. This feature provides a high degree of data security during unpredictable system operation brought on by low $V_{CC}$ levels.

## PACKAGES

The DS1553 is available in a 28-pin DIP and a 34-pin PowerCap module. The 28-pin DIP module integrates the crystal, lithium energy source, and silicon in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1553P after completion of the surface-mount process. Mounting the PowerCap after the surface-mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

### Figure 1. Block Diagram

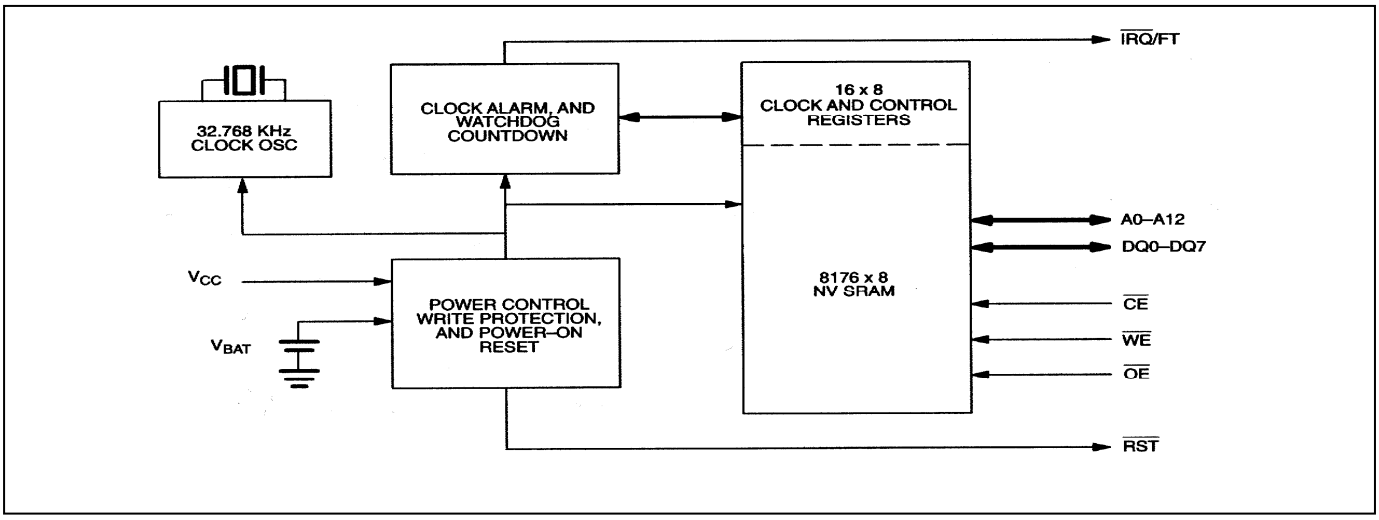


**Table 1. Operating Modes**

| $V_{CC}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | DQ0–DQ7 | MODE | POWER |
|---|---|---|---|---|---|---|
| $V_{CC} > V_{PF}$ | $V_{IH}$ | X | X | High-Z | Deselect | Standby |
| | $V_{IL}$ | X | $V_{IL}$ | $D_{IN}$ | Write | Active |
| | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Read | Active |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High-Z | Read | Active |
| $V_{SO} < V_{CC} < V_{PF}$ | X | X | X | High-Z | Deselect | CMOS Standby |
| $<V_{BAT}$ | X | X | X | High-Z | Data Retention | Battery Current |

## DATA READ MODE

The DS1553 is in read mode whenever $\overline{CE}$ (chip enable) is low and $\overline{WE}$ (write enable) is high. The device architecture allows ripple-through access to any valid address location. Valid data is available at the data input/output (DQ) pins within $t_{AA}$ after the last address input is stable, provided that $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data is available at the latter of chip-enable access ($t_{CEA}$) or at output-enable access time ($t_{OEA}$). The state of the DQ pins is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before $t_{AA}$, the data lines are driven to an intermediate state until $t_{AA}$. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data remains valid for output data hold time ($t_{OH}$) but will then go indeterminate until the next address access.

## DATA WRITE MODE

The DS1553 is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ and $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of a subsequent read or write cycle. Data in must be valid $t_{DS}$ prior to the end of the write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal is high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low, the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

The 5V device is fully accessible, and data can be written and read only when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ is below the power-fail point ($V_{PF}$)—the point at which write protection occurs—the internal clock registers and SRAM are blocked from any access. When $V_{CC}$ falls below the battery switch point $V_{SO}$ (battery supply level), device power is switched from the $V_{CC}$ pin to the internal backup lithium battery. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels.

The 3.3V device is fully accessible and data can be written and read only when $V_{CC}$ is greater than $V_{PF}$. When $V_{CC}$ falls below $V_{PF}$, access to the device is inhibited. If $V_{PF}$ is less than $V_{SO}$, the device power is switched from $V_{CC}$ to the internal backup lithium battery when $V_{CC}$ drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{SO}$, the device power is switched from $V_{CC}$ to the internal backup lithium battery when $V_{CC}$ drops

below $V_{SO}$. RTC operation and SRAM data are maintained from the battery until $V_{CC}$ is returned to nominal levels.

All control, data, and address signals must be powered down when $V_{CC}$ is powered down.

## BATTERY LONGEVITY

The DS1553 has a lithium power source that is designed to provide energy for the clock activity and clock and RAM data retention when the $V_{CC}$ supply is not present. The capability of this internal power supply is sufficient to power the DS1553 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of $V_{CC}$. Each DS1553 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than $V_{PF}$, the lithium energy source is enabled for battery backup operation.

## INTERNAL BATTERY MONITOR

The DS1553 constantly monitors the battery voltage of the internal battery. The Battery Low Flag (BLF) bit of the Flags register (B4 of 1FF0h) is not writeable and should always be 0 when read. If a 1 is ever present, an exhausted lithium energy source is indicated, and both the contents of the RTC and RAM are questionable.

## POWER-ON RESET

A temperature-compensated comparator circuit monitors the $V_{CC}$ level. When $V_{CC}$ falls to the power-fail trip point, the $\overline{RST}$ signal (open drain) is pulled low. When $V_{CC}$ returns to nominal levels, the $\overline{RST}$ signal continues to be pulled low for 40ms to 200ms. The power-on reset function is independent of the RTC oscillator and is therefore operational whether or not the oscillator is enabled.

## CLOCK OPERATIONS

Table 2 and the following paragraphs describe the operation of RTC, alarm, and watchdog functions.

### Table 2. Register Map

| ADDRESS | DATA | | | | | | | | FUNCTION/RANGE | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 1FFFh | 10 Year | | | | Year | | | | Year | 00-99 |
| 1FFEh | X | X | X | 10 M | Month | | | | Month | 01-12 |
| 1FFDh | X | X | 10 Date | | Date | | | | Date | 01-31 |
| 1FFCh | X | FT | X | X | X | Day | | | Day | 01-07 |
| 1FFBh | X | X | 10 Hour | | Hour | | | | Hour | 00-23 |
| 1FFAh | X | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 1FF9h | OSC | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 1FF8h | W | R | 10 Century | | Century | | | | Control | 00-39 |
| 1FF7h | WDS | BMB 4 | BMB3 | BMB2 | BMB 1 | BMB 0 | RB 1 | RB0 | Watchdog | |
| 1FF6h | AE | Y | ABE | Y | Y | Y | Y | Y | Interrupts | |
| 1FF5h | AM4 | Y | 10 Date | | Date | | | | Alarm Date | 01-31 |
| 1FF4h | AM3 | Y | 10 Hours | | Hours | | | | Alarm Hours | 00-23 |
| 1FF3h | AM2 | 10 Minutes | | | Minutes | | | | Alarm Minutes | 00-59 |
| 1FF2h | AM1 | 10 Seconds | | | Seconds | | | | Alarm Seconds | 00-59 |
| 1FF1h | Y | Y | Y | Y | Y | Y | Y | Y | Unused | — |
| 1FF0h | WF | AF | 0 | BLF | 0 | 0 | 0 | 0 | Flags | — |

X = Unused, Read/Writable Under Write and Read Bit Control
FT = Frequency Test Bit
$\overline{OSC}$ = Oscillator Start/Stop Bit
W = Write Bit
R = Read Bit
WDS = Watchdog Steering Bit
BMB0–BMB4 = Watchdog Multiplier Bits
RB0–RB1 = Watchdog Resolution Bits
AE = Alarm Flag Enable
Y = Unused, Read/Writable Without Write and Read Bit Control
ABE = Alarm in Battery-Backup Mode Enable
AM1–AM4 = Alarm Mask Bits
WF = Watchdog Flag
AF = Alarm Flag
0 = 0 Read Only
BLF = Battery Low Flag

## CLOCK OSCILLATOR CONTROL

The clock oscillator may be stopped at any time. To increase the shelf life of the backup lithium battery source, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB of the Seconds register (B7 of 1FF9h). Setting it to 1 stops the oscillator; setting it to 0 starts the oscillator. The DS1553 is shipped from Dallas Semiconductor with the clock oscillator turned off, with the $\overline{OSC}$ bit set to 1.

## READING THE CLOCK

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state, allowing data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted when a 1 is written into the read bit, B6 of the Control register (1FF8h). As long as a 1 remains in the Control register read bit, updating is halted. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command was issued. Normal updates to the external set of registers resume within 1 second after the read bit is set to 0 for a minimum of 500µs. The read bit must be 0 for a minimum of 500µs to ensure the external registers are updated.

## SETTING THE CLOCK

The 8th bit, B7 of the Control register, is the write bit. Setting the write bit to 1, like the read bit, halts updates to the DS1553 (1FF8h–1FFFh) registers. After setting the write bit to 1, RTC registers can be loaded with the desired RTC count (day, date, and time) in 24-hour BCD format. Setting the write bit to 0 then transfers the values written to the internal RTC registers and allows normal operation to resume.

## CLOCK ACCURACY (DIP MODULE)

The DS1553 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C. The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. The electrical environment also affects clock accuracy and caution should be taken to place the RTC in the lowest level EMI section of the PC board layout. For additional information, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*, available on our website at www.maxim-ic.com/appnoteindex.com.

## CLOCK ACCURACY (PowerCap MODULE)

The DS1553 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module typically keeps time accuracy to within ±1.53 minutes per month (35ppm) at +25°C. The electrical environment affects clock accuracy and caution should be taken to place the RTC in the lowest level EMI section of the PC board layout. For additional information, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*, available on our website at www.maxim-ic.com/appnoteindex.com.

## FREQUENCY TEST MODE

The DS1553 frequency test mode uses the open-drain $\overline{IRQ}$/FT output. With the oscillator running, the $\overline{IRQ}$/FT output toggles at 512Hz when the FT bit is 1, the Alarm Flag Enable bit (AE) is 0, and the Watchdog Steering bit (WDS) is 1 or the Watchdog register is reset (Register 1FF7h = 00h). The $\overline{IRQ}$/FT output and the frequency test mode can be used as a measure of the actual frequency of the 32.768kHz RTC oscillator. The $\overline{IRQ}$/FT pin is an open-drain output that requires a pullup resistor for proper operation. The FT bit is cleared to 0 on power-up.

## USING THE CLOCK ALARM

The alarm settings and control for the DS1553 reside within registers 1FF2h–1FF5h. Register 1FF6h contains two alarm-enable bits: Alarm Enable (AE) and Alarm in Backup Enable (ABE). The AE and ABE bits must be set as described below for the $\overline{IRQ}$/FT output to be activated for a matched alarm condition.

The alarm can be programmed to activate on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS1553 is in the battery-backed state of operation to serve as a system wakeup. Alarm mask bits AM1–AM4 control the alarm mode. Table 3 shows the possible settings. Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting.

### Table 3. Alarm Mask Bits

| AM4 | AM3 | AM2 | AM1 | ALARM RATE |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Once per second |
| 1 | 1 | 1 | 0 | When seconds match |
| 1 | 1 | 0 | 0 | When minutes and seconds match |
| 1 | 0 | 0 | 0 | When hours, minutes, and seconds match |
| 0 | 0 | 0 | 0 | When date, hours, minutes, and seconds match |

When the RTC register values match Alarm register settings, the Alarm Flag bit (AF) is set to 1. If the Alarm Flag Enable (AE) is also set to 1, the alarm condition activates the $\overline{IRQ}$/FT pin. The $\overline{IRQ}$/FT signal is cleared by a read or write to the Flags register (Address 1FF0h) as shown in Figures 2 and 3. When $\overline{CE}$ is active, the $\overline{IRQ}$/FT signal may be cleared by having the address stable for as short as 15ns and either $\overline{OE}$ or $\overline{WE}$ active, but it is not guaranteed to be cleared unless $t_{RC}$ is fulfilled. The alarm flag is also cleared by a read or write to the Flags register, but the flag does not change states until the end of the read/write cycle and the $\overline{IRQ}$/FT signal has been cleared.

**Figure 2. Clearing $\overline{IRQ}$ Waveforms**

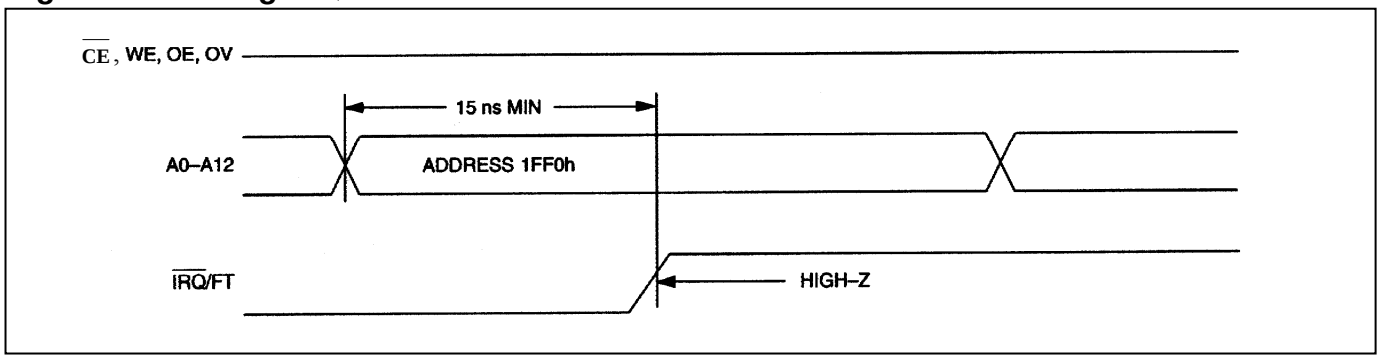
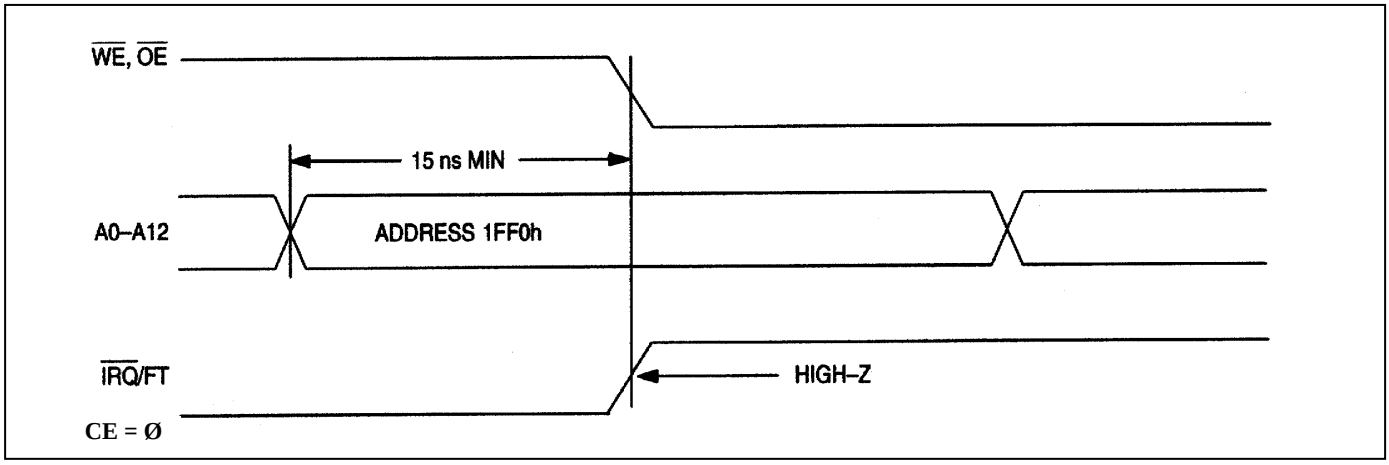
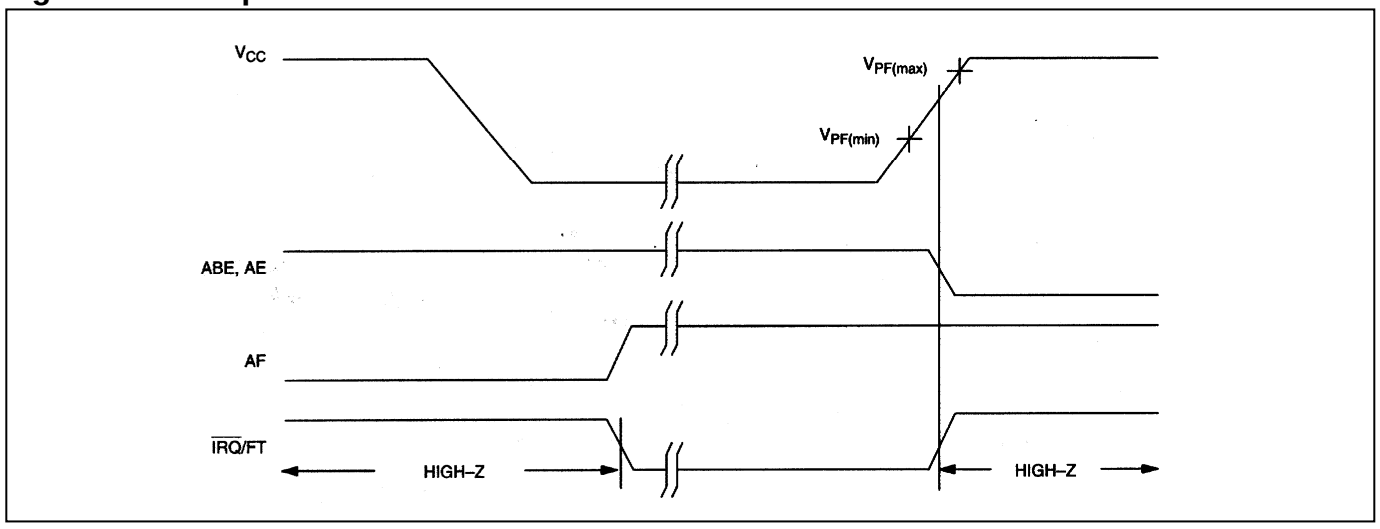



**Figure 3. Clearing $\overline{IRQ}$ Waveforms**




The $\overline{IRQ}$/FT pin can also be activated in the battery-backed mode. The $\overline{IRQ}$/FT goes low if an alarm occurs and both ABE and AE are set. The ABE and AE bits are cleared during the power-up transition, however, an alarm generated during power-up sets AF. Therefore, the AF bit can be read after system power-up to determine if an alarm was generated during the power-up sequence. Figure 4 illustrates alarm timing during the battery-backup mode and power-up states.

**Figure 4. Backup Mode Alarm Waveforms**



## USING THE WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control processor. The user programs the watchdog timer by setting the desired amount of timeout into the 8-bit Watchdog register (Address 1FF7h). The five Watchdog register bits BMB4–BMB0 store a binary multiplier and the two lower-order bits RB1–RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The watchdog timeout value is then determined by the multiplication of the 5-bit multiplier value with the 2-bit resolution value. (For example: writing 00001110 in the Watchdog register = 3 x 1 second or 3 seconds.) If the processor does not reset the timer within the specified period, the Watchdog Flag (WF) is set and a processor interrupt is generated and stays active until either the Watchdog Flag (WF) is read or the Watchdog register (1FF7) is read or written.

The most significant bit of the Watchdog register is the Watchdog Steering Bit (WDS). When set to 0, the watchdog activates the $\overline{IRQ}$/FT output when the watchdog times out.

When WDS is set to 1, the watchdog outputs a negative pulse on the $\overline{RST}$ output for 40ms to 200ms. The Watchdog register (1FF7) and the FT bit are reset to 0 at the end of a watchdog timeout when the WDS bit is set to 1.

The watchdog timer resets when the processor performs a read or write of the Watchdog register. The timeout period then starts over. Writing a value of 00h to the Watchdog register disables the watchdog timer. The watchdog function is automatically disabled upon power-up and the Watchdog register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT output and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied.

## POWER-ON DEFAULT STATES

Upon application of power to the device, the following register bits are set to 0:

WDS = 0, BMB0–BMB4 = 0, RB0–RB1 = 0, AE = 0, and ABE = 0.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range
EDIP .....……..-40°C to +85°C
PowerCap.....……..-55°C to +125°C
Lead Temperature (soldering, 10s)…….....+260°C
(**Note:** EDIP is hand or wave-soldered only.) (Note 8)
Soldering Temperature (reflow)…….....+260°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

## OPERATING RANGE

| RANGE | TEMP RANGE | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ±10% or 5V ±10% |

## RECOMMENDED DC OPERATING CONDITIONS

($T_A$ = Over the operating range.)

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Logic 1 Voltage All Inputs | $V_{CC}$ = 5V ±10% | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3V | V | 1 |
| | $V_{CC}$ = 3.3V ±10% | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.3V | V | 1 |
| Logic 0 Voltage All Inputs | $V_{CC}$ = 5V ±10% | $V_{IL}$ | -0.3 | | +0.8 | | 1 |
| | $V_{CC}$ = 3.3V ±10% | $V_{IL}$ | -0.3 | | +0.6 | | 1 |

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0V ±10%, $T_A$ = Over the operating range.)

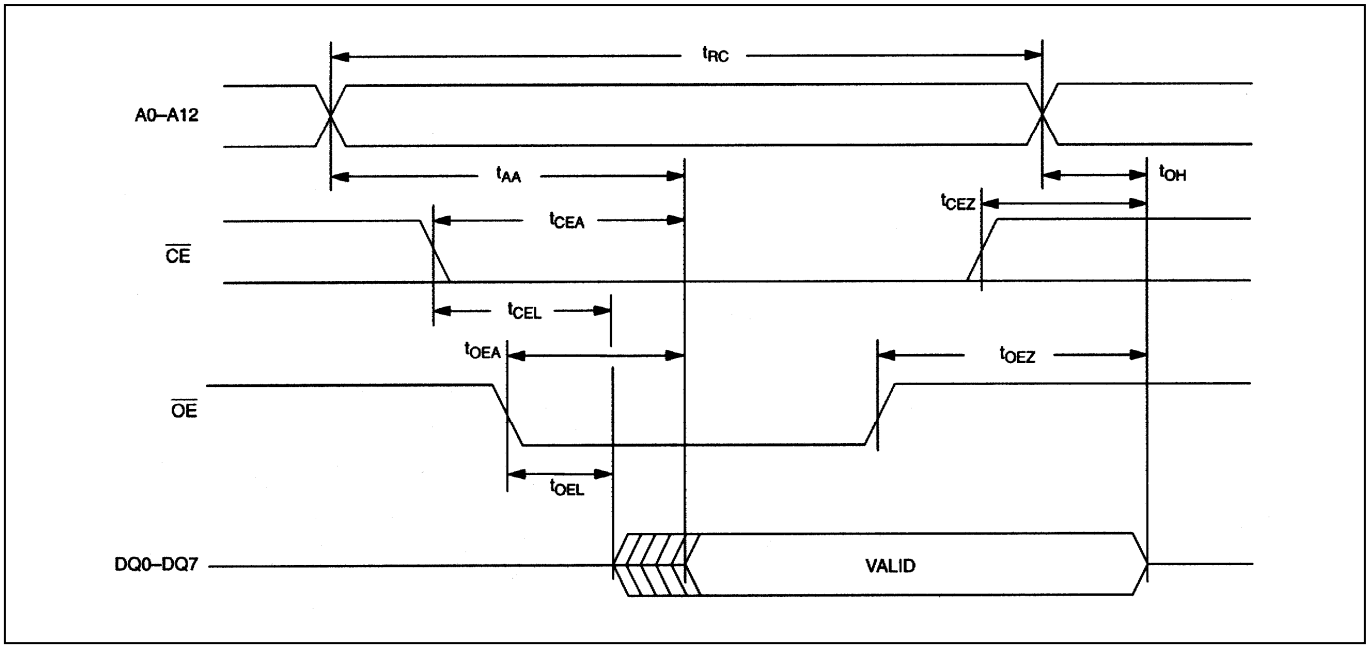
| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Active Supply Current | | $I_{CC}$ | | 15 | 50 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE}$ = $V_{IH}$) | | $I_{CC1}$ | | 1 | 3 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V) | | $I_{CC2}$ | | 1 | 3 | mA | 2, 3 |
| Input Leakage Current (Any Input) | | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (Any Output) | | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0mA) | | $V_{OH}$ | 2.4 | | | V | 1 |
| Output Logic 0 Voltage | $I_{OUT}$ = 2.1mA, DQ0-7 Outputs | $V_{OL1}$ | | | 0.4 | V | 1 |
| | $I_{OUT}$ = 7.0mA, $\overline{IRQ}$/FT and $\overline{RST}$ Outputs | $V_{OL2}$ | | | 0.4 | V | 1, 5 |
| Write Protection Voltage | | $V_{PF}$ | 4.20 | | 4.50 | V | 1 |
| Battery Switchover Voltage | | $V_{SO}$ | | $V_{BAT}$ | | V | 1, 4 |

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.3V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Active Supply Current | | $I_{CC}$ | | 10 | 30 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE}$ = $V_{IH}$) | | $I_{CC1}$ | | 0.7 | 2 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V) | | $I_{CC2}$ | | 0.7 | 2 | mA | 2, 3 |
| Input Leakage Current (Any Input) | | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current (Any Output) | | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0mA) | | $V_{OH}$ | 2.4 | | | V | 1 |
| Output Logic 0 Voltage | $I_{OUT}$ = 2.1mA, DQ0–7 Outputs | $V_{OL1}$ | | | 0.4 | V | 1 |
| | $I_{OUT}$ = 7.0mA, $\overline{IRQ}$/FT and $\overline{RST}$ Outputs | $V_{OL2}$ | | | 0.4 | V | 1, 5 |
| Write Protection Voltage | | $V_{PF}$ | 2.75 | | 2.97 | V | 1 |
| Battery Switchover Voltage | | $V_{SO}$ | | $V_{BAT}$ or $V_{PF}$ | | V | 1, 4 |

### Figure 5. Read Cycle Timing Diagram



## READ CYCLE, AC CHARACTERISTICS

($V_{CC}$ = 5.0V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | SYMBOL | 85ns ACCESS | | 100ns ACCESS | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Read Cycle Time | $t_{RC}$ | 85 | | 100 | | ns |
| Address Access Time | $t_{AA}$ | | 85 | | 100 | ns |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | 5 | | ns |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | 85 | | 100 | ns |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | 30 | | 35 | ns |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | 5 | | ns |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | 45 | | 55 | ns |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | 30 | | 35 | ns |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns |

## READ CYCLE, AC CHARACTERISTICS

($V_{CC}$ = 3.3V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | SYMBOL | 120ns ACCESS | | 150ns ACCESS | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | ns |
| Address Access Time | $t_{AA}$ | | 120 | | 150 | ns |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | 5 | | ns |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | 120 | | 150 | ns |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | 40 | | 50 | ns |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | 5 | | ns |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | 100 | | 130 | ns |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | 35 | | 35 | ns |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns |

## WRITE CYCLE, AC CHARACTERISTICS

($V_{CC}$ = 5.0V ±10%, $T_A$ = Over the operating range.)

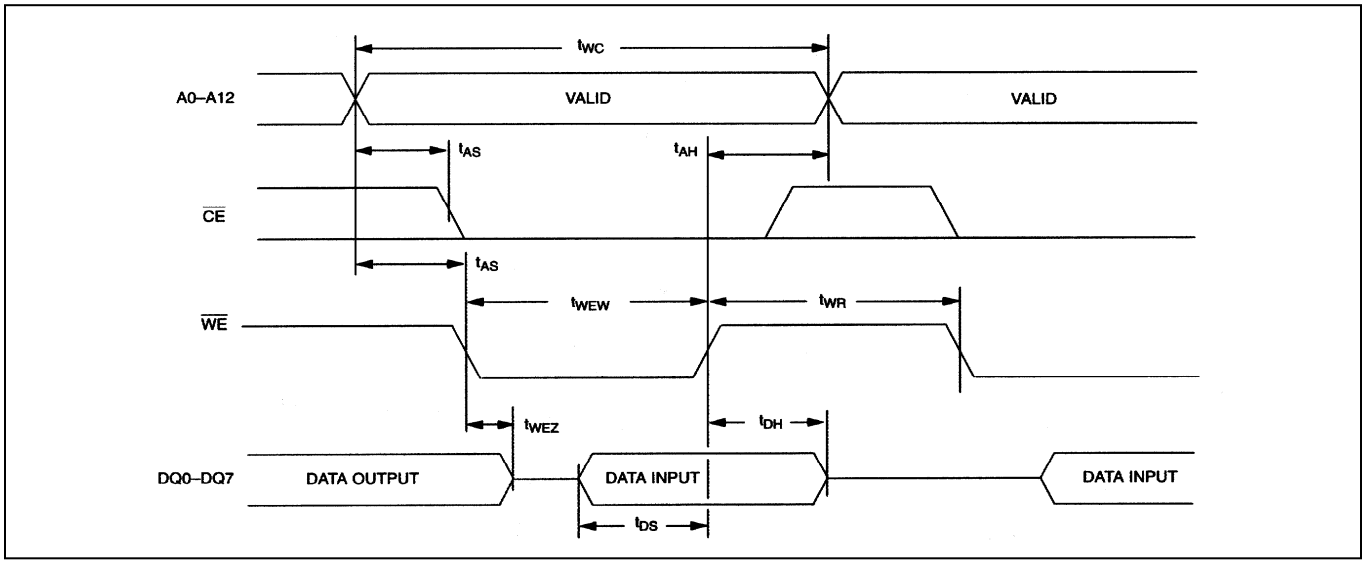
| PARAMETER | SYMBOL | 85ns ACCESS | | 100ns ACCESS | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Write Cycle Time | $t_{WC}$ | 85 | | 100 | | ns |
| Address Access Time | $t_{AS}$ | 0 | | 0 | | ns |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 65 | | 70 | | ns |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 70 | | 75 | | ns |
| Data Setup Time | $t_{DS}$ | 35 | | 40 | | ns |
| Data Hold time | $t_{DH}$ | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 5 | | 5 | | ns |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 30 | | 35 | ns |
| Write Recovery Time | $t_{WR}$ | 5 | | 5 | | ns |

## WRITE CYCLE, AC CHARACTERISTICS

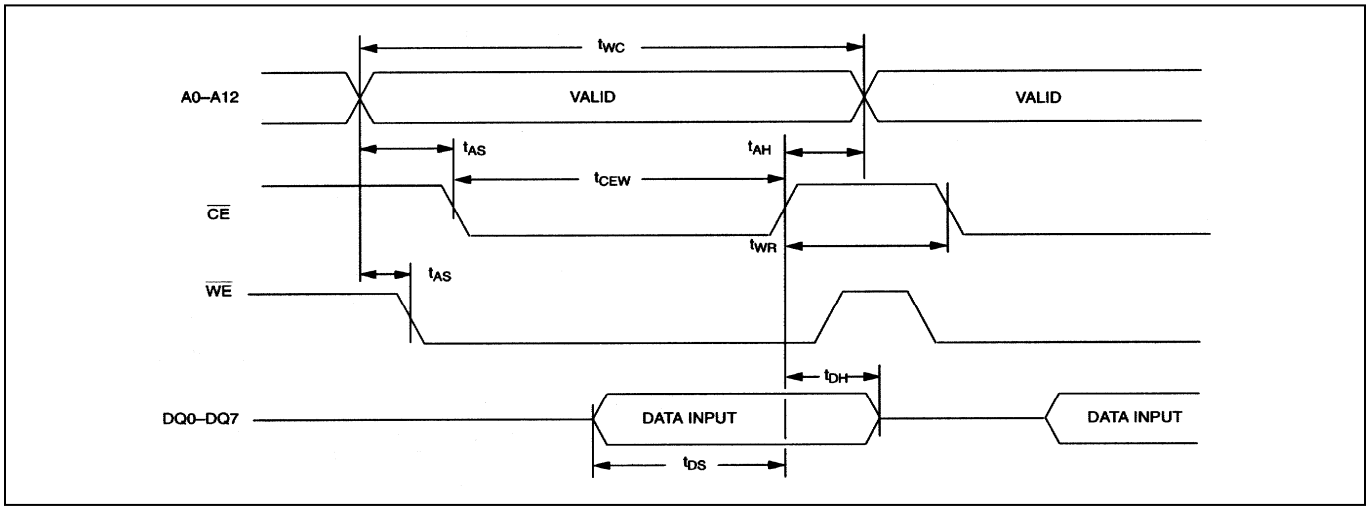
($V_{CC}$ = 3.3V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | SYMBOL | 120ns ACCESS | | 150ns ACCESS | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 100 | | 130 | | ns |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 110 | | 140 | | ns |
| Data Setup Time | $t_{DS}$ | 80 | | 90 | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | ns |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 40 | | 50 | ns |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns |

## Figure 6. Write Cycle Timing, Write-Enable Controlled




## Figure 7. Write Cycle Timing, Chip-Enable Controlled

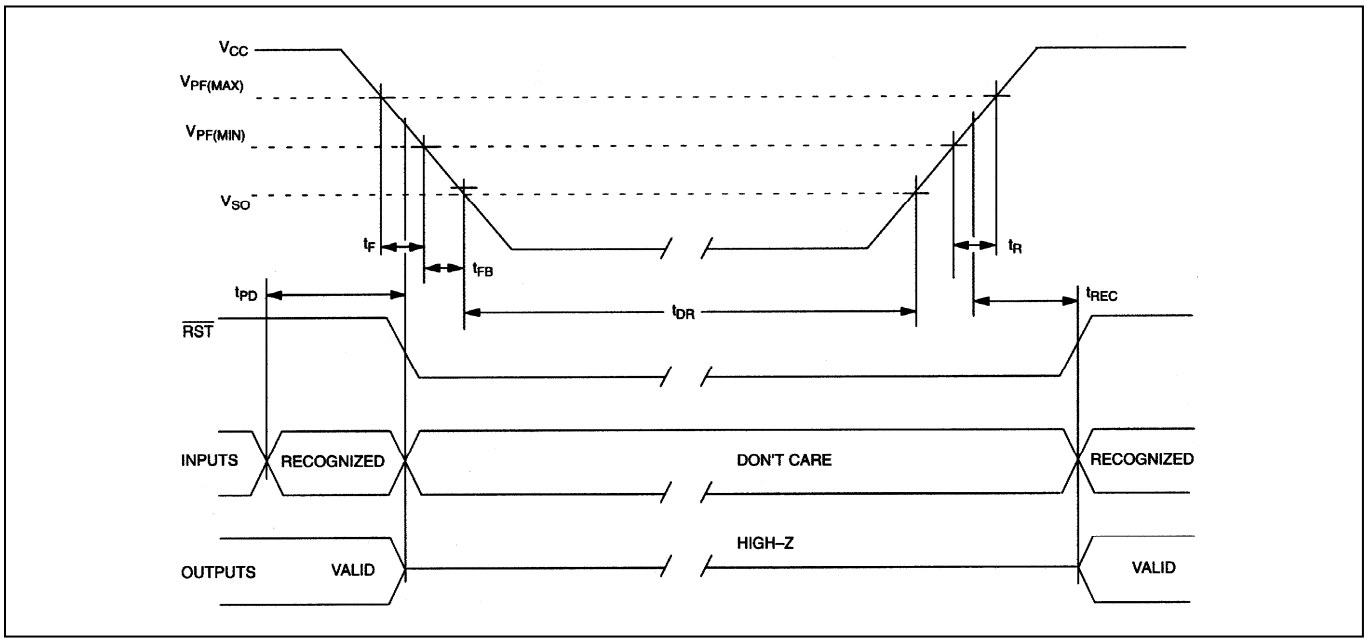


## POWER-UP/DOWN CHARACTERISTICS

($V_{CC}$ = 5.0V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$, Before Power-Down | $t_{PD}$ | 0 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$ | $t_F$ | 300 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF(MIN)}$ to $V_{SO}$ | $t_{FB}$ | 10 | | | µs | |
| $V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$ | $t_R$ | 0 | | | µs | |
| $V_{PF}$ to $\overline{RST}$ High | $t_{REC}$ | 40 | | 200 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 6, 7 |

### Figure 8. Power-Up/Down Waveform Timing 5V Device

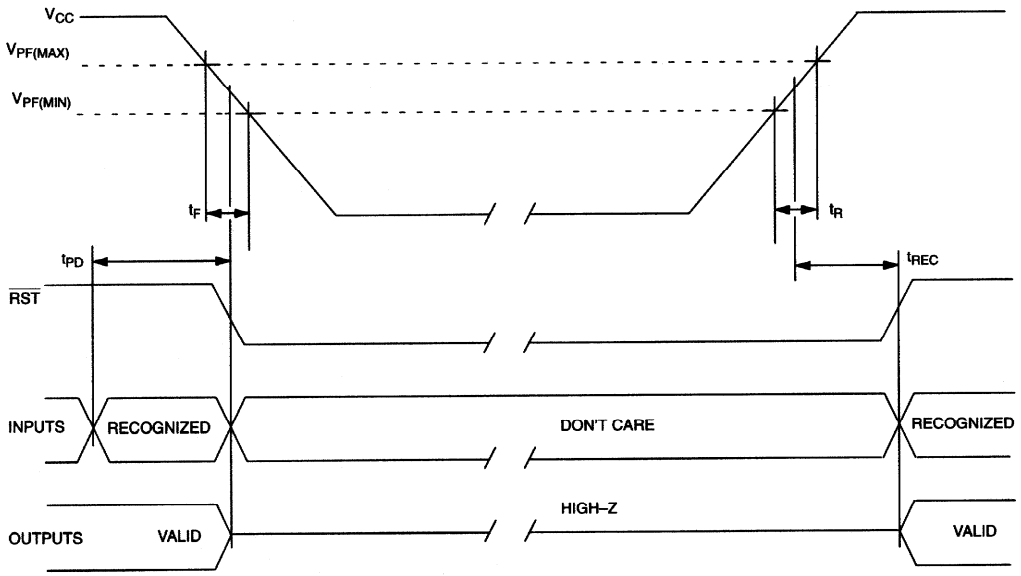


## POWER-UP/DOWN CHARACTERISTICS

($V_{CC}$ = 3.3V ±10%, $T_A$ = Over the operating range.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$, Before Power-Down | $t_{PD}$ | 0 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$ | $t_F$ | 300 | | | µs | |
| $V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$ | $t_R$ | 0 | | | µs | |
| $V_{PF}$ to $\overline{RST}$ High | $t_{REC}$ | 40 | | 200 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 6, 7 |

**Figure 9. Power-Up/Down Waveform Timing 3.3V Device**




## CAPACITANCE

($T_A$ = +25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on All Input Pins | $C_{IN}$ | | | 7 | pF | 1 |
| Capacitance on $\overline{IRQ}$/FT, $\overline{RST}$, and DQ Pins | $C_{IO}$ | | | 10 | pF | 1 |

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

## NOTES:

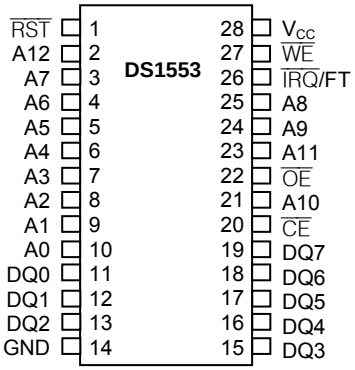
1) Voltage referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switch over occurs at the lower of either the battery voltage or $V_{PF}$.
5) The $\overline{IRQ}$/FT and $\overline{RST}$ outputs are open drain.
6) Data retention time is at +25°C.
7) Each DS1553 has a built-in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined for DIP modules as a cumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.
8) Real-time clock modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

In addition, for the PowerCap:

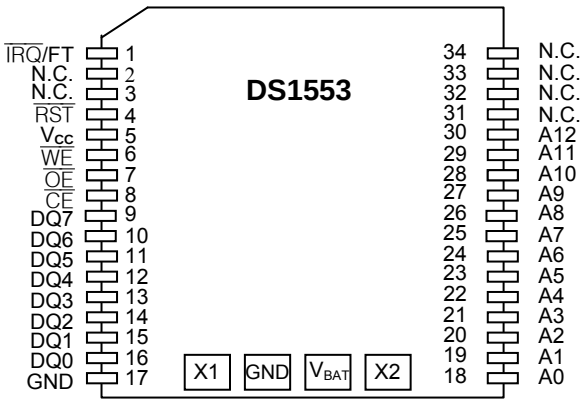
a. Maxim recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflow and use a solder wick to remove solder.

## PIN CONFIGURATIONS

TOP VIEW




**28-Pin Encapsulated Package (700-mil Extended)**




**34-Pin PowerCap Module Board (Uses DS9034PCX PowerCap)**

## PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 28 EDIP | MDP28+2 | **21-0241** | — |
| 34 PWRCP | PC1+2 | **21-0246** | — |

## REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|
| 8/10 | Updated the *Ordering Information* table; updated the storage and soldering temperatures and added the lead temperature in the *Absolute Maximum Ratings* section; changed 70ns Access to 85ns Access in the *Read Cycle, AC Characteristics* (5V) table and updated the min/max values for $t_{RC}$, $t_{AA}$, $t_{CEA}$, $t_{CEZ}$, $t_{OEA}$, and $t_{OEZ}$; changed 70ns Access to 85ns Access in the *Write Cycle, AC Characteristics* (5V) table and updated the min/max values for $t_{WC}$, $t_{WEW}$, $t_{CEW}$, $t_{DS}$, and $t_{WEZ}$; updated the *Package Information* table and removed the package drawings | 1, 13, 14, 19 |



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